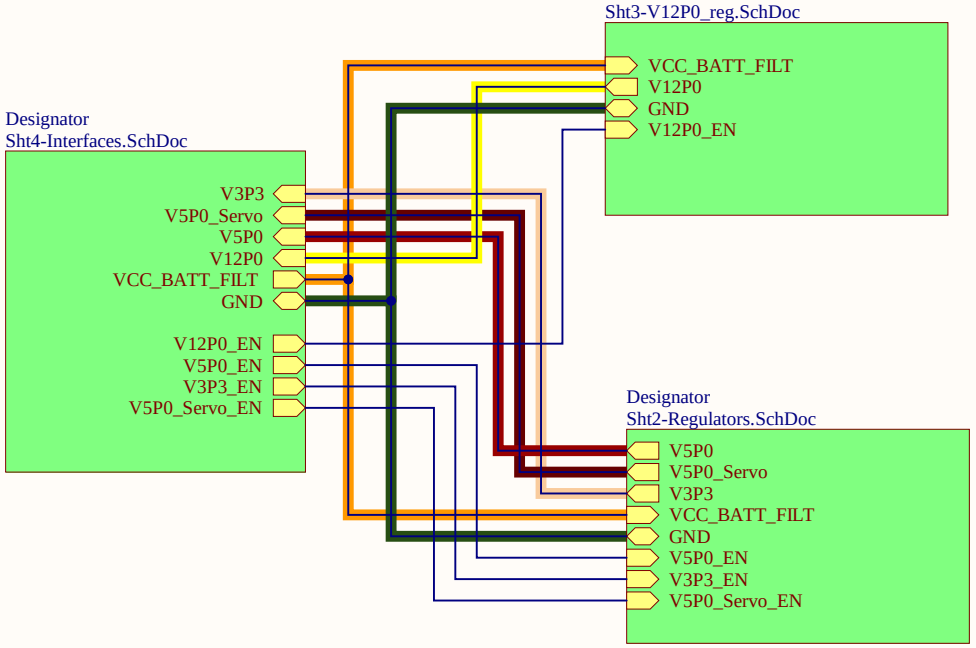

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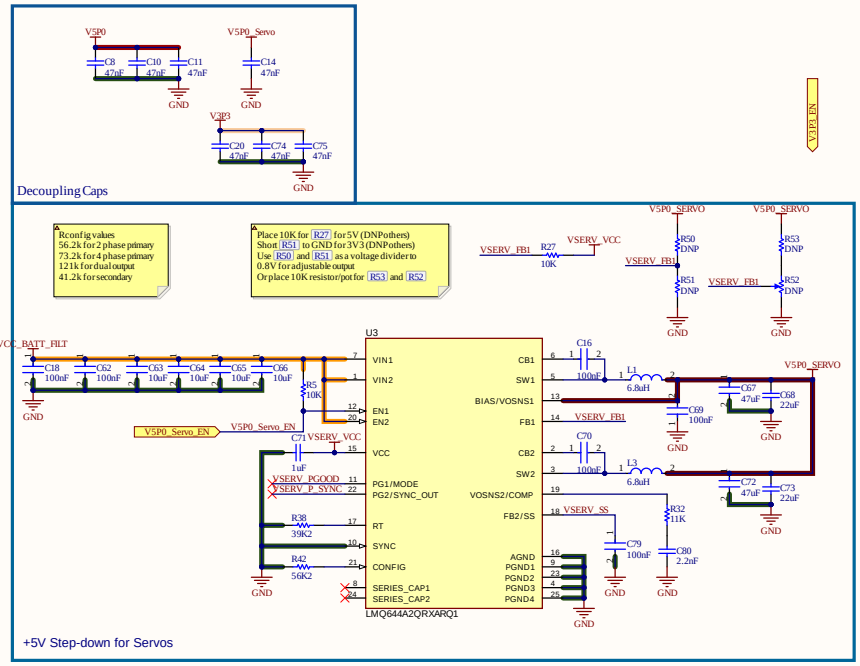
Size: A	Number	Revision
Date: 1/19/2024		Sheet of
File: C:\Users\..\Sht1-BlockDiagram.SchDoc		Drawn By:

Voltage Regulators



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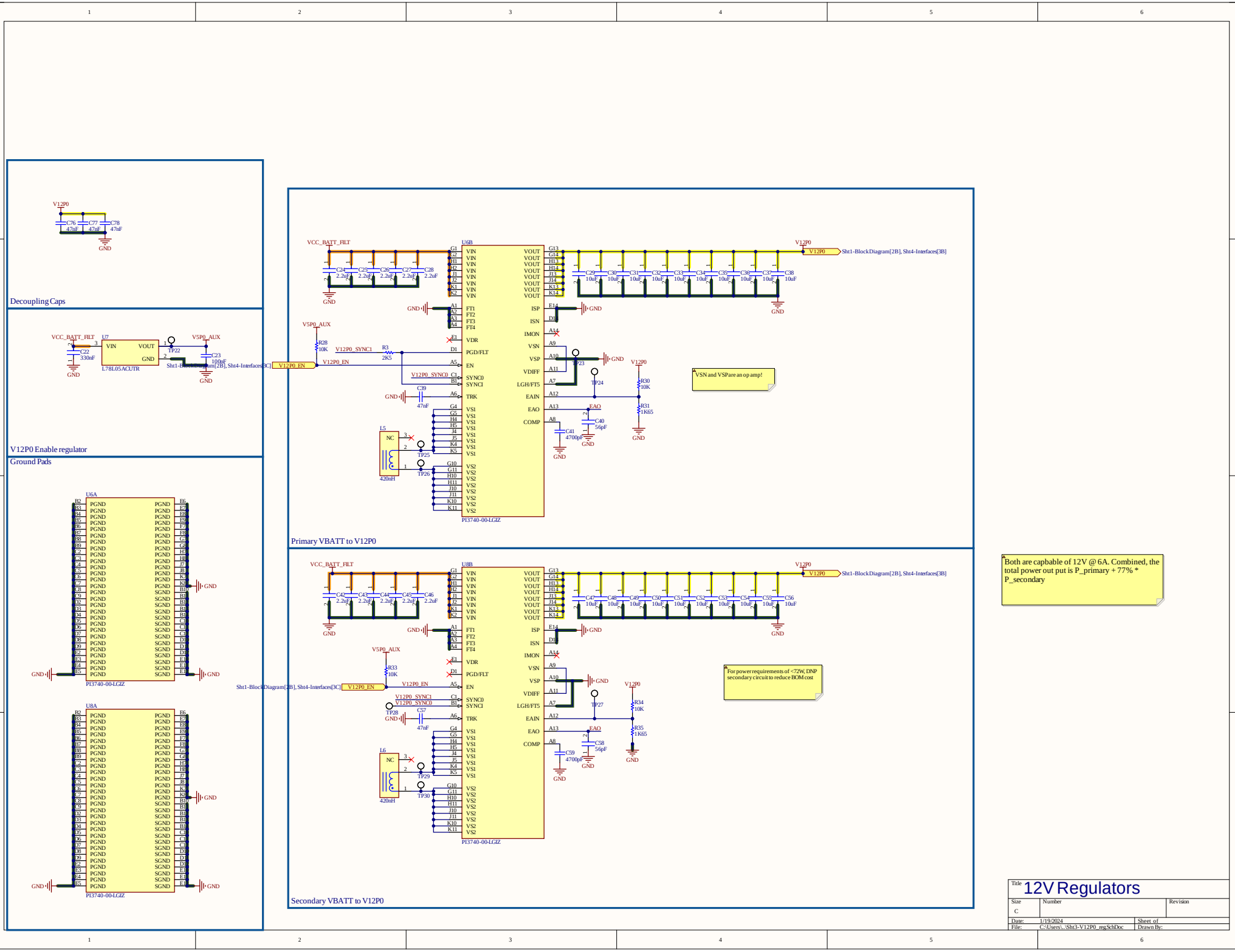
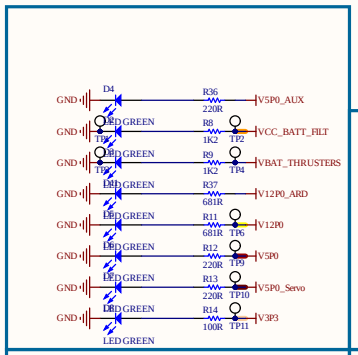
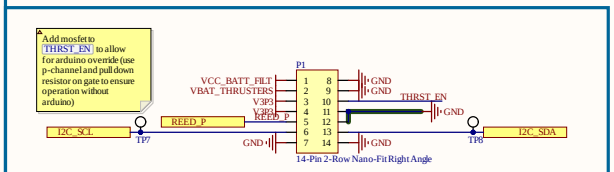
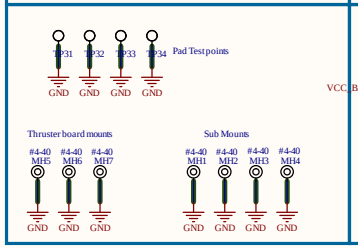
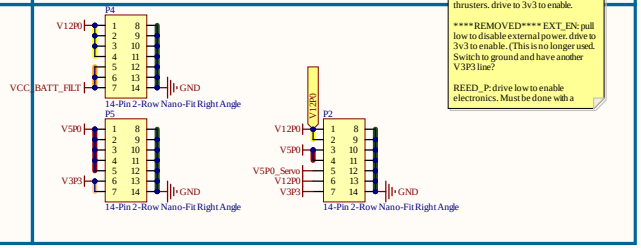

Decoupling Caps
V12P0
C76 47nF
C77 47nF
C78 47nF
GND
V12P0 Enable regulator
VCC_BATT_FILT
U7
VIN
VOUT
GND
L78L05ACUTR
C22 330nF
C23 100nF
TP22
V5P0_AUX
Sht1-Block Diagram[2B], Sht4-Interfaces[3C]
Ground Pads
U6A
U8A
PGND
SGND
PI3740-00-LGIZ
Primary VBATT to V12P0
U6B
C24 2.2uF
C25 2.2uF
C26 2.2uF
C27 2.2uF
C28 2.2uF
C29 10uF
C30 10uF
C31 10uF
C32 10uF
C33 10uF
C34 10uF
C35 10uF
C36 10uF
C37 10uF
C38 10uF
V12P0_EN
V12P0_SYNC1
V12P0_SYNC0
R28 10K
R3 2K5
C39 47nF
L5 420nH
TP23
TP24
TP25
TP26
R30 10K
R31 1K65
C40 56pF
C41 4700pF
VSN and VSPare an op amp!
Secondary VBATT to V12P0
U8B
C42 2.2uF
C43 2.2uF
C44 2.2uF
C45 2.2uF
C46 2.2uF
C47 10uF
C48 10uF
C49 10uF
C50 10uF
C51 10uF
C52 10uF
C53 10uF
C54 10uF
C55 10uF
C56 10uF
R33 10K
C57 47nF
L6 420nH
TP27
TP28
TP29
TP30
R34 10K
R35 1K65
C58 56pF
C59 4700pF
For power requirements of <72W, DNP secondary circuit to reduce BOM cost
Both are capbable of 12V @ 6A. Combined, the total power out put is P_primary + 77% * P_secondary
Title 12V Regulators
Size C
Number
Revision
Date: 1/19/2024
Sheet of
File: C:\Users\..\Sht3-V12P0_reg.SchDoc
Drawn By:

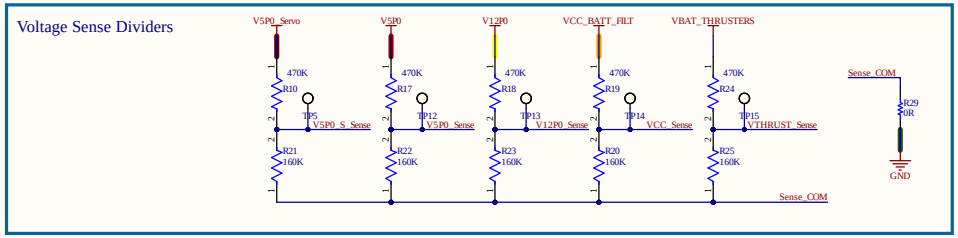
Interface

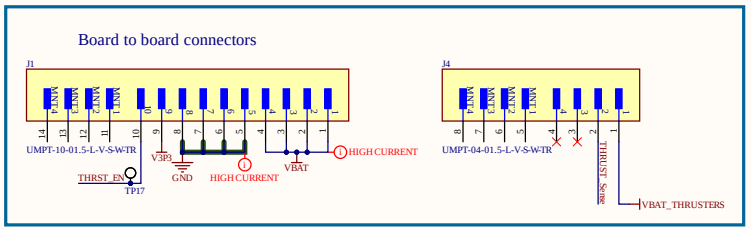


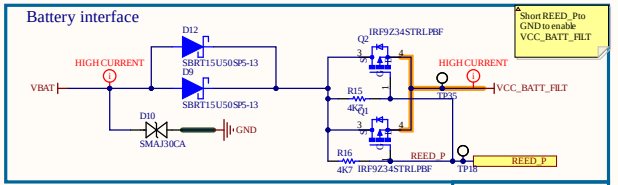


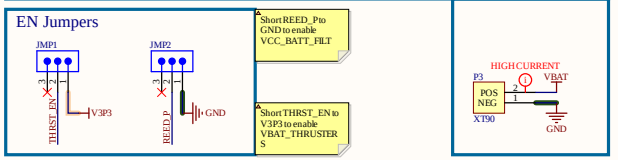


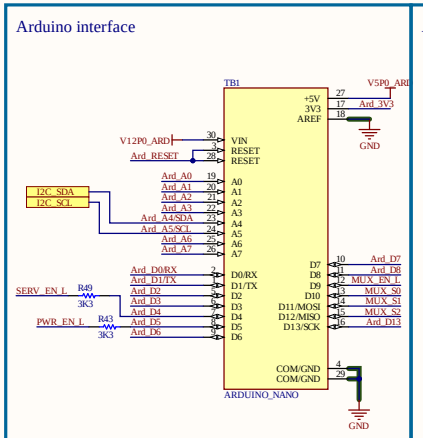


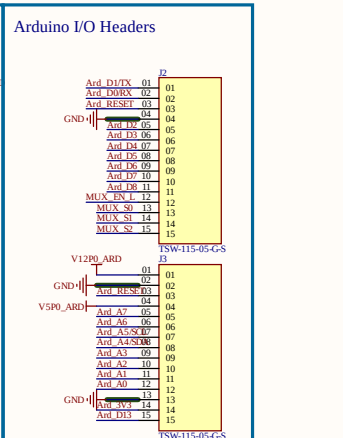


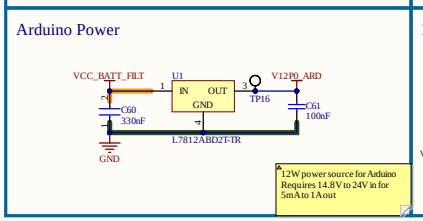


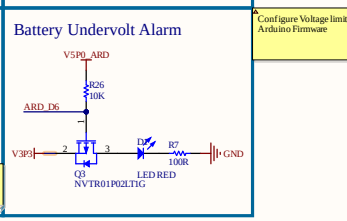






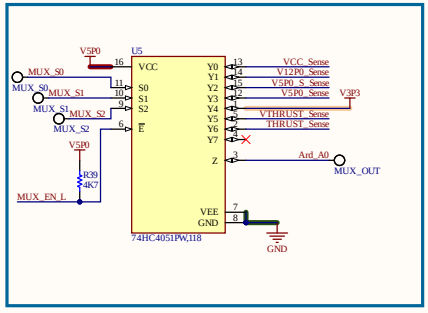


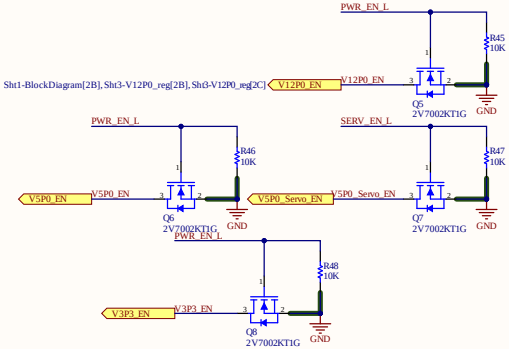




S2 S1 S0 Z E_L Signal
0 0 0 Y0 0 VCC_Sense
0 0 1 Y1 0 V12P0_Sense
0 1 0 Y2 0 V5P0_S_Sense
0 1 1 Y3 0 V5P0_Sense
1 0 0 Y4 0 V3P3
1 0 1 Y5 0 VTHRUST_Sense
1 1 0 Y6 0 THRUST_Sense
1 1 1 Y7 0 No connect
X X X X 1
for all signals with _Sense (except for thrust)
V_out = V_in * (160K) / (470k + 160K)
V_in = V_out * (470K + 160K) / (160K)

THRUST
V*1000 = A_out
(This this output needs to be amplified on future revisions)





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Interfaces and Microcontroller		
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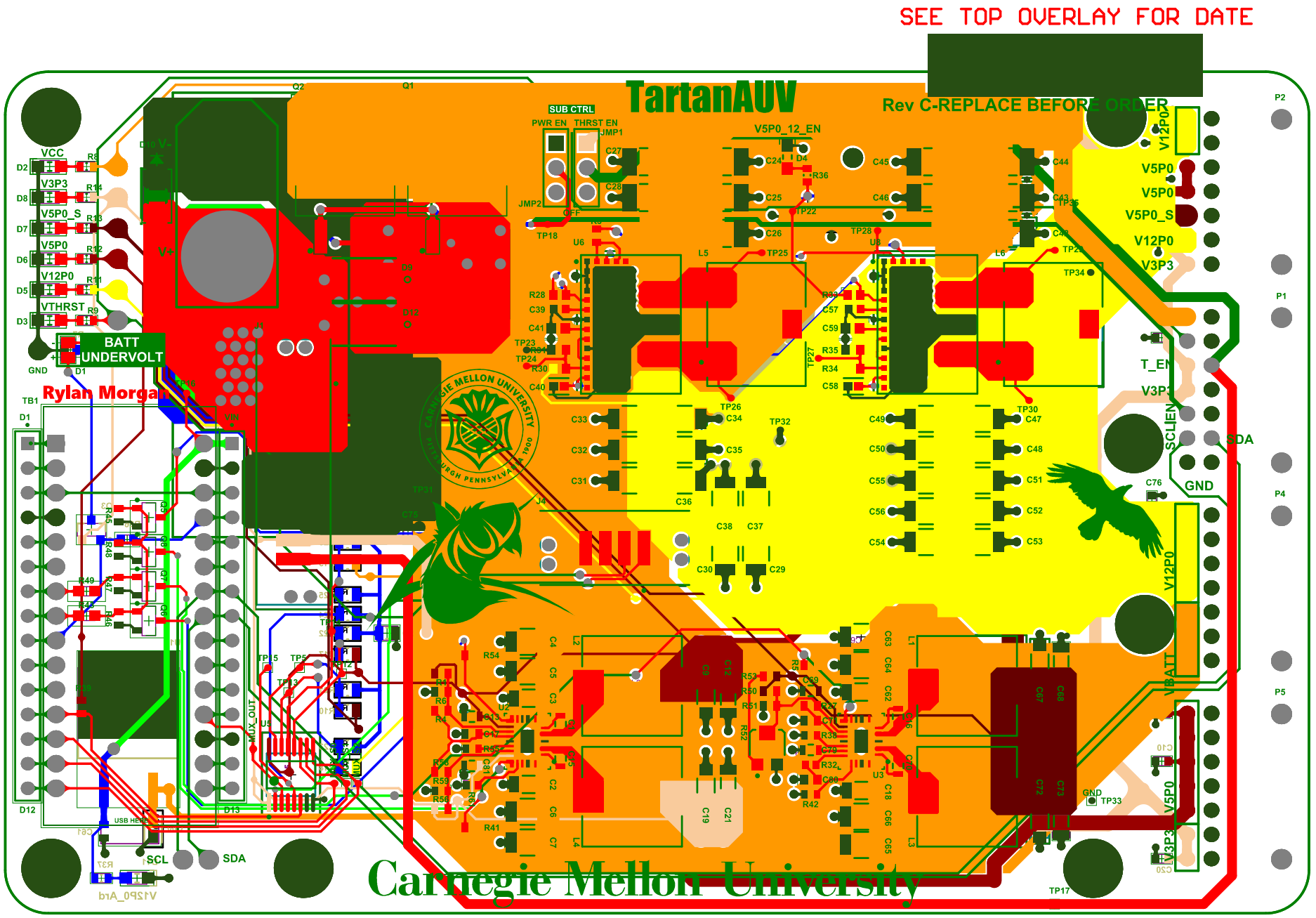
SEE TOP OVERLAY FOR DATE
TartanAUV
Rev C-REPLACE BEFORE ORDER
SUB CTRL
PWR EN
THRST EN
JMP1
JMP2
V5P0_12_EN
BATT UNDERVOLT
Rylan Morgan
VCC
V3P3
V5P0_S
V5P0
V12P0
VTHRST
GND
SCL
SDA
Carnegie Mellon University