



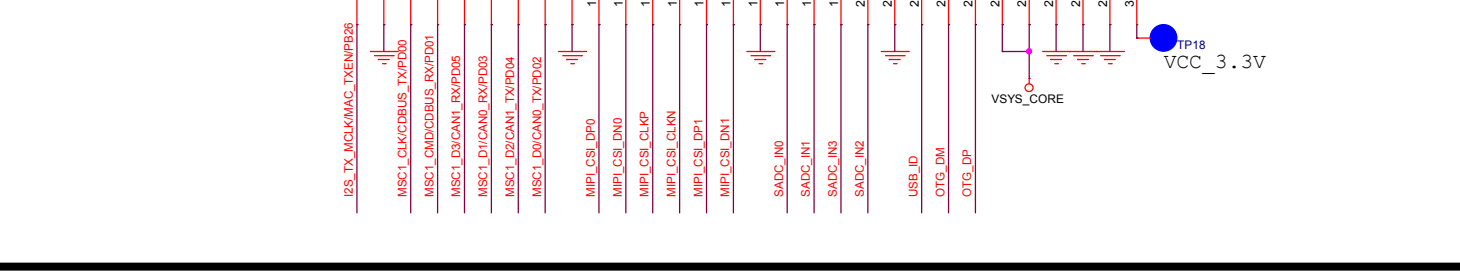
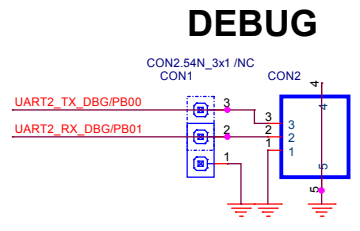
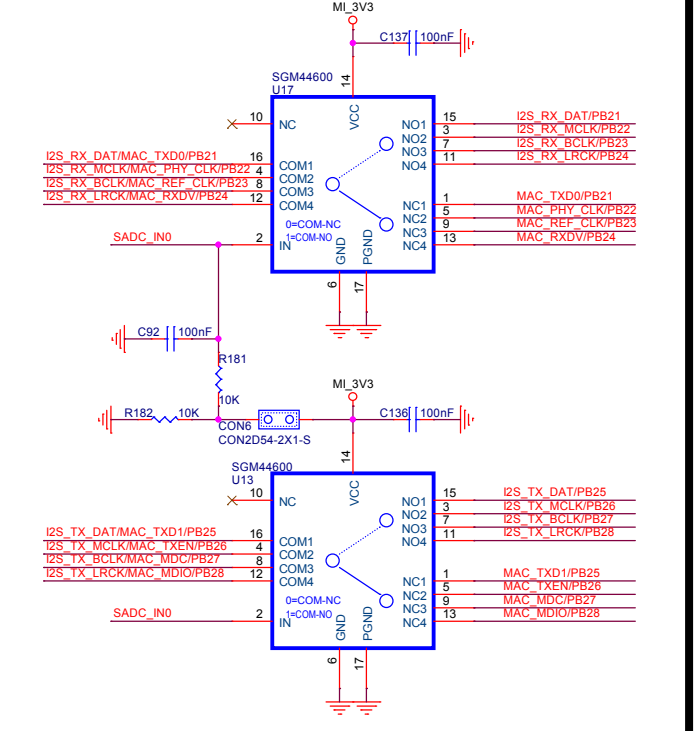
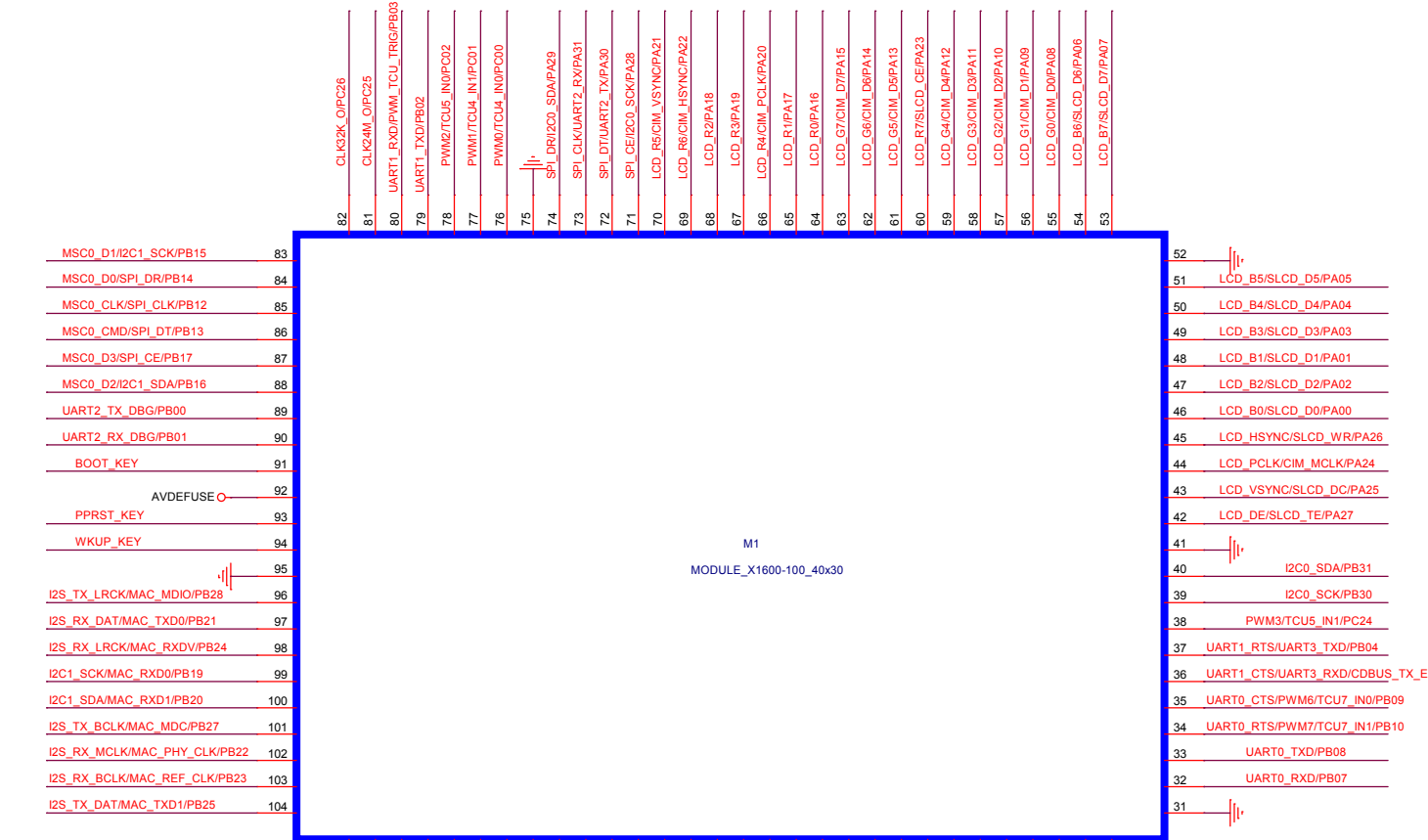
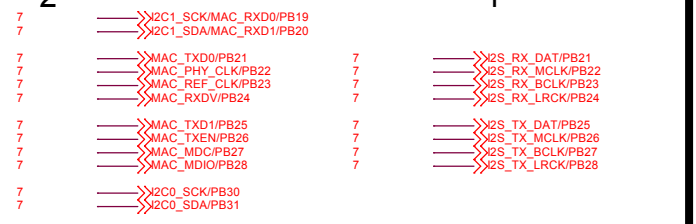
## HALLEY6\_BASEBOARD\_V2.0

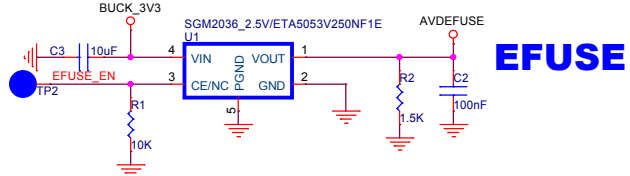
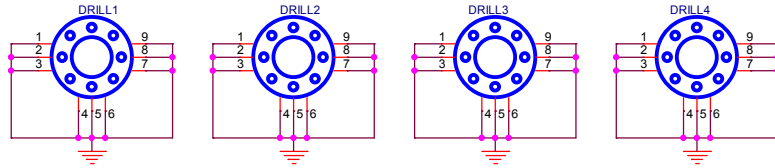
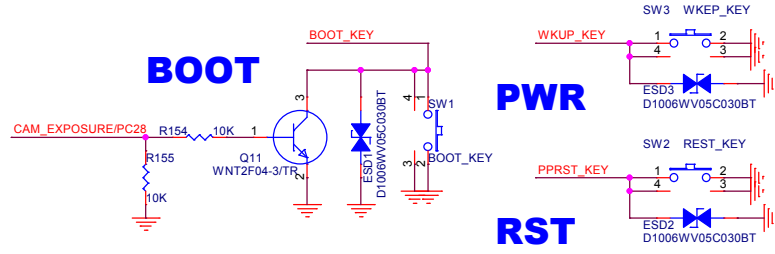
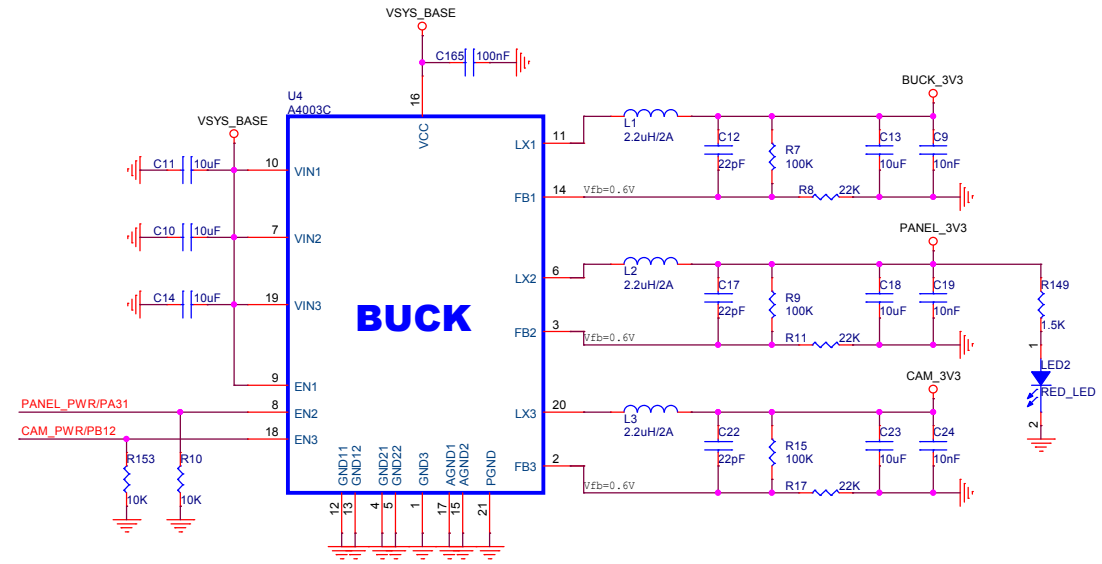
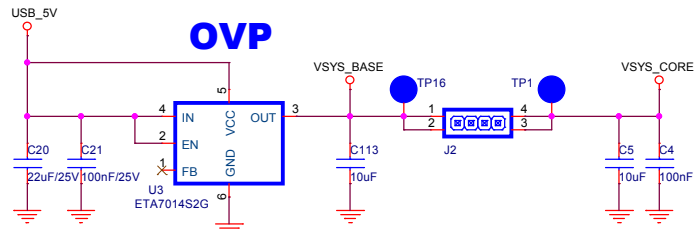
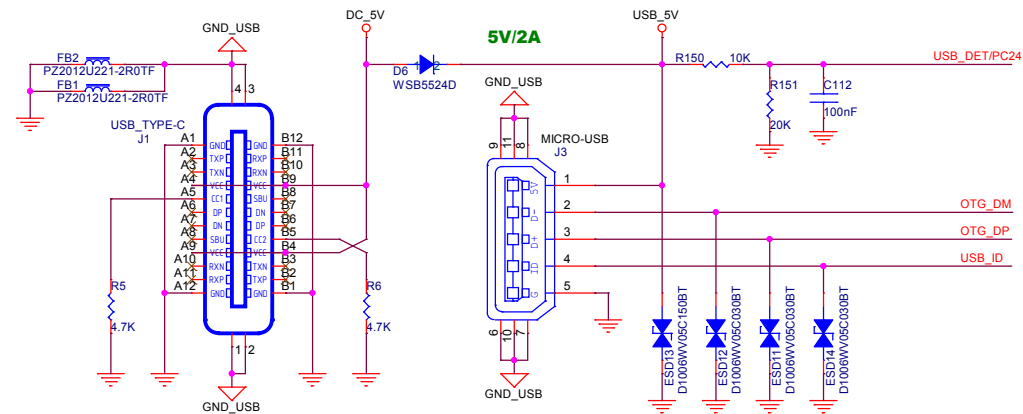
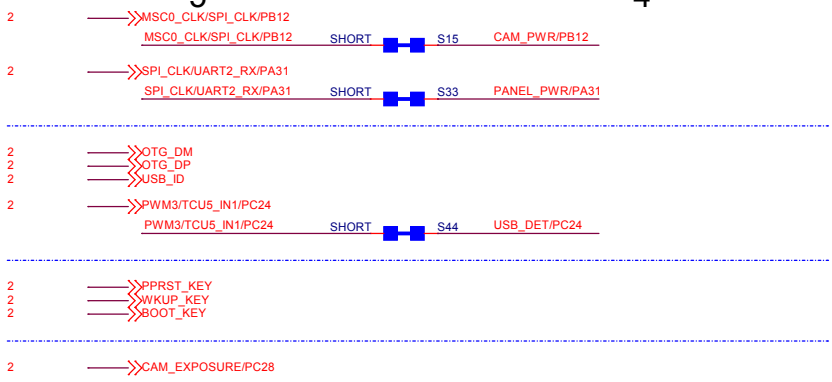
### Schematic Revision 2.0

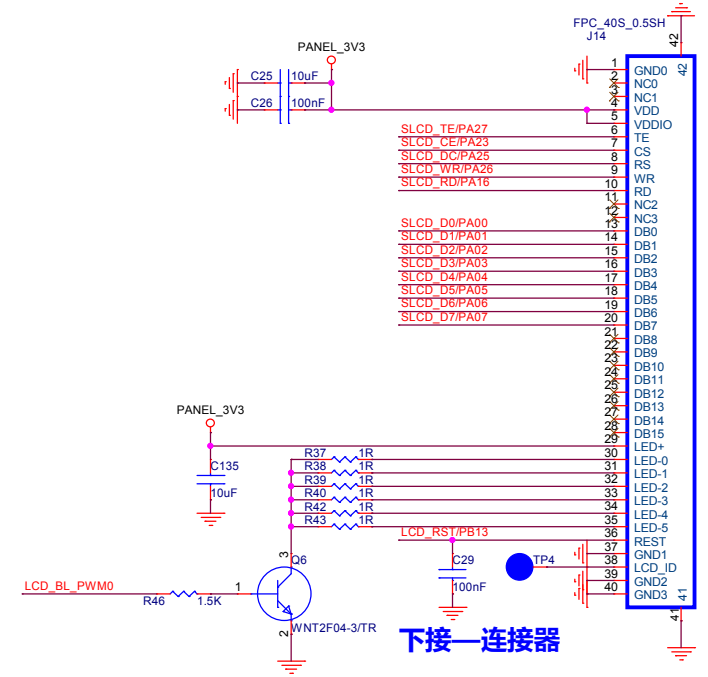
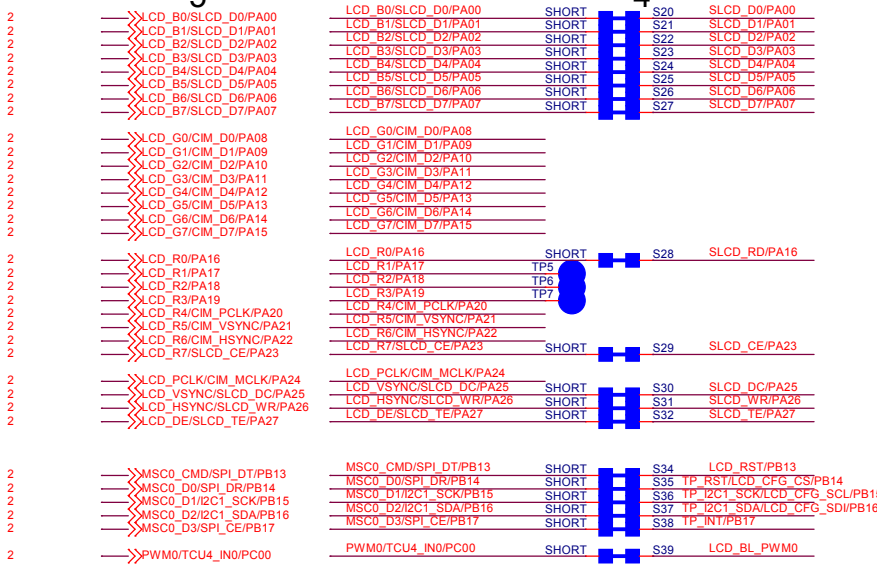
Title	Page
COVER	1
PAGE02_X1600_COREBOARD	2
PAGE03_POWER_USB	3
PAGE04_RGB_SLCD	4
PAGE05_DVP_MIPI_CAMERA	5
PAGE06_BTWIFI_SD_SADC	6
PAGE07_ETH_PHY_DAC_ADC	7
PAGE08_REVISION-HISTORY	8

#### Ingenic Schematic

Title		
HALLEY6_BASEBOARD_V2.0		
Size	Document Number	Rev
A3	<Doc>	V2.0
Date: Wednesday, January 05, 2022		
Sheet 1 of 9		

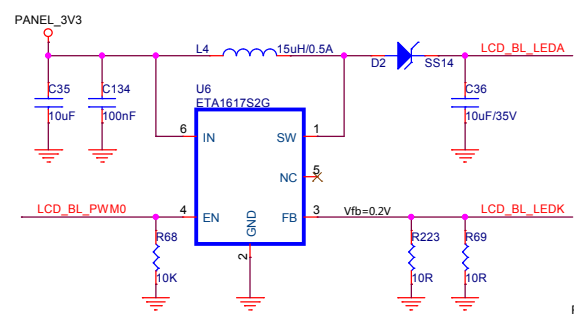




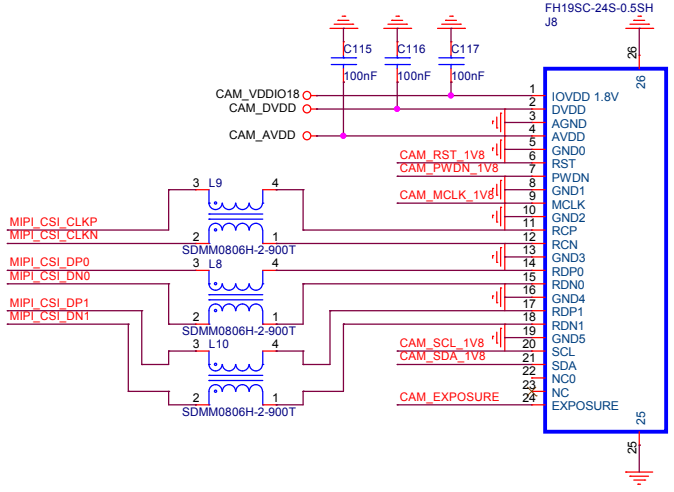
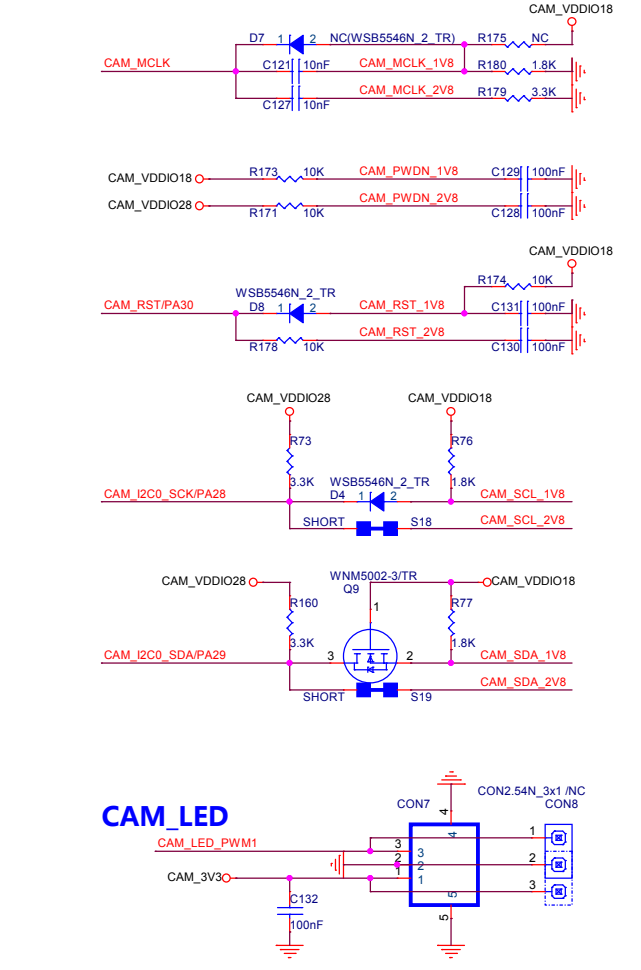
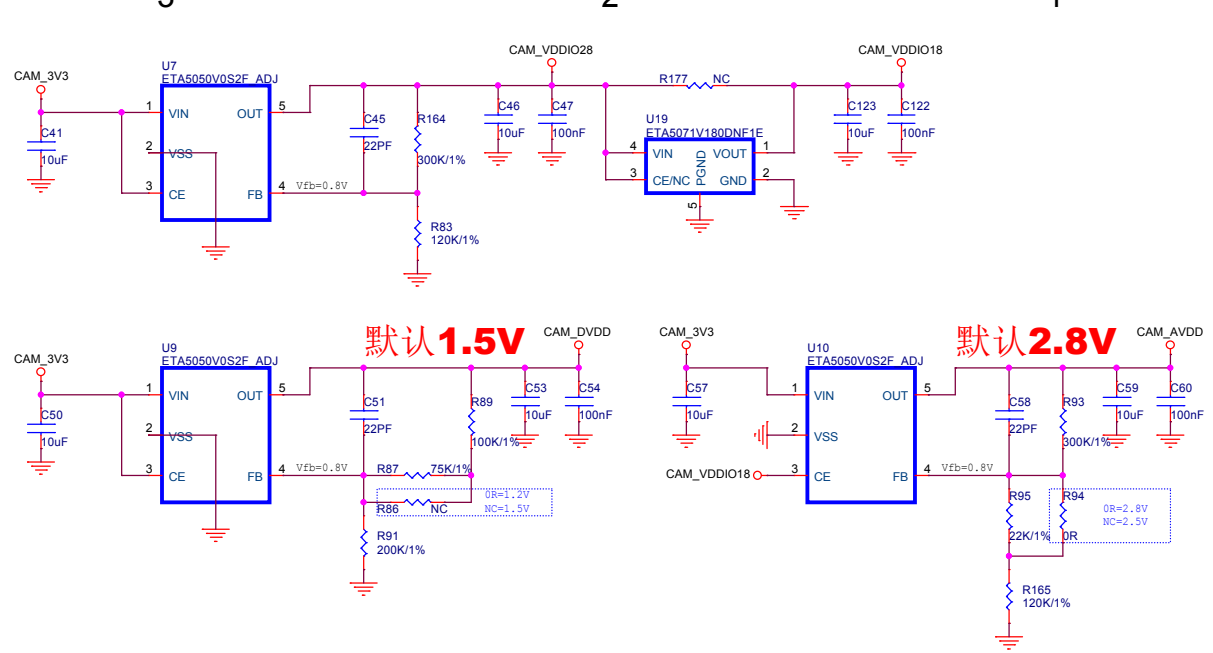
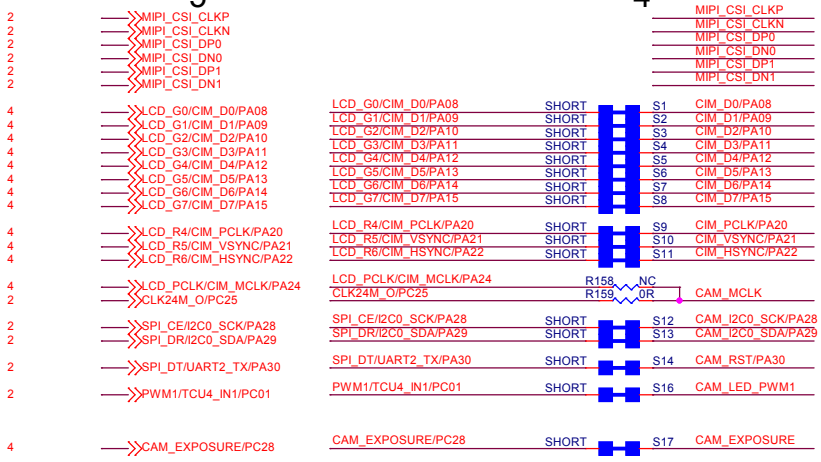


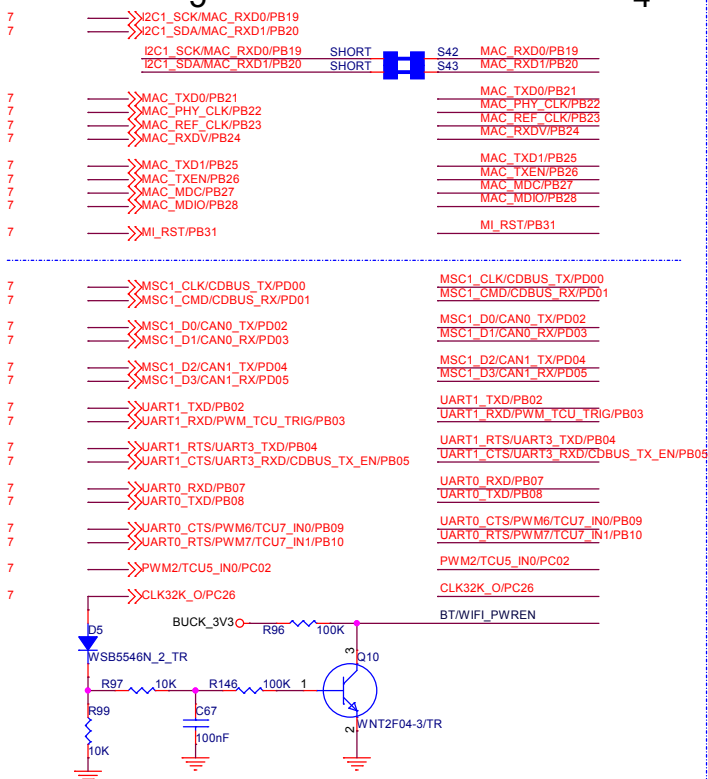
下接一连接器

上接一连接器

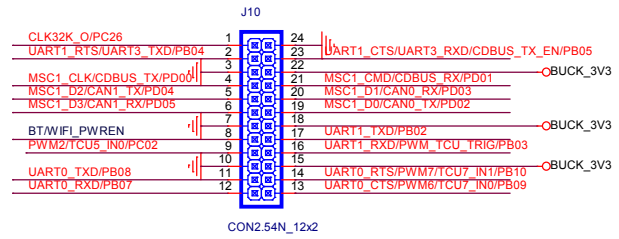


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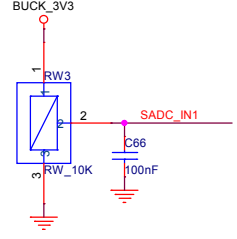
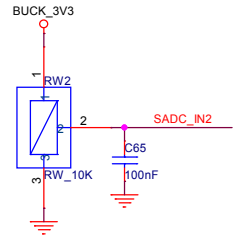
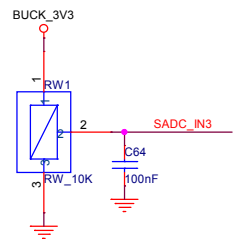




## BT/WIFI(UART\_MSC\_CDBUS\_CAN\_PWM\_TCU)

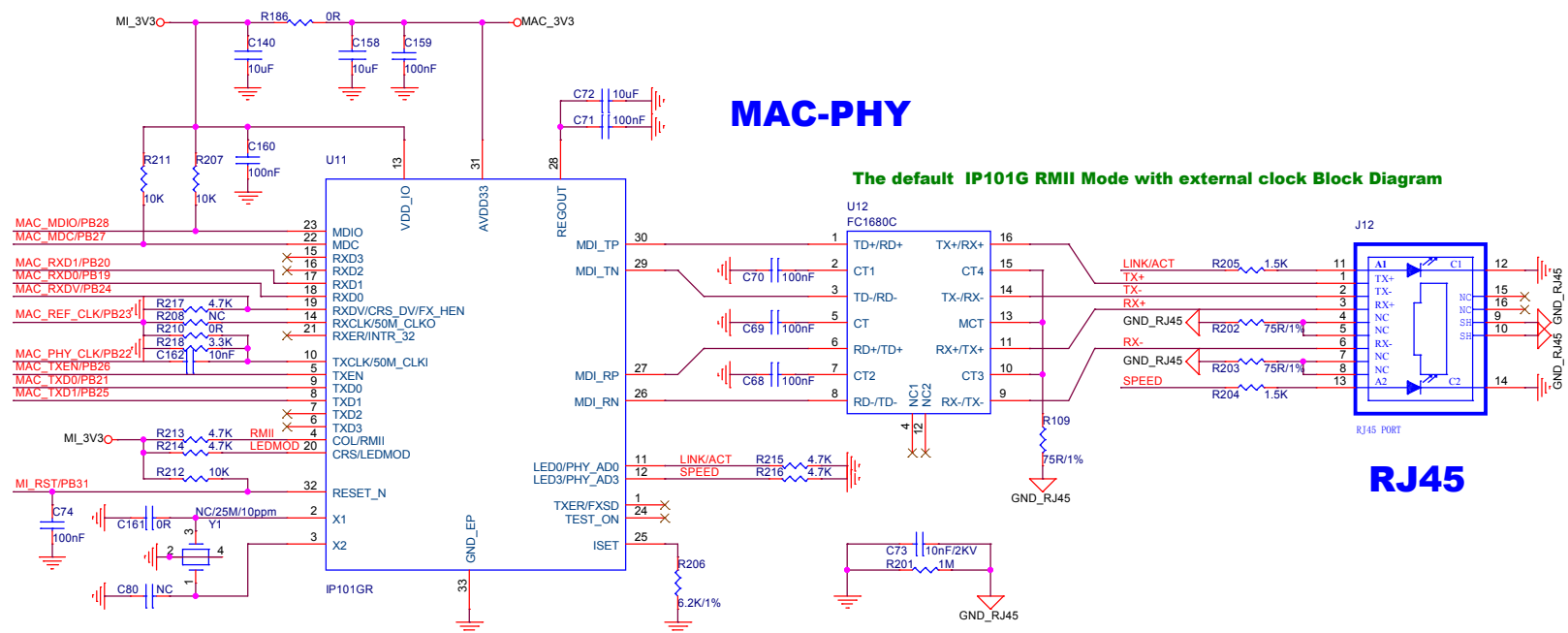


## ADC

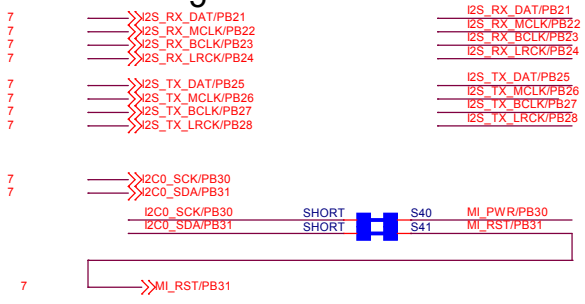


## MAC-PHY

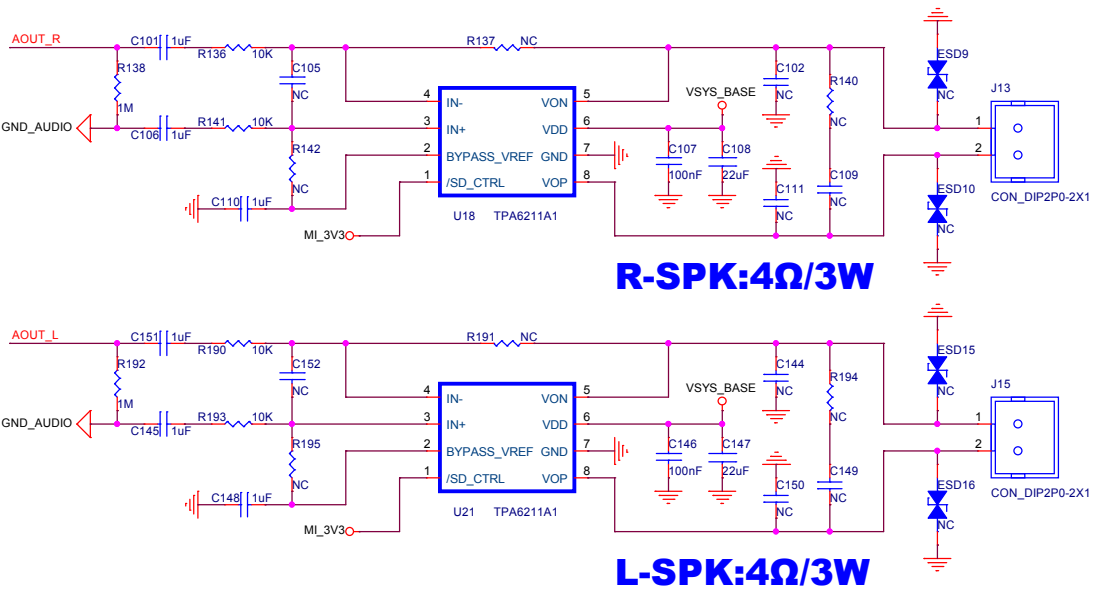
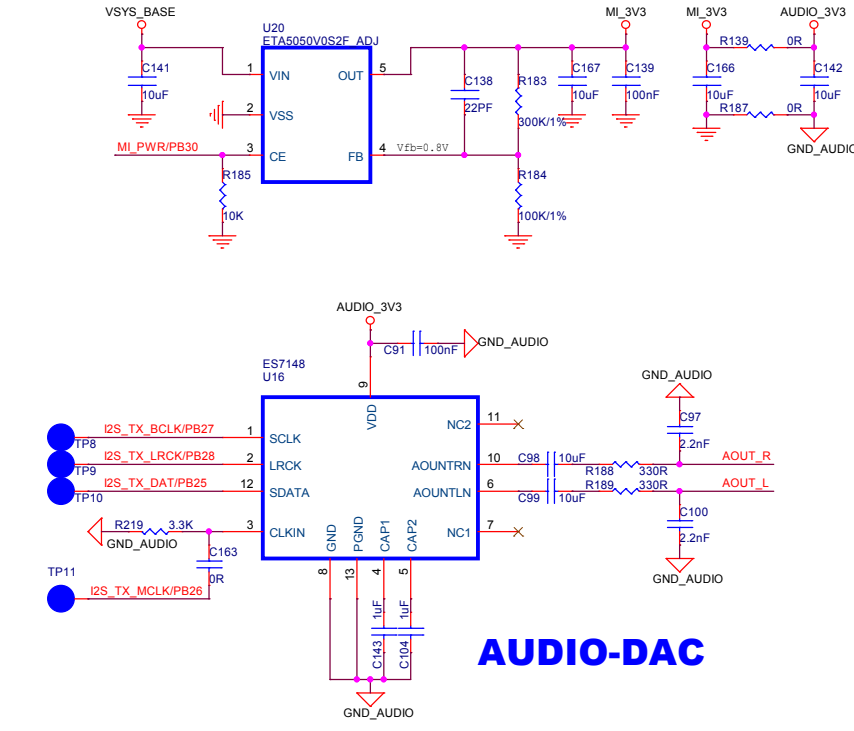
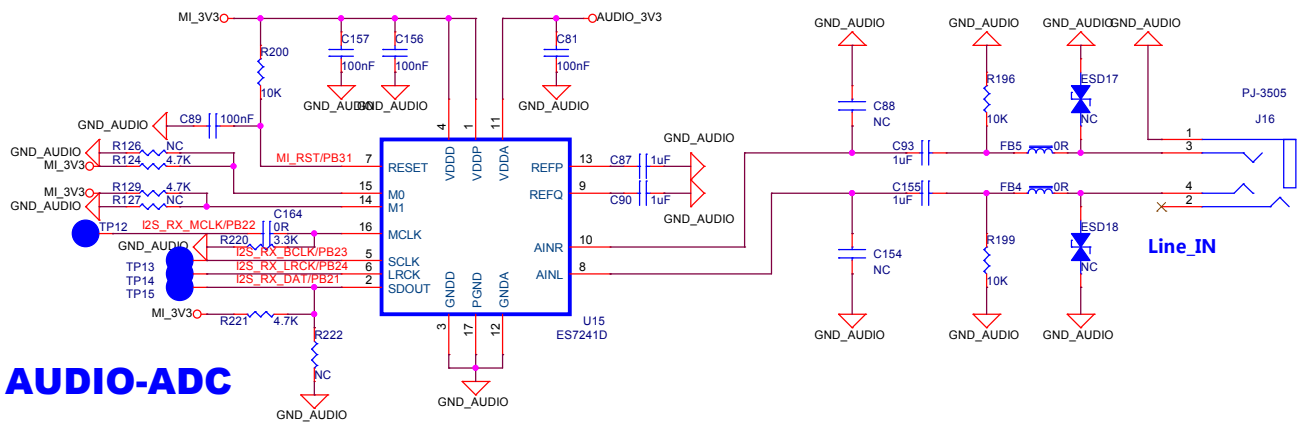
The default IP101G RMII Mode with external clock Block Diagram



## Ingenic Schematic



M1:M0	DESCRIPTION	SAMPLING	MCLK/LRCLK RATIO	
00	Single speed (Master-CLK)	8-50KHz	256	256,384,512,768,1024
01	Double speed (Master-CLK)	50-100KHz	128	128,192
10	Quad speed (Master-CLK)	100-200KHz	64	64
11	All speed (Slave-CLK)			



Date	Revision	Change
2021.08.04	V1.0	1. First Revision
2022.01.05	V2.0	1. AMIC接口改为LINE IN(J16) 输入 2. 更新RW1,RW2,RW3的封装  3. 删除L5  3. 模块接口M3, 30#删除GND,预留3.3V输出