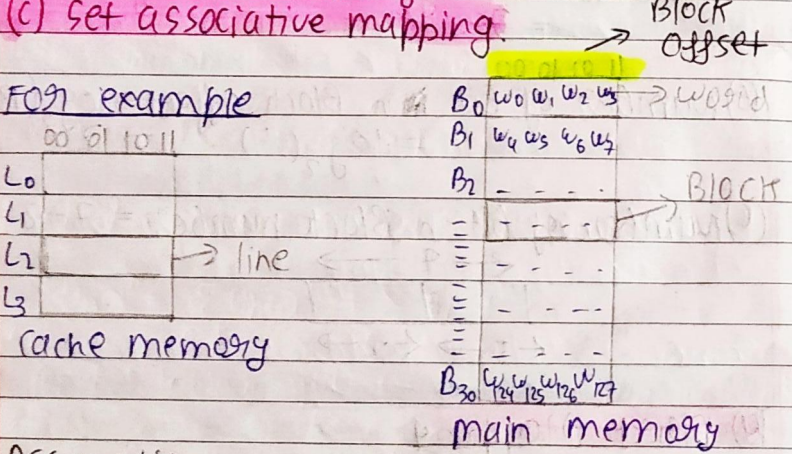
so that

(a) Small enough, frequent replacement of data
(b) large enough, so that store more data

(vii) cache memory mapping

cache memory mapping is a mechanism by which data (Block) of main memory copy into line of cache memory

Types of mapping
(a) Direct mapping
(b) Associative mapping
(c) Set associative mapping.



For example

Assumption
(i) main memory size = 128 words
(ii) main memory Block size = 4 words
(iii) cache memory size = 16 words
(iv) cache memory = main memory = 4 words
line size Block size

calculation from Assumption
(i) Total number of Block in main memory = $\frac{128}{4} = 32$

COA unit4

Topic - cache memories

(i) Small-sized, volatile and high speed memory.
(ii) Present b/w → Processor and main memory
(iii) Store - frequently used computer program
frequently used application
frequently used data.

(iv) cache memory Performance

(a) when Processor requests for data and Find the data in cache memory is called cache hit

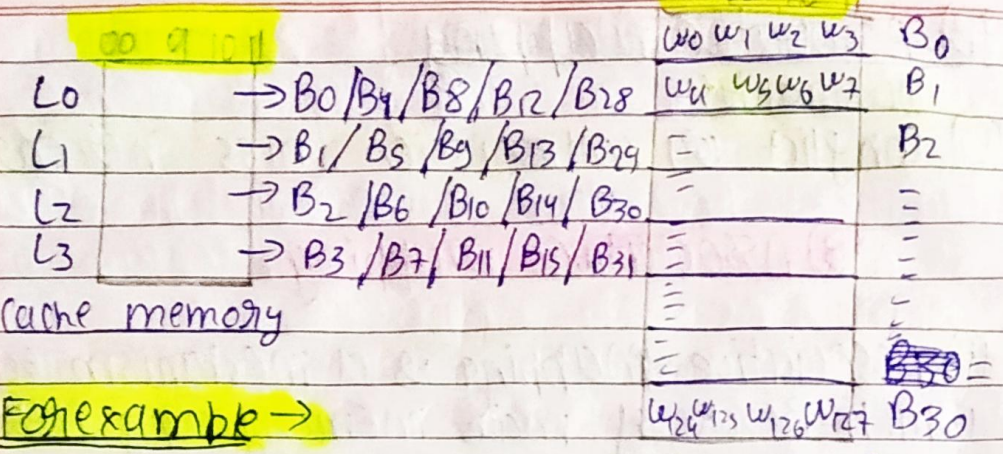
(b) when Processor requests for data and not Find the data in cache memory is called cache miss

(c) cache memory Performance measured in hit ratio = $\frac{\text{cache hit}}{\text{cache hit + cache miss}}$ by running representative program in computer.

(v) cache size

(a) Small enough, so that less expensive
(b) large enough, so that store more data

(vi) Block size / line size

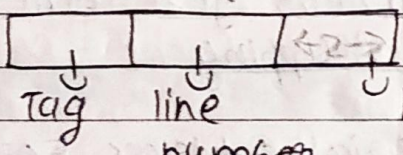


Forexample →

Block number - 0, 10, 7, 31

Ans 0 mod 4 → 0 → line 0
10 mod 4 → 2 → line 2
7 mod 4 → 3 → line 3
31 mod 4 → 3 → line 3

(iii) **Physical address for cache memory By direct mapping :-**



(a) Number of Bit in cache memory Physical address = Number of Bit in main memory Physical address = 7

(b) Number of Bit in line number = $\log_2$(Total number of line) = $\log_2(4) = 2$

(c) Number of Bit in Tag = 7 - 2 - 2 = 3

Tag - carries only a part of bits present in Block number.

(iv) No need of replacement algorithm.

(c) Set Associative Mapping

(i) Set Associative mapping is a mechanism by which Block of main memory copy into line of cache memory

(ii) Mapping function – $K \bmod S = i$
K – Block number (This value change, $B_0 \ldots B_{32}$)
i – cache memory set number.
S_{Total} – Number of Set.

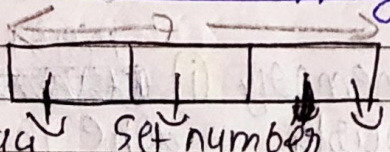
(iii) Set Associative = Direct mapping + Associative mapping

(iv) cache memory line divided into equal number of set

(v) Need of Replacement algo

(vi) Number of set = $\frac{\text{Total number of lines}}{K} = \frac{4}{2} = 2$

(vii) Physical address for cache memory By Set associative mapping



(a) → Same as in Associative mapping.
(b) Number of Bit Block offset = $\log_2$(Block size) = 2
(c) Number of Bit in Set number = $\log_2$(Number of set) = $\log_2(2) = 1$
(d) Number of Bit in Tag = 7 – 2 – 1 = 4

(iii) Give Better performance for small number of updation

(iii) Give Better performance for large number of updation

(iv) If There is a read miss in cache
(a) whole Block will move from main to cache memory
(b) Then requested word send to Processor

If There is a write miss in cache update the main memory

(iv) If There is a read and write miss in cache memory
(a) whole Block will move from main to cache memory
(b) The requested word send to Processor.

(x) Replacement algorithm in cache memory

Replacement algorithm is a algorithm to replace cache line with new memory Block from main.

These algorithm are - FIFO
- LRU
- Random select
- optimal replacement

(i) FIFO -

Virtual Memory

(i) Memory management capability of an OS
(ii) Working -

(a) A portion / file of Harddisk reserved

Separate portion - use in linux
Page file or Swap file - use in windows

(b) Principal - (a) Keep currently being use part of program / application in Ram

(b) Keep not currently being use part of program / application in portion / file.

(iii) Provide illussion of large memory to execute - (a) any number of program/application
(b) any size of program/application

(iv) Temporary memory, used only with RAM.