Dynamic Gate Control Based 4-stage Charge Pump

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***Abstract*—This paper presents a study of different control technique-based charge pump (CP) circuits for non-volatile memories. Basically, charge pumps are used to produce a higher voltage than the power supply voltage. The charge pump is a DC to DC converter which uses capacitors as energy storage elements to produce a higher or lower voltage. This paper presents a Charge pump circuit with cross-connected PMOS cells. The expectation of this paper is to achieve the outcome of removing the substrate bias effect and improving the voltage gain by controlling substrate voltage. The control topology-based four-stage Charge-Pump circuits are designed in synopses tools and simulated in 28nm standard CMOS technology.**

I. Introduction

For reduction in power consumption,the power supply voltage tends to be scaled down.It also reduces noise margin and speed of operation, which is not favour in digital circuits.The performance of the low power memory device depends on the mechanisms of oxide tunneling which need constant high voltage irrespective of the MOS technology and scaling.The Charge-Pump circuit provides higher on-chip voltage with low power supply voltage. The Charge-Pump circuit utilize charge transfer switches (CTS) for transferring charges and pumping capacitors as energy storage elements.The series connected capacitors are resulting in high voltage gain because of lower output impedance as the number of stages increase.The substrate-bias effect of Charge Transfer Switches in the Charge-Pump circuit in a single n-well CMOS fabrication process causes their threshold voltages to increase which leads to degradation of Voltage gain.

II. Circuit Design

The voltage gain of the Charge-Pump circuit Substrate control is designed with two auxiliary PMOS to control the substrate of charge transfer switch in each stage of Charge-Pump this removes substrate bias effect and limits further increment of the threshold voltage of Charge Transfer Switches in higher stages of the Charge-Pump circuit.The dynamic gate control is provided by one PMOS and one NMOS. In dynamic gate control based Charge-Pump the gate terminal voltage of Charge Transfer Switches PMOS is controlled to reduce the ON resistance of the Charge Transfer Switches PMOS. the body terminals of all the PMOS in the second stage are connected to common node which is at the highest potential in this state. Thus removing body effect in all the PMOS in the second stage and threshold voltage of Charge Transfer Switch PMOS P2 remains constant and Reducing the ON Resistance will increase Gain and efficiency.The circuit above Fig 1 solve substrate bias issue in Dickson Charge-Pump and the expected output waveform is mentioned in this figure Fig 2.All the reference Material are used from these 3 papers [1–3].

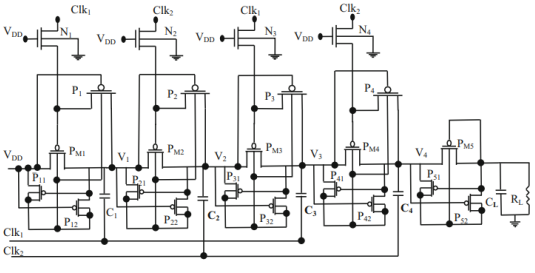

Fig. 1. Dynamic gate control based 4-stage charge pump.

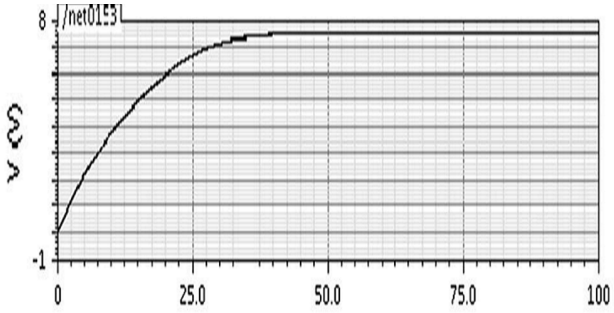

Fig. 2. Expected Waveform for input voltage of 1.8 ,operating frequency of 10 MHz, output resistance 1 MΩ, output load capacitance 40 pF, pumping capacitance of 20 pF,CLKHIGH = 1.8 V and CLKLOW = 0 V.

References

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