Positive Edge triggered D Flip Flop using Clocked MOS logic (Dynamic)

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Abstract

Positive Edge triggered D Flip Flop using Clocked MOS logic (Dynamic) This circuit has a great advantage over the conventional CMOS or Pass Transistor. We have used a Two-phase clock that is nonoverlapping routing delay would not cause clock skew. The implemented logic function or the logic gate is achieved through 2 modes of operation: Precharge and Evaluate. The number of transistors required here is less (N+2) than 2N in the Static CMOS circuits. This circuit is still a ratio-less circuit as in the case of Static. The static power loss is very less in a dynamic logic circuit and has a faster switching speed because of lower load capacitance.

1 Reference Circuit Details

The total count of the transistor is 12 along with an inverter with 2 transistors to provide a complimented clock the supply voltage that has been used is 5 volt along with 2 capacitors with 1pf capacitance two clocks signal are provided with one being complimented form of other i.e Two-phase clock. The circuit behaves in master-slaves combination when clock=0 Master stage is ON and it samples data at Qm=D along with that slave stage is OFF it holds its previous stage when the clock=1 the Master stage is OFF it will hold its previous stage while slave stage will be ON and it will process the data of Master Stage Qs=Qm. The circuit is positive-edge triggered since it samples the data at the rising edge of the clock.

2 Reference Circuit

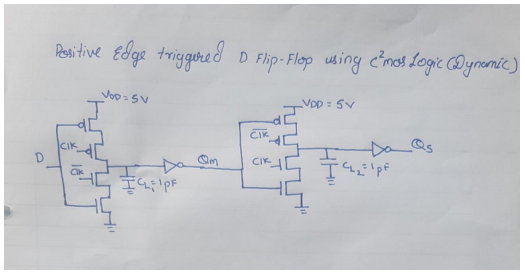

Figure 1: Reference circuit diagram.

3 Reference Circuit Waveforms

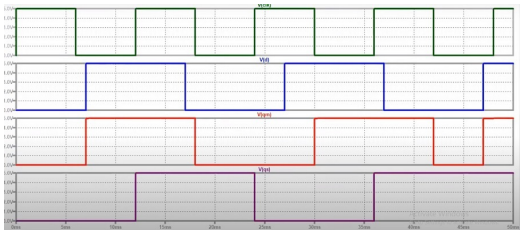

Figure 2: Reference waveform.

References

[1] D. E. Azab. Integrated circuit design. https://eee.guc.edu.eg/Courses/Electronics/ELCT701%20Integr

[2] I. S. Dhanjal. Master-slave positive edge triggered d flip-flop using clocked cmos logic. https://www.youtube.com/watch?v=oOgEtQfoajs&t=926s.

[3] poonam kadam. Vlsi deisgn. BOOK.