Positive Edge triggered D Flip Flop using Clocked MOS logic (Dynamic)

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Abstract

Positive Edge triggered D Flip Flop using Clocked MOS logic (Dynamic) This circuit has a great advantage over the conventional CMOS or Pass Transistor. We have used a Two-phase clock that is nonoverlapping routing delay would not cause clock skew. The implemented logic function or the logic gate is achieved through 2 modes of operation: Precharge and Evaluate. This circuit a ratio-less circuit. This circuit faster-switching speed because of a lower load capacitance of 0. 0001uf.In total 14 transistors are used and I have set the internal complemented clock. The problem of clock slew and race around condition is now solved the only disadvantage of this circuit is the dependence on the complemented clock.

1 Circuit Details

The total count of the transistor is 14 along with an inverter with 2 transistors to provide a complimented clock. The supply voltage that has been used is 5 volt along with 2 capacitors with 0.0001uf capacitance for Precharge and Discharge the voltage value at this capacitor is crucial because they determine speed, leakage power, area, and output of the circuit. two clock signals are provided with one being complimented form of other i.e Two-phase clock. The circuit behaves in master-slaves combination when clock=0 Master stage is ON and it samples data at Qm=D along with that slave stage is OFF it holds its previous stage when the clock=1 the Master stage is OFF it will hold its previous stage while slave stage will be ON and it will process the data of Master Stage Qs=Qm. The circuit is positive-edge triggered since it samples the data at the rising edge of the clock. The technology used over here is 130nm with pfet and nfet length mentioned in cir file are length 1 and width 0.5 and latter length 0.42 and width 0.5 . The clock parameter are as follows Vintial 0 Von 5 Tdelay 7 ms Trise 10ps Tfall 10ps Ton 10ms Ttotal 20ms Ncycles infinite similarly D input clock parameters are Vintial 0 Von 5 Tdelay 0s Trise 10ps Tfall 10ps Ton 6ms Ttotal 12ms Ncycles infinte. A transient analysis was done for 100ms with a step size of 0.002ms.
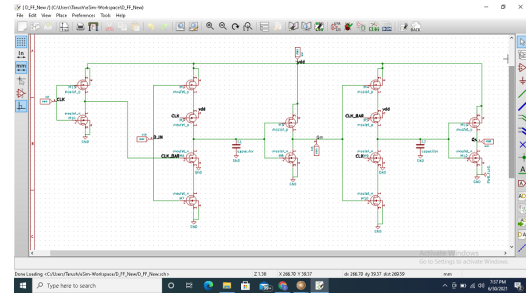
2 Implemented Circuit

Figure 1: Implemented circuit diagram.
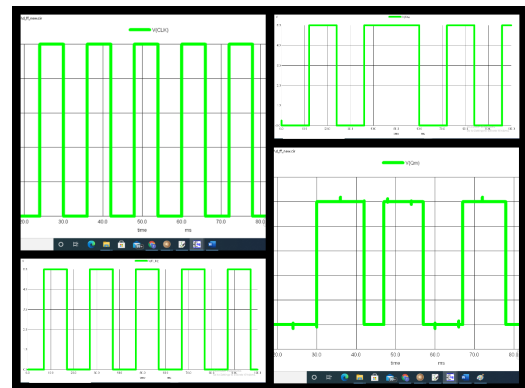
3 Implemented Waveforms

Figure 2: Implemented waveform.

References

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