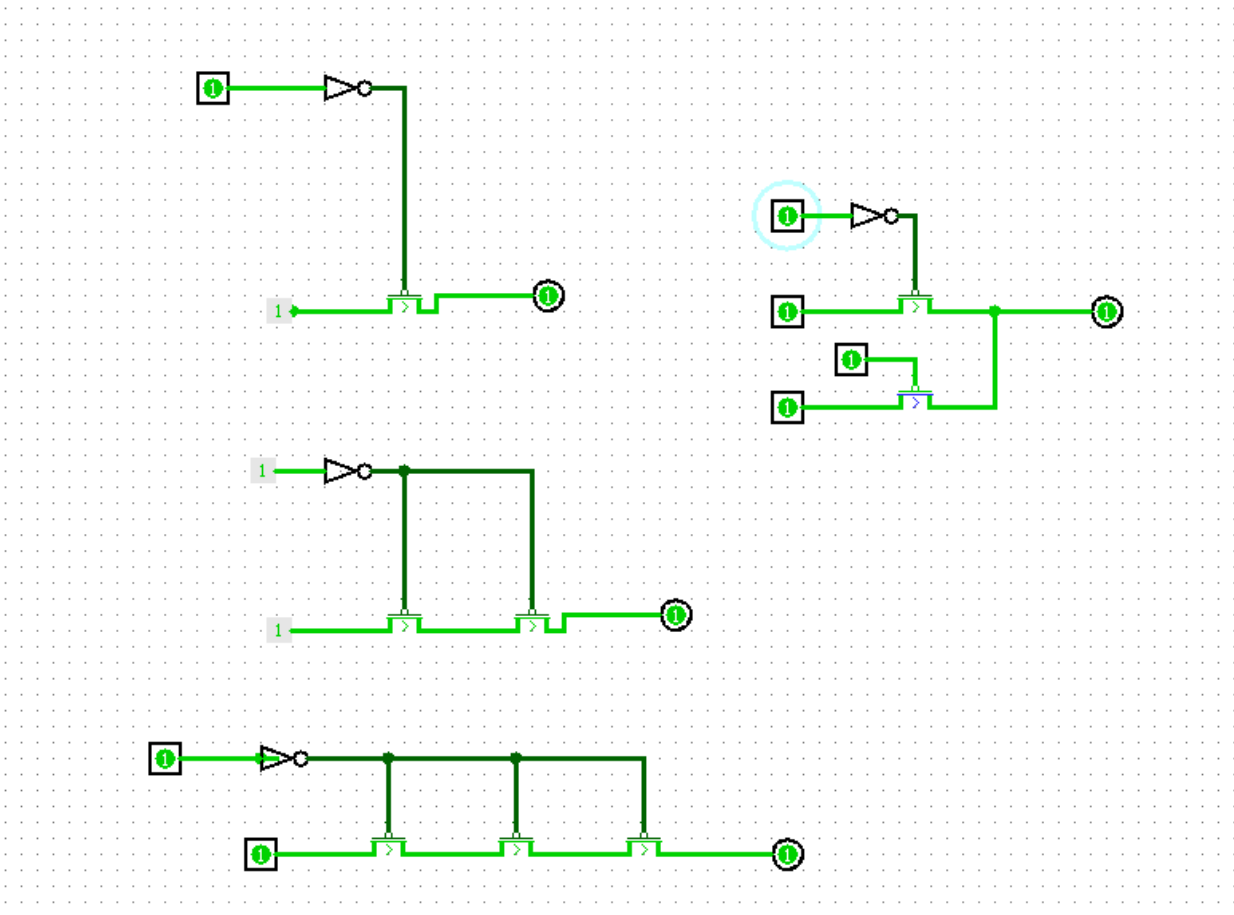


Lab 1: Logic simulation Sub-blocks

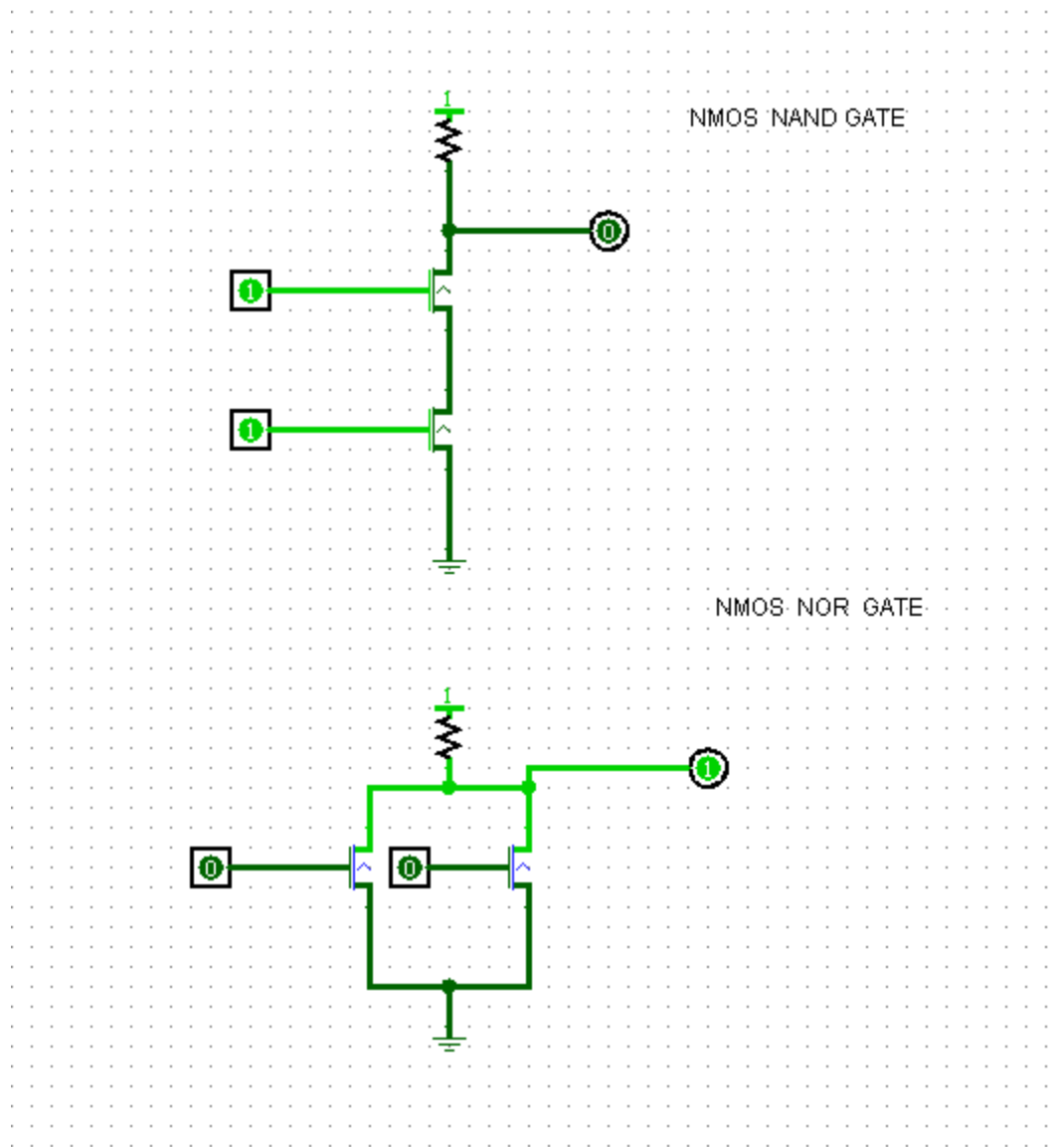
Exercise 1 (series parallel structures):

Simulate the following structures:

(Follow Lab1 steps to simulate)



Exercise 2 (NMOS gates):



Assignment:

(Design and simulate)

1. Create series structure with 4 PMOS transistors and verify the functionality (Assume A, B,C, and D are the inputs). **(5 points)**
2. Using NMOS logic, create 5 input NAND, NOR, AND and OR gates. **(10 points)**
3. Implement the following using CMOS Logic.
$$Y = \overline{AB + CD + E}$$
(10 points)
4. Implement the following using CMOS Logic.
$$Y = AB + CD + E$$
(5 points)
5. Create a library of gates (NAND, NOR, AND, OR, XOR) from the Lab 1 and implement the following using your library(See tutorial sub-circuits). $Y = AB + C$ **(15points)**
6. Implement and verify the functionality using existing library of Gates in logic-sim
 $Y = A + BC + D$ **(5points)**

Submission:

Submit your .circ file containing your various transistor-level/logic level implementations.

- The simulation files p1.circ, p2.circ, p3.circ, p4.circ, p5.circ and p6.circ
- Zip the above five files. Zip file name is your role number.

Course work submission through

<https://u.pcloud.com/#page=puplink&code=dla7ZryX8KQJqyj4J1iTVRnHiSYlkYbhV>

(use email subject Lab1_Logicsim_your roll number).

This work is due on: : 19th January, 11 PM