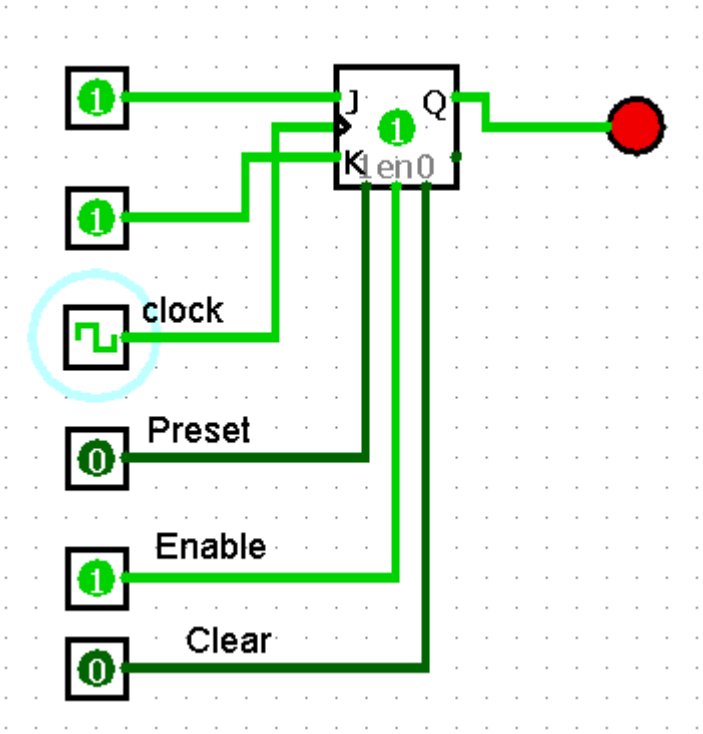
INDIAN INSTITUTE OF TECHNOLOGY PATNA

CS226-Lab6

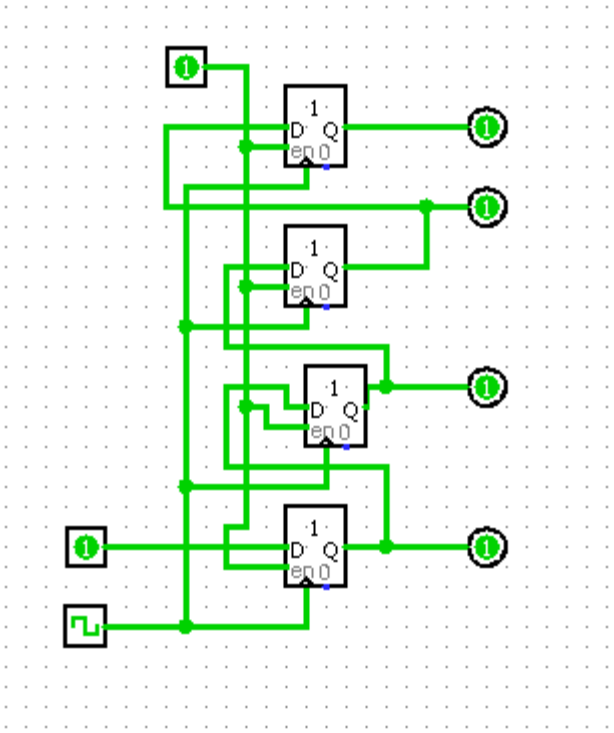
(Sequential Logic Design)

Q0: Study basic sequential elements SR, J-K ,T and D flip flops.

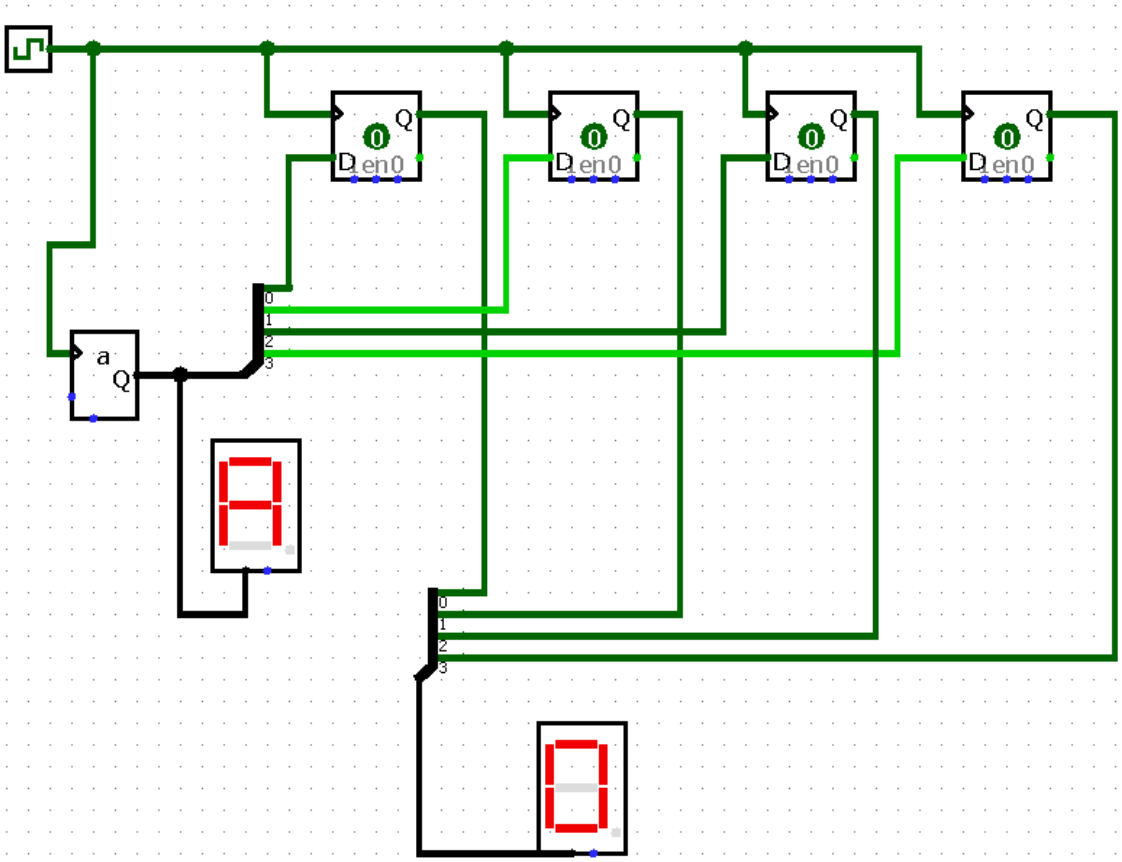
Eg. J-Kexample is shown here. Test all possible input combinations for each of the memory elements.



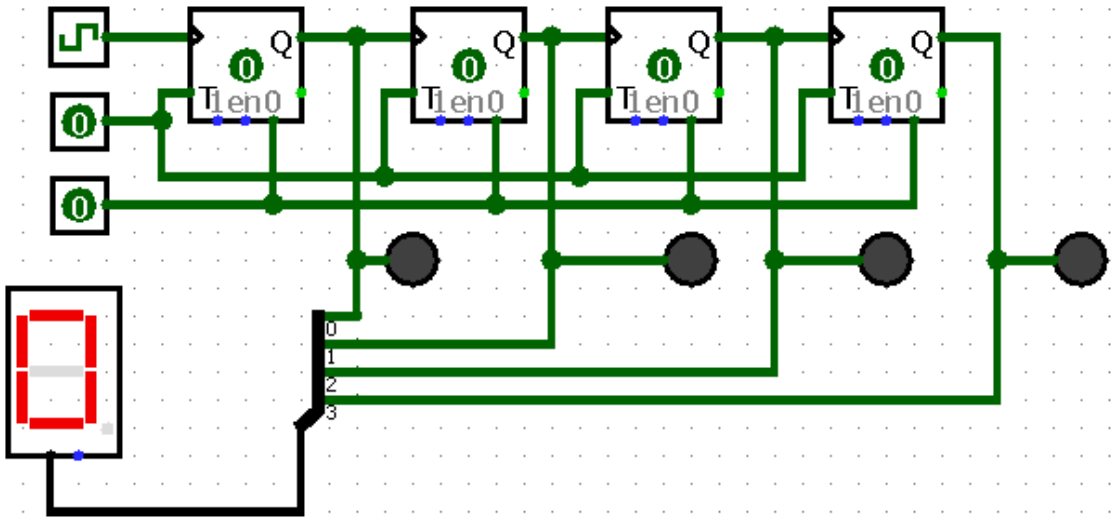
Q1: Simulate a 8 bit shift register using logic-sim. A 4 bit shift register design is shown. Display using both LEDs and Hex digit Display.



Q2: Simulate a 4 bit parallelin Parallel out(PIPO) register. Design a 4 bit parallel in Parallel out(PIPO) register.



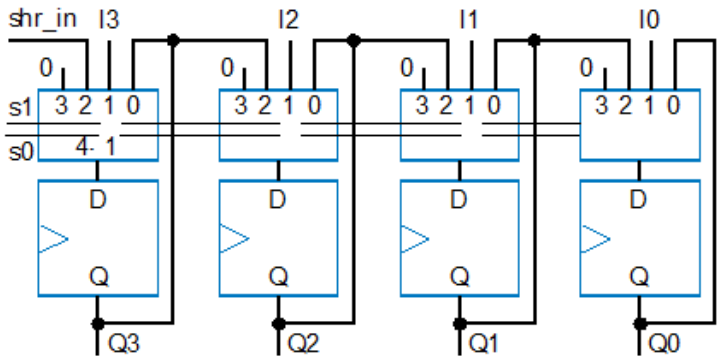
Q3: Simulate a 4 bit counter using T flip flops. Design a 6 bit counter using T flip flops



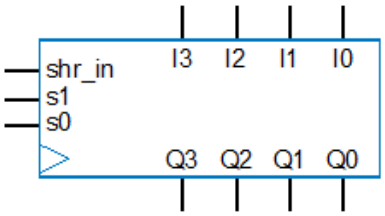
Q4:Simulate the multi-function Shift register using logic-sim. Design an 8 bit version.

Functions:

s1	s0	Operation
0	0	Maintain present value
0	1	Parallel load
1	0	Shift right
1	1	(unused - let's load 0s)

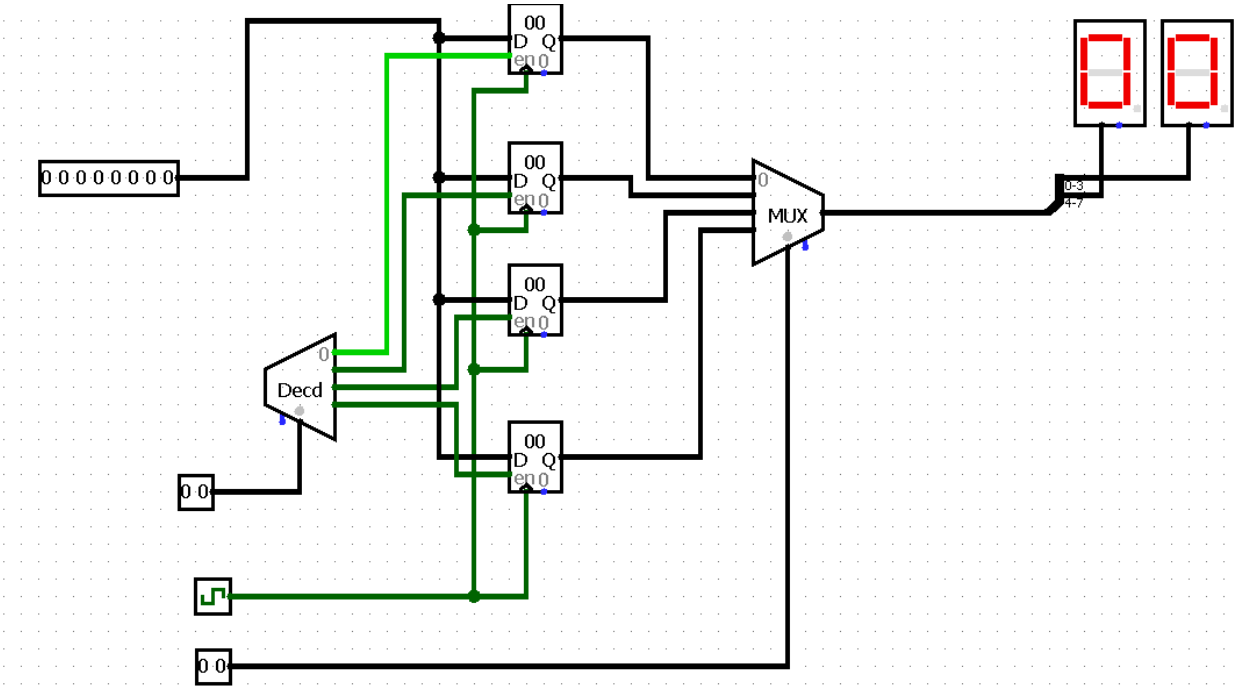


(a)



(b)

Q5: Here a 4x8 register file is shown. Design a 16x16 register file (include register file enable)



Submission:

- **Simulation report** (screen shots of design and simulation output). The simulation files Q0.circ, Q1.circ, Q2.circ, Q3.circ, Q4.circ, and Q5.circ

- Zip the above files. file name is your role number.

Course work submission through:

https://u.pcloud.com/#page=puplink&code=AVc7Zy0Yc92Ob0QhGFVb2SU73rmb0XWcy

This work is due 16th March 11.30 PM.