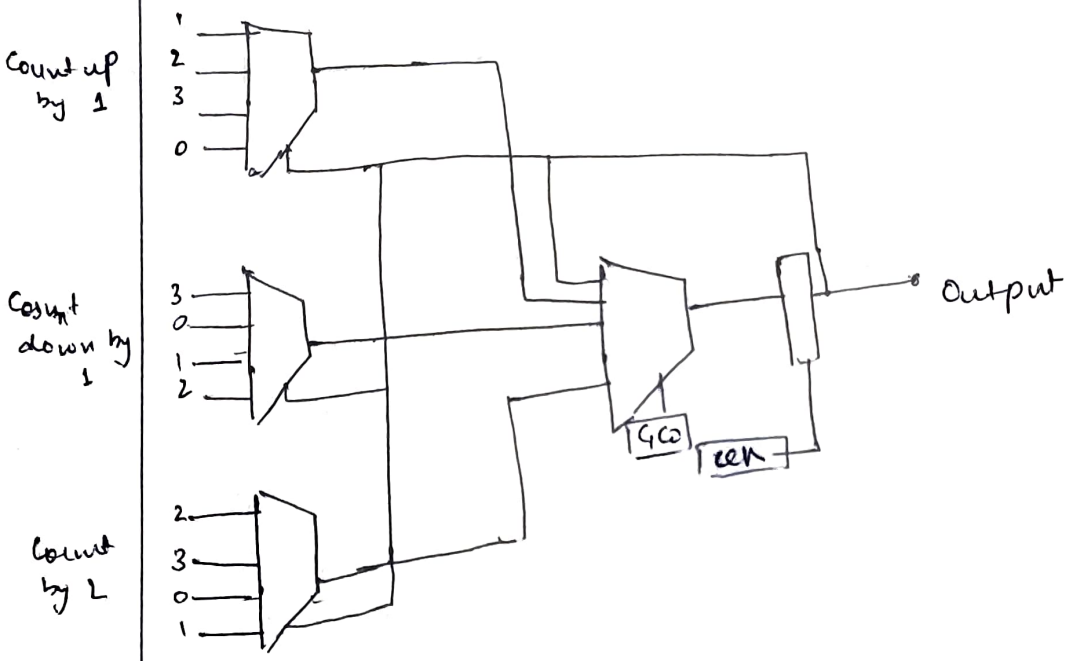
TARUSI MITTAL
19015565

REPORT

Que 1:-

I_1	I_0	Function
0	0	Stop Count
0	1	Count up by 1
1	0	Count down by 1
1	1	Count by 2



Que 2:- Comparison Between Two Designs

1) Without pipeline registers:

→ In this case we will get the output instantly ie after only 1 clock cycle. But the throughput of the design is less than that of the design with pipeline registers.

→ There is some delay due to the various gates used.

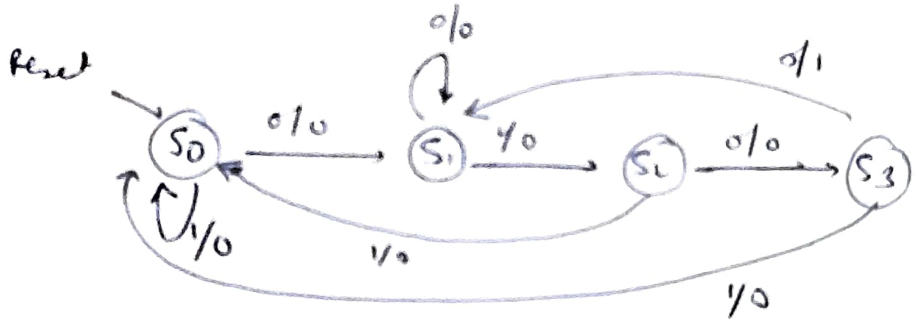
(ii) With pipeline registers.

In this case the delay will be same as that in the above case but the throughput will get doubled because of pipelining. We will get output after every two clock cycle ~~because~~ but throughput is doubled.

Latency is same in both cases

Que 3:-

(i) For detecting 0100.



S_1	S_0	A (Input)	S_1'	S_0'	Output (Y)
0	0	0	0	1	0
0	0	1	0	0	0
0	1	0	0	1	0
0	1	1	1	0	0
1	0	0	1	1	0
1	0	1	0	0	0
1	1	0	0	1	1
1	1	1	0	0	0

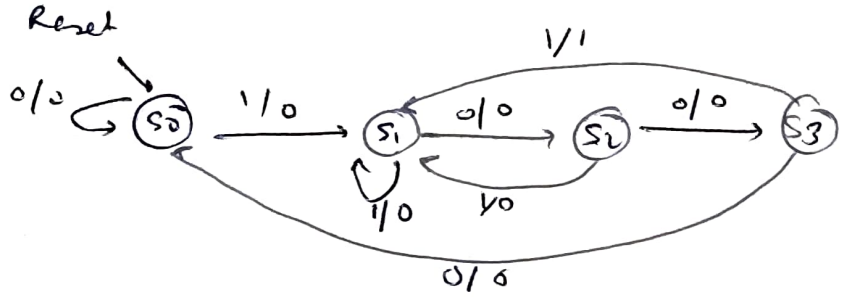
S_0S_1 \ A	0	1
0 0	0	0
0 1	0	0
1 1	0	0
1 0	1	0

$$S_1' = \bar{S_1} S_0 A + S_1 \bar{S_0} \bar{A}$$

$$\bar{S_0} = \bar{A}$$

$$Y = S_1 S_0 \bar{A}$$

(ii) For detecting 1001



S_1	S_0	Input (A)	S_1'	S_0'	Output (Y)
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	0	1	0
1	0	0	1	1	0
1	0	1	0	1	0
1	1	0	0	0	0
1	1	1	0	1	1

S_1S_0 \ A	0	1
0 0	0	0
0 1	1	0
1 1	0	0
1 0	1	0

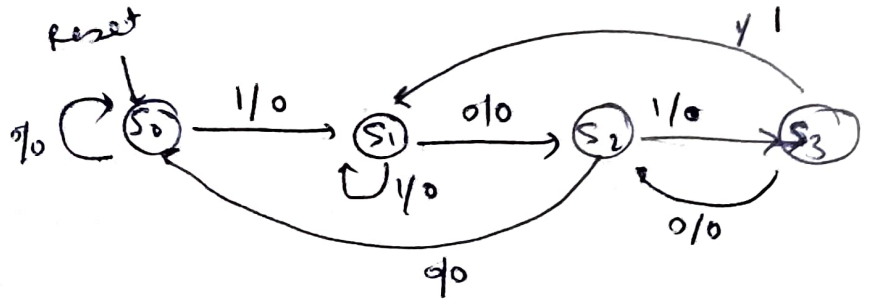
S_1S_0 \ A	0	1
0 0	0	1
0 1	0	1
1 1	0	1
1 0	1	1

$$S_0' = S_1\bar{S_0} + A$$

$$S_1' = \bar{S_1}S_0\bar{A} + S_1\bar{S_0}\bar{A}$$

$$Y = S_1 S_0 A$$

(iii) For detecting 1011.



S_1	S_0	Input (A)	S_1'	S_0'	Output (Y)
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	0	1	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	1	0	0
1	1	1	0	1	1

S_1S_0 \ A	0	1
00	0	0
01	1	0
11	1	0
00	0	1

S_1S_2 \ A	0	1
00	0	1
01	0	1
11	0	1
10	0	1

$$S_1' = S_1\bar{S}_0A + S_0\bar{A}$$

$$S_0' = A$$

$$Y = S_1S_0A$$

→ for detecting either of 0100, 1001 and 1011, we will simply take OR of these three cases.