Question 0:

SR Flip Flop

Clock	S	R	Q(t)	Q'(t)	State
0	X	X	Q(t-1)	Q'(t-1)	Memory
1	0	0	Forbidden		
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	Q(t-1)	Q'(t-1)	Memory

Truth Table
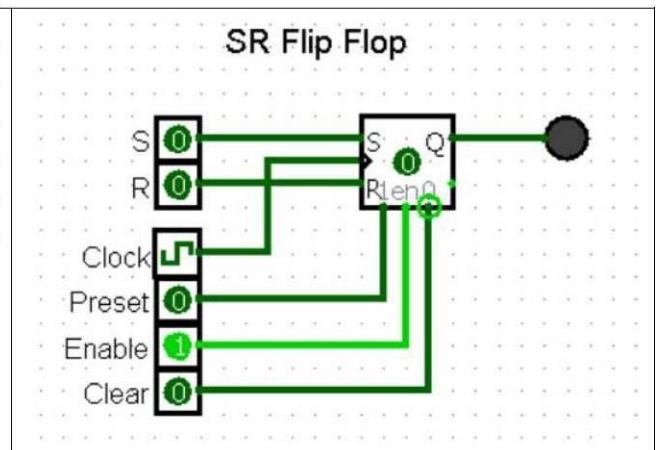
SR Flip Flop

JK Flip Flop

Clock	J	K	Q(t)	Q'(t)	State
0	X	X	Q(t-1)	Q'(t-1)	Memory
1	0	0	Q(t-1)	Q'(t-1)	Memory
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	Q'(t-1)	Q(t-1)	Toggle

Truth Table
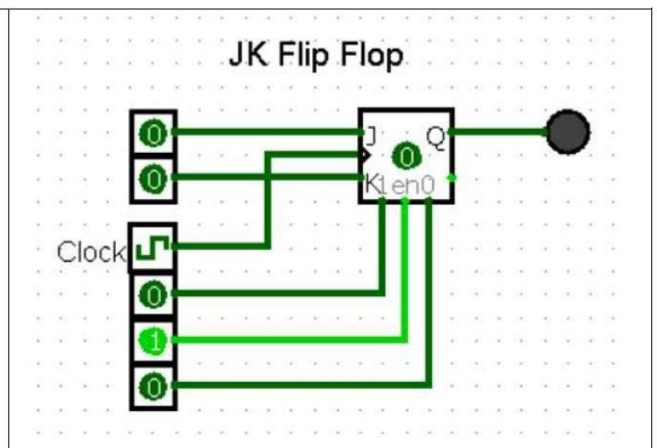
JK Flip Flop

D Flip Flop

Clock	D	Q(l)	State
0	X	Q(t-1)	Memory
1	0	0	Reset
1	1	1	Set

Truth Table

D Flip Flop

Clock

D

Preset

Enable

Clear
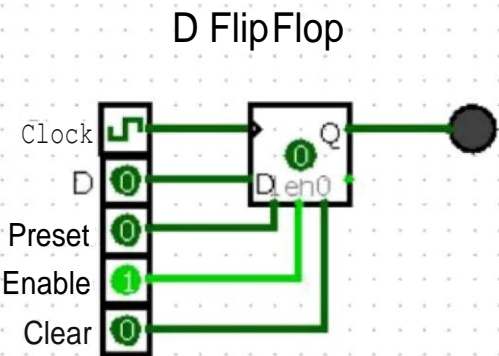
T Flip Flop

Clock	T	Q(l)	State
0	X	Q(1-1)	Memory
1	0	Q(1-1)	Memory
1	1	Q'(t-1)	Toggle

Truth Table

T Flip Flop

Clock
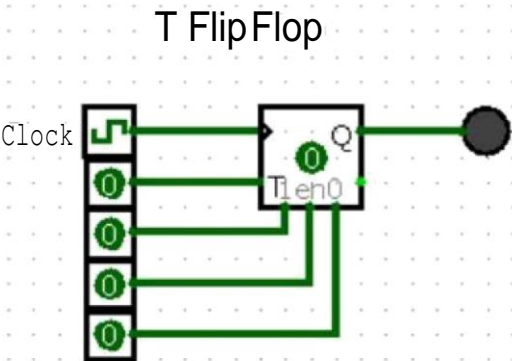
Question 1:

Question 2:

Question 3:

Bit 1 (LSB)   Bit 2   Bit 3   Bit 4   Bit 5   Bit 6 (MSB)

Clock

T 0

Reset 0

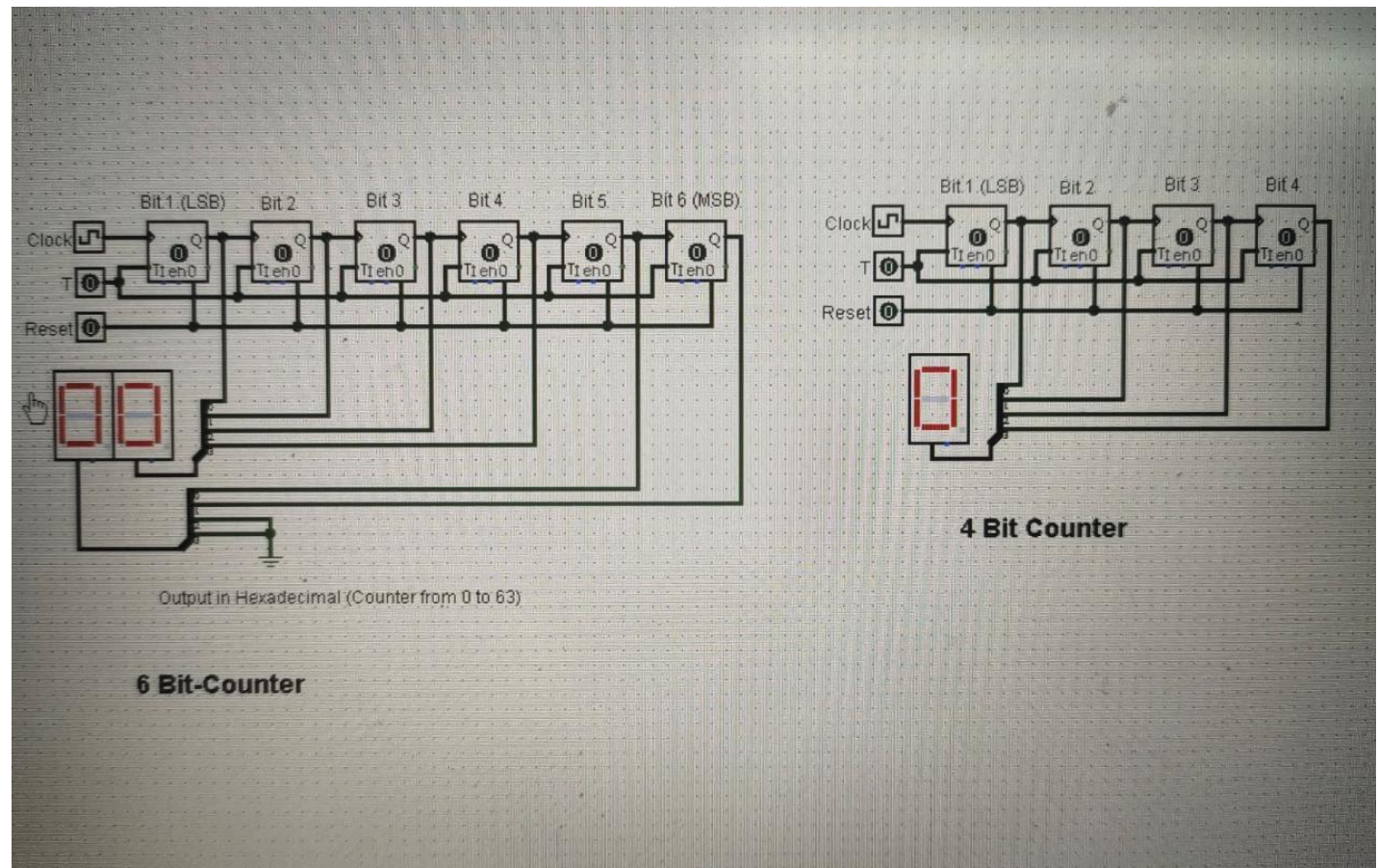Output in Hexadecimal (Counter from 0 to 63)

6 Bit-Counter

Bit 1 (LSB)   Bit 2   Bit 3   Bit 4

Clock

T 0

Reset 0

4 Bit Counter

Bit 1 (LSB)   Bit 2   Bit 3   Bit 4   Bit 5   Bit 6 (MSB)

Clock

T 0

Reset 0

Output in Hexadecimal (Counter from 0 to 63)

6 Bit-Counter

Bit 1 (LSB)   Bit 2   Bit 3   Bit 4

Clock

T 0

Reset 0

4 Bit Counter
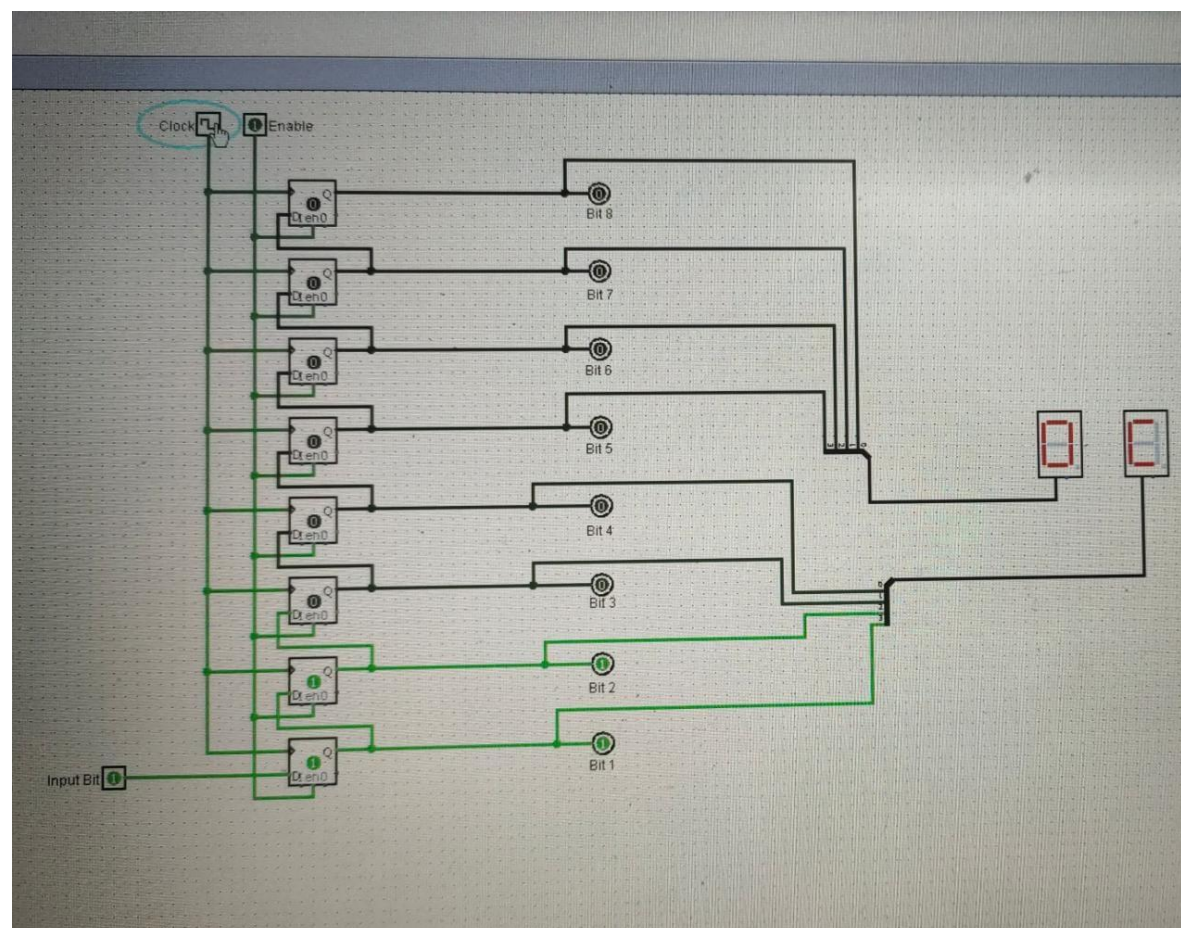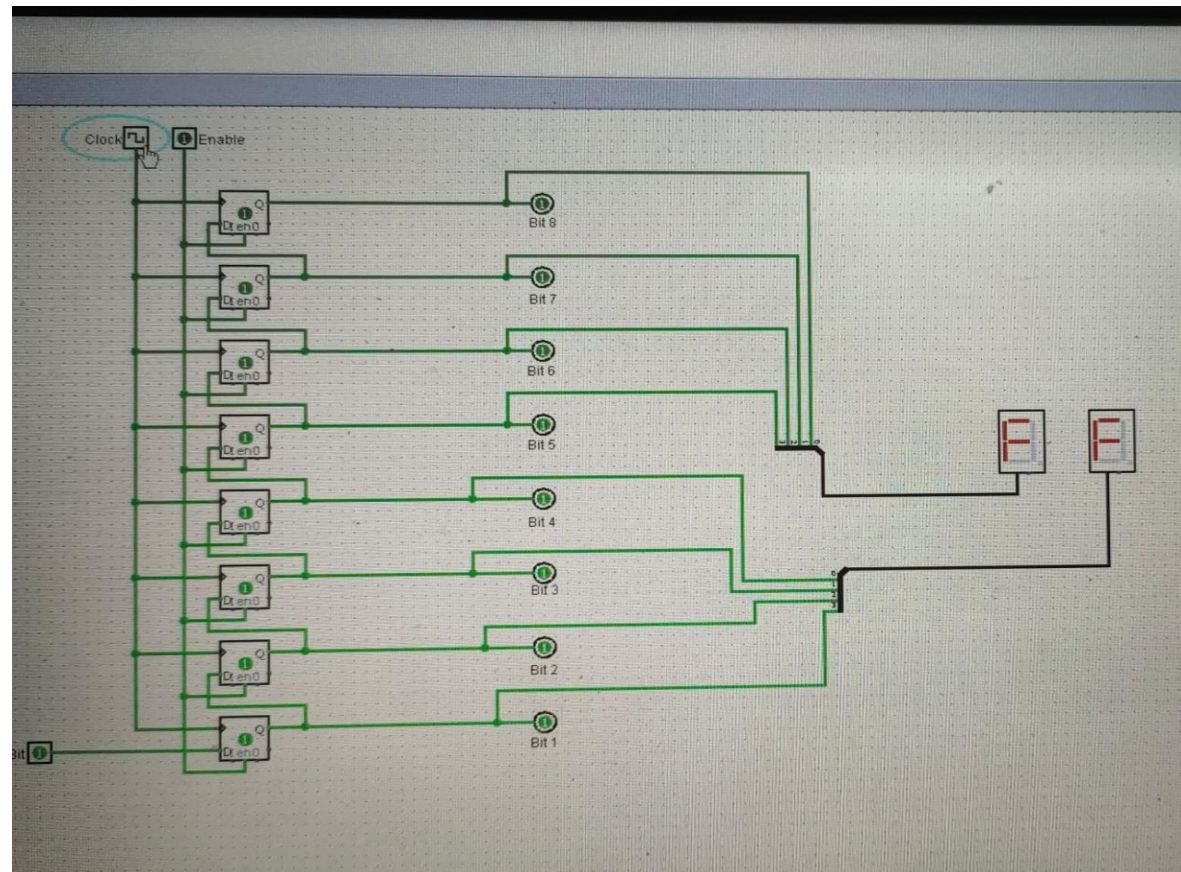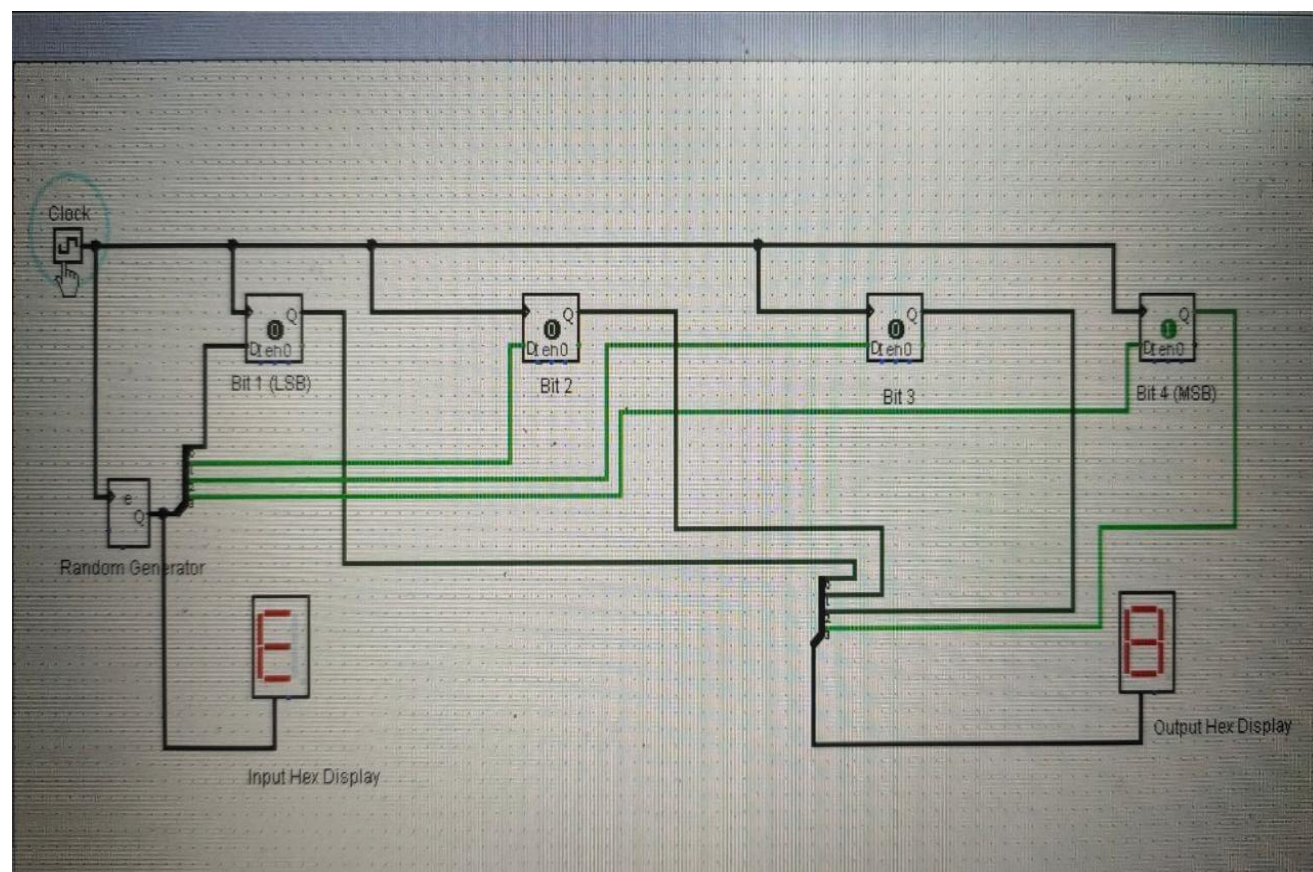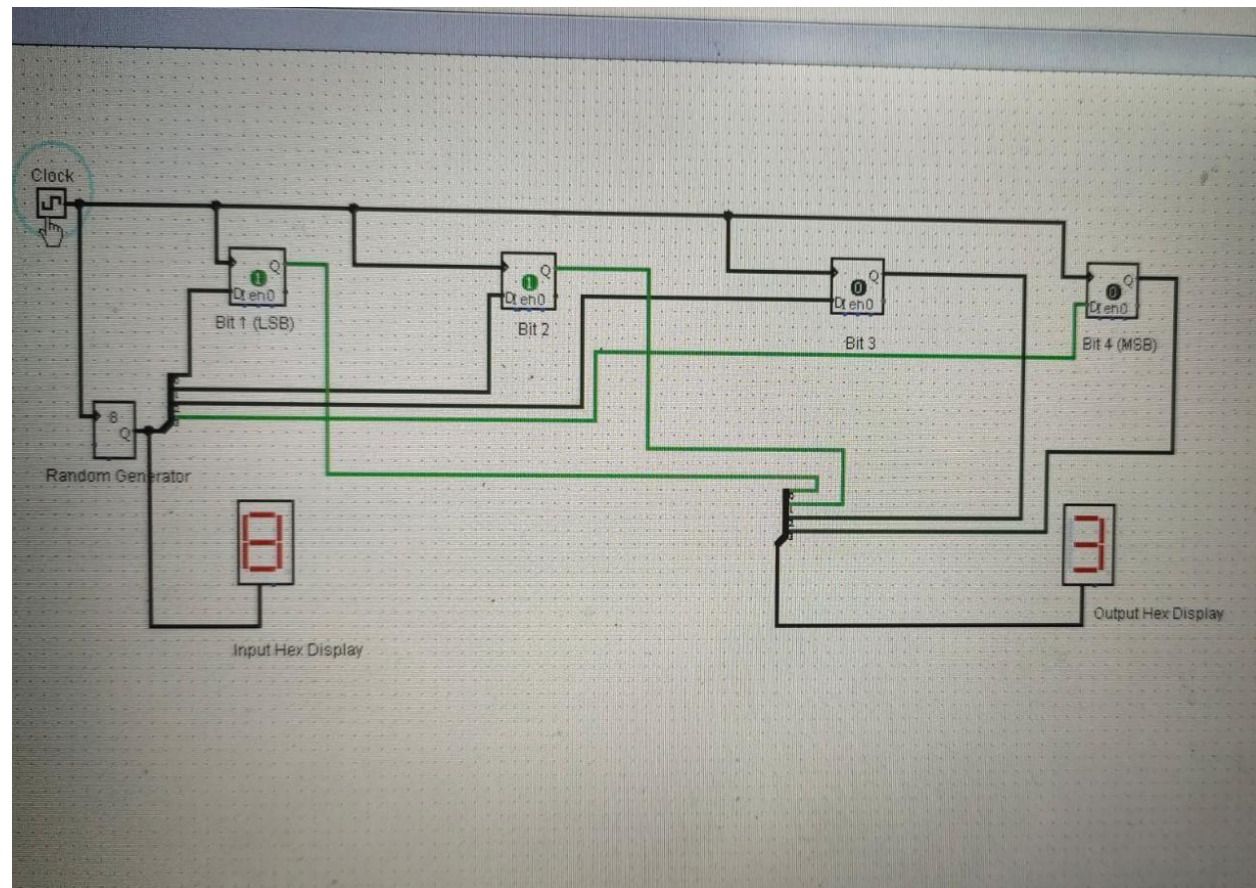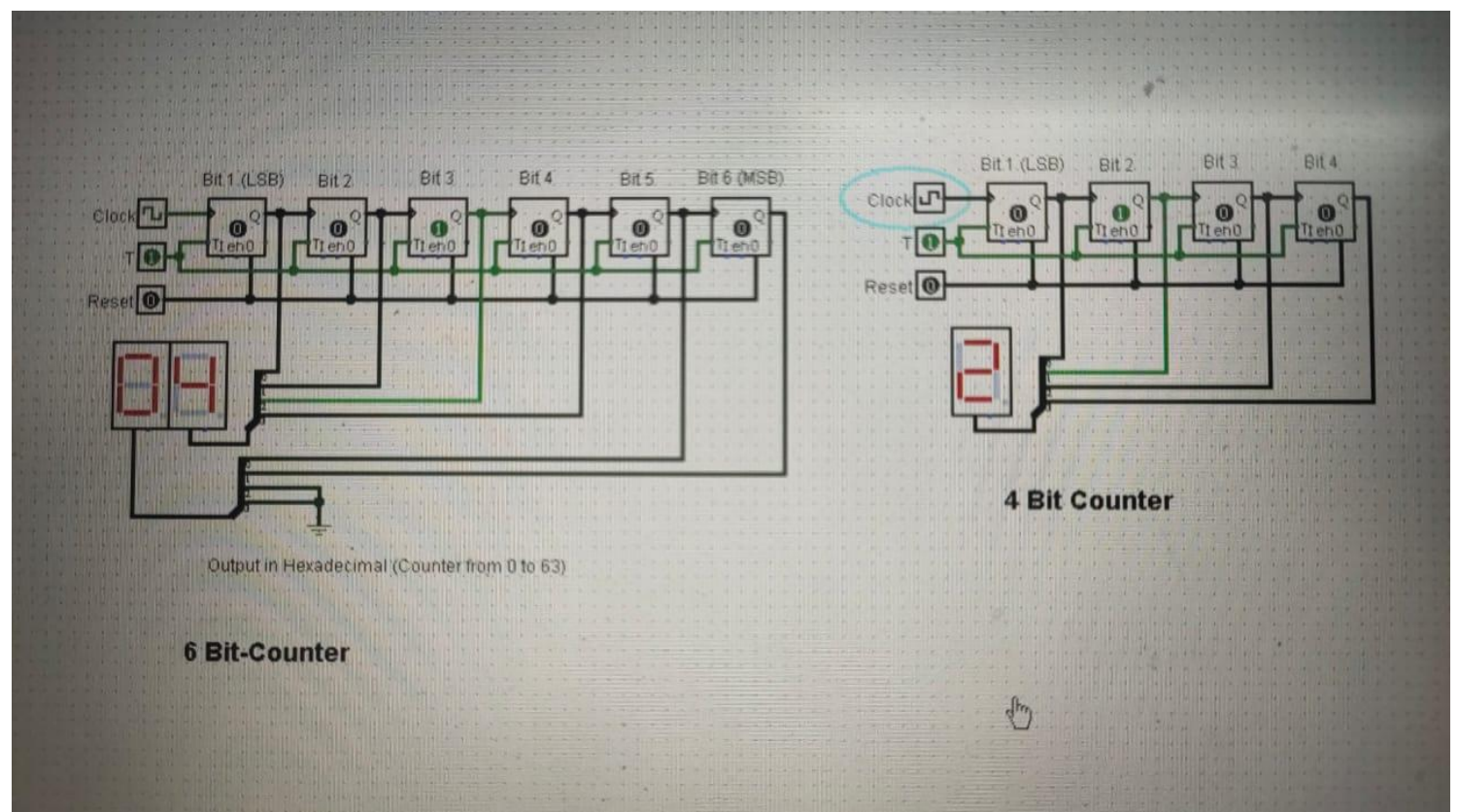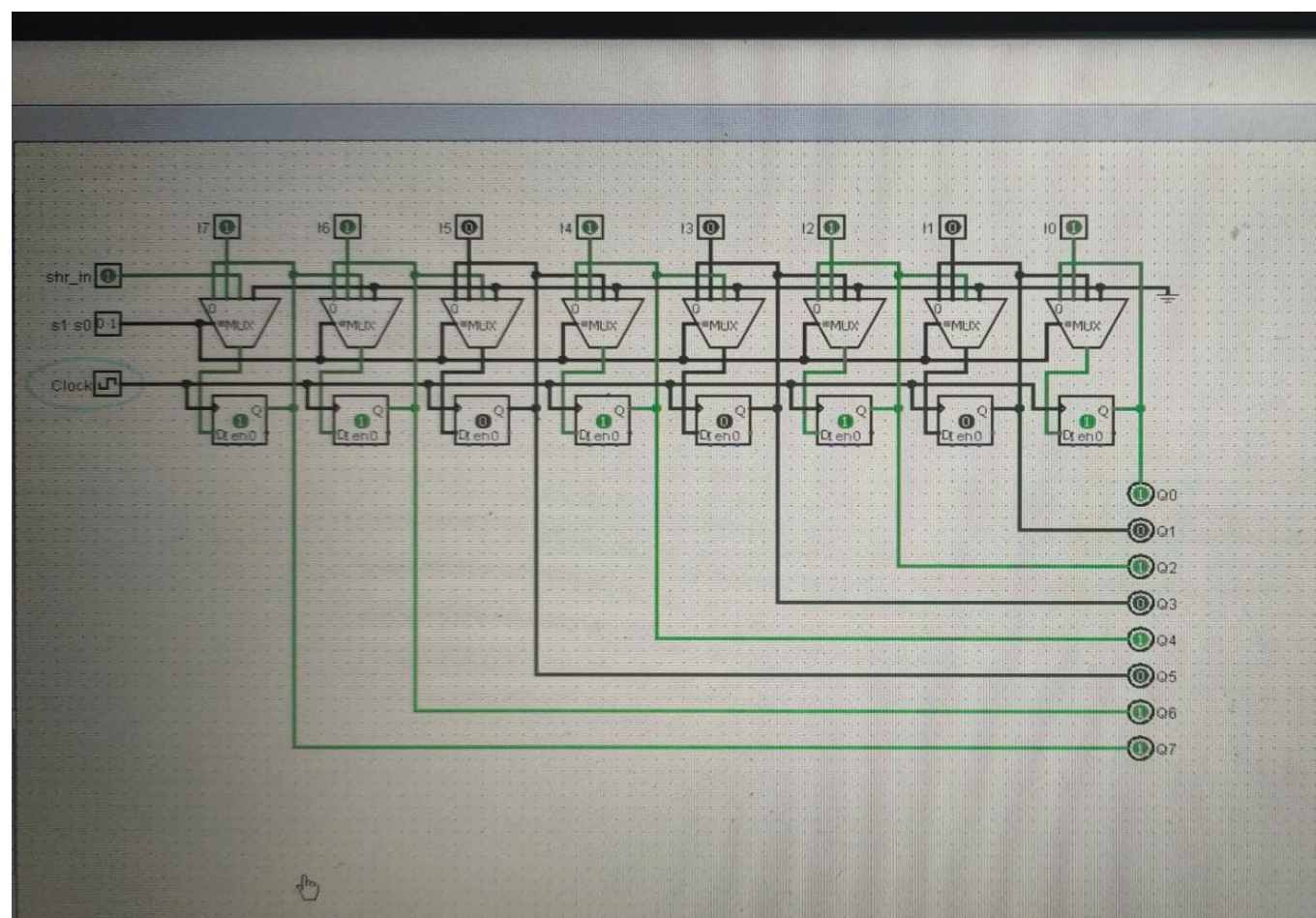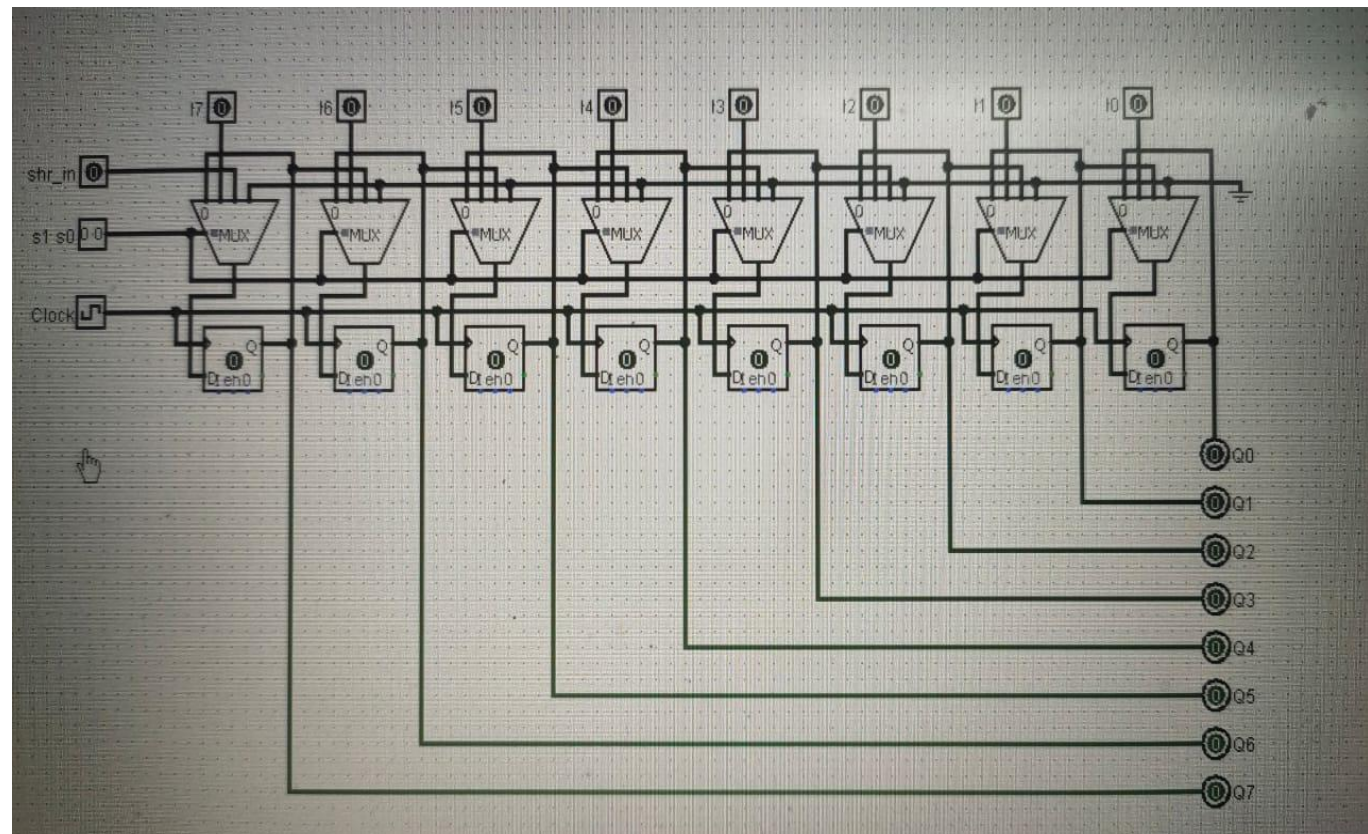
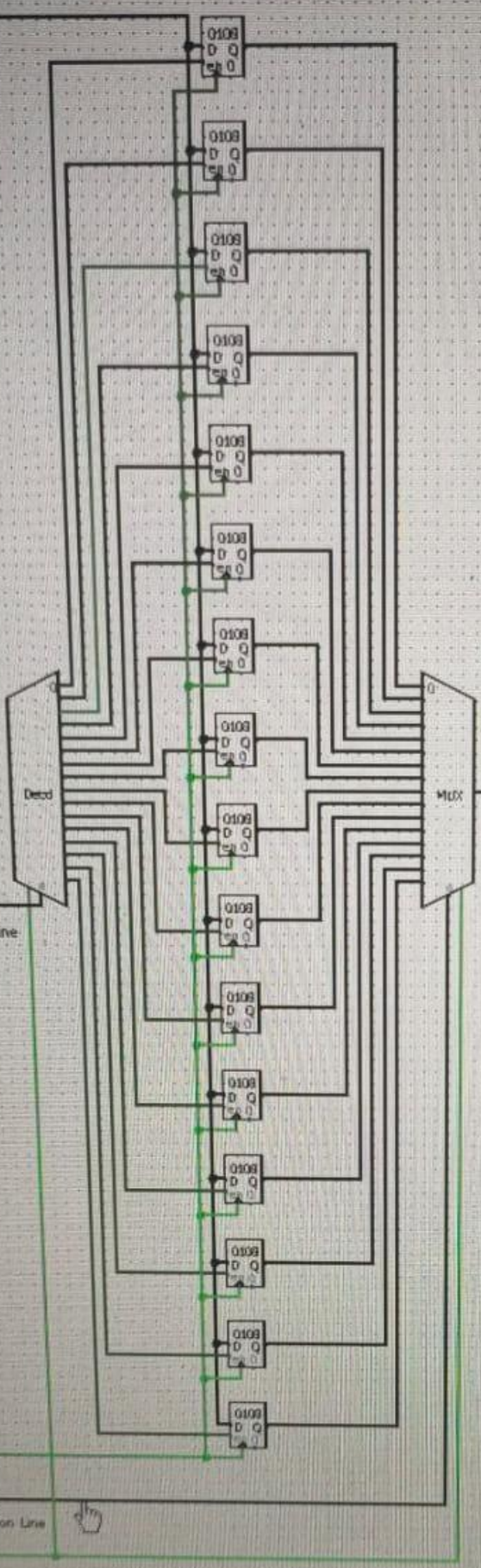## Question 4:

Question 5:
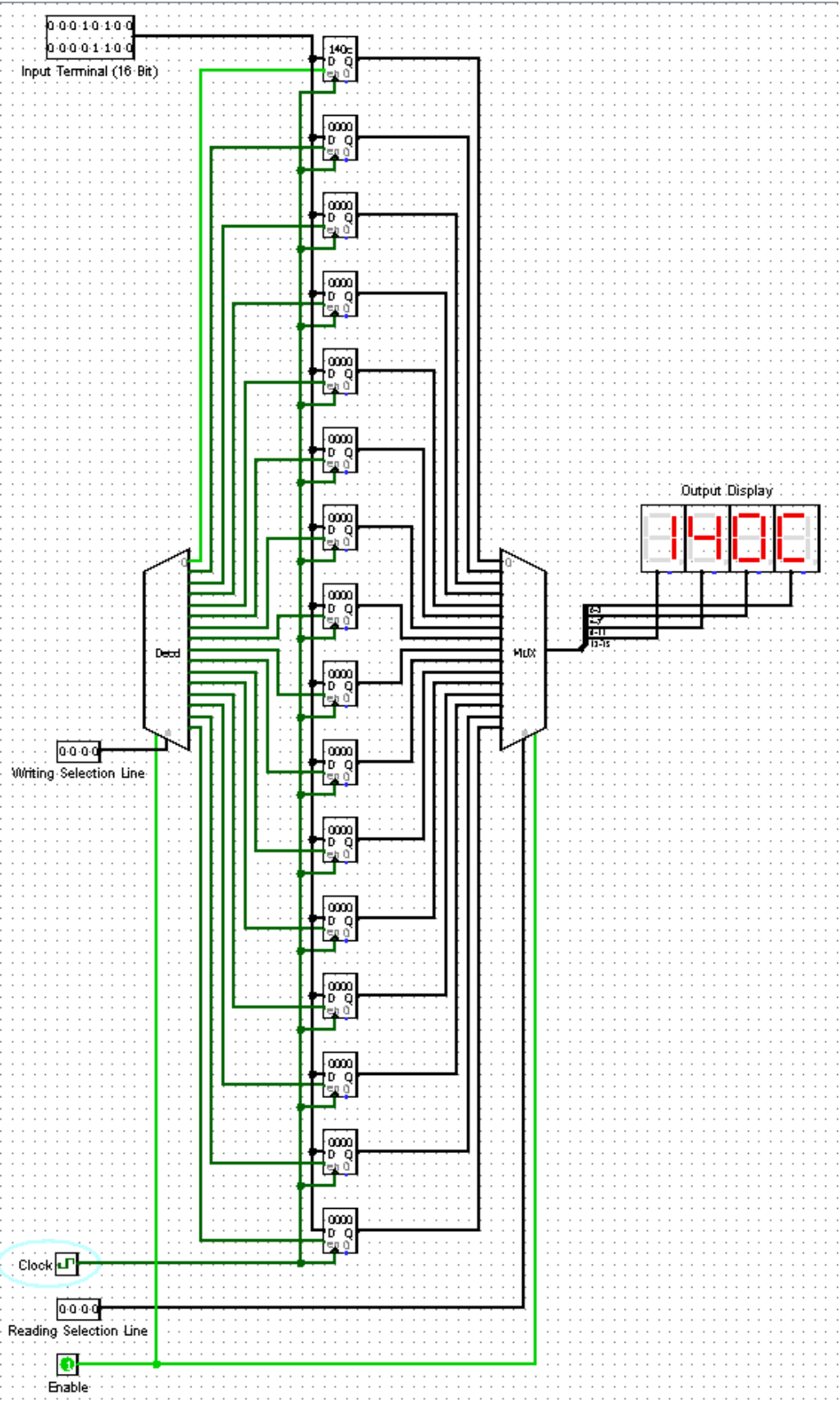
0-0-0-0-0-0-0-1
0-0-0-0-1-0-0-0
Input Terminal (16 Bit)

0109
D Q
0

0108
D Q
0

0108
D Q
0

0108
D Q
0

0108
D Q
0

0108
D Q
0

0108
D Q
0

Output Display

0108

0108
D Q
0

Decd

MUX

0108
D Q
0

0-0-1-0
Writing Selection Line

0108
D Q
0

0108
D Q
0

0108
D Q
0

0108
D Q
0

0109
D Q
0

0109
D Q
0

Clock

0-0-0-0
Reading Selection Line

Enable