INDIAN INSTITUTE OF TECHNOLOGY PATNA

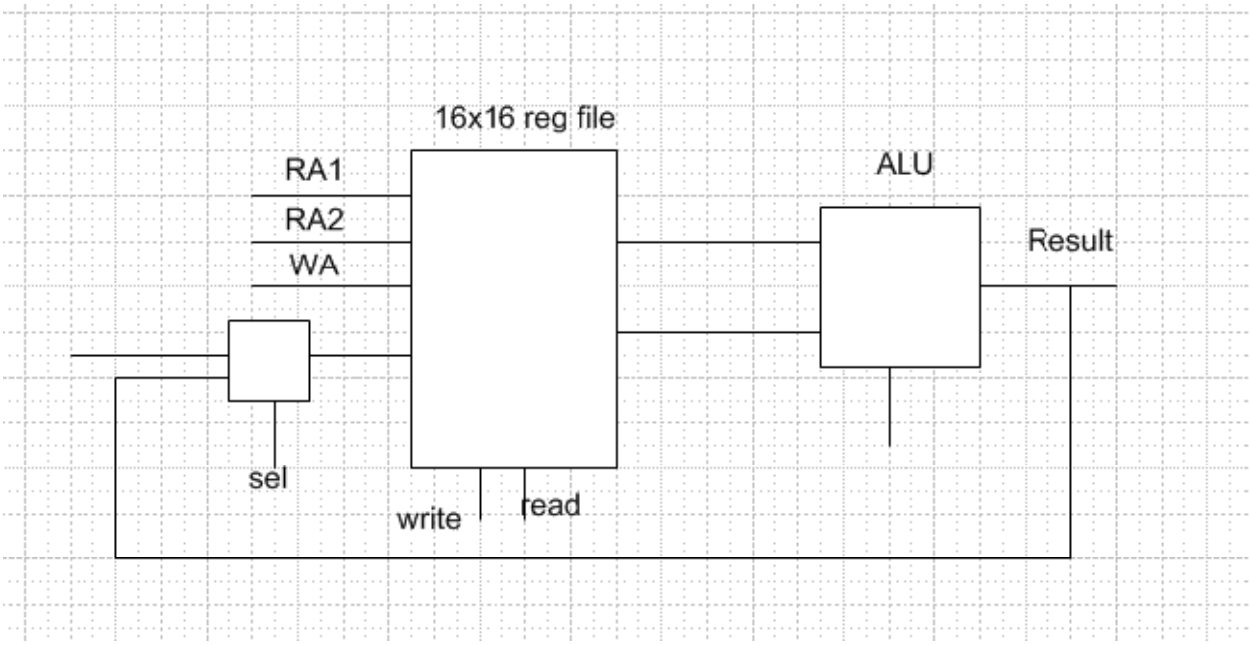
CS226-Lab7

(Sequential Logic Design)

Q1: Design a register file (16x16) with two read ports and one write port. Perform read and write operation and simulate with appropriate inputs **(40 points)**

Q2 : Combine register file and ALU designed in the previous labs to form the structure below. Write1,2,…10 data to registers(1 to 10) and computer the sum and write result in another register(reg 15).

(60 points)



Submission:

- **Simulation report** (screen shots of design and simulation output). The simulation files Q0.circ, Q1.circ, and Q2.circ,

- Zip the above files. file name is your role number.

Course work submission through:
https://u.pcloud.com/#page=puplink&code=zgc7ZId62CnOX2mYvs3c42K9Qn5LotsHX

This work is due 23rd March 11.30 PM.