Operating Systems

Assignment - 2

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Que 1:- Given:

Physical Address = 48 bits
Virtual Address = 64 bits
Page Size = 8kb = $8 * 1024$ bytes = $8 * 1024 * 8$ bits
= 16 bit number.

No. of pages (bits) = $\frac{\text{Virtual space}}{\text{Page Size}}$
= 48 bits.

We will take that frame size = page size.
No of frames (bits) = $\frac{\text{Physical space}}{\text{Frame Size}}$
= 32 bits.

Now, given a word addressable memory,
Word size = 4 bytes
= $4 * 8$ bits
= 5 bits are needed for each word.

No of words in a page = $\frac{2^{16}}{2^{5}} = 2^{11}$

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Given the valid entries in TLB possible = 128

⇒ we can store a reference to 128 pages.

Maximum words that can be stored = 128 * no of words

$= 128 \times 2^{11}$

$= 2^7 \times 2^{11}$

$= 2^{18}$

⇒ As the memory is word addressable, $\boxed{2^{18}}$ maximum unique addresses can be accessed in the TLB without a miss

Ques 2: No of page frames = 5

Sequence :- 3, 8, 2, 3, 9, 1, 6, 3, 8, 9, 3, 6, 2, 1, 3

→ option (2) ⇒ Both infer the same no of page faults.

USING FIFO

Sequence	F_1	F_2	F_3	F_4	F_5	Hit/fault
	X	X	X	X	X	
3	3	X	X	X	X	F
8	3	8	X	X	X	F
2	3	8	2	X	X	F
3	3	8	2	X	X	H
9	3	8	2	9	X	F
1	3	8	2	9	1	F
6	6	8	2	9	1	F
3	6	3	2	9	1	F

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	F_1	F_2	F_3	F_4	F_5	Page 3 Hit / Fault
8	6	3	8	9	1	F
9	6	3	8	9	1	H
3	6	3	8	9	1	H
6	6	3	8	9	1	H
2	6	3	8	2	1	F
1	6	3	8	2	1	H
3	6	3	8	2	1	H

= 9 faults, 6 Hits — FIFO

Using LRU → 9 faults, 6 Hits

→ LRU = FIFO

seq	F_1	F_2	F_3	F_4	F_5	Hit / Fault
	X	X	X	X	X	
3	3	X	X	X	X	F
8	3	8	X	X	X	F
2	3	8	2	X	X	F
3	3	8	2	X	X	H
9	3	8	2	9	X	F
1	3	8	2	9	1	F
6	3	6	2	9	1	F
3	3	6	2	9	1	H
8	3	6	8	9	1	F
9	3	6	8	9	1	H
3	3	6	8	9	1	H
6	3	6	8	9	1	H
2	3	6	8	9	2	F
1	3	6	1	9	2	F
3	3	6	1	9	2	H

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Que 3: let the page size is of 'x' bits.

Size of $T_1 = 2^x$ bytes

Now as 1 page entry size = 4 bytes.

No of entries in $T_1 = \frac{2^x}{4}$

No of entries in T_1 = No of second level page tables.

Total size of second level page tables $= \frac{2^x}{4} \times 2^x$

IIly no of entries in 2nd level page tables = no of 3rd level page tables

$= \frac{2^x}{4} \times \frac{2^x}{4}$

IIly total no of entries in all 3rd level page tables =

$= \frac{2^x}{4} \times \frac{2^x}{4} \times \frac{2^x}{4}$

$= 2^{3x-6}$ —— ①

Size of virtual memory $= \frac{2^{46}}{2^x} = 2^{46-x}$ —— ②

As ① should be equal to ②

$3x-6 = 46-x \Rightarrow x = 13.$

$\Rightarrow$ $\boxed{\text{Page size} = 13 \text{ bits or } = 2^{13} \text{ bytes} = 8\,KB}$

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Que 4:- Virtual address = 32 bits
Physical Address size = 36 bits
Physical Memory size = 2^{36} bytes.
Page frame size = 4K bytes = 2^{12} bytes.

No of bits for offset = 12
No of bits required to access physical memory size =
= 36 − 12 = 24.

∴ In the 3rd level of page table 24 bits are required to access an entry.

9 bits of Virtual Address is used to access 2nd level page table entry.
Size of pages in 2nd level = 4 bytes.
Size of 2nd level page table = $2^9 \times 4 = 2^{11}$ bytes

⇒ There are $\frac{2^{36}}{2^{11}}$ possible locations to store the page table.
⇒ 2nd page table requires 25 bits
Ily 1st page table requires 25 bit

Concluding.

First page table requires	= 25 bits
Second page table requires	= 25 bits
Third page table requires	= 24 bits.

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Que 5: No of page frames = 3
sequence = 1, 2, 1, 3, 7, 4, 5, 6, 3, 1

Using LRU

Sequence	F_1	F_2	F_3	Hit / fault
	X	X	X	
1	1	X	X	F
2	1	2	X	F
1	1	2	X	H
3	1	2	3	F
7	1	7	3	F
4	4	7	3	F
5	4	7	5	F
6	4	6	5	F
3	3	6	5	F
1	3	6	1	F

Hits = 1
fault = 9

P.T.O.

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Using Optimal Page Algorithm

Sequence	F_1	F_2	F_3	Hit / Fault
	X	X	X	
1	1	X	X	F
2	1	2	X	F
1	1	2	X	H
3	1	2	3	F
7	1	7	3	F
4	1	4	3	F — (A)
5	1	5	3	F — (B)
6	1	6	3	F
3	1	6	3	H
1	1	6	3	H

Hits = 3

Faults = 7

⇒ At the positions (A) and (B) if the 1 or 3rd page would have been replaced then their could have been 2 more page faults.
So if the operator is well-equipped with the process running then the optimal algorithm is the best.

x — x — x — x — END — x — x — x — x