INDIAN INSTITUTE OF TECHNOLOGY PATNA

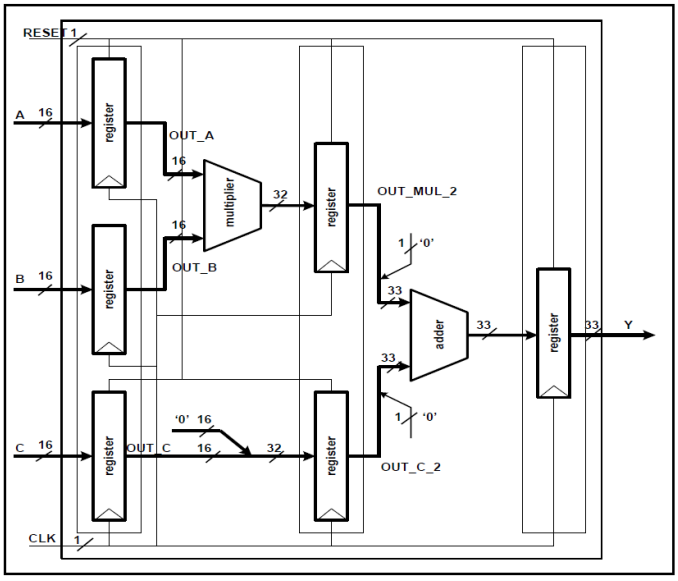
CS226 Lab

Lab 9-FSM

1. Repeat Q1 of Lab 8, with multiplexer based FSM design.
   (Q1: Design a 2-bit counter that behaves according to the two control inputs Io and I1 as follows. I0, I1 = 0,0: Stop counting; I0, I1 = 0,1: count up by one; I0, I1 = 1,0: count down by one; I0, I1 = 1,1: count by two.)

   (30 points)

2. Figure shows the implementation of Y=A*B+C. A,B and C variables are 16bit inputs. Simulate two design with pipeline registers and without pipeline registers. Compare the two implementations(Report should include your analysis)



(40 points)

3: Design and simulate an FSM that takes one input and has one output. Output is 1 if and only if last four values of input have been either 0100, 1001 or 1011.

(30 points)

Submission:

Submit your .circ files and Hand written report is required for problems. Submit through

https://u.pcloud.com/#page=puplink&code=0Eo7ZSYtjVvAx0AYIldu70IFmo5JWOuAk

- Zip the above five files. Zip file name is your role number.

This work is due on: : 7th April 2021, 11.30 PM.