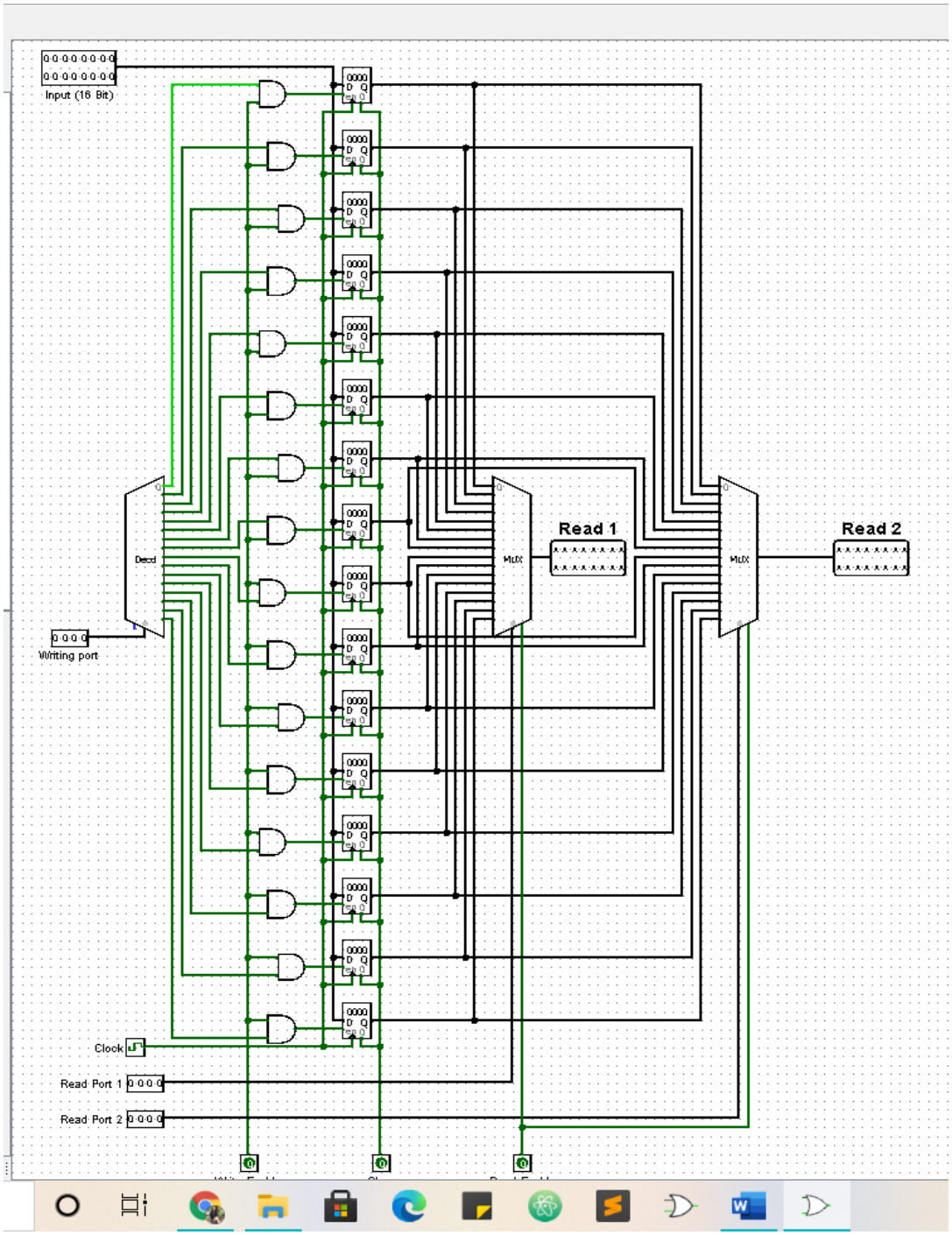
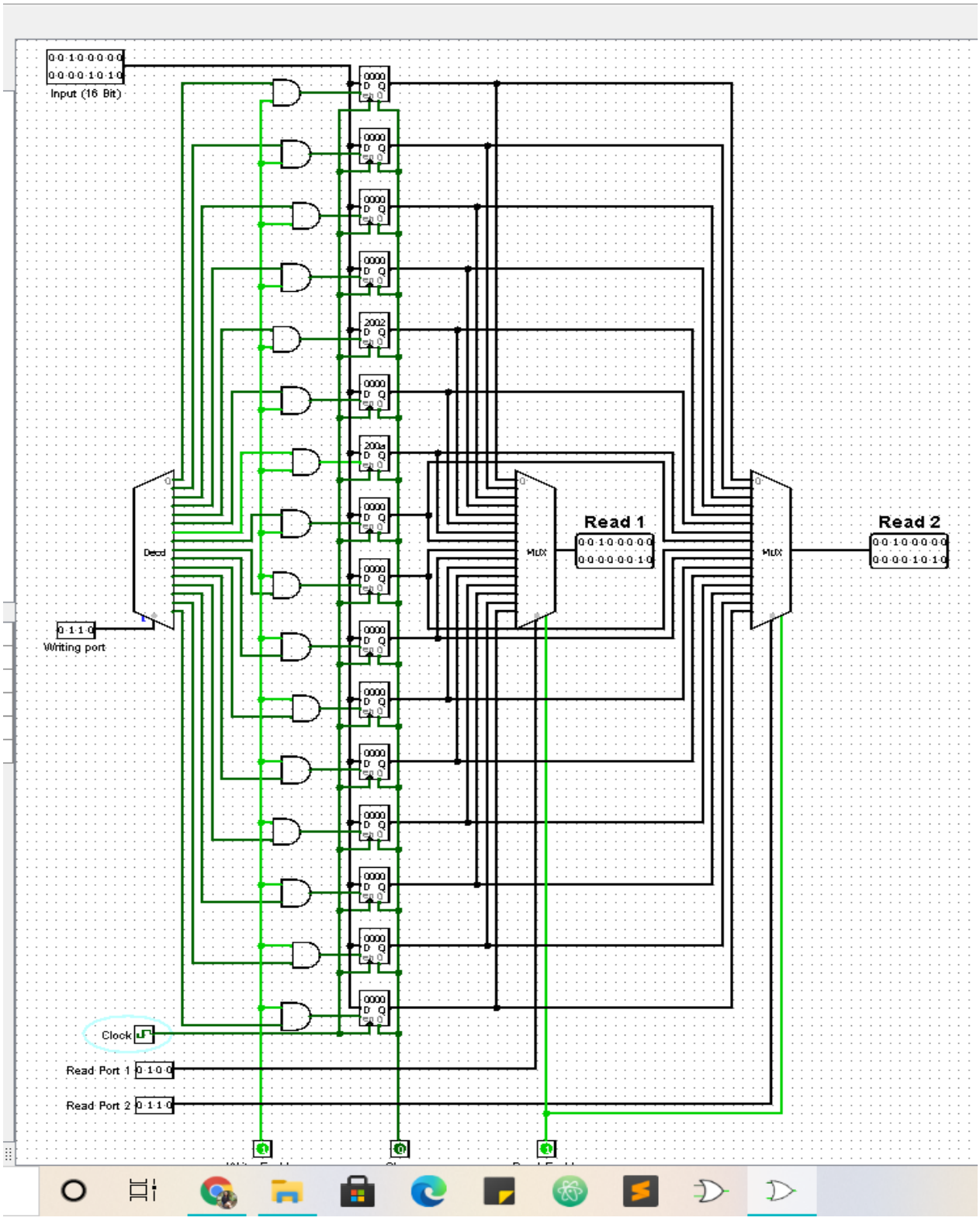
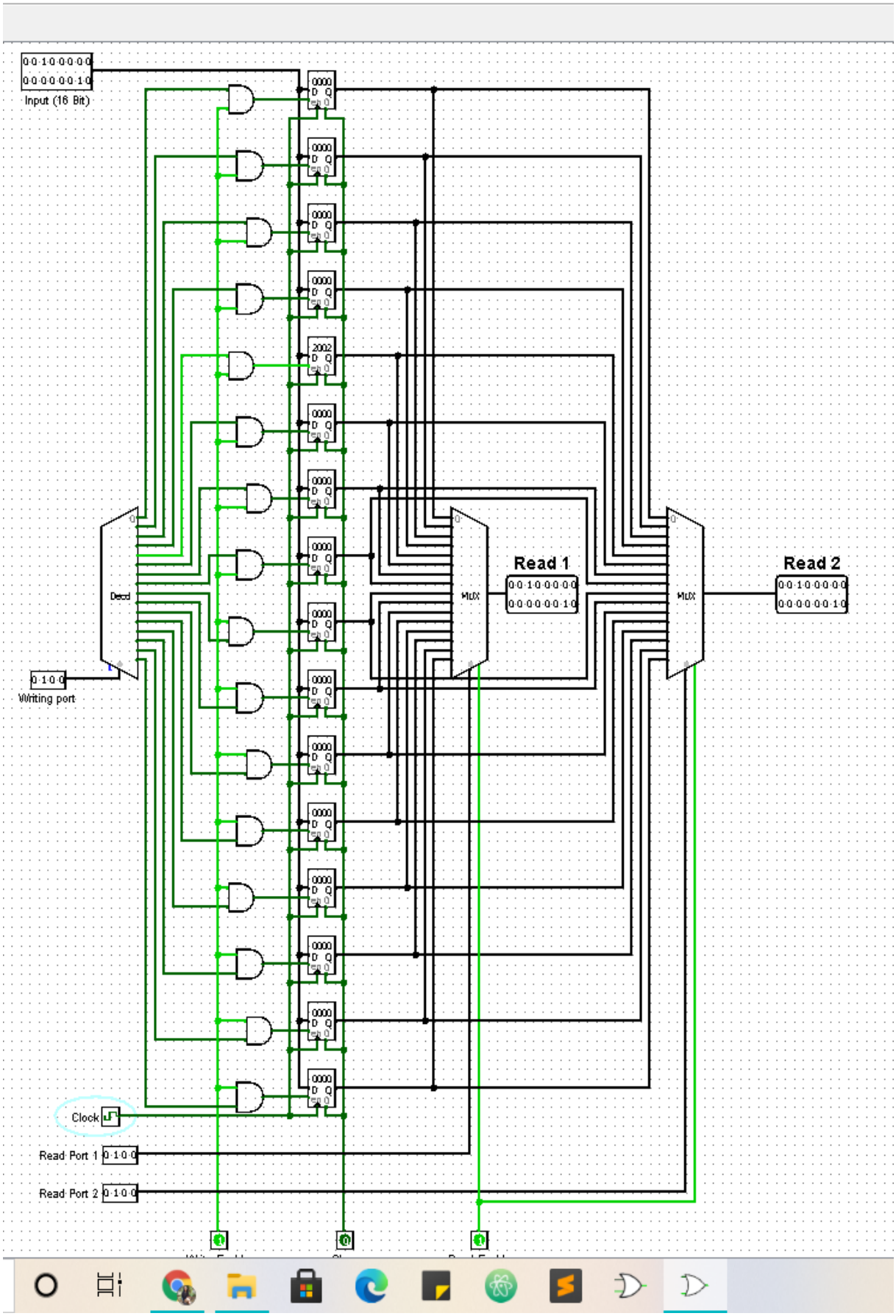
Question 1:

Design:



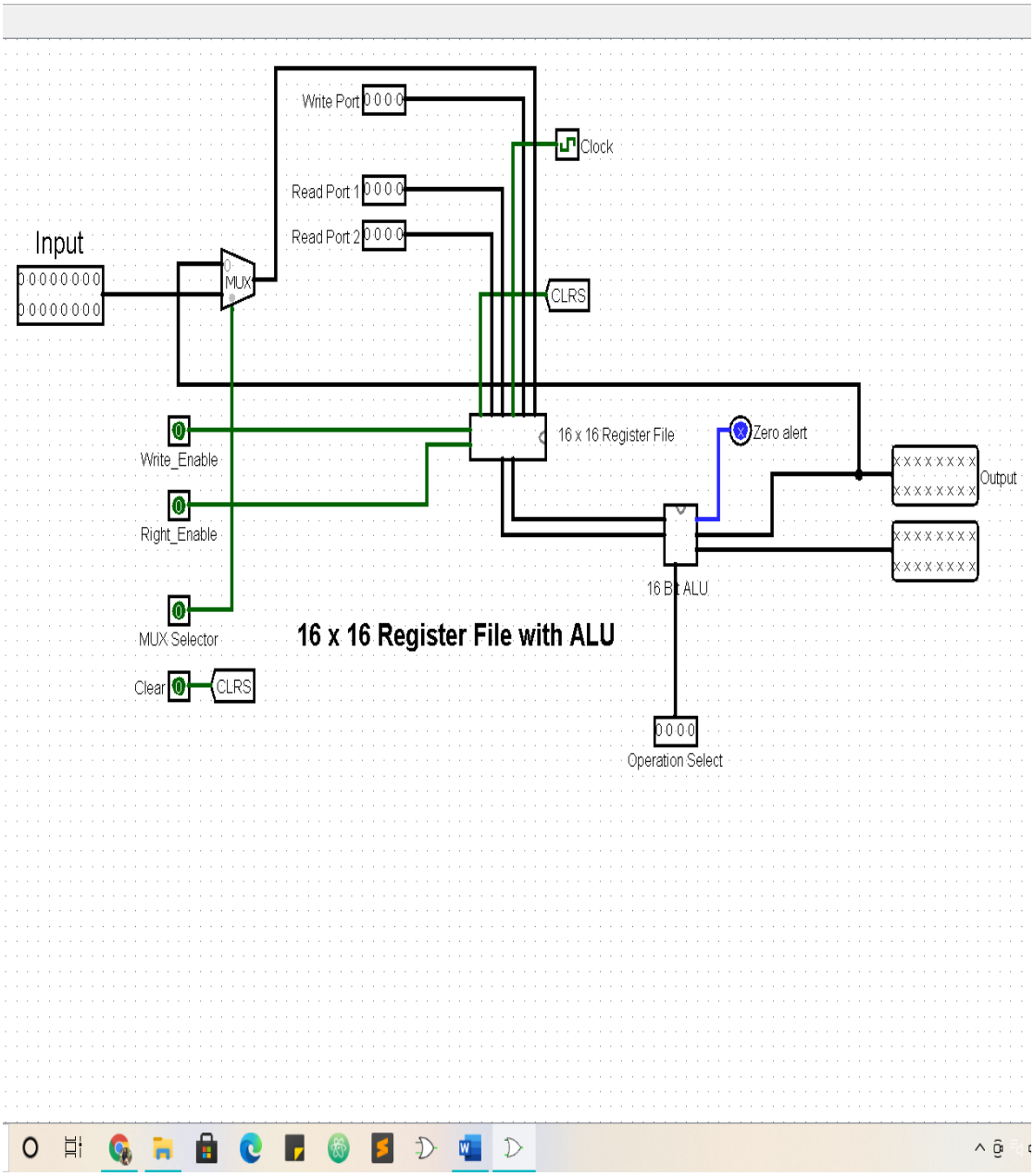
Simulation:

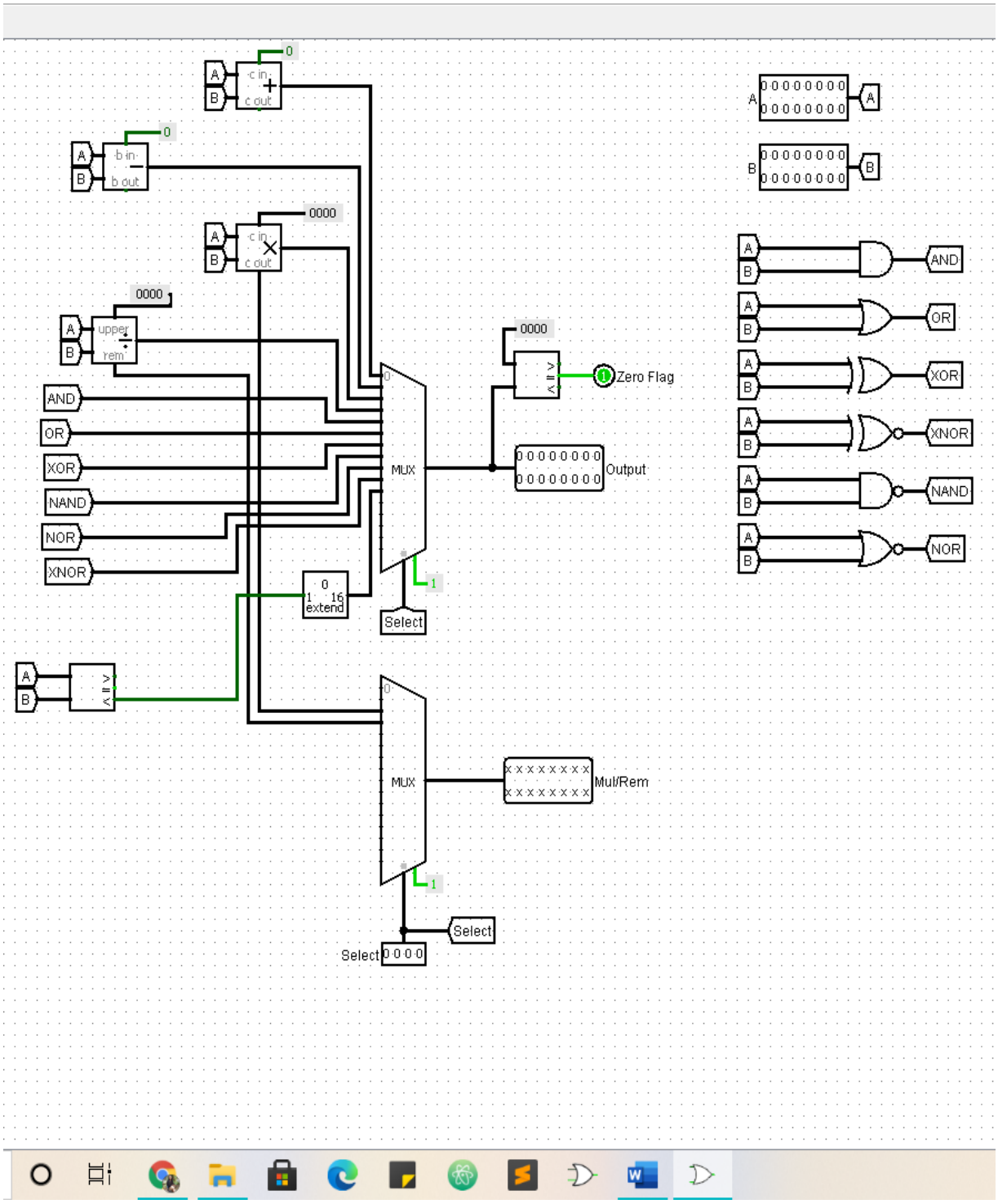

Input (16 Bit)
Decd
Writing port
Clock
Read Port 1
Read Port 2
MUX
Read 1
MUX
Read 2


Input (16 Bit)
Decd
Writing port
MUX
Read 1
MUX
Read 2
Clock
Read Port 1
Read Port 2

Question 2:

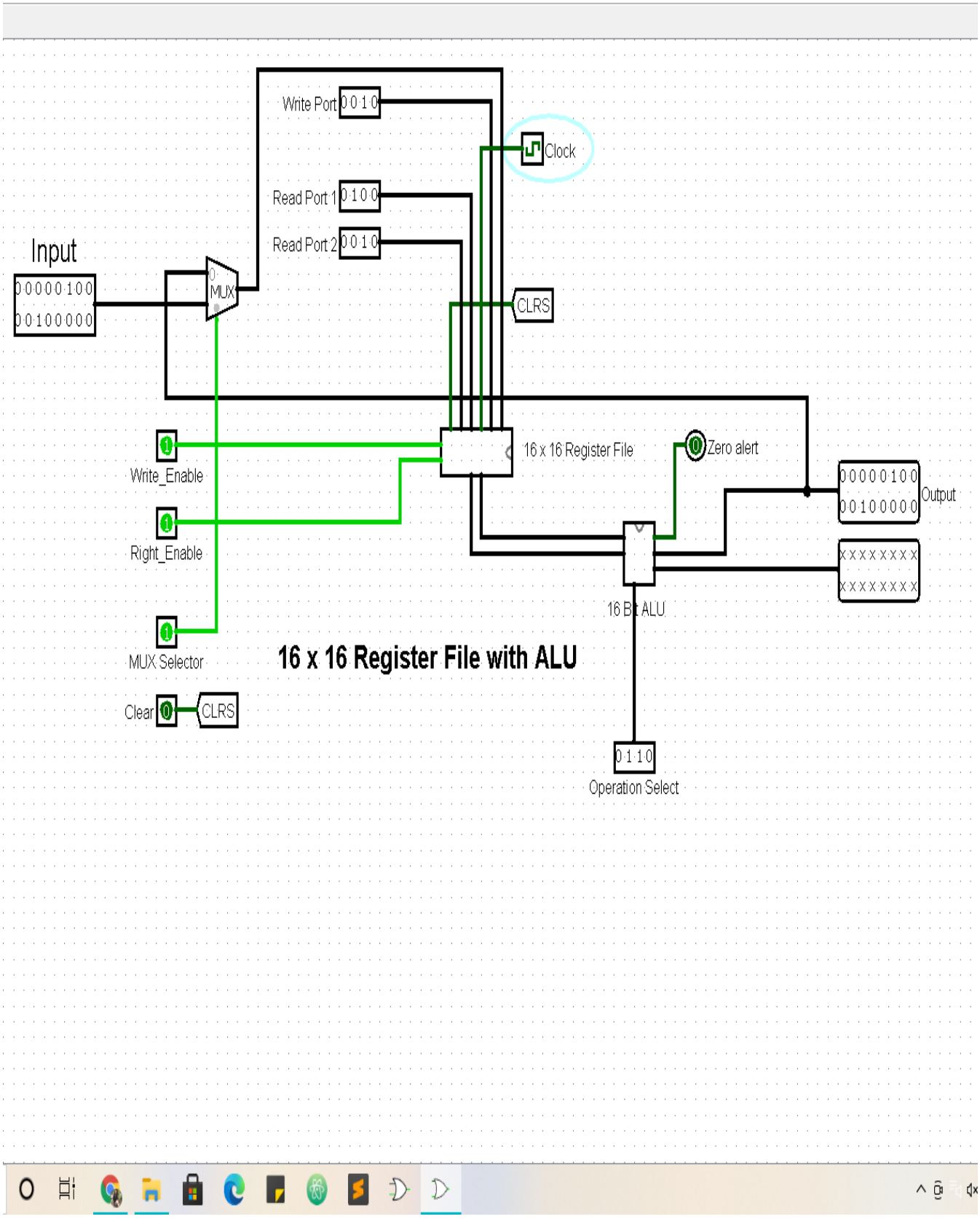
Design:

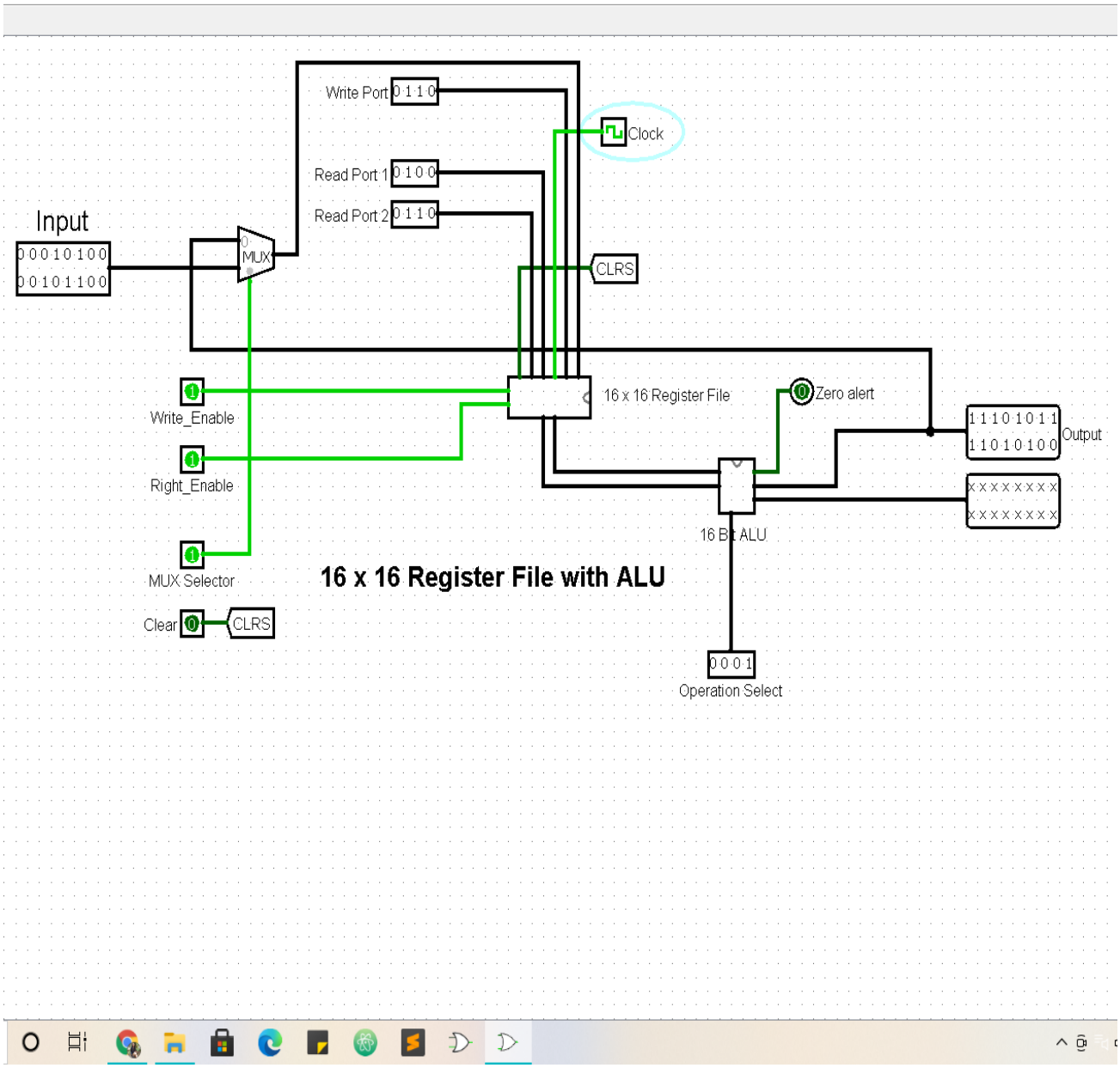




c in
c out
b in
b out
upper
rem
AND
OR
XOR
NAND
NOR
XNOR
MUX
Select
extend
Zero Flag
Output
Mul/Rem

Simulation:


Write Port
0 0 1 0
Clock
Read Port 1
0 1 0 0
Read Port 2
0 0 1 0
Input
0 0 0 0 0 1 0 0
0 0 1 0 0 0 0 0
MUX
CLRS
Write_Enable
16 x 16 Register File
Zero alert
0 0 0 0 0 1 0 0
0 0 1 0 0 0 0 0
Output
Right_Enable
x x x x x x x x
x x x x x x x x
16 Bit ALU
MUX Selector
16 x 16 Register File with ALU
Clear
CLRS
0 1 1 0
Operation Select


Write Port 0 1 1 0
Clock
Read Port 1 0 1 0 0
Read Port 2 0 1 1 0
Input
0 0 0 1 0 1 0 0
0 0 1 0 1 1 0 0
0
MUX
CLRS
Write_Enable
Right_Enable
MUX Selector
Clear 0
CLRS
16 x 16 Register File
Zero alert
1 1 1 0 1 0 1 1
1 1 0 1 0 1 0 0
Output
x x x x x x x x
x x x x x x x x
16 Bit ALU
16 x 16 Register File with ALU
0 0 0 1
Operation Select