Department of Electrical & Computer Engineering (ECE)

North South University

Course Code: 331,

Course Title: Microprocessor Interfacing & Embedded System

Final Exam Summer 2021

Time: 25 Minutes **Marks: 20**
Name:
Student ID and section:

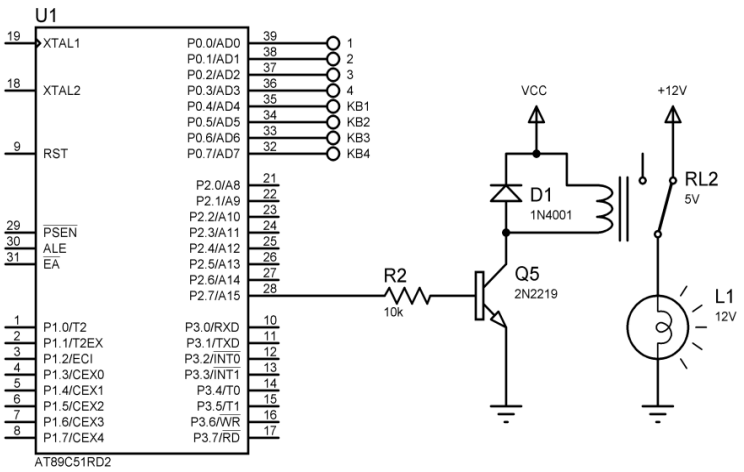
Please read the questions very carefully and answer accordingly. ***All the answers should be written in the answer script that has been provided****. Calculators/pens/pencils are allowed.* ***You must surrender any textbook/notebook/cell-phone****. Adopting any unfair means during the exam will automatically result in expulsion without any prior/post notice.* ***You must return back your question paper with your answer script.*** *Answer* ***all of the sets*** *of the questions given.* ***Clearly indicate the number of the questions being answered (Example: Answer to the question: 3 (a)(i)***

Answer one out of two of the questions given below

1.

(a) Explain how to **access** and **configure** individual bit as **input** for 8051 application. **[2.5+2.5]**

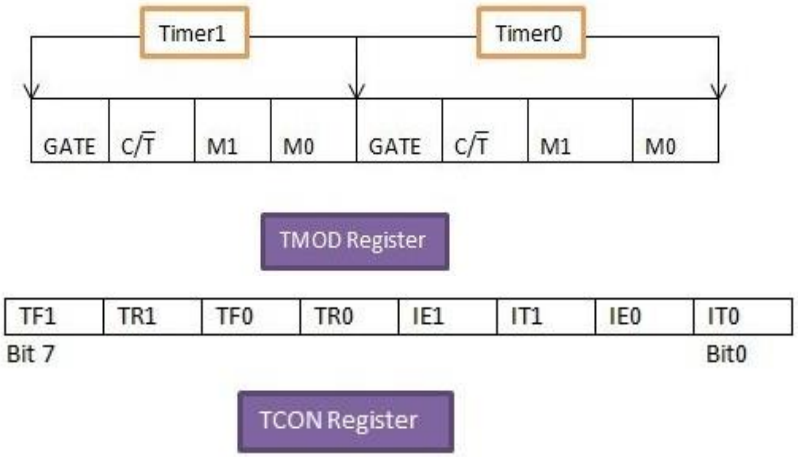
(b) Consider the following 8051 interfacing problem. Crystal frequency: 11.059MHz.The relay coil is to be energized at an interval of 10 ms. Use **timer** routine to implement the operation. **[1+1+1+1+1]**



i) Initialize **TMOD** for timer 0 , mode 1 operation

ii) Initialize TH0 and TL0 for 10 ms delay

iii) Construct the delay loop with appropriate timer flag setting
iv) Access and configure relevant pin as needed
v) Call back delay loop from the main function as needed



For level triggered: interrupt is enabled for a low at INTx pin.

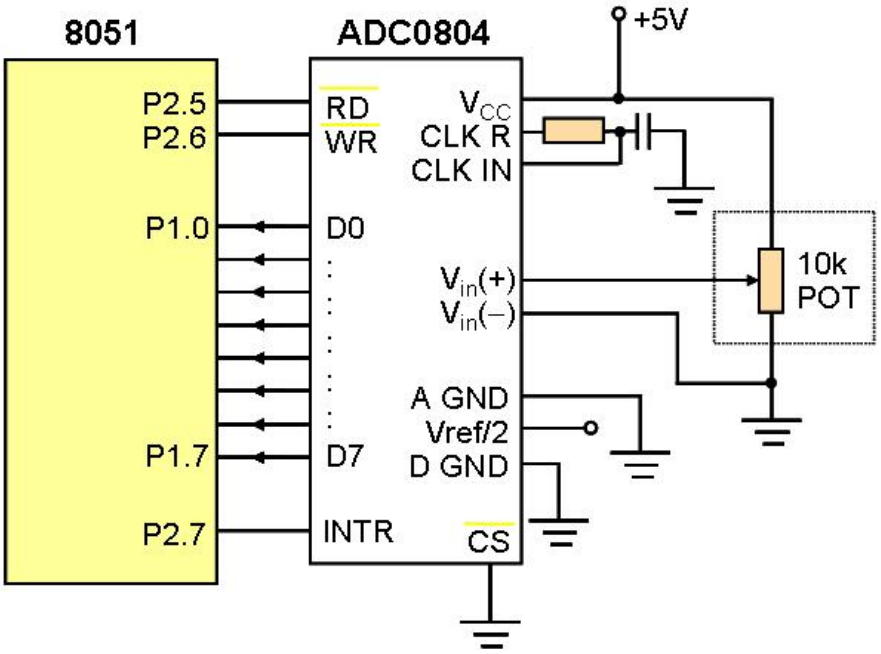
For edge triggered: interrupt is enabled for a high to low transition at INTx pin.

TCON REGISTER:

2. Answer all the questions given below

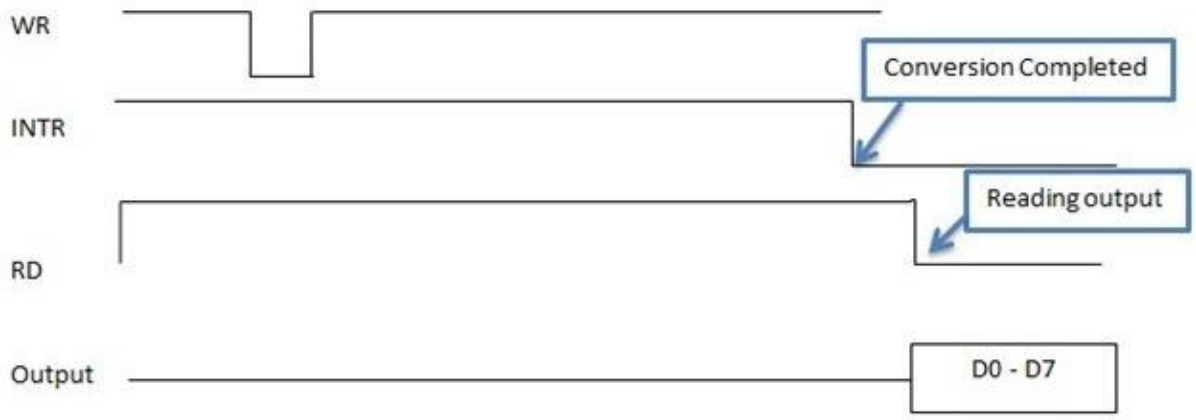
(a) What are the two main steps for analog to digital conversion? Show that the quantization error increases as the range of voltage levels to be sensed increases. Use 3 bit ADC as an example **[2.5+2.5]**

(b) Consider the following 8051 interfacing problem. **[1+1+1+1+1]**



The ***delay between consecutive analog to digital conversion*** will be dynamically adjusted. If the analog reading (V_{analog}) goes >= VCC/2, delay is 40 ms while if goes <VCC/2 , delay is 20 ms

i. Initialize the digital reading input port of 8051
ii. Define and configure WR, RD and INTR pins
iii. Define ADC routine
iv. Call back delay function in ADC routine as needed. The off time for WR is 10 ms as shown below
v. Conditional call back in main function as determined from the analog to digital code conversion equation given below. You can use global variable



Hints:

-function to create required delay

```
 void delay(unsigned int msec ) // Delay function
{
inti,j ;
for(i=0;i<msec;i++)
for(j=0; j<1275; j++);
}
```

- Equation to derive analog value read

V_{analog}= ADC code *LSB in decimal

Full scale = 5V

N=8 bits

LSB= Full scale/2^N

N=8

Full scale=5-0=5 (for 5V VCC)

ADC code: **0000 0000** to **1111 1111** in binary