



University of Asia Pacific

Department of CSE

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Q1. Find the number of misses for a cache with 16, 1-word blocks given the following sequence of memory block accesses: 0,8, 0, 6, 8, 25,13,9,8,0 for each of the following cache configurations

1. Direct Mapped Cache:

We know,

Cache set address = (Requested address) mod (number of blocks in cache)

Given,

Number of blocks = 16

Request address = 0, 8, 0, 6, 8, 25,13,9,8,0

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0 mod 16=0 0 MISS	MEM[0]															
8 mod 16=8 8 MISS									MEM[8]							
0 mod 16=0 0 HIT	MEM[0]															
6 mod 16=6 6 MISS							MEM[6]									
8 mod 16=8 8 HIT									MEM[8]							
25 mod 16=9 25 MISS										MEM[25]						
13 mod 16=13 13 MISS														MEM[13]		
9 mod 16=9 9 MISS										MEM[9]						
8 mod 16=8 8 HIT									MEM[8]							
0 mod 16=0 0 HIT	MEM[0]															

Here, Hit = 4 and Miss = 6

2. Set associative:

2-way, 4-way, 8-way, and 16-way set associative (use LRU replacement policy)

▪ 2-way set associative

Set = (num of block in cache)/ (num of way)

$$=16/2 = 8 \text{ set}$$

Address = (requested address) mod (num of set)

Given,

Number of blocks = 16

Request address = 0, 8, 0, 6, 8, 25,13,9,8,0

	0		1		2		3		4		5		6		7	
	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
0 mod 8=0 0 MISS	MEM[0]															
8 mod 8=0 8 MISS		MEM[8]														
0 mod 8=0 0 HIT	MEM[0]															
6 mod 8=6 6 MISS													MEM[6]			
8 mod 8=0 8 HIT		MEM[8]														
25 mod 8=1 25 MISS			MEM[25]													
13 mod 8=5 13 MISS											MEM[13]					
9 mod 8=1 9 MISS			MEM[9]													
8 mod 8=0 8 HIT		MEM[8]														
0 mod 8=0 0 HIT	MEM[0]															

Here, Hit = 4 and Miss = 6

- **4-way set associative**

Set = (num of block in cache)/ (num of way)

$$= 16/4 = 4 \text{ set}$$

Address = (requested address) mod (num of set)

Given,

Number of blocks = 16

Request address = 0, 8, 0, 6, 8, 25,13,9,8,0

	0				1				2				3			
	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3
0 mod 4=0 0 MISS	MEM[0]															
8 mod 4=0 8 MISS		MEM[8]														
0 mod 4=0 0 HIT	MEM[0]															
6 mod 4=2 6 MISS									MEM[6]							
8 mod 4=0 8 HIT		MEM[8]														
25 mod 4=1 25 MISS					MEM[25]											
13 mod 4=1 13 MISS						MEM[13]										
9 mod 4=1 9 MISS							MEM[9]									
8 mod 4=0 8 HIT		MEM[8]														
0 mod 4=0 0 HIT	MEM[0]															

Here, Hit = 4 and Miss = 6

▪ **8-way set associative**

Set = (num of block in cache)/ (num of way)

$$= 16/8 = 2 \text{ set}$$

Address = (requested address) mod (num of set)

Given,

Number of blocks = 16

Request address = 0, 8, 0, 6, 8, 25, 13, 9, 8, 0

	0								1							
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0 mod 2=0 0 MISS	MEM[0]															
8 mod 2=0 8 MISS		MEM[8]														
0 mod 2=0 0 HIT	MEM[0]															
6 mod 2=0 6 MISS			MEM[6]													
8 mod 2=0 8 HIT		MEM[8]														
25 mod 2=1 25 MISS					MEM[25]											
13 mod 2=1 13 MISS						MEM[13]										
9 mod 2=1 9 MISS							MEM[9]									
8 mod 2=0 8 HIT		MEM[8]														
0 mod 2=0 0 HIT	MEM[0]															

Here, Hit = 4 and Miss = 6

- **16-way set associative**

Set = (num of block in cache)/ (num of way)

$$= 16/16 = 1 \text{ set}$$

Address = (requested address) mod (num of set)

Given,

Number of blocks = 16

Request address = 0, 8, 0, 6, 8, 25, 13, 9, 8, 0

	0															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0 mod 1=0 0 MISS	MEM[0]															
8 mod 1=0 8 MISS		MEM[8]														
0 mod 1=0 0 HIT	MEM[0]															
6 mod 1=0 6 MISS			MEM[6]													
8 mod 1=0 8 HIT		MEM[8]														
25 mod 1=0 25 MISS				MEM[25]												
13 mod 1=0 13 MISS					MEM[13]											
9 mod 1=0 9 MISS						MEM[9]										
8 mod 1=0 8 HIT		MEM[8]														
0 mod 1=0 0 HIT	MEM[0]															

Here, Hit = 4 and Miss = 6

- **Fully associative**

Given,

Number of blocks = 16

Request address = 0, 8, 0, 6, 8, 25, 13, 9, 8, 0

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0 MISS	MEM [0]															
8 MISS		MEM [8]														
0 HIT	MEM [0]															
6 MISS			MEM [6]													
8 HIT		MEM [8]														
25 MISS				MEM [25]												
13 MISS					MEM [13]											
9 MISS						MEM [9]										
8 HIT		MEM [8]														
0 HIT	MEM [0]															

Here, Hit = 4 and Miss = 6