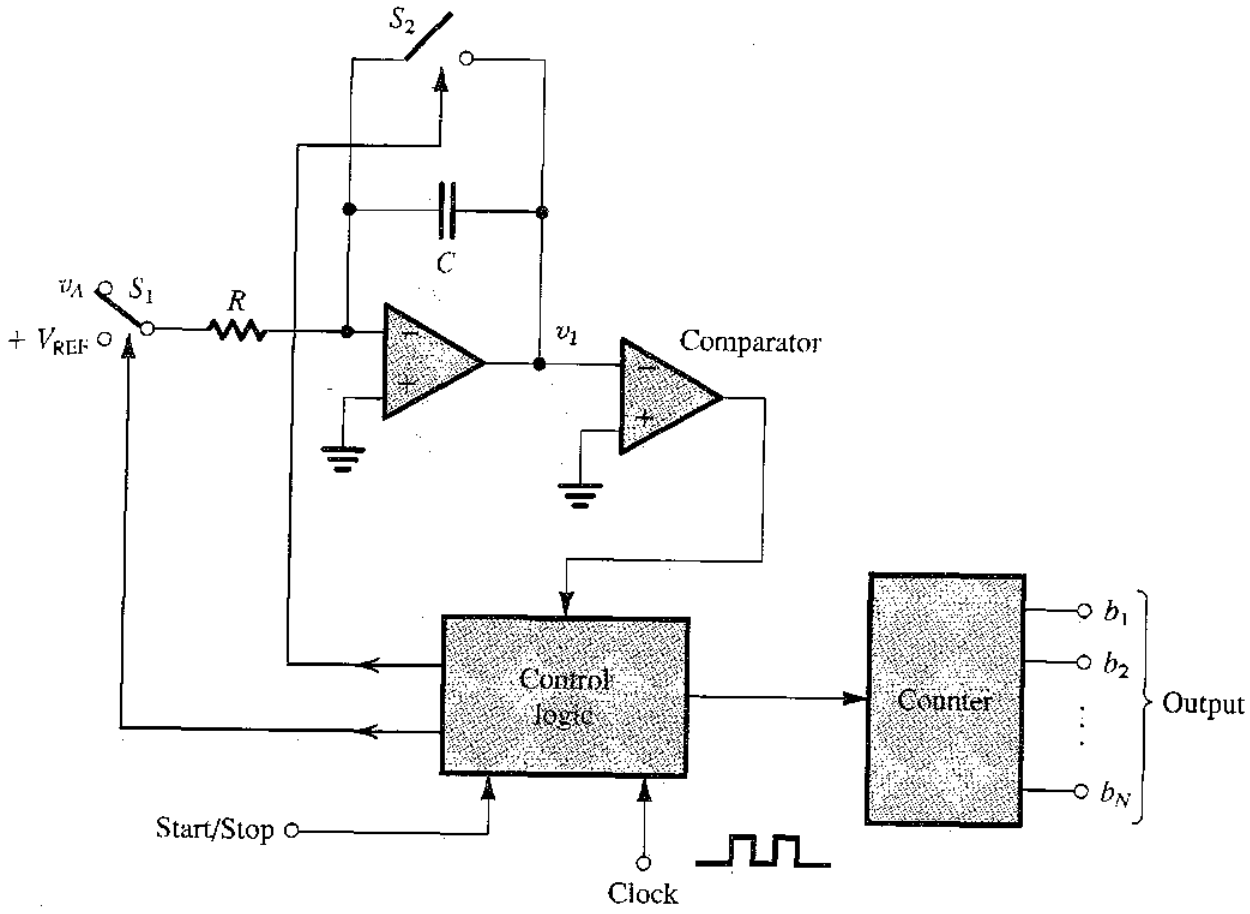
Lecture 28

EC103

Dual Slope ADC

- A very popular high resolution (12- to 14-bit) (but slow) ADC scheme is being shown.
- Below we describe its working principle:

1. Assume that the input signal υ_A is negative.
2. Prior to start of the conversion cycle, the switch S_2 is closed, thus discharging the capacitor, and setting υ_1 is zero.
3. The conversion cycle begins with opening S_2, and connecting the integrator input through the switch $S_1$to the analog input.
4. Since υ_A is negative, a current will flow through R in the direction away from the Integrator.



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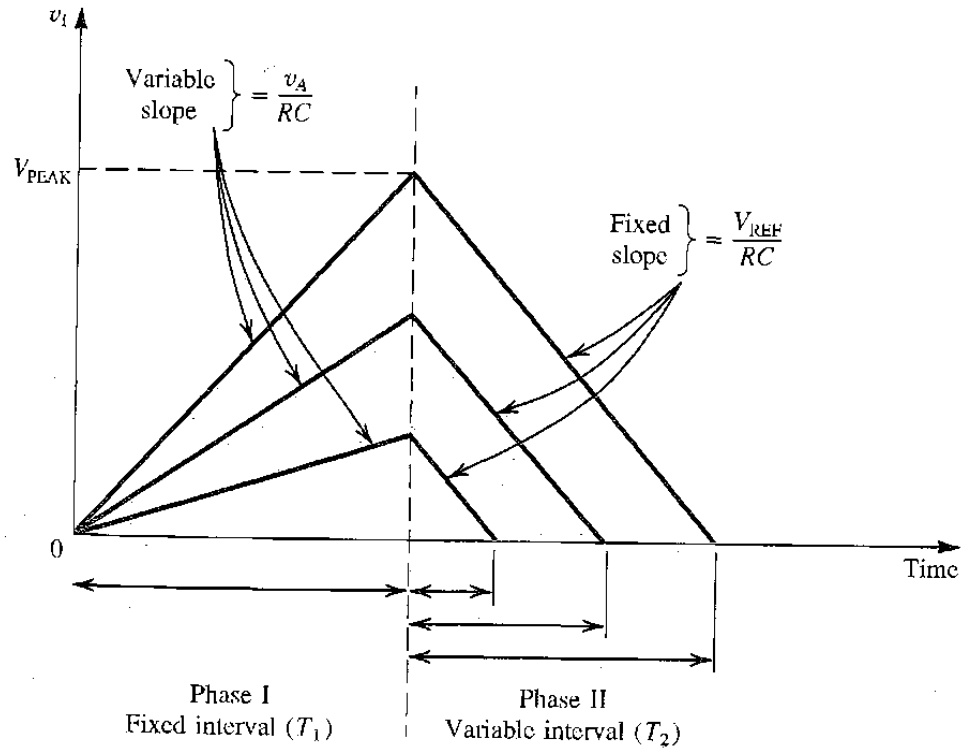
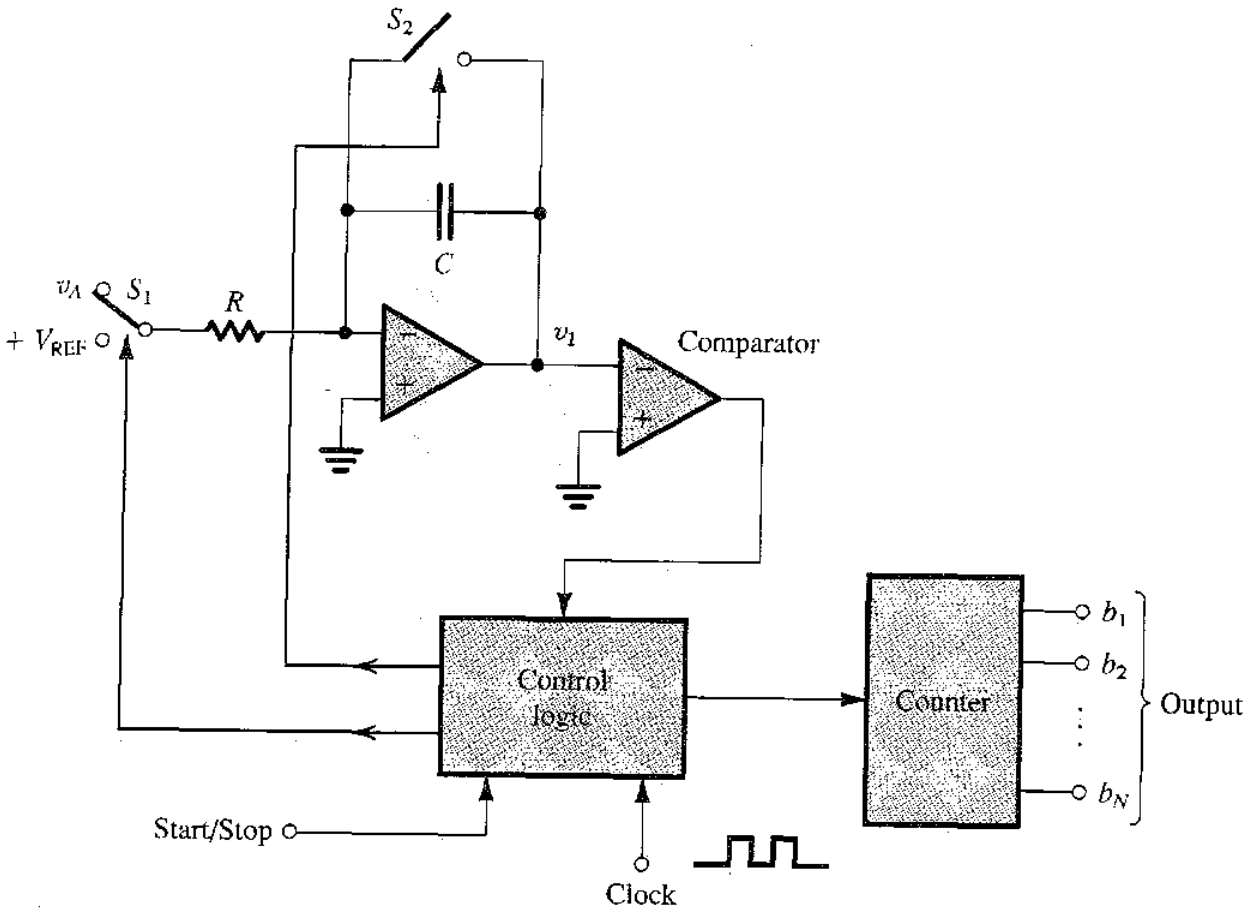
3. The conversion cycle begins with opening S_2, and connecting the integrator input through the switch $S_1$to the analog input.
4. Since υ_A is negative, a current $I = \frac{\upsilon_A}{R}$ will flow through R in the direction away from the Integrator.

5. Thus υ_1 rises linearly with a slope $= \frac{I}{C} = \frac{\upsilon_A}{RC}$ as shown in the adjacent figure.



Dual Slope ADC

6. Simultaneously, the counter is enabled, and it counts the pulses from a fixed-frequency clock.
7. This phase of conversion process continues for a fixed duration T_1. It ends when the counter has accumulated a fixed count denoted N_{ref}. Usually, for a N-bit converter $N_{ref} = 2^N$.



Dual Slope ADC

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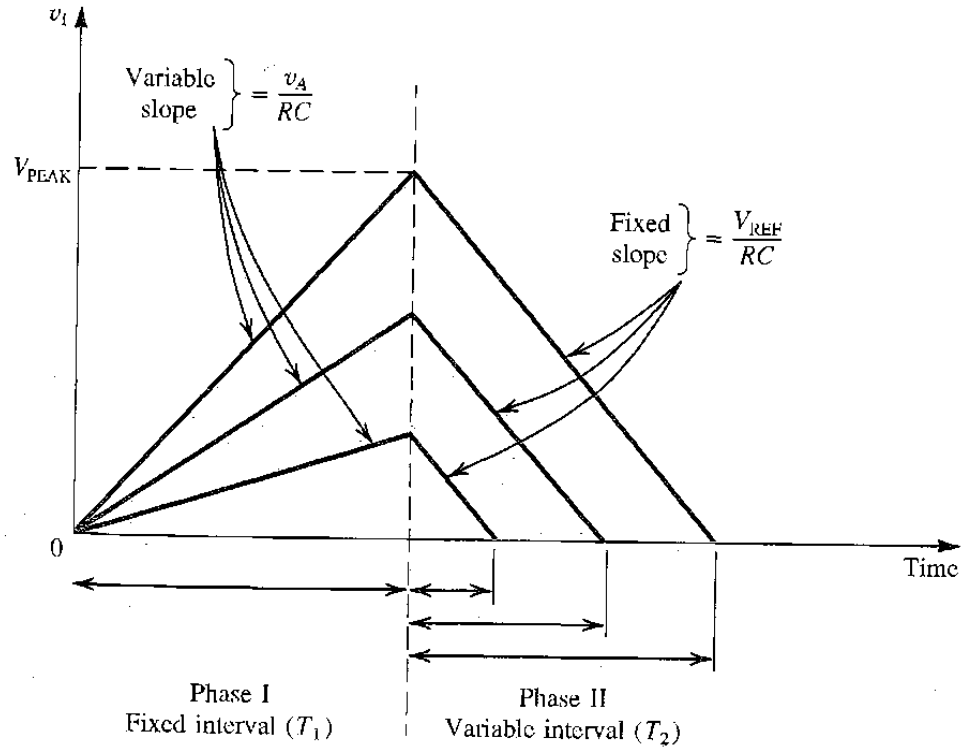
7. This phase of conversion process continues for a fixed duration T_1. It ends when the counter has accumulated a fixed count denoted N_{ref}. Usually, for a N-bit converter $N_{ref} = 2^N$.
8. Denoting the peak voltage at the output of the integrator as V_{peak}, we can write by the reference to the adjacent figure:

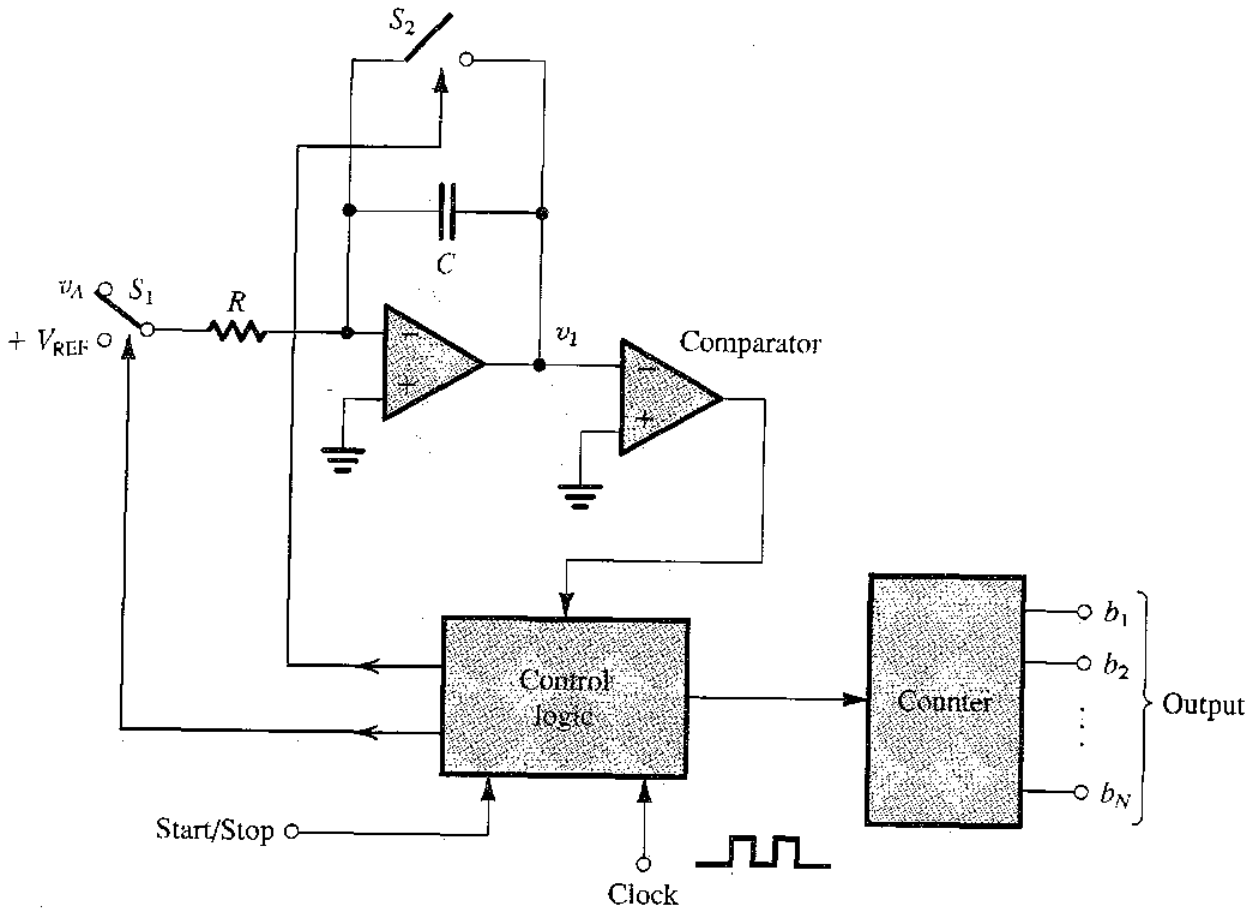
$$\frac{V_{peak}}{T_1} = \frac{\upsilon_A}{RC} \quad \text{... (i).}$$

9. At the end of this phase, the counter is reset to zero.



Dual Slope ADC

10. Phase II of the conversion begins at $t = T_1$ by connecting the integrator input through the switch S_1 to the positive reference voltage V_{ref}.
11. The current into the integrator reverses direction and is equal to $\frac{V_{ref}}{R}$.



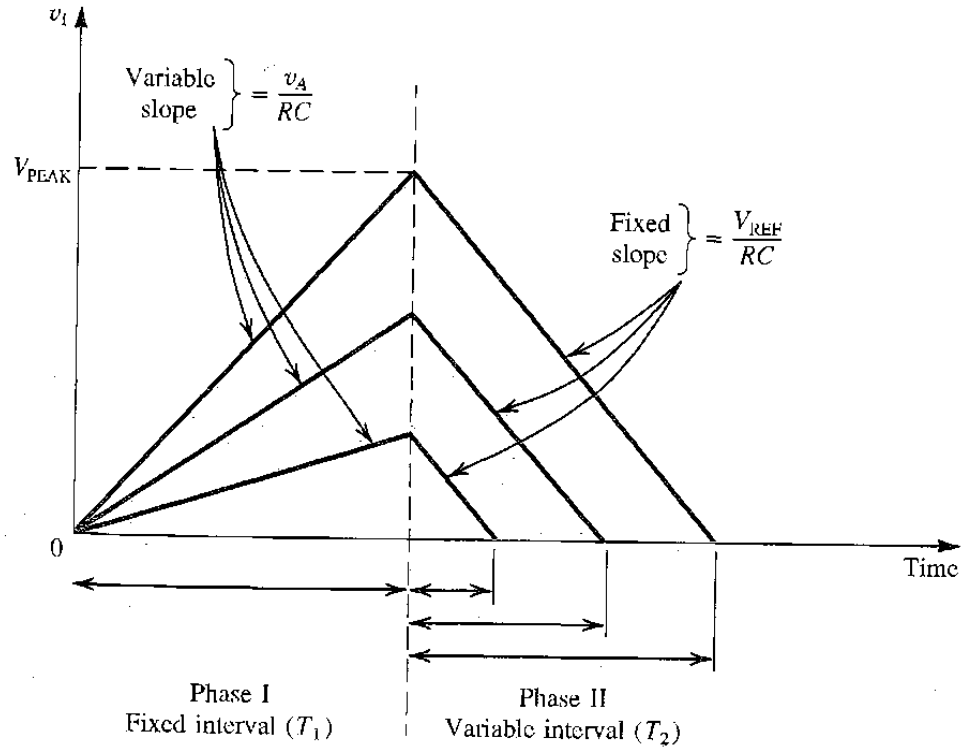
Dual Slope ADC

10. Phase II of the conversion begins at $t = T_1$ by connecting the integrator input through the switch S_1 to the positive reference voltage V_{ref}.

11. The current into the integrator reverses direction and is equal to $\frac{V_{ref}}{R}$.

12. Thus υ_1 decreases linearly with a slope of V_{ref}/RC.

13. Simultaneously, the counter is enabled, and it counts the pulses from the fixed-frequency clock.



Dual Slope ADC

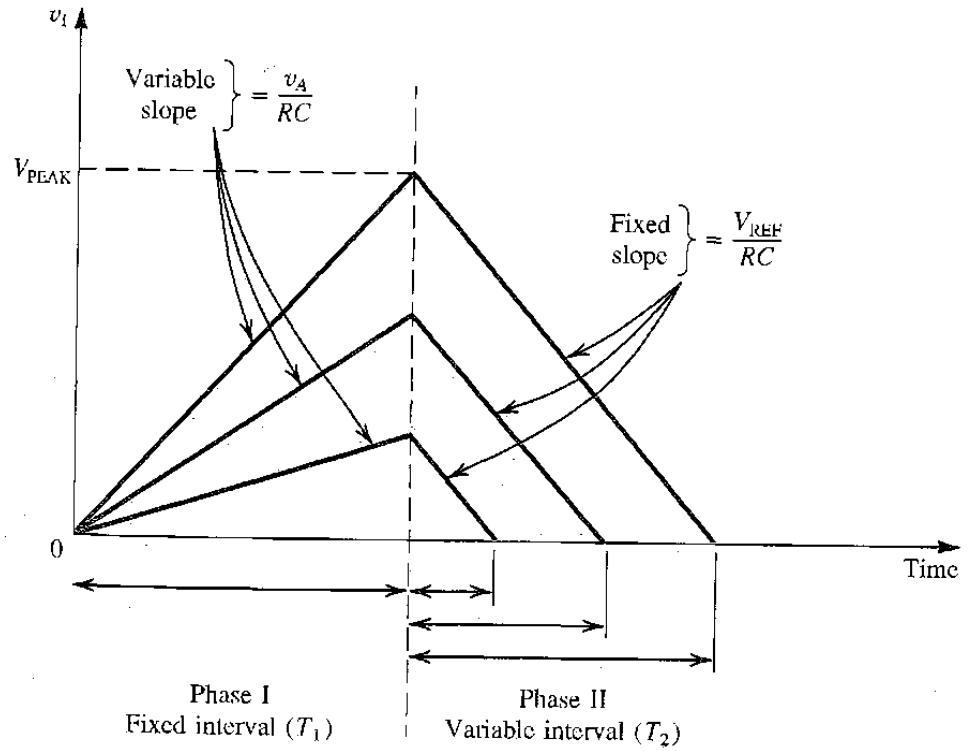
14. When υ_1 reaches zero volts, the comparator signals the control logic to stop the counter.

15. Denoting the duration of the phase II by T_2, we can write by the reference to the adjacent figure:

$$\frac{V_{peak}}{T_2} = \frac{V_{ref}}{RC} \qquad \text{... (ii).}$$

16. Combining equations (i) and (ii), we get

$$T_2 = \quad T_1 \left(\frac{\upsilon_A}{V_{ref}}\right) \quad \text{... (iii).}$$



Dual Slope ADC

17. We can also conclude from the equation (iii):

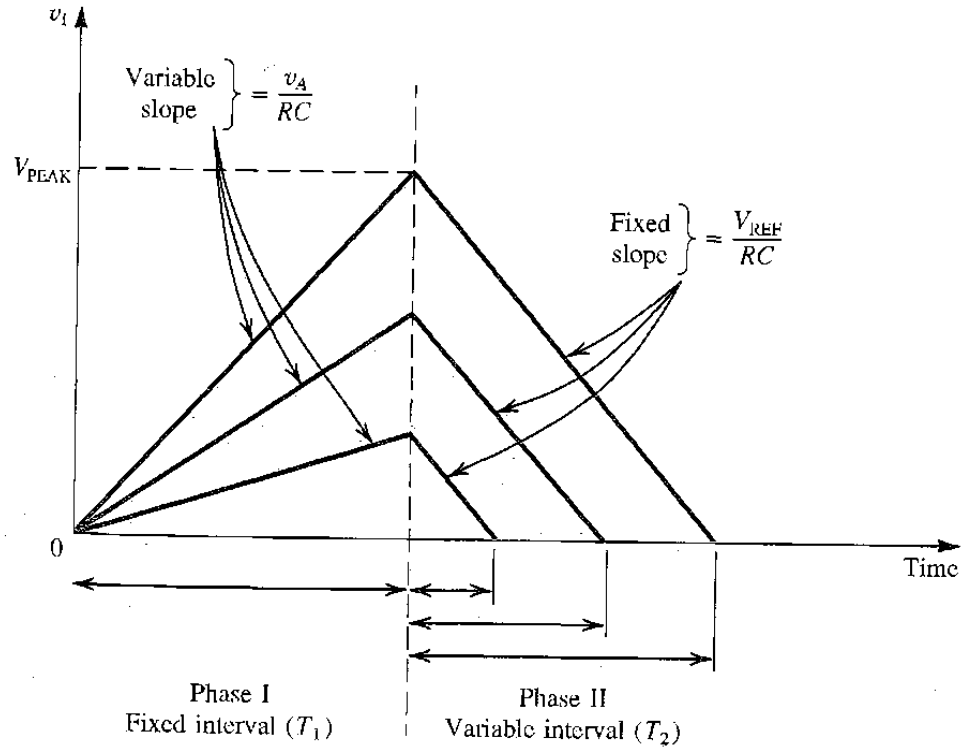
$$n = n_{ref}\left(\frac{\upsilon_A}{V_{ref}}\right) \quad \text{... (iv),}$$

where $\frac{n}{n_{ref}} = \frac{T_2}{T_1}$

as n_{ref} is the counter reading after T_1 interval,

And n is the counter reading after T_2 interval.

18. Thus the counter reading n gives digital equivalent to υ_A.



Lecture 29

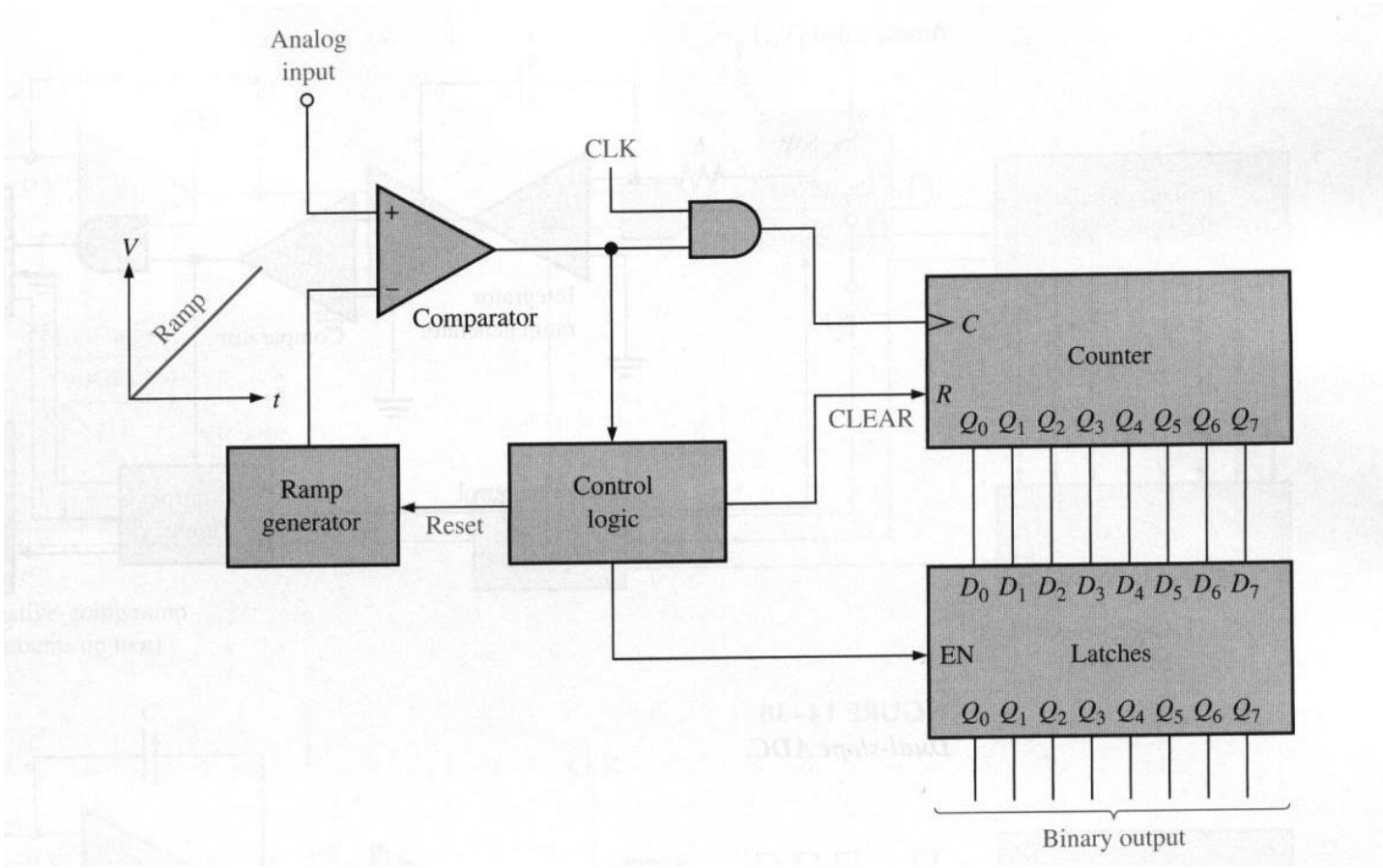
EC103

Example on Dual Slope ADC

- Consider a 8-bit dual-slope ADC with a 2 MHz clock and has $V_{ref} = -4\ V$. The fixed interval T_1 is the time taken for the counter to accumulate a count of 2^N. What is the time required to convert an input voltage equal to 2 V.?

- Ans. 0.192 ms.

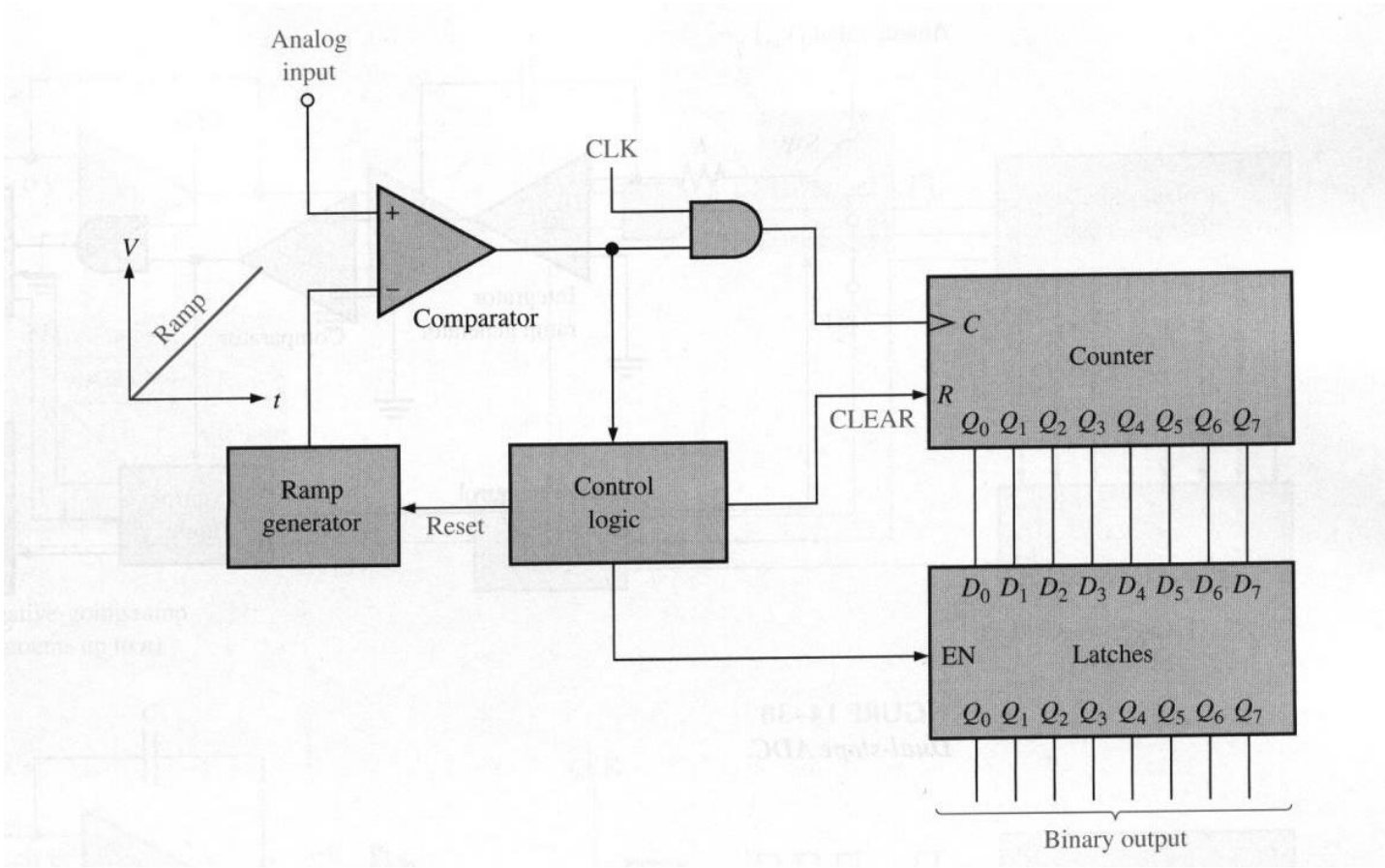
Single Slope ADC



- It uses a linear ramp generator to produce a constant-slope reference voltage.
- At the beginning of a conversion cycle, the counter is in the reset state, and the ramp generator output is 0 V.
- The analog input is greater than the reference voltage at this point. Hence, produces a high-level output from the comparator.
- This high level enables the clock to the counter, and starts the ramp generator.

Single Slope ADC

- When the increasing ramp generator output attains a level equal to the analog input, the comparator produces a low-level output.
- At this point, the ramp is reset, and the binary count is stored in the latches by the control logic.
- This binary count is a digital Equivalent to the analog input.



Example on Single Slope ADC

- $R = 10\ k\Omega, C = 0.1\ \mu F, V_{ref} = 1\ V, analog\ input = 2\ V,$ $clock\ frequency = 100\ kHz.$
- What is the binary count after the conversion?

- Ans. **200**