

**Indian Institute of Information Technology, Guwahati**  
**CS104: Computer Organization**  
**Mid-Semester**

**Total = 60 Marks**

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**Note:-**

1. There may be more than one correct option for some questions in Section A.
2. In such a case, marks will be awarded if only all the right options are selected, i.e., there is no partial marking in section A.
3. There is no negative marking.

**Section A**

**1 mark X 10 = 10 marks**

- Q1. Which of the following is/are true about Amdahl's Law?
  - a. Finding the overall speedup when only part of the system is improved.
  - b. Finding the overall execution time.
  - c. Referred to as quantitative principles in design.
  - d. It is also known as the law of diminishing return.
- Q2. In which register the instruction is in the form of a binary code that specifies what action the processor is to take?
  - a. Program Counter
  - b. Instruction Registers
  - c. Memory Address Register
  - d. Stack Pointer
- Q3. Which of the following is/are true regarding subroutine in MIPS?
  - a. By using subroutine, the same sequence of instructions can be used many times without the need to rewrite them repeatedly.
  - b. Subroutine requires no extra space in the memory.
  - c. \$v0-\$v1 register holding return functions results.
  - d. \$ra is the return address register to go back to the caller.
- Q4. Which of these statements is/are true regarding stack frame in MIPS?
  - a. \$sp is a stack pointer.
  - b. The data segment is where the variables are defined.
  - c. To allocate a stack frame of X bytes, we have to decrement the stack pointer by X at the start of the function.
  - d. To allocate a stack frame of X bytes, we have to increment the stack pointer by X at the start of the function.



Q5. Which of the following is/are true regarding the ISA?

- a. ISA fixed-width encoding is simple compared to variable width.
- b. ISA fixed-width encoding is complex as compared to variable width.
- c. ISA fixed-width takes less space in memory or caches.
- d. Variable-length takes less space in memory or caches.

Q6. Which of the following statements is/are true? (1 marks)

- a. Three address instructions usually resulted in less number of instructions as compared to others.
- b. Three address instructions usually resulted in more number of instructions as compared to others.
- c. Zero address instructions usually resulted in less number of instructions as compared to others.
- d. Zero address instructions usually resulted in more number of instructions as compared to others.

Q7. Match the following instruction to the corresponding addressing modes

- |                          |                 |
|--------------------------|-----------------|
| i. lw \$t0, 100(\$t1)    | a. Immediate    |
| ii. add \$t1, \$t2, \$t3 | b. Displacement |
| iii. add \$t0, 4         | c. Register     |
- a. i(a), ii(b), iii(c)
  - b. i(c), ii(a), iii(b)
  - c. i(b), ii(a), iii(c)
  - d. i(b), ii(c), iii(a)

Q8. Which of the following is/are true for the floating-point addition of two numbers using IEEE-754?

- a. Right shift the mantissa of the smaller number.
- b. Right shift the mantissa of the larger number.
- c. The number of shifting is equal to the difference between the exponents of the larger number and the smaller number.
- d. The number of shifting is equal to the sum of the exponents of the larger number and smaller number.

Q9. It is required to design a control unit using a microprogrammed control unit. Suppose there are 67 control signals. Which of the following statements is/are true?

- a. If we design using horizontal microinstruction encoding, then every control word is of length 67 bits.
- b. If we design using horizontal microinstruction encoding, then every control word is of length 7 bits.
- c. If we design using vertical microinstruction encoding, then every control word is of length 67 bits.
- d. If we design using vertical microinstruction encoding, then every control word is of length 7 bits.



- Q10. If \$t1 = 1000H and in Memory[1040] we have data FF25H, then  $\text{lw } \$t0, 40(\$t1)$  implies
- \$t0 = 1040H
  - \$t0 = 4010H
  - \$t0 = FF25H
  - \$t0 = 25FFH

### Section B

5 marks X 4 = 20 marks

Q1. A compiler designer is trying to decide between two code sequences for a particular machine. The hardware designers have supplied the following facts:

Instruction Class	CPI for this instruction class
A	3
B	2
C	1

For a particular high-level language statement, the compiler writer is considering two code sequences that require the following instruction counts:

Code Sequence	Instruction Count for this instruction class		
	A	B	C
1	1	2	4
2	3	1	1

Which code sequence executes the most instructions? Which will be faster? What is the CPI for each sequence? (1 + 2 + 2 = 5 marks)

Q2. Suppose that a machine A executes a program with IC = 50,000,000; average CPI = 2.5, and clock rate = 1.0 MHz.

- What is the execution time in seconds? (2 marks)
- Out of the total execution time, 50% is consumed by multiply operations. It is required to make the program run 1.5 times faster. By how much must the speed of the multiplier be improved? (3 marks)

Q3. There are 150 control signals in a processor data path. To implement diagonal schemes, the control signals are divided into 5 groups 5, 10, 16, 65, and 54. Determine the control word size for the horizontal, vertical and diagonal schemes (1 + 1 + 3 = 5 marks)

Q4. Using IEEE 754 single-precision add the two decimal numbers  $N1 = 128.6875$  and  $N2 = 42.125$ . Represent the final results in hexadecimal format. (5 marks)

Handwritten calculations for Q4:

$$\begin{array}{r}
 128.6875 \\
 + 42.125 \\
 \hline
 170.8125
 \end{array}$$

Conversion to hexadecimal:  $170.8125_{10} = A2.5_{16}$



### Section C

10 marks X 3 = 30 marks

Q1. Answer the following:-

- a. Represent the decimal number 123.50 in IEEE 754 single-precision number. The final answer should be in hexadecimal format. (2 marks)
- b. Using Booth's Algorithm multiply  $-9 \times 7$  (8 marks)

Q2. Answer the following:-

- a. Consider  $N1 = 63$  and  $N2 = -63$ . Represent these numbers using:- (1+1 = 2 marks)
  - i. Signed magnitude representation
  - ii. Two's complement representation
- b. Using the non-restoring division method, perform  $17 \div 4$  (8 marks)

Q3. Write a MIPS program to add N consecutive digits from the memory location. Here in the first memory location, N is stored. The next N locations consist of the numbers to be added. Finally, you have to store the result in the (N+2)th location in the memory. (10 marks)

[Sample Input/ Output Format:

Input Format:

.num: word 5, 1, 2, 3, 4, 5, 0

Output: sum = 15

.num: word 5, 1, 2, 3, 4, 5, 15]

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