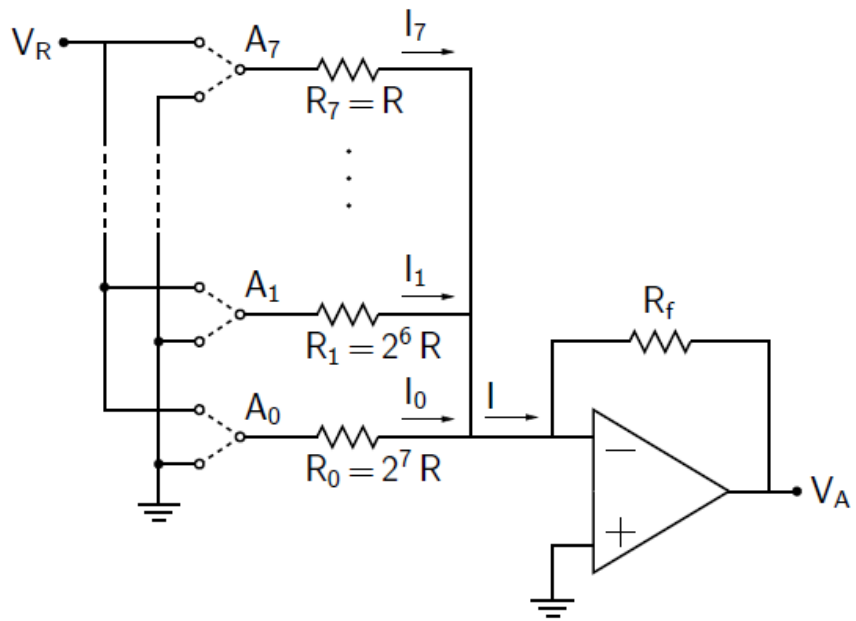
Tutorial 9

EC103

DAC, ADC [part-1]

Q.



* What is the maximum output voltage (in magnitude)? $V_R = 5\,\mathrm{V}$. $R_f = R$

A.

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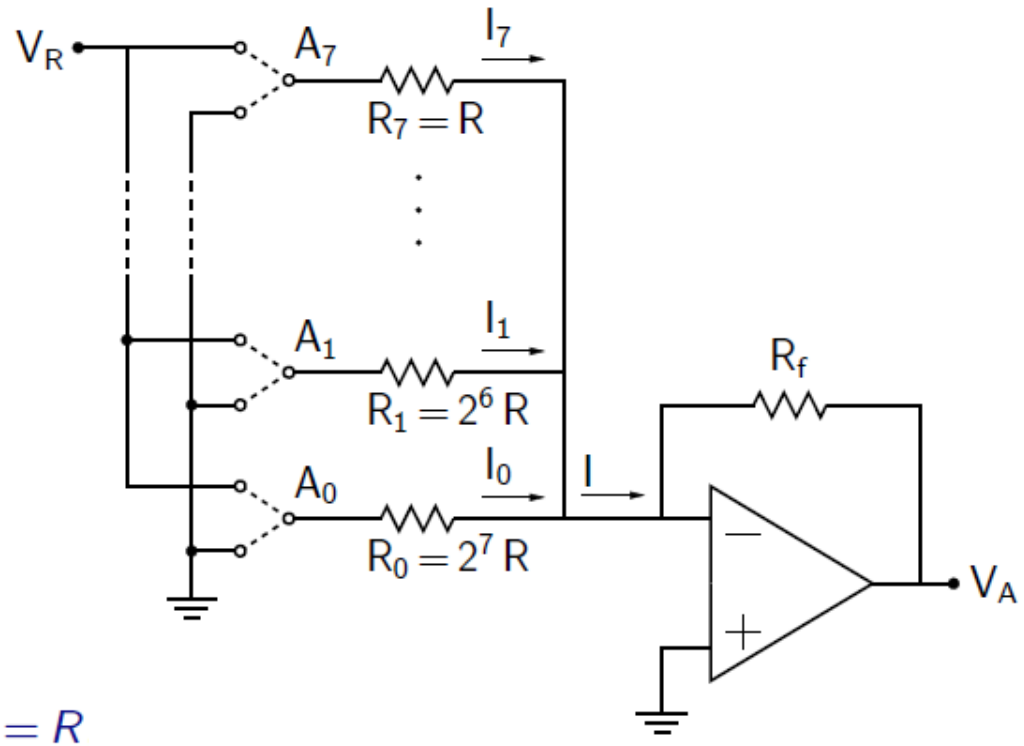
$$V_A = -\frac{V_R}{2^{N-1}} \frac{R_f}{R} \left[S_7 2^7 + \cdots + S_1 2^1 + S_0 2^0 \right].$$

Maximum V_A (in magnitude) is obtained when the input is `1111 1111`.

$$|V_A|^{\max} = \frac{5}{128} \times 1 \times \left[2^0 + 2^1 + \cdots + 2^7 \right] = \frac{5}{128} \times \left(2^8 - 1 \right) = 5 \times \frac{255}{128} = 9.961\,\mathrm{V}\,.$$

Q.



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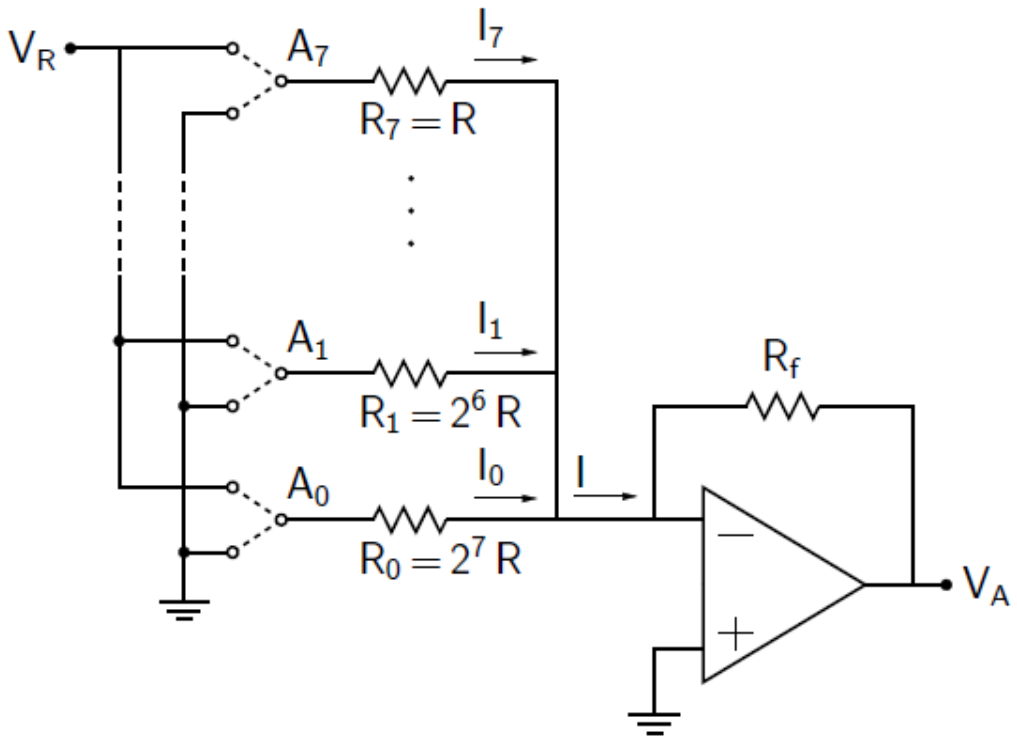
$$= -\frac{5}{128} \times 1 \times \left[2^7 + 2^5 + 2^3 + 2^2 + 2^0\right] = -5 \times \frac{173}{128} = -6.758\,\mathrm{V}\,.$$

Q.



$V_R = 5\,\text{V}.$ $\quad R_f = R$

* If the resistors are specified to have a tolerance of 1 %, what is the range of $|V_A|$ corresponding to input 1111 1111?

A.

$|V_A|$ is maximum when (a) currents I_0, I_1, etc. assume their maximum values, with $R_k = R_k^0 \times (1 - 0.01)$ and (b) R_f is maximum, $R_f = R_f^0 \times (1 + 0.01)$.
(The superscript '0' denotes nominal value.)

$$\rightarrow |V_A|^{\text{max}}_{11111111} = V_R \times \frac{255}{128} \times \left.\frac{R_f}{R}\right|^{\text{max}} = 5 \times \frac{255}{128} \times \frac{1.01}{0.99} = 10.162\,\text{V}.$$

Similarly, $|V_A|^{\text{min}}_{11111111} = 5 \times \frac{255}{128} \times \frac{0.99}{1.01} = 9.764\,\text{V}.$

Q.

- Why is this (the configuration in the last question) not an acceptable situation?

A.

* ΔV_A for input 1111 1111 $= 10.162 - 9.764 \approx 0.4\,\mathrm{V}$ which is larger than the resolution ($0.039\,\mathrm{V}$) of the DAC. This situation is not acceptable.

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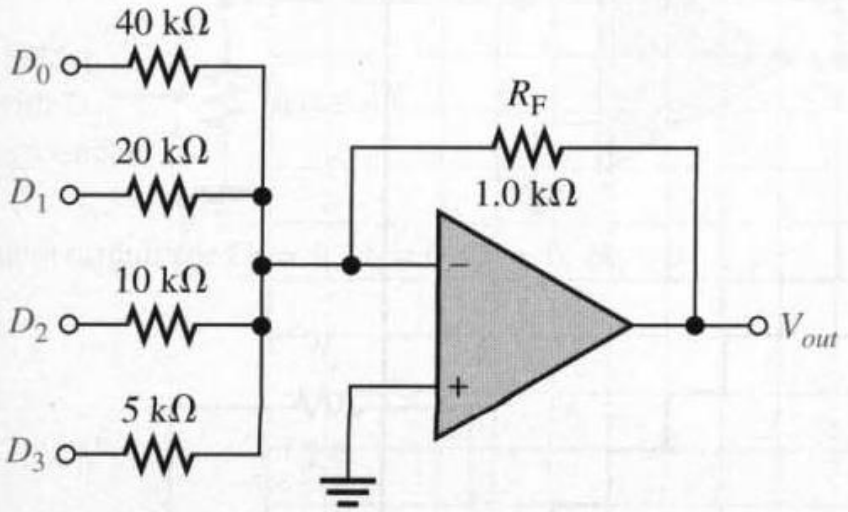
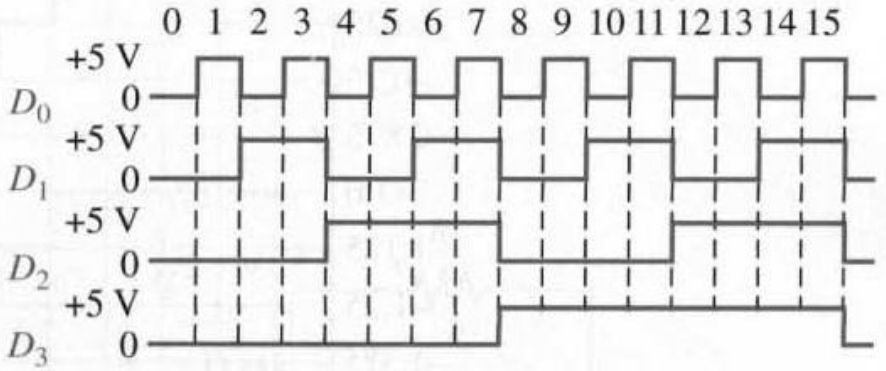
- Extra point:

* The output voltage variation can be reduced by using resistors with a smaller tolerance. However, it is difficult to fabricate an IC with widely varying resistance values (from R to $2^{N-1}R$) and each with a small enough tolerance.

Q. Determine the output of the DAC in Figure 14–21(a) if the waveforms representing a sequence of 4-bit binary numbers in Figure 14–21(b) are applied to the inputs. Input D_0 is the least significant bit (LSB).



(a)



(b)

FIGURE 14–21

A.

Solution First, determine the current for each of the weighted inputs. Since the inverting (−) input of the op-amp is at 0 V (virtual ground) and a binary 1 corresponds to +5 V, the current through any of the input resistors is 5 V divided by the resistance value.

$$I_0 = \frac{5\text{ V}}{40\text{ k}\Omega} = 0.125\text{ mA}$$

$$I_1 = \frac{5\text{ V}}{20\text{ k}\Omega} = 0.25\text{ mA}$$

$$I_2 = \frac{5\text{ V}}{10\text{ k}\Omega} = 0.5\text{ mA}$$

$$I_3 = \frac{5\text{ V}}{5\text{ k}\Omega} = 1.0\text{ mA}$$

A.

There is essentially no current at the inverting op-amp input because of its extremely high impedance. Therefore, assume that all of the current goes through the feedback resistor R_F. Since one end of R_F is at 0 V (virtual ground), the drop across R_F equals the output voltage, which is negative with respect to virtual ground.

$$V_{OUT(D0)} = (1.0\ \text{k}\Omega)(-0.125\ \text{mA}) = -0.125\ \text{V}$$
$$V_{OUT(D1)} = (1.0\ \text{k}\Omega)(-0.25\ \text{mA}) = -0.25\ \text{V}$$
$$V_{OUT(D2)} = (1.0\ \text{k}\Omega)(-0.5\ \text{mA}) = -0.5\ \text{V}$$
$$V_{OUT(D3)} = (1.0\ \text{k}\Omega)(-1.0\ \text{mA}) = -1.0\ \text{V}$$

From Figure 14–21(b), the first binary input code is 0000, which produces an output voltage of 0 V. The next input code is 0001, which produces an output voltage of −0.125 V. The next code is 0010, which produces an output voltage of −0.25 V. The next code is 0011, which produces an output voltage of −0.125 V + −0.25 V = −0.375 V. Each successive binary code increases the output voltage by −0.125 V, so for this particular straight binary sequence on the inputs, the output is a stairstep waveform going from 0 V to −1.875 V in −0.125 V steps. This is shown in Figure 14–22.

A.

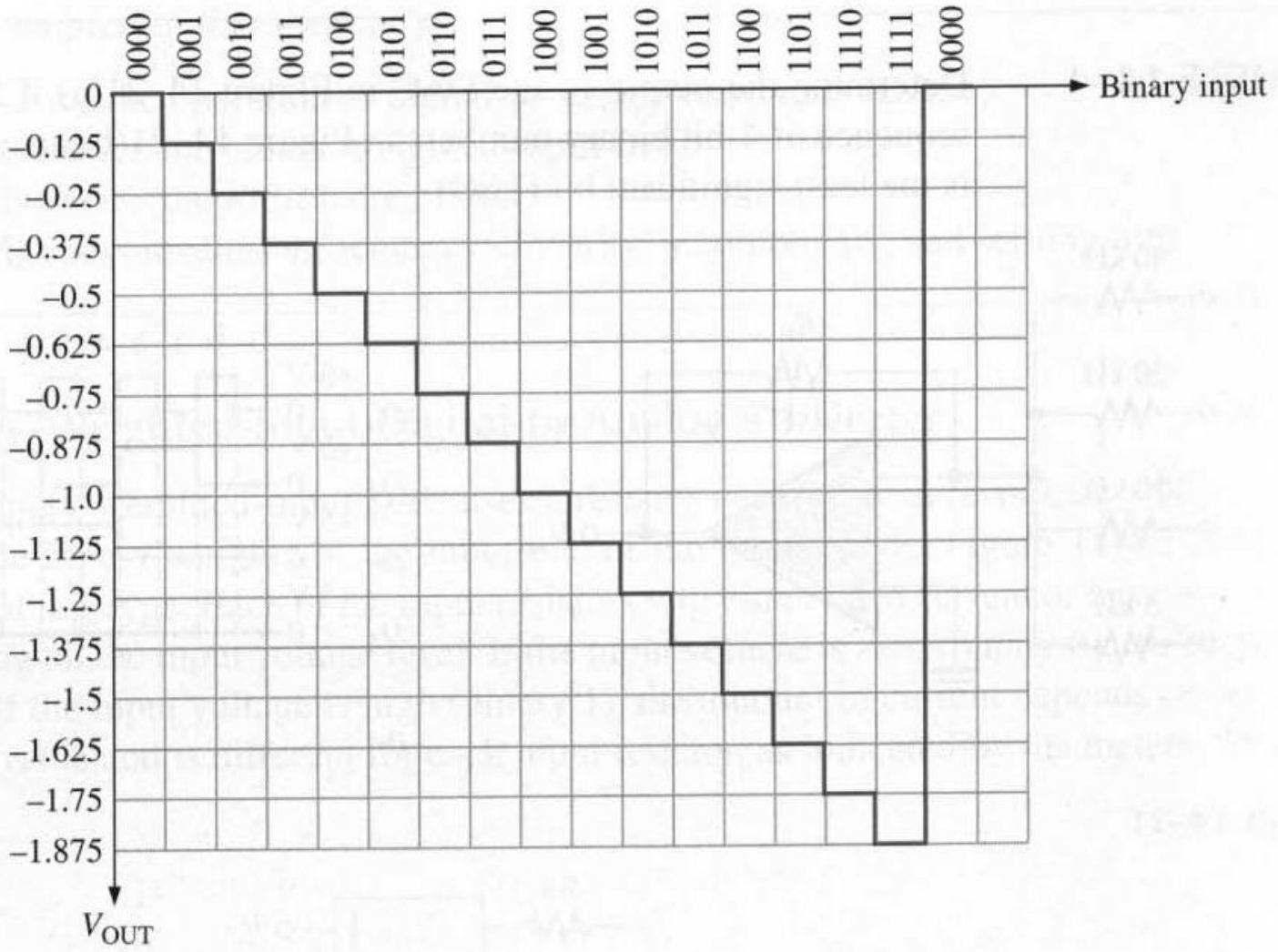


FIGURE 14–22
Output of the DAC in Figure 14–21.

Q.

Determine the resolution, expressed as a percentage, of **(a)** an 8-bit DAC and **(b)** a 12-bit DAC.

A.

Solution

(a) For the 8-bit converter,

$$\frac{1}{2^8 - 1} \times 100 = \frac{1}{255} \times 100 = \mathbf{0.392\%}$$

(b) For the 12-bit converter,

$$\frac{1}{2^{12} - 1} \times 100 = \frac{1}{4095} \times 100 = \mathbf{0.0244\%}$$

Q.

Determine the binary code output of the 3-bit flash ADC for the analog input signal in Figure 14–31 and the sampling pulses (encoder Enable) shown. For this example, $V_{REF} = +8$ V.

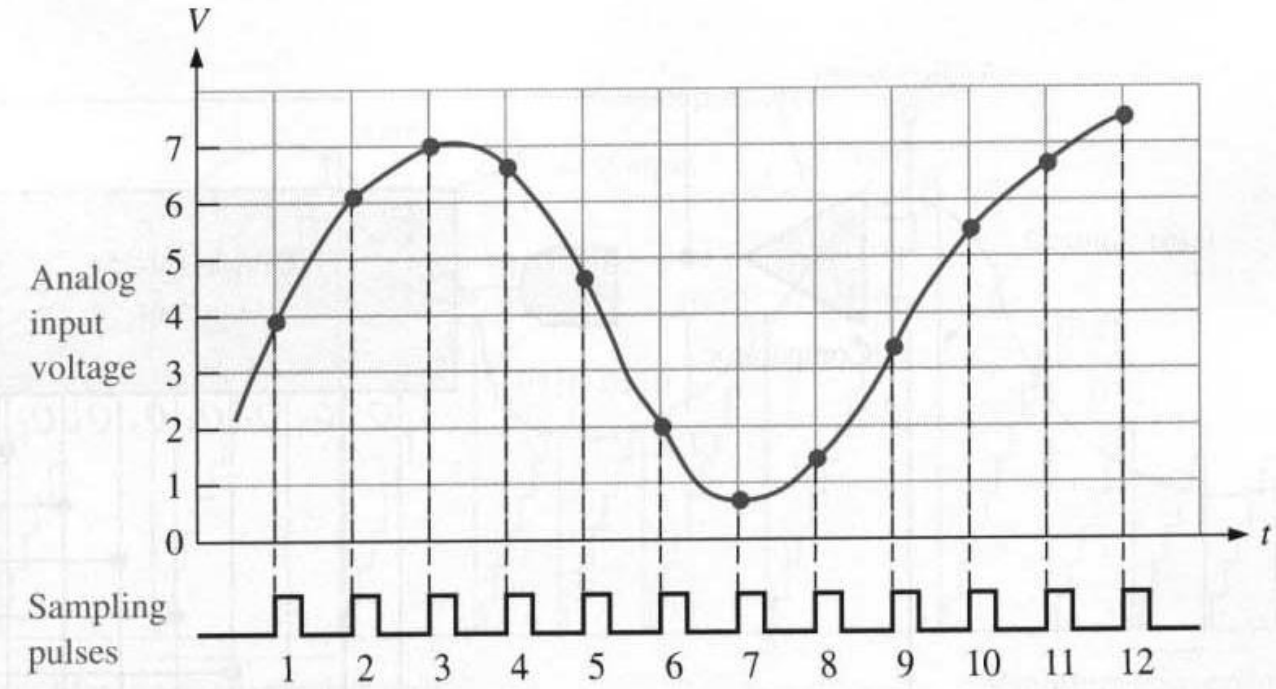


FIGURE 14–31
Sampling of values on an analog waveform for conversion to digital form.

A.

Solution The resulting A/D output sequence is listed as follows and shown in the waveform diagram of Figure 14–32 in relation to the sampling pulses.

100, 110, 111, 110, 100, 010, 000, 001, 011, 101, 110, 111

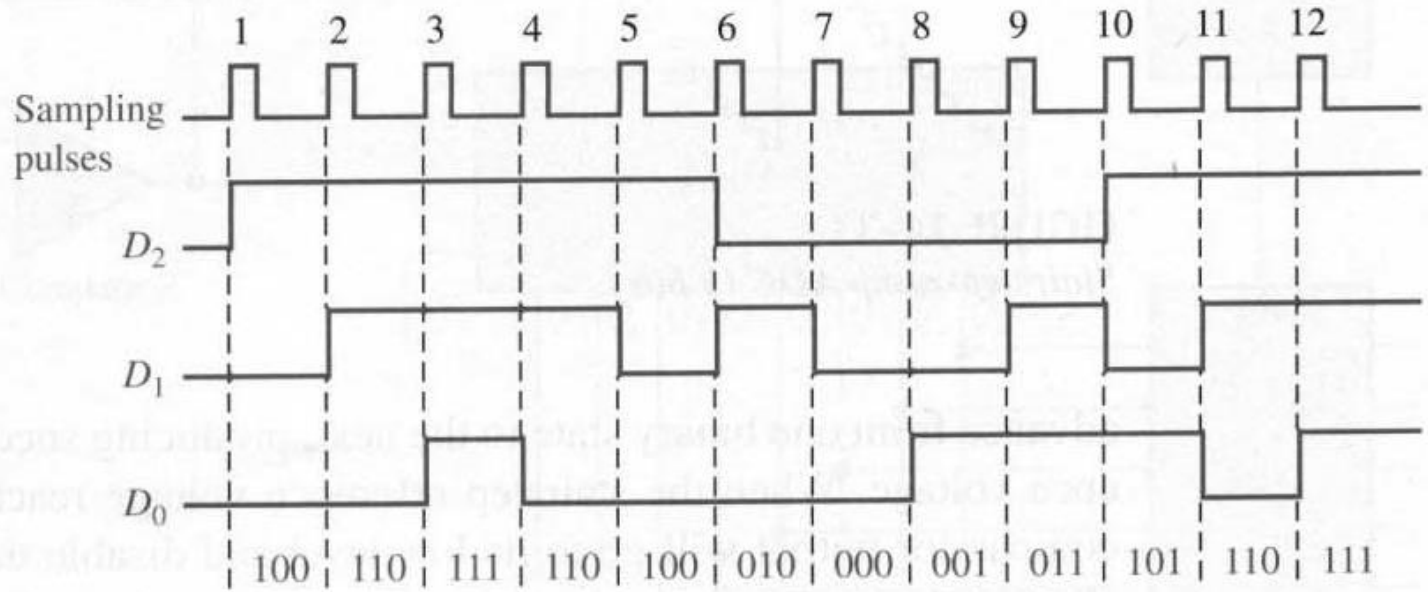


FIGURE 14–32
Resulting digital outputs for sampled values. Output D_0 is the least significant bit (LSB).