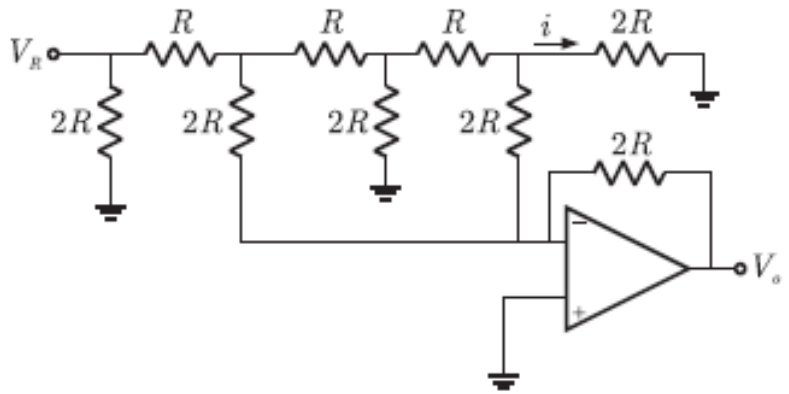
Tutorial 11

EC103

(GATE Questions: ADC , DAC)

Question 1 (GATE)

In the Digital-to-Analog converter circuit shown in the figure below,
$V_R = 10V$ and $R = 10k\Omega$



The current is

(A) $31.25\mu A$

(B) $62.5\mu A$

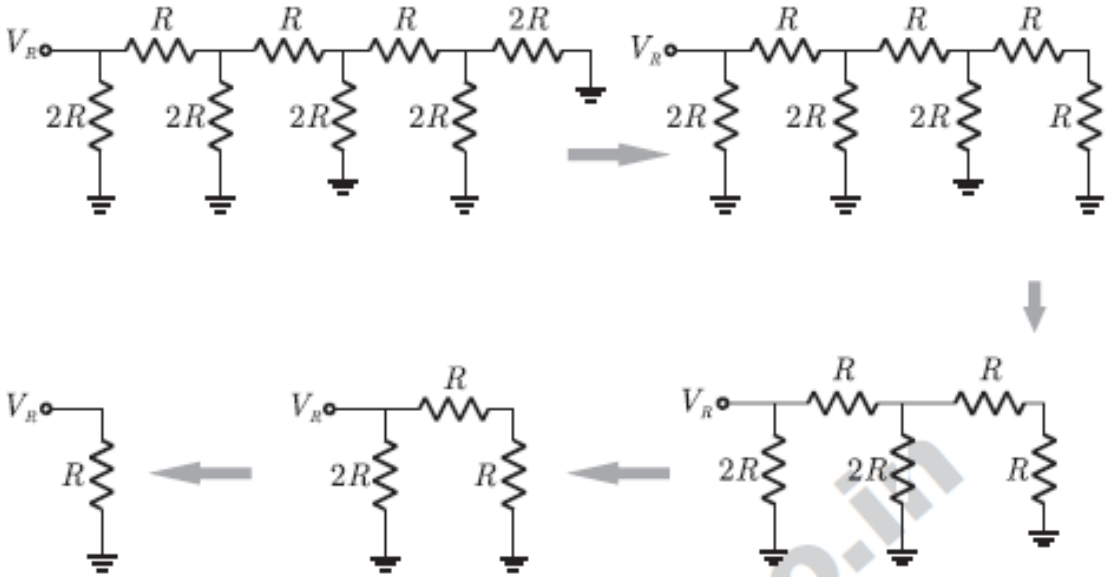
(C) $125\mu A$

(D) $250\mu A$

Answer

Option (B) is correct.

Since the inverting terminal is at virtual ground the resistor network can be reduced as follows

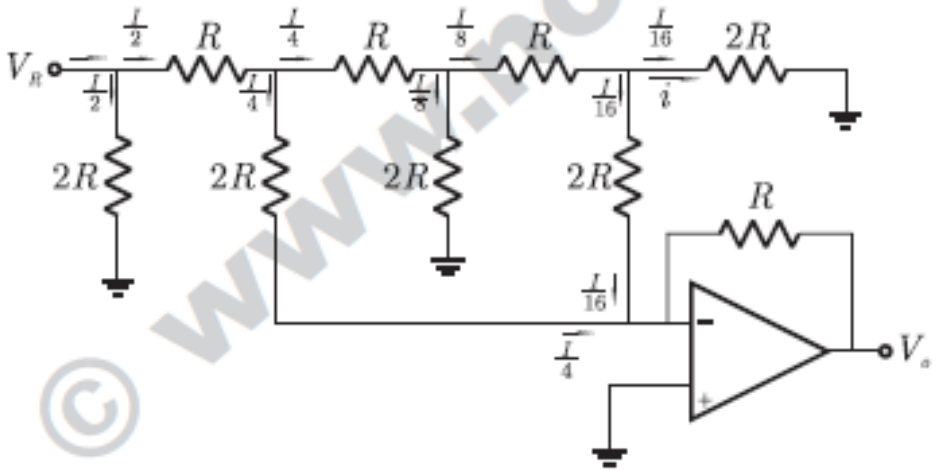


The current from voltage source is

$$I = \frac{V_R}{R} = \frac{10}{10k} = 1\text{ mA}$$

Answer

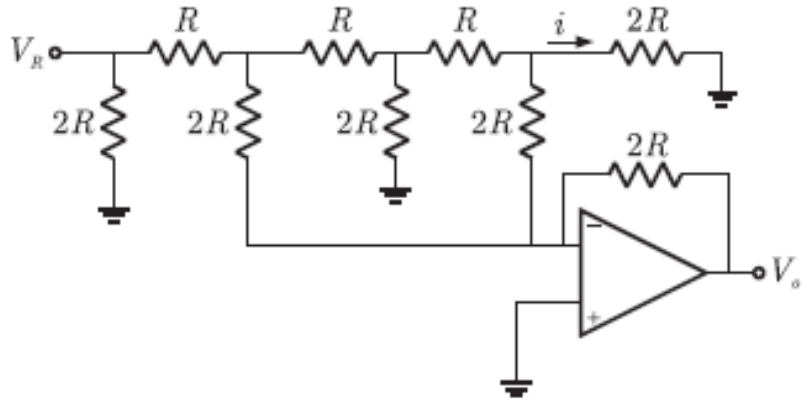
This current will be divide as shown below



Now $$i = \frac{I}{16} = \frac{1 \times 10^{-3}}{16} = 62.5\ \mu\ \text{A}$$

Question 2 (GATE)

In the Digital-to-Analog converter circuit shown in the figure below,
$V_R = 10V$ and $R = 10k\Omega$



The voltage V_0 is

(A) -0.781 V

(B) -1.562 V

(C) -3.125 V

(D) -6.250 V

Answer

Option (C) is correct.

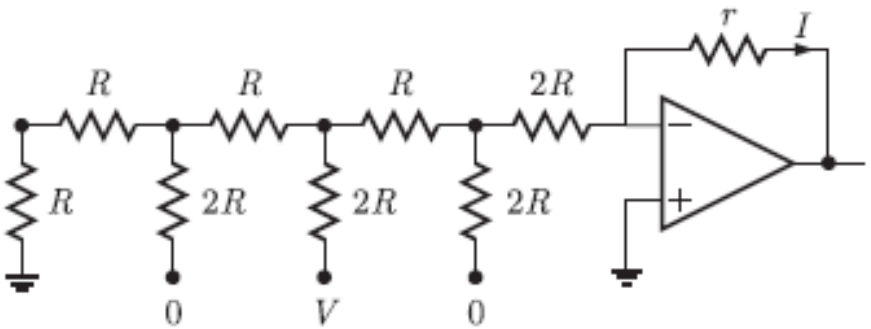
The net current in inverting terminal of OP - amp is

$$I = \frac{1}{4} + \frac{1}{16} = \frac{5I}{16}$$

So that $$V_0 = -R \times \frac{5I}{16} = -3.125$$

Question 3 (GATE)

The current I through resistance r in the circuit shown in the figure is



(A) $\frac{-V}{12R}$

(B) $\frac{V}{12R}$

(C) $\frac{V}{6R}$

(D) $\frac{V}{3T}$

Answer

- V/12R

Question 4 (GATE)

The circuit shown in the figure is a 4 bit DAC

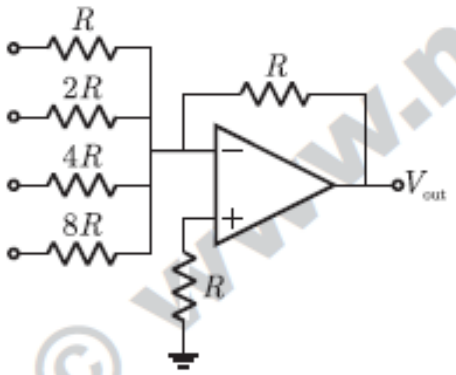


Fig. Q

The input bits 0 and 1 are represented by 0 and 5 V respectively. The OP AMP is ideal, but all the resistance and the 5 v inputs have a tolerance of ±10%. The specification (rounded to nearest multiple of 5%) for the tolerance of the DAC is

(A) ±35%
(B) ±20%
(C) ±10%
(D) ±5%

Answer

Option (A) is correct.

$$V_o = -V_1\left[\frac{R}{R}b_o + \frac{R}{2R}b_1 + \frac{R}{4R}b_2 + \frac{R}{4R}b_3\right]$$

Exact value when $V_1 = 5$, for maximum output

$$V_{oExact} = -5\left[1 + \frac{1}{2} + \frac{1}{4} + \frac{1}{8}\right] = -9.375$$

Maximum V_{out} due to tolerance

$$V_{omax} = -5.5\left[\frac{110}{90} + \frac{110}{2 \times 90} + \frac{110}{4 \times 90} + \frac{110}{8 \times 90}\right]$$

$$= -12.604$$

Tolerance $= 34.44\% = 35\%$

Question 5 (GATE)

The minimum number of comparators required to build an 8-bits flash ADC is

(A) 8

(B) 63

(C) 255

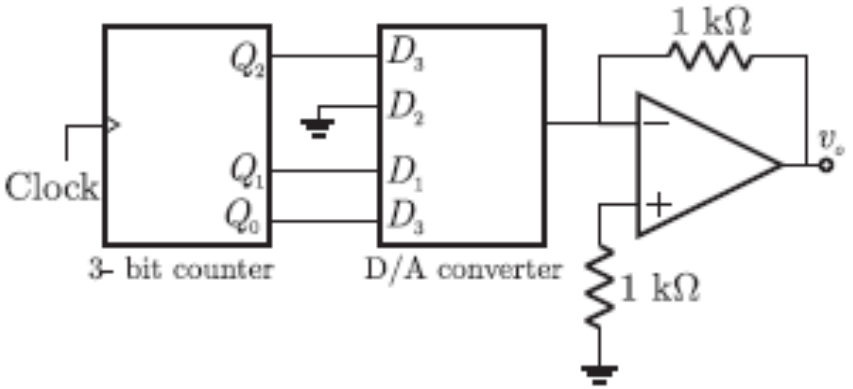
(D) 256

Answer

- (C) 255

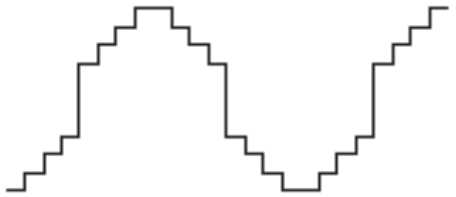
Question 6 (GATE)

A 4 - bit DAC is connected to a free - running 3 - big UP counter, as shown in the following figure. Which of the following waveforms will be observed at V_0 ?



In the figure shown above, the ground has been shown by the symbol ∇

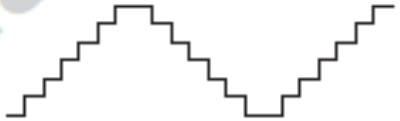
(A)



(B)

(C)

(D)



Answer

Option (B) is correct.

Q_2Q_1Q0	$D_3 = Q_2$	$D_2 = 0$	$D_1 = Q_1$	$D_0 = Q_0$	V_o
000	0	0	0	0	0
001	0	0	0	1	1
010	0	0	1	0	2
011	0	0	1	1	3
100	1	0	0	0	8
101	1	0	0	1	9
110	1	0	1	0	10
111	1	0	1	1	11
000	0	0	0	0	0
001	0	0	0	1	1

Question 7 (GATE)

The resolution of a 4-bit counting ADC is 0.5 volts. For an analog input of 6.6 volts, the digital output of the ADC will be

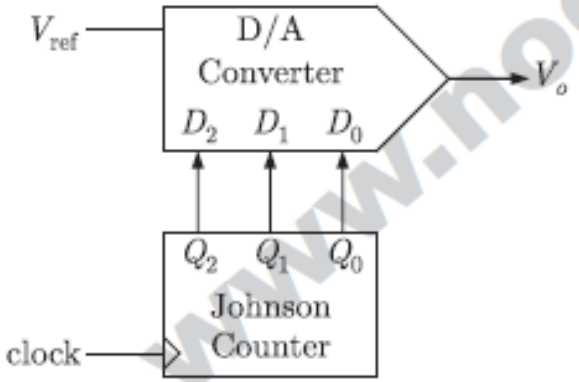
(A) 1011
(B) 1101
(C) 1100
(D) 1110

Answer

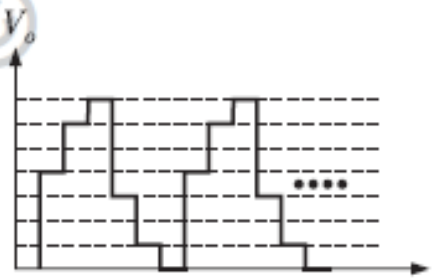
- (B) 1101

Question 8 (GATE)

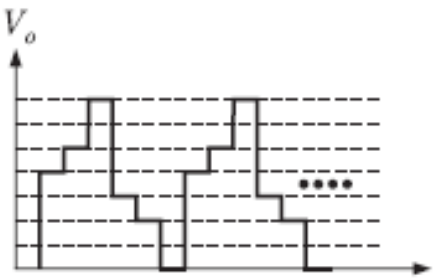
The output of a 3-stage Johnson (twisted ring) counter is fed to a digital-to analog (D/A) converter as shown in the figure below. Assume all states of the counter to be unset initially. The waveform which represents the D/A converter output V_o is



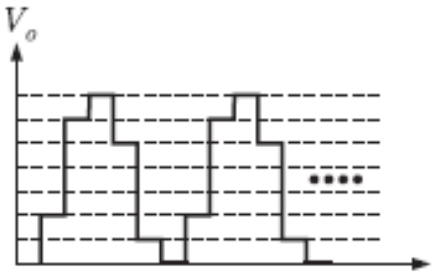
(A)



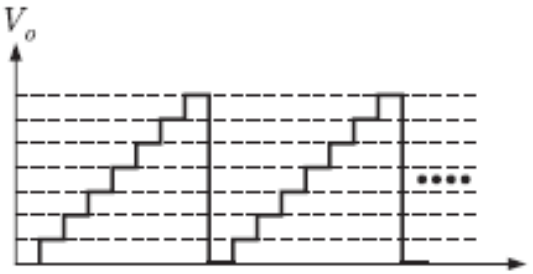
(B)



(C)



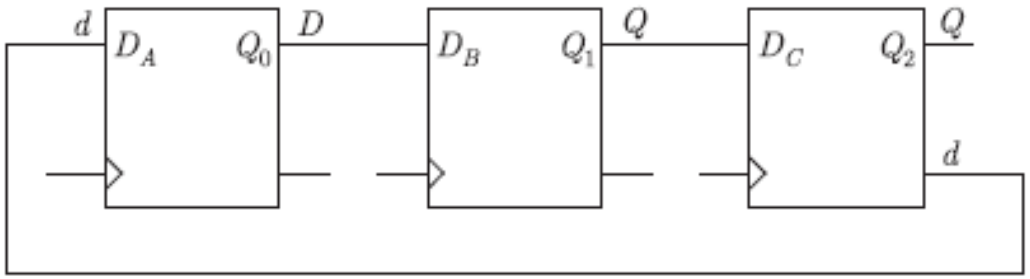
(D)



Answer

Option (A) is correct.

All the states of the counter are initially unset.



State Initially are shown below in table :

Q_2	Q_1	Q_0	
0	0	0	0
1	0	0	4
1	1	0	6
1	1	1	7

Question 9 (GATE)

The output Y of a 2-bit comparator is logic 1 whenever the 2-bit input A is greater than the 2-bit input B. The number of combinations for which the output is logic 1, is

(A) 4

(B) 6

(C) 8

(D) 10

Answer

Option (B) is correct.

$Y = 1$, when $A > B$

$A = a_1a_0$, $B = b_1b_0$

a_1	a_0	b_1	b_0	Y
0	1	0	0	1
1	0	0	0	1
1	0	0	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1

Total combination = 6