



**Instructions:**

1. There are 2 sections. Both sections have multiple questions/ sub-sections. P → def
  2. While Section I is compulsory, Section II has 3 sub-sections. You are required to answer any two of the 3 sub-sections in Section II. In the event that you answer all three, the best two will be considered. P → s

**SECTION I [30 Marks]**

### **Question A**

1. Only two companies manufacture smartphones. 20% of the smartphones from company SAM and 5% from company APP are defective. Company SAM produces twice as many smartphones as Company APP each week.

(a) What is the probability that a smartphone, randomly chosen from a week's production, is not defective (i.e. satisfactory)?

(b) If the chosen smartphone is defective, what is the probability that it came from Company SAM?

2. Prove that the information measure is additive: that the information gained from observing the combination of  $N$  independent events, whose probabilities are  $p_i$  for  $i = 1 \dots N$ , is the sum of the information gained from observing each one of these events separately and in any order.

3. What is the shortest possible code length, in bits per average symbol, that could be achieved for a six-letter alphabet whose symbols have the following probability distribution?

$$\left\{ \frac{1}{2}, \frac{1}{4}, \frac{1}{8}, \frac{1}{16}, \frac{1}{32}, \frac{1}{32} \right\}$$

4. Suppose that crows are black with a probability of 0.6, that they are male with a probability of 0.5, and female with a probability of 0.5, but that male crows are 3 times more likely to be black than female crows. If you see a non-black crow, what is the probability that it is male?

5. Let  $p(x)$  and  $q(x)$  be two probability distributions specified over integers  $x$ .

(a) What is the Kullback-Leibler (KL) distance between these distributions?

(b) If we have devised an optimally compact code for the random variable described by  $q(x)$ , what does the KL tell us about the effectiveness of our code if the probability distribution is  $p(x)$  instead of  $q(x)$ ?

(c) What happens to this metric if there are some forbidden values of  $x$  for which  $p(x) = 0$ , and other values of  $x$  for which  $q(x) = 0$ ?

6. For a binary symmetric communication channel whose input source is the alphabet  $X = \{0, 1\}$  with probabilities  $\{0.5, 0.5\}$  and whose output alphabet is  $Y = \{0, 1\}$ , having the following channel matrix where  $\epsilon$  is the probability of transmission error:  $\begin{pmatrix} 1 - \epsilon & \epsilon \\ \epsilon & 1 - \epsilon \end{pmatrix}$

(a) How much uncertainty is there about the input symbol once an output symbol has been received?

(b) What is the mutual information  $I(X; Y)$  of this channel?

(c) What value of  $\epsilon$  maximises the uncertainty  $H(X|Y)$  about the input symbol given an output symbol?

$$\begin{aligned}
 a). P(\text{defect in SAM}) &= 1 - 0.2 = 0.8 \\
 &\quad \text{or} \quad 1 - 0.05 = 0.95 \\
 &= \frac{2}{7} \times 0.8 + \frac{5}{7} \times 0.95
 \end{aligned}$$

b)  $P = 0.2 \times \frac{2}{3} = \frac{0.4}{3} = 0.133$

~~1/2 from SAM~~  
SAM protocol

$$0.5\left(\frac{3}{4} + P\right) = 0.5\left(\frac{1}{4} + (1-P)\right)$$

$$\Rightarrow P =$$

## SECTION II [40 Marks]

### Question B

1. Construct an efficient, uniquely decodable binary code, having the prefix property and having the shortest possible average code length per symbol, for an alphabet whose five letters appear with these probabilities:

*guru*

| Letter | Probability |
|--------|-------------|
| A      | 1/2         |
| B      | 1/4         |
| C      | 1/8         |
| D      | 1/16        |
| E      | 1/16        |

(two black & male)

$$\frac{3}{4} \times 0.6 = 0.45$$

$$\text{fem} = \frac{1}{4} \times 0.6 = 0.15$$

How do you know that your code has the shortest possible average code length per symbol? (10)

2. Consider the second-order extension of the discrete memoryless source with three symbols  $S = (X, Y, Z)$  with the state probabilities  $P = (0.7, 0.15, 0.15)$  for its output. Apply Huffman encoding to compute the codewords for the extended source and also its efficiency. (10)

### Question C

- Prove that  $H(X, Y) = H(X) + H(Y|X)$ . (5)
- State and prove Jensen's inequality. (5)
- Consider a sequence of  $n$  binary random variables  $X_1, X_2, \dots, X_n$ . Each sequence with an even number of 1's has probability  $2^{-(n-1)}$  and each sequence with an odd number of 1's has probability 0. Find the mutual information  $I(X_1; X_2), I(X_2; X_3|X_1), \dots, I(X_{n-1}; X_n|X_1, \dots, X_{n-2})$ . (10)

### Question D

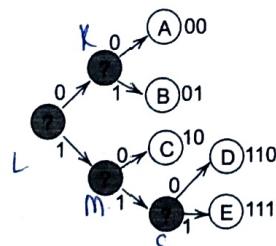
1. A two-state Markov process may emit '0' in State 0 or emit '1' in State 1, each with probability  $\beta$ , and return to the same state; or with probability  $1-\beta$  it emits the other symbol and switches to the other state. Thus it tends to be sticky or oscillatory, two forms of predictability, depending on  $\beta$ .

$$\begin{matrix} 0 & \rightarrow & 1 \\ \beta & & 1-\beta \end{matrix}$$

- What are the state occupancy probabilities for  $0 < \beta < 1$ ? (3)
- What are the entropy of State 0, the entropy of State 1, and the overall entropy of this source? Express your answers in terms of  $\beta$ . (4)
- For what value(s) of  $\beta$  do both forms of predictability disappear? What then is the entropy of this source? (3)

2. Huffman trees enable the construction of uniquely decodable prefix codes with optimal codeword lengths. The five codewords shown here for the alphabet  $S = \{A, B, C, D, E\}$  form an instantaneous prefix code.

$$(3) \quad (4) \quad (3)$$



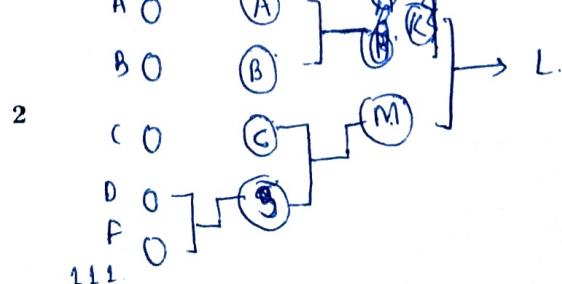
$$P(A), P(B), P(C), P(D), P(E),$$

$$H_A, H_B, H_C, H_D, H_E,$$

$$H = P_A H_A + P_B H_B + P_C H_C + P_D H_D + P_E H_E$$

$xx$   $xy$   $xz$   
 $yy$   $yz$   
 $zz$

- Give a probability distribution for the five letters that would result in such a tree. (3)
- Calculate the entropy of that distribution. (3)
- Compute the average codeword length for encoding this alphabet. Relate your results to the Source Coding Theorem. (4)





**EC381: Embedded System**  
**Mid-Semester Examinations**  
**IIIT Guwahati**

**Time: 2 hours**

**Total 50 Marks**

**Section A**

**$3 \times 5 = 15$  Marks**

Q1. List the notable subsystems of an Embedded Systems?

Q2. With a neat diagram and example, explain event triggered and time triggered.

Q3. Using Rate Monotonic scheduling determines whether the system is schedulable or not for the following?

| Process | Execution Time | Period |
|---------|----------------|--------|
| A       | 1              | 8      |
| B       | 2              | 5      |
| C       | 1              | 10     |
| D       | 2              | 25     |

Washing machine  
Earthquake

Q4. What happens to the program status registers and the program counter during an exception in the ARM processor?

Q5. If we are manufacturing 1000 embedded devices and want to minimize the per-unit cost, then which choice should we select from the following.

|          | $C_{NRE}$ (Non Recurring Expenditure) | $C_{UNIT}$ (Unit Cost) |
|----------|---------------------------------------|------------------------|
| Choice A | 50,000                                | 1000                   |
| Choice B | 100,000                               | 1000                   |
| Choice C | 250,000                               | 400                    |

**Section B**

**$5 \times 3 = 15$  Marks**

Q6. Draw a bubble diagram of PIC16F877 and explain its architecture?

Q7. With an example, discuss how you can implement a nested subroutine in ARM?

Q8. Consider the following two processes A and B.

| Process A |         |                |        |  | Process B |         |                |        |
|-----------|---------|----------------|--------|--|-----------|---------|----------------|--------|
|           | Arrives | Execution Time | End By |  |           | Arrives | Execution Time | End By |
| A1        | 0       | 1              | 2      |  | B1        | 0       | 3              | 6      |
| A2        | 2       | 1              | 4      |  | B2        | 6       | 3              | 12     |
| A3        | 4       | 1              | 6      |  | B3        | 12      | 3              | 18     |
| ...       | ...     | ...            | ...    |  | ...       | ...     | ...            | ....   |

18 units of time

Show the execution of the two processes using fixed-priority preemptive scheduling where A has higher priority.

E D F

**Section C****6 x 2 = 12 Marks**

Q9. With a neat block diagram explain a multiple bus system. Represent a UML state diagram of bus bridge operation.

Q10. With a neat block diagram explain the architecture of the 8051 microcontroller?

**Section D****8 Marks**

Q11 Using Least Laxity First Algorithm show the scheduling of the following processes:-

| Process | Arrival | Duration | Deadline |
|---------|---------|----------|----------|
| A       | 0       | 6        | 32       |
| B       | 3       | 3        | 6        |
| C       | 6       | 12       | 37       |
| D       | 9       | 8        | 30       |

Show up to 16 units of time. If, at any instance, the same laxity occurs, then schedule according to FCFS

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INDIAN INSTITUTE OF INFORMATION TECHNOLOGY GUWAHATI

End-Semester Examination

EC 361: VLSI Design

Time: 3 Hours, Total Marks: 90, Date: 25<sup>th</sup> April 2023

**Note:**

- (i) Answer all questions.
- (ii) Write down the assumptions clearly, if any. No queries will be entertained during the exam hours.

1. (a) Consider a CMOS inverter with a capacitive load of  $C_L$ . The PMOS and NMOS aspect ratios are  $(\frac{W}{L})_p$  and  $(\frac{W}{L})_n$  respectively,  $k'_n = \mu_n C_{ox}$ ,  $k'_p = \mu_p C_{ox}$ , threshold voltages of PMOS and NMOS are  $|V_{tp}|$  and  $V_{tn}$  respectively. If the input voltage transits from 0 to  $V_{DD}$ , prove that propagation delay at the output, i.e. time it takes for the output to drop to  $\frac{V_{DD}}{2}$  from  $V_{DD}$  is  $\tau_{PHL} = \frac{C_L}{k'_n(\frac{W}{L})_n(V_{DD}-V_{tn})} \left[ \frac{2V_{tn}}{V_{DD}-V_{tn}} + \ln \left\{ \frac{3V_{DD}-4V_{tn}}{V_{DD}} \right\} \right]$ . Similarly, when the input transits from  $V_{DD}$  to 0, prove that the propagation delay at the output while rising from 0 to  $\frac{V_{DD}}{2}$  is  $\tau_{PLH} = \frac{C_L}{k'_p(\frac{W}{L})_p(V_{DD}-|V_{tp}|)} \left[ \frac{2|V_{tp}|}{V_{DD}-|V_{tp}|} + \ln \left\{ \frac{3V_{DD}-4|V_{tp}|}{V_{DD}} \right\} \right]$  [8+7]

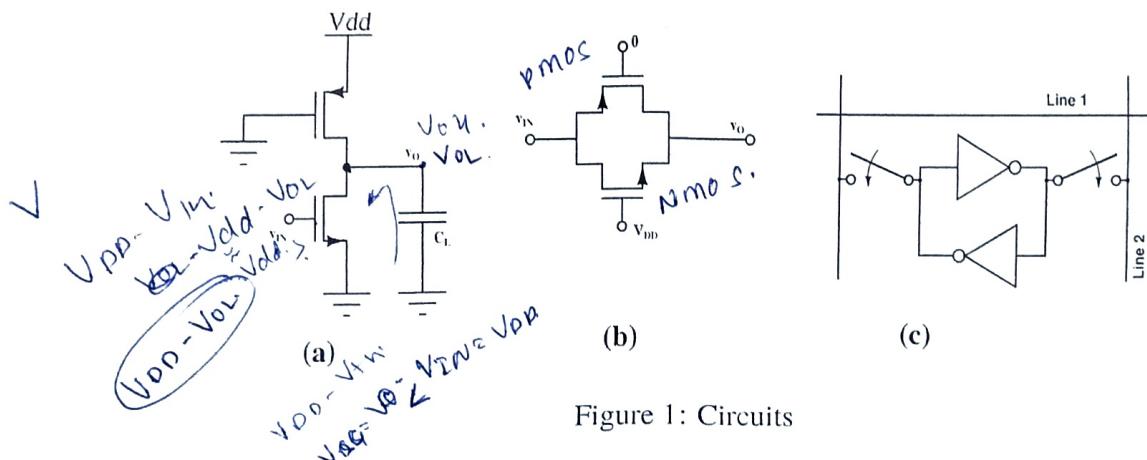


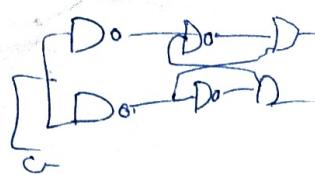
Figure 1: Circuits

2. Consider the pseudo NMOS inverter of Fig. 1(a). For the circuit,  $V_{in} = |V_{tp}| = V_t$ . Conductance parameters of NMOS and PMOS are  $k_n$  and  $k_p$  respectively and they are related as  $k_n = rk_p$ .
- (a) Derive the following noise margin parameters of the above circuit, viz.  $V_{on}$ ,  $V_{ol}$ ,  $V_{ih}$  and  $V_{il}$ . [3+3+3+3]
  - (b) Also, derive the threshold voltage of the circuit  $V_{TH}$ , where  $V_{in} = V_{out} = V_{TH}$  [3]
3. For the complementary pass transistor of Fig. 1(b), assume  $v_{in} = V_{DD}$ .

$$V_o \approx V_{DD}$$

$$V_{in} = V_{DD}$$

- (a) Express the equivalent resistance of the PMOS,  $R_{eq,p}$ , and of the NMOS,  $R_{eq,n}$  as  $v_o$  varies through 0,  $|V_{tp}|$ ,  $V_{DD} - V_{tn}$ . Plot  $R_{eq,p}$ ,  $R_{eq,n}$  and the equivalent resistance of the CMOS pass switch w.r.t.  $v_o$ . [2+2+3]
- (b) Draw the gate level schematic of a typical **clocked** SR flip flop. For the same circuit, draw its transistor level equivalent circuit, designed using CMOS logic. For this circuit, determine the gate count. [2+4+2]
4. (a) Consider a 4-input NOR gate and a 4-input NAND gate. Both these gates are to be sized with reference to an inverter. The said gates are to be designed using  $0.5 \mu m$  process technology. The reference inverter circuit has PMOS aspect ratio of 6 and NMOS aspect ratio of 1.5. Draw the circuits and size the transistors appropriately. [4+6]
- (b) Consider a simple SR flip-flop designed with two back-to-back connected NOR gate. Drawing the transistor level schematic, explain how the output of the flip-flop changes from  $S = 1, R = 0$  state to  $S = 0, R = 1$  state by properly identifying the operations of the transistors. ( Detailed mathematical derivations are not required ) [5]
5. (a) Consider the symbolic representation of a typical memory cell of an SRAM in Fig. 1(c). Put the names of the lines Line 1, Line 2. Draw the transistor level circuit of the memory cell. Explain the role of a sense amplifier in a typical SRAM structure. Explain how read operation is performed by the circuit if the initial content is  $V_Q = "1" = V_{DD}$ . Also, explain how a write operation done if the memory content is  $V_Q = "1"$  and the user wishes to write "0" [2+4+2+4+3]
6. (a) Draw the CMOS transistor level schematic of a 2 input NOR gate. At one input, a square wave with a 50 % duty cycle and time period  $T$  is fed and in another input a square wave of 50 % duty cycle and time period  $\frac{T}{2}$ . Draw clearly the input waveforms and the output waveform. [2+3]
- (b) Consider the case when both inputs are shorted and  $v_{in} = v_o = v_{TH}$ , by using proper voltage levels, prove that one of the PMOS transistor is in saturation and the other one is in linear region and identify them. [2+3]
- (c) If  $V_{tn} = |V_{tp}| = V_t$ , prove that  $v_{TH} = \frac{V_t + \sqrt{\frac{k_p}{4k_n}(V_{DD} - V_t)}}{1 + \sqrt{\frac{k_p}{4k_n}}}$ , where  $k_p$  and  $k_n$  are transconductance of PMOS and NMOS respectively. [5]



10 pouc

1.

Total marks: 70

Time: 10:30 am -12:30 pm

(Please note that all the parts of a single Section have to be answered combinedly in answer sheets.)

..... E 8

Marks  $3 \times 10 = 30$

$0.051 - 0.1$

15

## **Section I:**

- i. Determine the cut off frequency for the  $TE_{20}$  mode for an air-filled waveguide of broad wall and narrow wall dimensions of 2.5 cm and 1.25 cm respectively.

ii. What is the value of SWR of a transmission line terminated by the matched load?  $\eta = 0 \Rightarrow Z_L = Z_0$

iii. The input power of a H-plane Tee at H-arm is -10 dB. What is the output power at other two terminals?

iv. The normalized load admittance is  $0.228 - j0.35$ . Calculate the value of load impedance which is connected to a transmission line of characteristic impedance 75 Ohm?

v. Consider the S matrix      0.2      0.6      Is it a reciprocal and lossless microwave component? *antil*  
                                 0.6      0.1

vi. A  $120\ \Omega$  load is to be matched to a  $75\ \Omega$  transmission line. Calculate the characteristic impedance of the quarter-wave transformer line segment which can be used to match a  $75\ \Omega$  line to a  $120\ \Omega$  load?

vii. A lossless  $60\ \Omega$  line is terminated by a  $60 + j60\ \Omega$  load. Find reflection coefficient (both magnitude and phase angle) without using smith Chart.

viii. The input power in a two-hole directional coupler is 1 mW. Calculate the coupled power if the coupling factor is 15 dB.

ix. Calculate return loss if the reflection coefficient of a port is 5 dB.

x. For a rectangular waveguide of internal dimension,  $a \times b$  ( $a > b$ ), the cut off frequency for the  $TE_{11}$  mode is the arithmetic mean of the cutoff frequencies for  $TE_{10}$  mode and  $TE_{20}$  mode. If  $a = \sqrt{5}\ \text{cm}$ , find the value of ' $b$ '.

Marks: 40

## Section II:

1. A 50-ohm line is terminated to a load with an unknown impedance. The standing wave ratio  $S=2$  on the line and a voltage maximum occurs  $\lambda/8$  from load. (a) Determine the load impedance (b) How far is the first minimum voltage from the load? (6)
  2. Draw the input impedance of a lossless line: (a) when shorted (b) when open circuited. Also write the expression for input impedance for both the cases. (8)
  3. Design a single stub matching network to match a load impedance  $60 -j80 \Omega$  to a transmission line of characteristic impedance  $50 \Omega$ . Also draw a proper diagram. (10)
  4. With the help of a neat diagram, explain even and odd mode excitation. (6)
  5. Write short note: (any one)
    - a. Planar transmission line
    - b. Branch line Coupler(10)

22 x<sup>+</sup>  
28 x<sup>+</sup>  
28 x<sup>+</sup>

$$(10) \quad \frac{22}{\cancel{2}} \times \cancel{7}$$

$$Z_{in} = Z_0 \left[ \frac{Z_L + Z_0 \tan \theta}{Z_0 + Z_L \tan \theta} \right] \quad (Q \cos \theta)$$



**EC381: Embedded System  
End-Semester Examinations  
IIIT Guwahati**

**Time: 3 hours**

**Total 50 Marks**

**Section A**

**3 marks x 7 = 21 marks**

**Q1.** Briefly explain the different bits in the PSW (program status word) register of 8051.

**Q2.** Define the following terms with suitable graphs.

- a. Periodic      b. Non-Periodic      c. Sporadic

**Q3.** Briefly distinguish between top-down and bottom-up design methodology in HDL?

**Q4.** Answer the followings (more than one correct option possible):-

A. Which of the following statements is/ are true?

- I. reg is the only legal type on the left-hand side of an always@ block = or <= sign  
II. wire is the only legal type on the left-hand side of an always@ block = or <= sign  
III. wire elements are the only legal type on the left-hand side of an assign statement.  
~~IV.~~ reg elements are the only legal type on the left-hand side of an assign statement

B. Which of the following statements is/ are true?

- I. wire elements can only be used to model combinational logic  
II. wire elements can only be used to model both combinational and sequential logic  
III. reg elements can only be used to model sequential logic  
~~IV.~~ reg elements can only be used to model both combinational and sequential logic

C. Which of the following statements is/are true regarding wire and reg elements?

- I. Both appear on the right-hand side of assign statements and always@ block = or <= signs.  
II. Both can be connected to the input ports of module instantiations.  
III. reg elements can be connected to the output port of a module instantiation.  
~~IV.~~ reg elements cannot be connected to the output port of a module instantiation

*Carry f(a)  
Overflow*  
**Q5.** Consider the following assembly code

CMP r1, r2  
BNE SKIP      Not eq.  
CMP r3, r4  
BEQ SKIP      equal.  
SUBNE r5, r5, #10       $r5 = r5 + 10$ .

SKIP ...

Using ARM postfix conditional execution, how can you improve the above code density?

**Q6.** Estimate the external connection requirements for a 128 x 8 memory?

**Q7.** Consider register r1=1000 and the memory content as shown in the table below:-

| Address               | Value |
|-----------------------|-------|
| r <sub>1</sub> . 1000 | 5     |
| r <sub>2</sub> 1004   | 10    |
| r <sub>3</sub> 1008   | 15    |
| r <sub>4</sub> 100C   | 20    |

What happens after the execution of the following ARM instructions.

- a. LDMIA r1, {r3, r5, r6}      b. LDMIB r1, {r3, r5, r6}

$$\begin{aligned}r_1 &= r_3 \\r_1 &= r_5\end{aligned}$$

Inc Before

**Section C****5 marks x 2 = 10 marks**

**Q8.** Suppose an 8-bit word is 10111001, determine the even parity bits, hamming code word and illustrate how to correct when a bit error occurs for data bit 3, i.e. instead of 10111001 we have 10111101?

**Q9.** Design a 2:1 mux using the assign statement in Verilog HDL. Now use the 2:1 mux to implement an 8:1 mux.

**Section D****6 marks x 2 = 12 Marks**

**Q10.** Consider the following processes with the arrival and burst time as shown in the table below:-

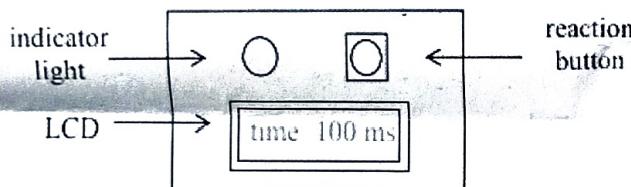
| Process | Arrival | Burst Time |
|---------|---------|------------|
| A       | 0       | 12         |
| B       | 1       | 6          |
| C       | 4       | 4          |
| D       | 5       | 10         |

Round  
Period  
 $\frac{2}{2} =$

Schedule the above showing the gant chart and calculate the average waiting time and average turnaround time using.

- a. FCFS
- b. Preemptive Shortest Job First or Shortest Remaining Time First
- c. Round Robin with a time quantum of 2

**Q11.** It is required to design a reaction timer that measures the time between turning the light on and the user pushing the button as shown in the diagram.



6.  
 $\times 10$   
Resolution  
 $\frac{1}{12} \times 6$

A microcontroller with the following specification is used to design the reaction timer.

- I. A built-in 16 bit timer - Timer get incremented once every instruction cycle
- II. 1 instruction cycle = 6 clock cycles
- III. clock frequency = 12 MHz
- a. Calculate the resolution and range of the reaction timer (2 marks)
- b. Without using a prescaler and terminal count register, design the timer so that it can keep count for every milli sec. (4 marks)

**Section E****7 marks x 1 = 7 Marks**

**Q12.** Using Least Laxity First (LLF) algorithm show the scheduling of the following processes:-

| Process | Arrival | Duration | Deadline |
|---------|---------|----------|----------|
| A       | 0       | 9        | 30       |
| B       | 3       | 4        | 31       |
| C       | 6       | 6        | 28       |

Show up to 16 units of time. If at any instance the same laxity occurs then schedule according to FCFS.

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Q1. What are the typical design constraints of an embedded system? (2 marks)

Q2. Briefly explain the different ports of the 8051 microcontroller? (2 marks)

Q3. Write an ARM based code snippet to demonstrate the copying of a block of memory (128 Bytes aligned). Briefly explain the code. (5 marks)

Assumptions:

Loading of 32 bytes of data at the same time

r9: address of the source

r10: address of the destination

r11: end address of the source

Q4. Using the least laxity first (LLF) shows the scheduling of the following three processes. (6 marks)

|    | Arrives | Execution | Deadline |
|----|---------|-----------|----------|
| T1 | 0       | 10        | 33       |
| T2 | 4       | 3         | 28       |
| T3 | 5       | 10        | 29       |

M. D. S. Wilson

Q5. Consider 2 designs of an ARM based microprocessor D1 and D2. D1 has a 5 stage pipeline with execution time of 2 ns, 1 ns, 2 ns, 3 ns and 1 ns. While the design D2 has 8 pipeline stages each with 1 ns execution time. The Latch Delay for both the designs is 1 ns. How much time can be saved using design D2 over design D1 for executing 1000 instructions? (represent the answer in ns) (5 marks)



Indian Institute of Information Technology Guwahati

BTech: Electronics and Communications Engineering

Information Theory and Coding (EC353)

Quiz 2, 8 Feb 2023

Timing: 9:10 to 9:50 AM

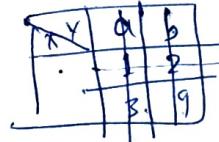
Semester-VI

Max mark: 25

Note: Select any four questions appropriately to answer. The maximum mark is 25.

1. Suppose Sandip has  $n$  coins, among which there may or may not be one counterfeit coin. If there is a counterfeit coin, it may be either heavier or lighter than the other coins. The coins are to be weighed by a balance. Find an upper bound on the number of coins  $n$  so that  $k$  weighings will find the counterfeit coin (if any) and correctly declare it to be heavier or lighter. (5)
2. Let  $X$  be a random variable taking on a finite number of values. What is the (general) inequality relationship of  $H(X)$  and  $H(Y)$  if a)  $Y = 2^X$ , b)  $Y = \cos X$ ? (6)
3. Let  $p(x, y)$  be given by

|   |   | Y             |               |
|---|---|---------------|---------------|
|   |   | 0             | 1             |
| X | 0 | $\frac{1}{3}$ | $\frac{1}{3}$ |
|   | 1 | 0             | $\frac{1}{3}$ |



Find:

- a)  $H(X), H(Y)$
- b)  $H(X|Y), H(Y|X)$
- c)  $H(X, Y)$
- d)  $H(Y) - H(Y|X)$
- e)  $I(X; Y)$

Draw a Venn diagram for the quantities in parts (a) through (e). (7)

4. Let  $X_1 \rightarrow X_2 \rightarrow X_3 \rightarrow \dots \rightarrow X_n$  form a Markov chain in this order; that is, let  $p(x_1, x_2, \dots, x_n) = p(x_1)p(x_2|x_1)\dots p(x_n|x_{n-1})$ . Reduce  $I(X_1; X_2, \dots, X_n)$  to its simplest form. (6)
5. A discrete memoryless source has an alphabet of three letters,  $x_i, i = 1, 2, 3$ , with probabilities 0.4, 0.4, and 0.2, respectively. Find the binary Huffman code for this source and determine the average number of bits needed for each source letter. (7)

- Good Luck -



भारतीय सूचना प्रौद्योगिकी संस्थान गुवाहाटी

INDIAN INSTITUTE OF INFORMATION TECHNOLOGY GUWAHATI  
Mid-Semester Examination

EC 361: VLSI Design

Time: 2 Hours, Total Marks: 50, Date: 18<sup>th</sup> February 2023

Note:

- (i) Answer ALL questions.
- (ii) Write down the assumptions clearly, if any. No queries will be entertained during the exam hours.

1. Answer the following :

- (a) Write a short note, with illustration, on Latch-up process in a CMOS inverter and its possible remedy. [5]
- (b) Describe DRC and LVS in a typical ASIC development process [5]
- (c) Identify the advantages and disadvantages of Full Scaling and Constant Field Scaling in VLSI design. [5]
- (d) Consider a p-type semiconductor substrate. Show how oxide layer is grown on the substrate layer. Explain with illustration how an n-well can be formed on the oxide-layer-p-type substrate-layer. [5]

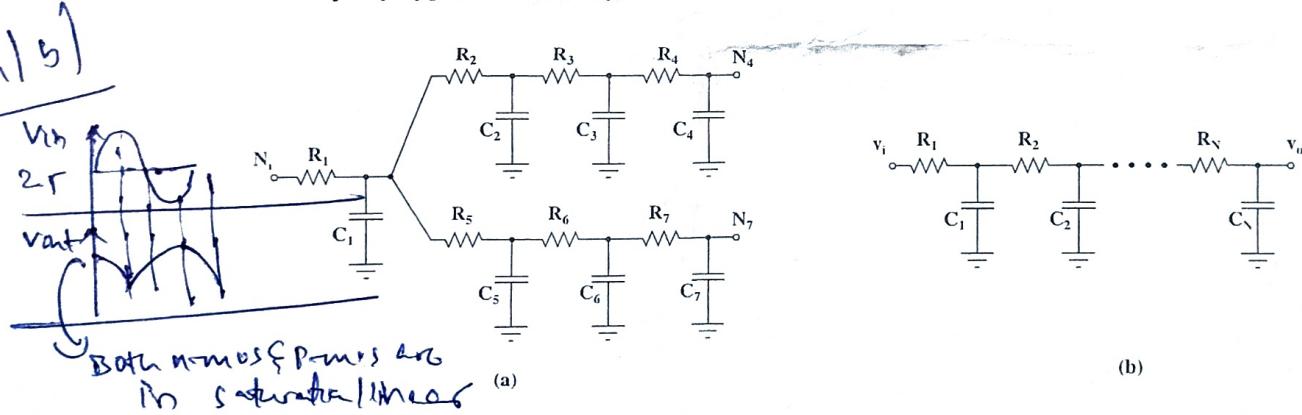


Figure 1: Circuits

2. (a) Describe using a typical RC circuit the Elmor's delay with proper mathematical expression. [2]
- (b) For the circuit of Fig. 1(a), determine the delay from node  $N_i$  to  $N_4$ . [3]
- (c) For the circuit of Fig. 1(b), consider all resistance values are  $R_i = R/N$  and all capacitance values are  $C_i = C/N$ . For this circuit, prove that for large values of  $N$ , delay from  $v_i$  to  $v_o$  is approximately  $\frac{RC}{2}$  [5]

$$V_{DSN} = (V_{in})_{nmos}$$

$$V_{DSP} = V_{DD} - V_{out}$$

Substituting in that eqn & differentiate with  $\frac{d}{dt}v_{in}$

$$V_{in} + 2.6 = V_{out}$$

$$V_{out} = V_{IL} + 2.6$$

$$\Rightarrow 4.6 \text{ V}$$

Similarly to find  $V_{OL}$

$$I_D(\text{trans})_{nmos} = I_D(\text{sat})_{nmos}$$

write formula & diff with  $\frac{d}{dt}v_{in}$   
 $\downarrow v_{out} = -1$ ,

$v_{in}$

you'll get

$$3V_{in} + 0.8 = 3V_{out}$$

$$V_{OL} = 3.06 \text{ V}$$

3. Consider an inverter circuit with an enhancement type NMOS driver and enhancement type NMOS load. Load is diode connected, i.e., drain and gate terminal of the load are shorted. Process parameter values are,  $V_T(V_{SB} = 0) = 0.8$  V,  $V_T(V_{SB} \approx 5) = 1$  V,  $\mu_n C_{ox} = 45 \mu A V^{-2}$ ,  $V_{DD} = 5$  V.
- Find the values of  $V_{OH}$ ,  $V_{OL}$  and  $NM_L$ . [2+2+3]
  - Calculate the DC power consumption of the inverter circuit. [3]
4. Consider a CMOS inverter circuit. With  $V_{DD} = 5$  V,  $\mu_n C_{ox} = 45 \mu A V^{-2}$ ,  $\mu_p C_{ox} = 15 \mu A V^{-2}$ ,  $V_{tn} = |V_{tp}| = 0.8$  V,  $W_{NMOS} = 4 \mu m$ ,  $L_{NMOS} = 1 \mu m$ ,  $V_{IH} = 2.8$  V. DC characteristics of the inverter shows perfect symmetry.
- Find  $V_{OH}$ ;  $V_{OL}$ ;  $NM_H$  and  $NM_L$ ;  $(W/L)_p$ . [1+1+2+2]
  - Draw the piece-wise linear transfer characteristics of the inverter. If a sinusoid of  $V_m = 0.3\sin(2\pi(1000)t) + 2.5$  V is given as the input to the inverter, plot both input and output signal. [1+3]

$$V_{IL} = \frac{2V_{out} + -V_{DD} + V_{TP} + KrV_{TN}}{1+Kr} \rightarrow \frac{1}{8}(3V_{DD} + 2V_{tn})$$

$$V_{IH} = \frac{2KrV_{out} + V_{DD} + V_{TP} + KrV_{TN}}{1+Kr} \rightarrow \frac{1}{8}(5V_{DD} - 2V_{tn})$$

$$2.8V = \frac{1}{8}(5 \times 5 - 2 \times V)$$

$$\frac{25 - 2 \times 0.8}{25 + 1.6} = \frac{23.2}{26.6} = \frac{23.2}{26.6}$$

$$V_{IL} = \frac{1}{8}((V_{AS} - V_{TN})(V_{DD}) - (V_{DS})^L)$$

Given  $V_{tn} = V_{tp} = 0.8$

$K_p = k_n$

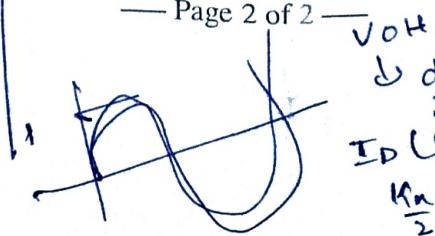
$\mu_p C_{ox} \left(\frac{W}{L}\right)_p = \mu_n C_{ox} \left(\frac{W}{L}\right)_p$

Given  $\left(\frac{W}{L}\right)_p = \frac{4}{3}$

$$V_{IL} = \frac{1}{8}(3V_{DD} + 2V_{tn})$$

$$= 2.045 \rightarrow$$

— Page 2 of 2 —



$V_{OH}$

$\frac{dV_{out}}{dV_{in}} = -1$

$I_D(\text{saturated})_{NMOS} = I_D(\text{saturated})_{PMOS}$

$$\frac{k_n}{2} (V_{ASn} - V_{TN})^2 = \frac{k_p}{2} (V_{ASp} - V_{TP})^2$$

# Indian Institute of Information Technology Guwahati

End Semester Examination  
Microwave Engineering EC 371  
27<sup>th</sup> April 2023



Time: 10 am -1 pm

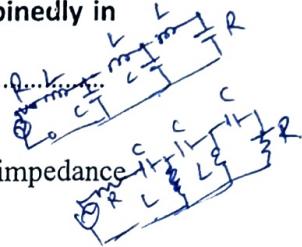
Total marks: 110

(Please note that all the parts of a single Question have to be answered combinedly in answer sheets.)

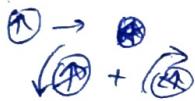
## Question 1

- Design a maximally flat low pass filter with a cut off frequency of 2 GHz, impedance of  $50 \Omega$  and at least 15 dB insertion loss at 3 GHz. Draw a neat diagram.
- Draw the diagram of a 3<sup>rd</sup> order bandpass filter.
- Explain Richards' transformation and Kuroda identities along with the suitable diagrams.

(6+4+10=20)



## Question 2:



- Construct a four port circulator by using magic tees and nonreciprocal phase shifter.
- Explain Faraday rotation. Also explain the principle of Faraday Rotation Isolator with the help of suitable diagram.
- Write the applications of circulator and isolator.

(5+10+5=20)

## Question 3:

- Explain Single Pole Double Throw (SPDT) series and shunt switches along with suitable diagrams which include biasing circuitry.
- Calculate the insertion loss in ON and OFF positions for a SPDT series switch operating at 1.8 GHz and constructed using Microsemi UM 9605 PIN diode with junction capacitance  $C_j = 0.5 \text{ pF}$  and resistance under forward bias condition  $R_f = 1.5 \Omega$ . Assume lead inductance  $L_i = 0.5 \text{ nH}$ , resistance under reverse bias condition  $R_r = 2 \Omega$  and  $Z_o = 50 \Omega$ .

(10+10 = 20)

## Question 4:

*interelectrode Capacitance, lead inductance, transit time, skin depth, power, BW*

- Explain the limitation of conventional tube.

- Draw a neat diagram and explain the working principle of,

Two Cavity Klystron Amplifier

**OR**

Travelling Wave Tube Amplifier.

- A 400 kW cylindrical magnetron operating at X-band has the following set of parameters.

Anode Voltage  $V_{dc} = 32 \text{ kV}$ , Beam current  $I_{dc} = 84 \text{ A}$ , radius of cathode and anode cylinder 6 cm and 12 cm respectively, magnetic flux density ( $B$ ) =  $0.01 \text{ Wb/m}^2$ . Calculate cyclotron angular frequency, cut off magnetic flux density and efficiency.

(7+7+6 = 20)

*Thankyou*

### Question 5:

Draw the V-I characteristic of a GaAs Gunn diode and explain the transferred electron effect with the help of energy band diagram.

OR

Explain the principle of IMPATT diode as an avalanche transit time device. (10)

### Question 6:

Draw the diagram of sectorial and pyramidal horn antennas. Explain the different types of feeding techniques for a patch antenna. (3+7 = 10)

### Question 7:

a. The Triquint TIC6000528 GaN HEMT has the following scattering parameters at 1.9 GHz ( $Z_0 = 50 \Omega$ )

$$\begin{aligned}S_{11} &= 0.869 \angle -159^\circ \\S_{12} &= 0.031 \angle -9^\circ \\S_{21} &= 4.250 \angle 61^\circ \\S_{22} &= 0.507 \angle -117^\circ\end{aligned}$$

$$\begin{aligned}|S_{11}| &< 1 \\|S_{22}| &< 1 \\1 &= \frac{Z_0 - Z_L}{Z_0 + Z_L}\end{aligned}$$

Determine the stability of this transistor by using the  $K-\Delta$  test and the  $\mu$ -test.

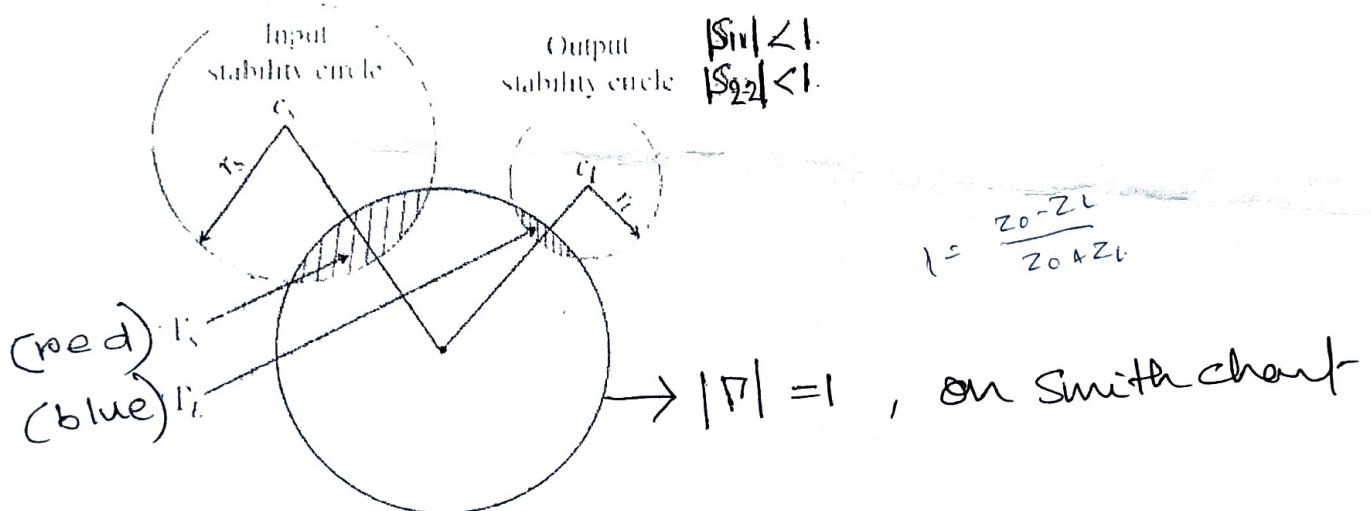


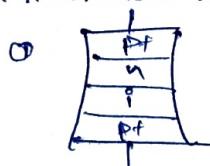
Fig.1

b. Consider Figure 1 and state the significance of the regions marked in red and blue colours.

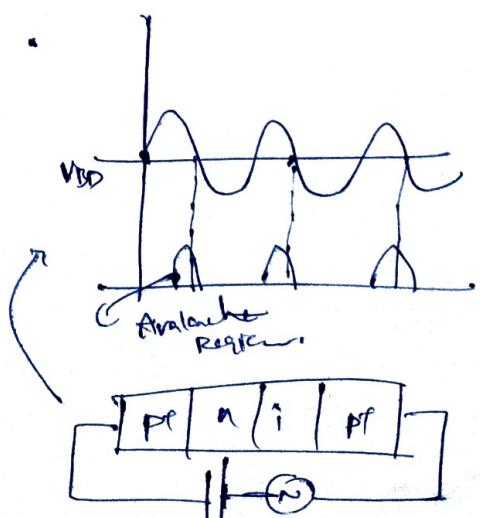
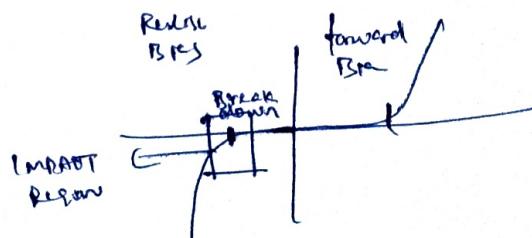
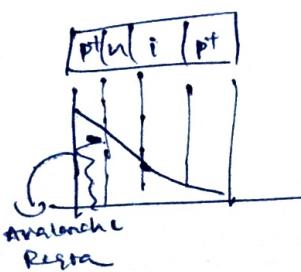
c. Calculate the value of output reflection coeff ( $\Gamma_{out}$ ) for a negative resistance of  $10 \Omega$ . (5+2+3 = 10)

Q1 IMPATT diode  $\leftrightarrow$  impact ionization avalanche transit time device

High power device  
works in (3-100) GHz  
Main disadvantage is phase noise



Electric field profile



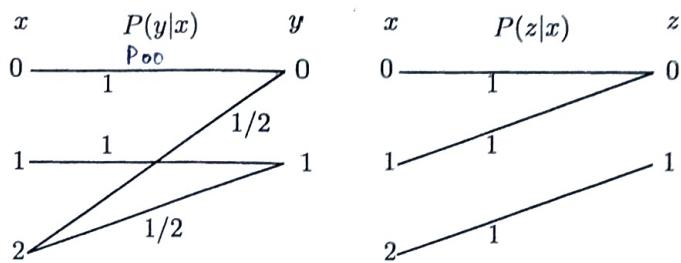


Timing: 10:00 AM to 1:00 PM

Semester-VI

Max mark: 100

- A source  $X$  produces letters from a three-symbol alphabet with the probability assignment  $P_X(0) = \frac{1}{4}$ ,  $P_X(1) = \frac{1}{4}$ , and  $P_X(2) = \frac{1}{2}$ . Each source letter  $x$  is transmitted through two channels simultaneously with outputs  $y$  and  $z$  and the transition probabilities as given below.



Calculate  $H(X)$ ,  $H(Y)$ ,  $H(Z)$ ,  $H(Y, Z)$ ,  $I(X; Y)$ ,  $I(X; Z)$ ,  $I(X; Y|Z)$ , and  $I(X; Y, Z)$ . (15)

- Consider Shannon's channel capacity theorem, for a continuous communication channel having bandwidth  $W$  Hertz, perturbed by additive white Gaussian noise of power spectral density  $N_0$ , and average transmitted power  $P$ .
  - Is there any limit to the capacity of such a channel if you increase its signal-to-noise ratio  $\frac{P}{N_0 W}$  without limit? If so, what is that limit?
  - Is there any limit to the capacity of such a channel if you can increase its bandwidth  $W$  in Hertz without limit, but while not changing  $N_0$  or  $P$ ? If so, what is that limit?
- Consider an alphabet of 8 symbols whose probabilities are as follows: (5)
 

|               |               |               |                |                |                |                 |                 |
|---------------|---------------|---------------|----------------|----------------|----------------|-----------------|-----------------|
| A             | B             | C             | D              | E              | F              | G               | H               |
| $\frac{1}{2}$ | $\frac{1}{4}$ | $\frac{1}{8}$ | $\frac{1}{16}$ | $\frac{1}{32}$ | $\frac{1}{64}$ | $\frac{1}{128}$ | $\frac{1}{128}$ |

  - What is the entropy of the above symbol set?
  - Construct a uniquely decodable prefix code for the symbol set and explain why it is uniquely decodable and why it has the prefix property.

- Consider a systematic  $(8, 4)$  LBC whose parity check equations are

$$\begin{aligned} v_4 &= u_1 + u_2 + u_3 \\ v_5 &= u_0 + u_1 + u_2 \\ v_6 &= u_0 + u_1 + u_3 \\ v_7 &= u_0 + u_2 + u_3 \end{aligned}$$

Write the generator and parity check matrices and Draw the encoder diagram. (10)

5. In an LBC, the syndrome is given by

(15)

$$S_1 = r_1 + r_2 + r_3 + r_5$$

$$S_2 = r_1 + r_2 + r_4 + r_6$$

$$S_3 = r_1 + r_3 + r_4 + r_7$$

(a) Find the parity check matrix. (2)

(b) Draw the encoder circuit. (4)

(c) Find the code word for all input sequences. (4)

(d) How many errors it can detect and correct? (2)

(e) What is the syndrome for the received data 1011011? (3)

6. Using standard array, decode the received vector 110111 for a (6,3) LBC with the parity

matrix  $\begin{bmatrix} 1 & 0 & 1 \\ 0 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix}$ . (10)

7. Design a single-error correcting Hamming code for a message length of 3. Determine if the code is perfect or not. (10)

8. Consider the  $(2, 1, 2)$  convolution encoder with  $g^{(1)} = (111)$  and  $g^{(2)} = (101)$ .

(a) Find the constraint length. (1)

(b) Find the rate.  $R = \frac{k}{n(l+m)}$ . (1)

(c) Draw the encoder block diagram. (3)

(d) Find the generator matrix. (2)

(e) Find the codeword for the message sequence (11101) using time-domain and transfer-domain approach. (8)

9. Decode a  $(2, 1, 2)$  convolution code using Viterbi algorithm. Consider the received sequence as (01, 10, 11, 00, 00). (15)

$$L = g^T \begin{bmatrix} m-m-1 \\ 3-3-1 \end{bmatrix}$$

$$\begin{aligned} g_1 &= u \oplus s_1 \oplus s_2 \\ g_2 &= u \oplus s_2 \end{aligned}$$

$v_1(v) \cdot x(v_2(v))$

$\leq n(t)$

$\boxed{1}$