Mohd. Tasleem Khan, Ph.D.

CONTACT INFORMATION

Room EM2.10, Department of EECE,
School of Engineering and Physical Sciences,
Heriot-Watt University,
Edinburgh, UK.

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CAREER OBJECTIVE

To strive for attaining academic and research excellence through continuous learning

EDUCATION

Linköping University, Sweden

Postdoctoral Research Fellow Jul. 2021 to Feb. 2024

- **Topic**: *"High Speed Algorithms and Architectures for Beyond 5G Communication Systems"*
  Supervisor: Prof. Oscar Gustafsson

Indian Institute of Technology Guwahati, India

Doctor of Philosophy (VLSI) Jan. 2014 to Jul. 2019

- **Thesis Topic**: *"Low Complexity Distributed Arithmetic based Pipelined VLSI Architectures for LMS Adaptive Filters"*
- **CPI**: 9.450
  Supervisor: Prof. Shaik Rafi Ahamed

Heriot-Watt University, UK

Postgraduate Degree (in Academic Practice for Higher Edu.) Sep. 2024 - 2026

Aligarh Muslim University, India

Bachelor of Technology (Electronics) Jul. 2013

- **Project**: *"Design and Development of a Wireless Controlled Light Dimmer using* PIC12F675 *microcontroller"*
- **CPI**: 9.355 (hons.)
  Supervisor: Prof. Ekram Khan

SSSC (Physics, Chemistry and Mathematics), Senior Secondary School Jul. 2009

- **Percentage**: 76.25 %

SSC (General Subjects), S.T.S High School Jul. 2007

- **Percentage**: 80.40 %

SKILLS SET

- **Simulation Tools**: Verilog, System Verilog, VHDL, C, MATLAB, Python.
- **Synthesis Tools**: Cadence RTL Compiler, Cadence Virtuoso, Cadence SOC Encounter, Synopsis Design Compiler, Synopsis Design Vision.
- **Hardware Kits**: Xilinx FPGAs (Xilinx ZYNQ, Virtex, SOCs) and CPLDs.

RESEARCH INTERESTS

VLSI for Signal Processing/Communication Systems/Machine Learning, Digital IC Design, Embedded System Design, Computer Architectures.

Teaching Experience

Heriot-Watt University, UK

- *Assistant Professor* (Teaching and Research) Feb. 2024– Present
  Courses Taken:
  - Advanced Digital Electronics (B31DE) (Sem 2, AY24/25)
  - Embedded Systems (B31DD) (Sem 1, AY25/26)

Linköping University, Sweden

- *Teaching Assistant:* Switching Theory and Digital Tech. Jun. 2021– Feb. 2024

Indian Institute of Technology Dhanbad, India

- *Assistant Professor* (Teaching and Research) Feb. 2020–Sep. 2021
  Courses Taken: Digital Circuit and Microprocessor, Embedded System Design and Digital Integrated Circuits.

Indian Institute of Technology Guwahati, India

- *Teaching Assistant:* Digital Circuit and Microprocessor, Introduction to VLSI, VLSI Digital Signal Processing and Embedded System Lab Feb. 2015–Jul. 2019

Industry/ Consultant Experience

King Abdullah University of Science and Technology (KAUST), KSA

- Research Consultant (Machine Learning) May. 2020–Feb. 2021

TSMC, Hsinchu, Taiwan

- Principal Engineer (Standard Cell Layout) Jul. 2019–Dec. 2019

ZiaSemi, Bangalore, India

- Graduate Engineer (Memory Layout) Jul. 2013–Dec. 2013

Projects

- **Design and implementation of adaptive noise canceller** *sponsored by FRS (Budget 4000000 INR)*, IIT Dhanbad. Awarded, June. 2021
- **Novel VLSI architectures for accelerating LSTM Engines** *sponsored by DST-SRG (Budget 9000000 INR)*, Govt. of India. Awarded, Feb. 2021
- **Design, architecture and simulation of a radix-4 for LSTM RNNs.** *sponsored by KAUST, KSA.* Completed, March 2021

Journal Publications

1. B. Chen, **M.T. Khan**, et al., "COMET: Co-Optimization of a CNN Model using Efficient-Hardware OBC Techniques" in IEEE Transactions on Circuits and Systems I (Submitted)
2. **M.T. Khan**, Yuan Ding and George Goussetis, "Next-Gen Digital Predistortion from Hardware Acceleration of NNs: Trends, Challenges and Future" in IEEE Transactions on Neural Networks and Learning Systems (in Minor Revision, Manuscript ID: TNNLS-2025-S-38891)
3. **M.T. Khan**, "COBALT: Column-swapping Optimized Bit-serial Accelerator for LSTM Tasks" in IEEE Journal of Solid-State Circuits (Submitted, Manuscript ID: JSSC-25-0567)
4. Nadeem et al., **M.T. Khan**, "DEDUCE-Net: Achieving Extreme Parameter Efficiency for Semantic Segmentation in Autonomous Driving" in IEEE Transactions on Neural Networks and Learning Systems (Submitted, IEEE Transactions on Automation Science and Engineering)
5. **M.T. Khan** and M. Alhartomi " Digit-Serial DA-based Fixed-Point RNNs: A Unified Approach for Enhancing Architectural Efficiency", *IEEE Transactions on Neural Networks and Learning Systems* [DOI: 10.1109/TNNLS.2024.3425569]
6. **M.T. Khan** and J. Hazarika " An Area and Energy Efficient Serial-Multiplier", *IEEE Embedded Systems Letters* Jan. 2024, [10.1109/LES.2024.3352540]

7. **M.T. Khan** and O. Gustafsson " Stochastic Analysis of LMS Algorithm with Delayed Block Coefficient Adaptation", *IEEE Transactions on Signal Processing* [Submitted, arXiv:2306.00147]

8. M. Alhartomi, **M.T. Khan**, et al." Low-Area and Low-Power VLSI Architectures for Long Short-Term Memory Networks", *IEEE Journal on Emerging and Selected Topics in Circuits and Systems* Dec. 2023, [10.1109/JETCAS.2023.3330428]

9. J. Hazarika, **M.T. Khan**, S. R. Ahamed and H. B. Nemade " An Efficient Implementation Approach to FFT Processor for Spectral Analysis", *IEEE Transactions on Instrumentation and Measurement* Aug. 2023, [10.1109/TIM.2023.3301891]

10. **M.T. Khan**, H.E. Yantir, K.N. Salama and A.M. Eltawil " Architectural Trade-off Analysis for Accelerating LSTM Network using Radix-r OBC Scheme", *IEEE Transactions on Circuits and Systems I* Jan. 2023, [10.1109/TCSI.2022.3217091]

11. **M.T. Khan**, M. Alhartomi, S. Alzahrani, R.A. Shaik and R. Alsulami " Two Distributed Arithmetic Based High Throughput Architectures of Non-Pipelined LMS Adaptive Filters", *IEEE Access* Jul. 2022, [DOI: 10.1109/ACCESS.2022. 3192619]

12. **M.T. Khan** and R.A. Shaik, " High-Performance VLSI Architecture of DLMS Adaptive Filter for Fast-Convergence and Low-MSE", *IEEE Transactions on Circuits and Systems II* Jan. 2022, [DOI: 10.1109/TCSII.2022.3141687]

13. **M.T. Khan**, R.A. Shaik and M. Alhartomi, " An Efficient Scheme for Acoustic Echo Canceller Implementation using Offset Binary Coding", *IEEE Transactions on Measurements and Instrumentation* Dec. 2021, [DOI:10.1109/TIM.2021.3132087]

14. **M.T. Khan**, J. Kumar, R.A. Shaik and J. Faridi, " Partial-LUT Designs for Low-Complexity Realization of DA-Based BLMS Adaptive Filter", *IEEE Transactions on Circuits and Systems II* Nov. 2020, [10.1109/TCSII.2020.3035693]

15. **M.T. Khan** and R.A. Shaik, " High-Throughput and Improved-Convergent Design of Pipelined Adaptive DFE for 5G Communication", *IEEE Transactions on Circuits and Systems II* Aug. 2020, [10.1109/TCSII.2020.3018637]

16. **M.T. Khan** and R.A. Shaik "High-Performance Hardware Design of Block LMS Adaptive Noise Canceller for In-ear Headphones", Apr. 2020, *IEEE Consumer Electronics Magazine.* [DOI: 10.1109/MCE.2020.2976418]

17. K.P. Yalamarthy, S. Dhall, **M.T. Khan** and R.A. Shaik, " Low-Complexity Distributed Arithmetic based Pipelined Architecture for a LSTM Network", *IEEE Transactions on VLSI System* Sep. 2019, [DOI:10.1109/TVLSI.2019.2941921]

18. R. K. Sharma, **M.T. Khan**, R.A. Shaik and J.Hazarika, " Novel Time-shared and LUT-less Pipelined Architecture for LMS Adaptive Filter", *IEEE Transactions on VLSI System* Sep. 2019, [DOI: 10.1109/TVLSI.2019.2935399]

19. J. Hazarika, **M. T. Khan**, R.A. Shaik and H.B. Nemade, "Energy Efficient VLSI Architecture of Real-Valued Serial Pipelined FFT", *IET Computers and Digital Techniques*, Jun. 2019 [DOI: 10.1049/iet-cdt.2019.0025]

20. **M.T. Khan** and R.A. Shaik, "Optimal Complexity Architectures for Pipelined Distributed Arithmetic based LMS Adaptive Filter", *IEEE Transactions on Circuits and Systems I*, vol. 66, no. 2, pp. 630-642, Feb. 2019. [DOI: 10.1109/ TCSI.2018.2867291]

21. **M.T. Khan**, R.A. Shaik and Surya Prakash Matcha, "Improved Convergent Distributed Arithmetic based Low complexity Pipelined Least-Mean-Square Filter", *IET Circuits, Devices & Systems*, Apr. 2018 [DOI: 10.1049/iet-cds.2018.0041].

22. **M.T. Khan** and R.A. Shaik, "An Energy Efficient VLSI Architecture of Decision Feedback Equalizer for 5G communication system", *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 7, no. 4, pp. 569-581, Dec. 2017. [DOI: 10.1109/JETCAS.2017.2741499]

Conference Publications

1. **M. T. Khan**, O. Gustafsson, "Analyzing Step-Size Approximation for Fixed-Point Implementation of LMS and BLMS Algorithms", IEEE NORCAS, October 2023, Aalborg, **Denmark**.

2. **M. T. Khan**, O. Gustafsson, "ASIC Implementation Trade-Offs for High-Speed LMS and Block LMS Adaptive Filters", IEEE MWSCAS, August 2022, Fukuoka, **Japan**.

3. J. Hazarika, **M. T. Khan**, R.A. Shaik and H.B. Nemade, "An Area and Power Efficient Serial Commutator FFT with Recursive LUT Multiplier", IEEE MoSICom 2020 **Dubai**, UAE.

4. **M. T. Khan** and R.A. Shaik, " Optimal Complexity Architectures for Pipelined Distributed Arithmetic based LMS Adaptive Filter", *IEEE International Symposium on Circuits and Systems (ISCAS), May 2019*, Sapporo, **Japan**.

5. **M. T. Khan** and R.A. Shaik, " Low Complexity Distributed Arithmetic based Pipelined VLSI Architectures for LMS Adaptive Filters", *25th IEEE National Conference on Communication, Feb. 2019* [Thesis presentation]

6. J. Hazarika, **M. T. Khan**, R.A. Shaik and H.B. Nemade, "High Performance Multiplierless Serial Pipelined VLSI Architecture for Real-Valued FFT", *25th IEEE National Conference on Communication, Feb. 2019* [**Nominated for Best Paper**]

7. J. Hazarika, **M. T. Khan** and R.A. Shaik, "Low-Complexity Continuous-Flow Memory-Based FFT Architectures for Real-Valued Signals", *32nd IEEE International Conference on VLSI Design, Jan. 2019* [**Best Student Paper Award**].

8. **M. T. Khan** and R.A. Shaik, "Analysis and Implementation of Block Least Mean Square Adaptive Filter using Offset Binary Coding", *IEEE International Symposium on Circuits and Systems (ISCAS), May 2018*, Florence, **Italy**.

9. **M. T. Khan** and R.A. Shaik, "Enhanced Convergence Distributed Arithmetic Based LMS Adaptive Filter Using Convex Combination", *IEEE National Conference on Communication (NCC), Feb. 2018* Hyderabad, India.

10. **M. T. Khan** and R.A. Shaik, "Area and Power Efficient VLSI Architecture of Distributed Arithmetic Based LMS Adaptive Filter", *IEEE International Conference on VLSI Design-2018,* Pune, India.

11. **M. T. Khan** and R.A. Shaik, "VLSI Realization of Low Complexity Pipelined LMS Filter Using Distributed Arithmetic", *IEEE International Conference TENCON-2017*, Penang, **Malaysia**.

12. **M. T. Khan** and R.A. Shaik, "A New High Performance VLSI Architecture for LMS Adaptive Filter using Distributed Arithmetic", *IEEE International Symposium on VLSI (ISVLSI) 2017*, Bochum, **Germany**.

13. **M. T. Khan** and R.A. Shaik, "VLSI Implementation of Throughput Efficient Distributed Arithmetic Based LMS Adaptive Filter", *IEEE International Symposium on VLSI design and Test (VDAT)-2017*, Roorkee, India.

14. **M. T. Khan** and R.A. Shaik, Forrest Brewer "Low Complexity and Critical Path Based VLSI Architecture for LMS Adaptive Filter Using Distributed Arithmetic", *IEEE International Conference on VLSI Design-2017*, Hyderabad, India.

15. **M. T. Khan** and R.A. Shaik, A. Chatterjee. "Efficient Implementation of Concurrent Lookahead Decision Feedback Equalizer using Offset Binary Coding", *IEEE International Symposium on VLSI Design and Test VDAT-2016*, Guwahati, India".

16. **M. T. Khan** and R.A. Shaik, "Low Cost Implementation of Concurrent Decision Feedback Equalizer using Distributed Arithmetic", *IEEE India International Conference on Information Processing (IICIP)-2016*, Delhi, India.

17. P. K. Sharma, **M. T. Khan** and R.A. Shaik, "An Alternative Approach To Design Reconfigurable Mixed Signal VLSI DA Based FIR Filter", *IEEE Students' Technology Symposium (TechSym)-2016*, Kharagpur, India.

Positions/ Recognitions

- **Associate Editor**
  - *IEEE Signal Processing Letters* May 2025 - Present
  - *IEEE Transactions on Neural Networks and Learning Systems* Jan. 2025 - Present
  - *IEEE Transactions on Automation Science and Engineering* Nov. 2024 - Present
- **Reviewer**
  - *IEEE Transactions on Automation Science and Engineering*
  - *IEEE Transactions on Neural Networks and Learning Systems*
  - *IEEE Embedded System Letters*
  - *IEEE Transactions on Circuits and Systems I.*
  - *IEEE Transactions on Circuits and Systems II.*
  - *IEEE Transactions on Very Large Scale of Integration (VLSI) Systems.*
  - *IEEE Access.*
  - *Springer* Circuits, Systems and Signal Processing (*CSSP*).
  - *SpringerNature - Analog Integrated Circuit and Signal Processing.*
  - *SpringerNature - Signal, Image and Video Processing.*
  - *Elsevier* Journal of Parallel and Distributed Computing.
  - IEEE *International Symposium on Circuits and Systems* (*ISCAS*).
  - IEEE *International Symposium on VLSI* (ISVLSI)
  - IEEE *International Conference on Distributed Computing Systems* (ICDCS)
  - IEEE *International Joint Conference on Neural Networks* (IJCNN)
  - IEEE *Conference on Secure and Trustworthy and Cyberinfrastructure* (IEEE SaTC)
- **Organizing Committee and Area Chairs**
  - Area Chair at *IEEE ICASSP 2026*, Barcelona, Spain.
  - Area Chair at *IEEE ICJNN 2025*, Rome, Italy.

- TPC Member at *IEEE ICASSP 2026*, Barcelona, Spain.
- TPC Member at *IEEE ICDCS 2025*, Glasgow, U.K.
- TPC Member at *IEEE ISVLSI 2025*, Kalamata, Greece.
- TPC Member at *IEEE ICJNN 2025*, Rome, Italy.
- TPC Member at *IEEE SaTC 2025*, Ohio, USA.

- **Secretary**, Departmental Postgraduate Programme Committee, (*DPPC*), Electronics and Electrical Engineering Department, IIT Guwahati Mar. 2016 – Aug. 2017
- **Member**, Departmental Postgraduate Committee, (*DPGC*), Electronics Engineering Department, IIT Dhanbad Oct. 2020 – Jul. 2021
- **Volunteered** at IIT Guwahati for Instructor Enhancement Programme *IEP-2017*, National Conference on Communication, *NCC-2016*, and Technical Educational Quality Improvement Programme, *TEQIP-2016* .

PRESENTATIONS/ SEMINARS/ WORKSHOPS

Paper Presentations

- *IEEE NORCAS-2023*, Aalborg, Denmark.
- *IEEE MWSCAS-2022*, Fukuoka, Japan.
- *IEEE* VLSI Design and Embedded Systems, IEEE *VLSID-2019*, New Delhi, India.
- *IEEE* International Symposium on Circuits and Systems, *ISCAS-2018*, Florence, Italy. May 2018
- *IEEE* National Conference on Communication, *IEEE NCC-2018*, Hyderabad, India. Feb. 2018
- *IEEE* VLSI Design and Embedded Systems, IEEE *IEEE VLSID-2018*, Pune, India. Jan. 2018
- *IEEE TENCON-2017*, Penang, Malaysia. Nov. 2017
- *IEEE* International Symposium on VLSI *IEEE ISVLSI-2017*, Bochum, Germany. Jul. 2017
- *IEEE* VLSI Design and Test *VDAT-2017*, IIT Roorkee, Roorkee, India. Jun. 2017
- *IEEE* VLSI Design and Embedded Systems *VLSID-2017*, Hyderabad, India. Jan. 2017
- *IEEE* Students' Technology Symposium *TechSym-2016*, IIT Kharagpur, Kharagpur, India. Sept. 2016
- *IEEE* International India Conference on Information Processing *IICIP-2016*, Delhi Technological University, Delhi. Aug. 2016
- *IEEE* VLSI Design and Test, *IEEE VDAT-2016*, IIT Guwahati, Guwahati, India. May 2016

Workshops/Seminar

- Technical Advisor in Organizing Committee for Semiconductor Glasgow Focus at University of Glasgow, UK. May 2024
- Participated in ARM Education SICSA event as a representative for Heriot-Watt University at University of Glasgow, UK. May 2024
- *Active participant* in Test and Verification of large System-on-Chip using System Verilog at Linkoping Universitet, Sweden. Nov. 2022
- *Active participant* in ELLIIT Workshop at Linkoping Universitet, Sweden. Oct. 2022
- *Active participant* in ELLIIT Workshop at Lund Universitet, Sweden. Oct. 2021
- *Speaker* in Emerging Trends in Speech and Biomedical Signal Processing at Short Term Training Program, NIT Surat, India. Sep. 2020.
- *Active participant* in three day workshop on **Mobile Robotics** conducted by Think-Labs Solution, the Department of Electronics Engineering, AMU Aligarh, India. Feb. 2013

- *Participant* in workshop on **Recent Trends in Embedded System Design** conducted by the Department of Electronics Engineering, AMU Aligarh, India Mar. 2013.
- *Participated* in Workshop for **STM32 microcontroller** organized by **ST Microelectronics** at the Department of Electronics Engineering, AMU Aligarh, India Feb. 2012
- *Presenter* in **IO2S Energy Conclave** Seminar at Maulana Azad Library, AMU, Aligarh. Apr. 2012
- *Participated* in **Three Minute Thesis (3MT) Competition** organised by RSF-EEE, IIT Guwahati. Aug. 2017

Scholarships /Awards

- *Fellowship Award from SERB-DST* of **108476** INR. Apr. 2019
- *Student Travel Grant Award from IEEE CASS* of **1000** USD. Apr. 2019
- *Best Paper Awarded* of **35000** INR in VLSID-2019. Jan. 2019
- *Awarded* with Fellowship of **6000** INR in VLSID-2019. Dec. 2018
- *Fellowship Award* of **10000** INR in VLSID-2018. Jan. 2017
- *Student Travel Grant Award from IEEE CASS* of **550** USD Apr. 2018
- *Man of the Series Award* in Departmental Cricket League organised by RSF-EEE, IIT Guwahati. Feb. 2018
- *Scored* **99.45(approx.)** percentile in GATE 2013. Mar. 2013
- *Adjudged* **Star Performer** in the MATLAB workshop organized by Electronics Department, AMU Aligarh. May 2013
- *Awarded* with **2nd prize** in T-Shirt Painting, INNOVATIA the Open University Festival, AMU Aligarh. Apr. 2013
- *Awarded* **1st prize** of worth **5000 INR** in the seminar presentation of IO2S Energy Conclave. May 2012
- *Qualified* **Indian Institute of Technology (IIT)** Joint Entrance Examination. May 2009

Personal Information

Name: Mohd. Tasleem Khan
Father's Name: Mohd. Waseem Khan
Date of Birth: 17th, June 1991
Gender: Male
Marital Status: Married
Nationality: Indian
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Declaration

I hereby declare that all the details furnished by me are correct to the best of my knowledge and belief.

(**Mohd. Tasleem Khan**)

Referees

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