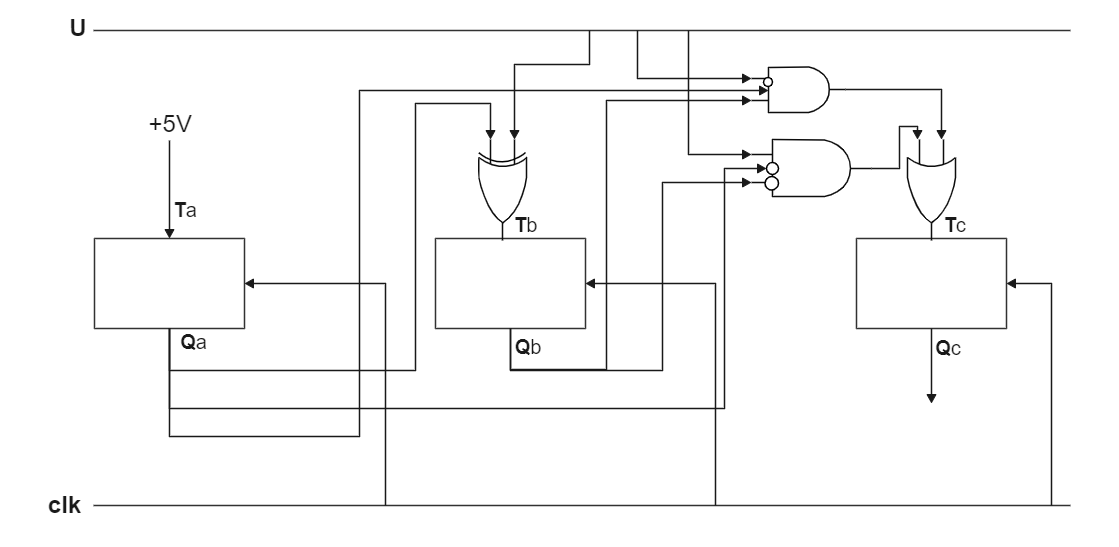
https://www.pes.edu/wp-content/uploads/2019/09/pes_logo.png

**END SEMESTER ASSESSMENT (ESA) B.TECH. (CSE)**

**III SEMESTER**

**UE18CS206 – DIGITAL DESIGN & COMPUTER ORGANIZATION LABORATORY**

**CIRCUIT DIAGRAM:**

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**MAIN VERILOG CODE:**

*module* tfr(input wire clk, reset, t, output wire out);

reg memory\_bit;

wire t\_in, m\_in;

assign t\_in =  t? ~memory\_bit:memory\_bit;

assign m\_in = reset?0:t\_in;

always @(posedge clk)

    begin

        memory\_bit <= m\_in;

    end

    assign out = memory\_bit;

*endmodule*

*module* updown(input wire clk, reset, u,input wire [2:0] q, output wire [2:0] out);

wire [2:0] t;

assign t[0] = 1;

assign t[1] = u^q[0];

assign t[2] = !u & q[1] & q[0] | u & !q[1] & !q[0];

tfr tfr\_0(clk, reset, t[0], out[0]);

tfr tfr\_1(clk, reset, t[1], out[1]);

tfr tfr\_2(clk, reset, t[2], out[2]);

*endmodule*

**TEST BENCH FILE:**

`timescale 1 ns / 100 ps

*module* updown\_tb;

reg clk, reset, u;

reg [2:0] q;

wire [2:0] temp;

output [2:0] out;

initial begin $dumpfile("updown.vcd");

$dumpvars(0,updown\_tb);

#150 $finish;

end

initial begin reset = 1'b1;

#10 reset = 1'b0;

end

initial clk = 1'b0;

always #5 clk = ~clk;

initial u = 1'b0;

always #75 u = ~u;

initial q = 3'b000;

updown updown\_0(clk, reset, u, q, out);

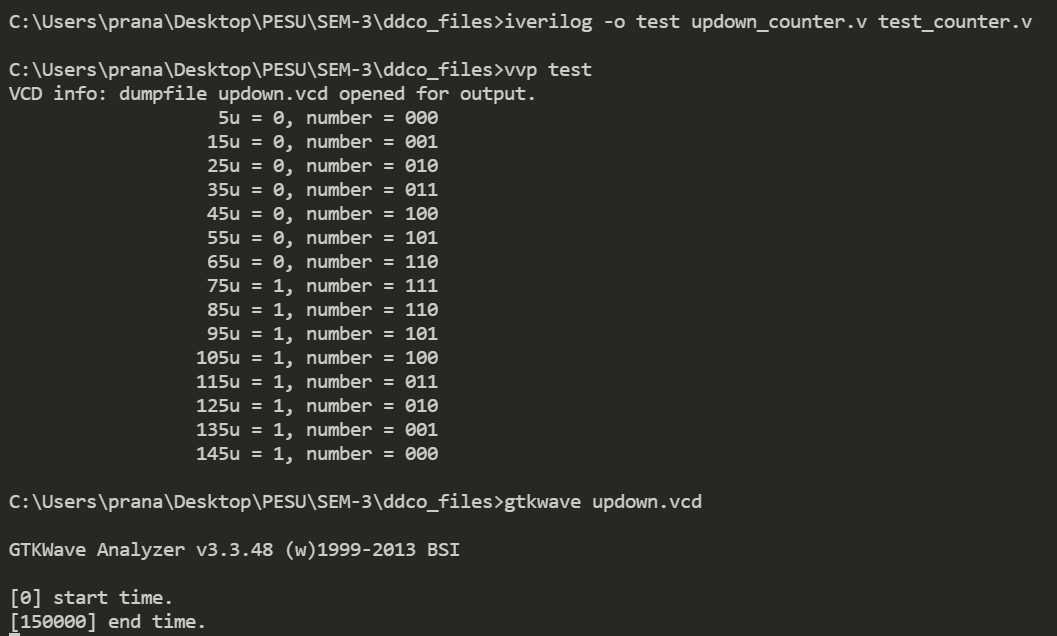
always@(out) begin $display($time, "u = %b, number = %b%b%b", u, out[2], out[1], out[0]);

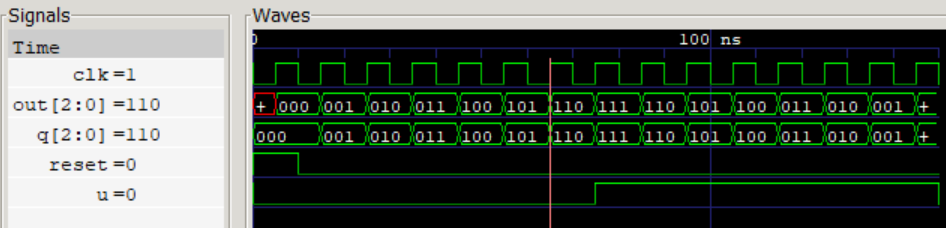
assign q = out;

end

*endmodule*

**SCREEN SHOT OF THE OUTPUT:**

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