

IE

course No: 1207

course title: VLSI Design

Design of VLSI System

- A practical Introduction, by Linda E.M. Spackenbury.

VLSI → very large scale integration.

1.1

Ic? set of circuit যখন তৈরি করেন common platform আবে
logic gate

1960 SSI (small scale integration)

1970 MSI (medium scale integration) (1K circuit)

1980 LSI (Large scale integration) (1 lac "

1990 VLSI (very large scale ") (10 million)

3rd approach of design: (1.3)

→ off the shelf design (circuit design রয়েছে হবে না)

- Full custom design (circuit নিজে design করে implement)

→ semicustom design (যাকি টুইচিং combination)

Nanotechnology:

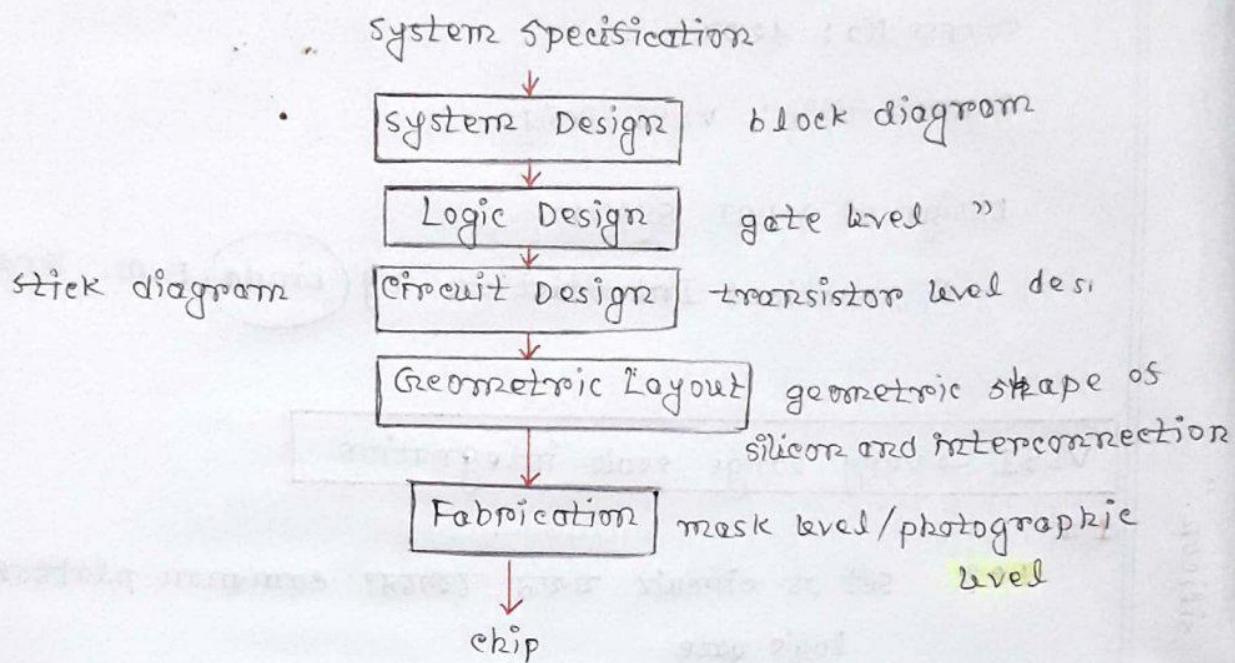
stick diagram is a pictorial representation of circuit in terms of the lines and connections required at each layer of the silicon.

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(IC: 555 timer,
operational
amplifier)

Fig: Full custom Design.

System Design: This takes the system specification and translate it into a block diagram of the architecture. This diagram shows the system's functional blocks, such as cache, registers, arithmetic, logic

Logic Diagram: Here each item drawn represents a particular logic function such as gate, control and timing logic is also included.

Circuit Design: Here the logic is translated into circuits with dimensions assigned to the transistors. Often drawn as stick diagram rather than conventional transistor symbol.

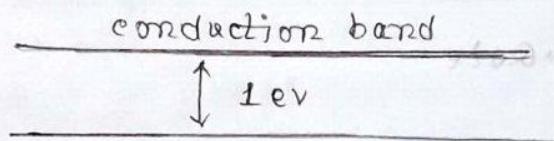
Geometric layout: Geometric shapes are generated for each silicon layer corresponding to their circuits and their interconnection.

MOSFET: Metal oxide semiconductor Field Effect Transistor.

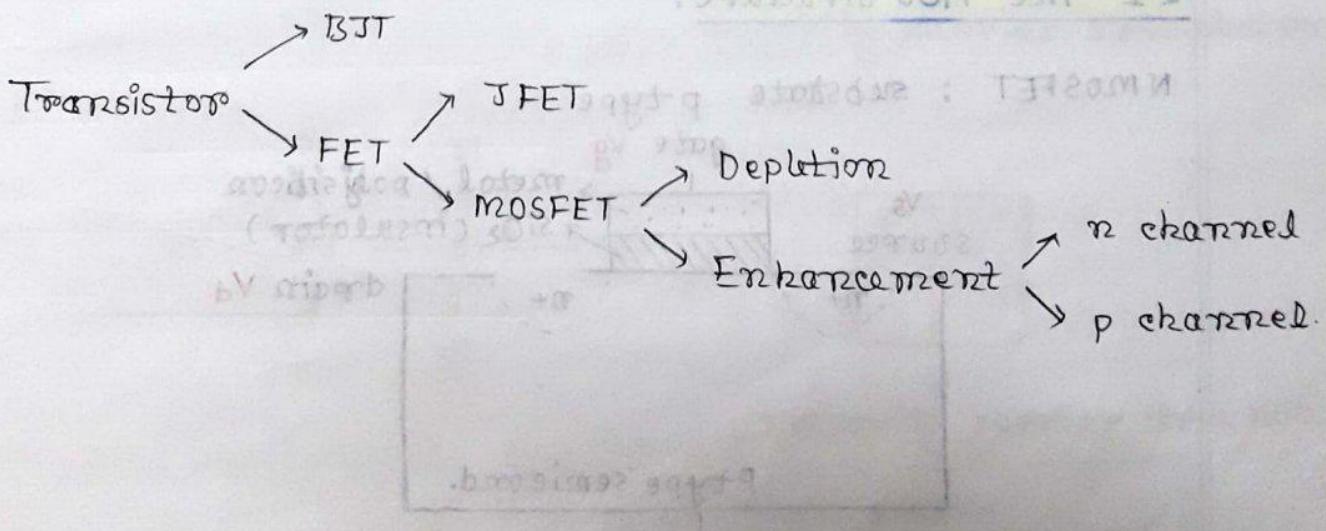
Transistor: is a semiconductor device used to

- switch
- amplifier

কেন silicon use করে?



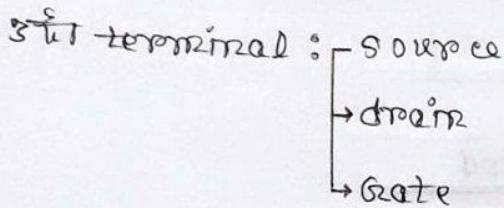
- room temperature (25°C) এ valence band থেকে conduction band এ electron যেতে পারে,
- silicon টা এ available. • কিন্তু costly.



FET → Field Effect Transistor

Electricity field use করে ট্রান্সিস্টর এ electron

এর সূত্র দিয়ে কোন হয়।

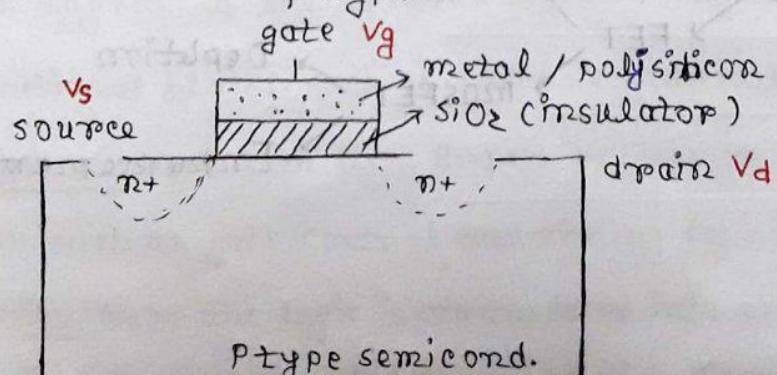


MOSFET : Depletion (আগে গোকে চানেল তৈরি করা)
 Enhancement (চানেল তৈরি করে পিছে নিয়ে হয় এবং তার মাধ্যমে চানেল তৈরি করা)

Enhancement → P-channel → PMOSFET
 → n-channel → NMOSFET

2.1 The MOS structure :

NMOSFET : substrate p-type



Body / Bulk / substrate voltage V_b

enhancement & gate & input দিয়ে চানেল তৈরি করা হয়,

capacitor

metal (conducting material)

oxide (insulator)

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semiconductor (conducting material)

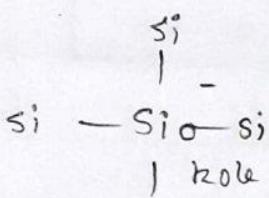
capacitor

Metal (gate)

Insulator (oxide) : SiO_2

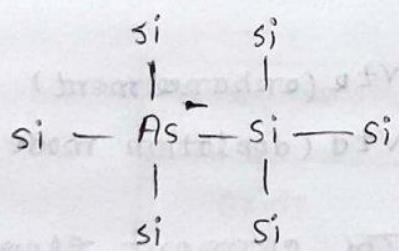
Metal (semiconductor material)

→ pure silicon doped with relatively small amounts of impurity.



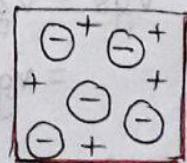
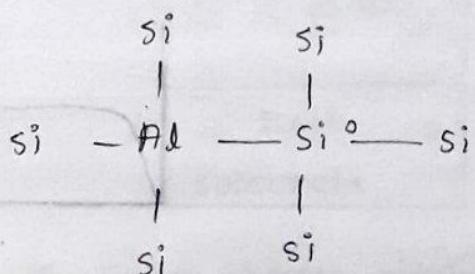
Doping & trivalent or pentavalent use As

- free electron
- + free hole
- ⊖ impurity atom
- ⊕ impurity atom



n-type

majority carrier free electron

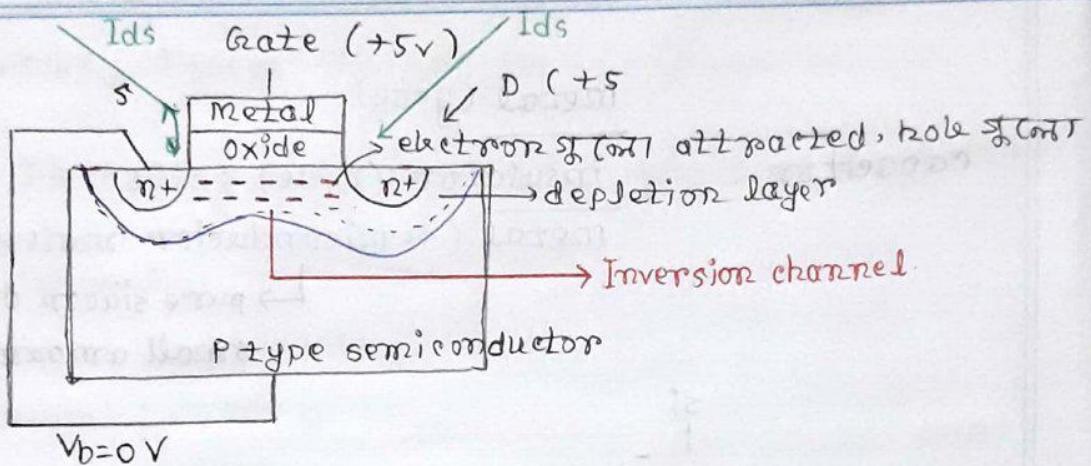


majority carrier free hole

p-type

(+ spotless blackboard being a common request)

2.2 Conduction:



Gate এর voltage কেন্দ্র তৈরি করে, তার বর্ষণ \rightarrow কানেক্ট চানেল।

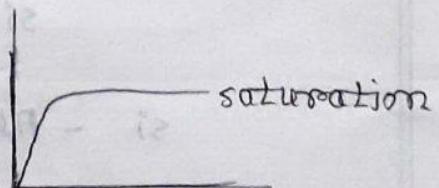
Drain এর voltage এর কারণে এলাই ফ্লো

2.3 Threshold voltage : V_t / V_{tE} (enhancement)

/ V_{td} (depletion mode)

এবং চার্টে যেনি voltage ফর্মে current ফ্লো হবে এবং আবে যেনি হবে, একটা স্থিতি saturated state এ চলে যাবে।

$$\begin{aligned} V_{gs} &= V_g - V_s \\ &= V_g - 0 = V_g \end{aligned}$$

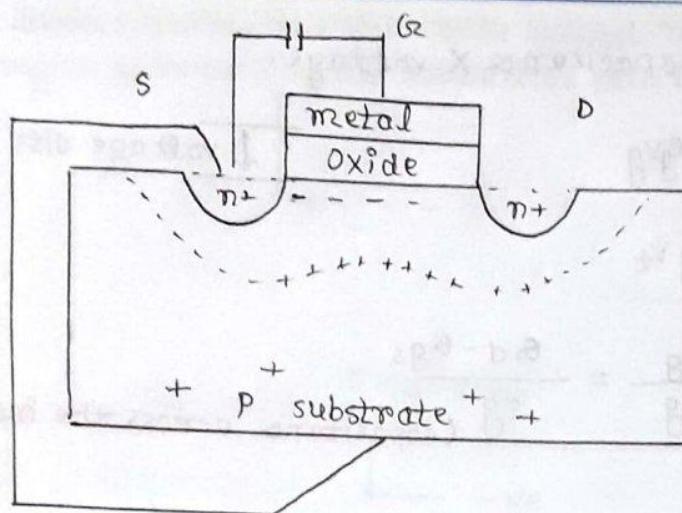


Threshold v : নির্দিষ্ট স্থিতির voltage ফর্মে just channel

to create হয়। (The input potential V_{gs} at which the surface just becomes inverted is called threshold voltage V_t)

Threshold Voltage: The input potential V_{GS} at which the surface just becomes inverted is called the threshold voltage V_T .

Below the threshold voltage an NMOS transistor is off and no current flows.



depletion layer ହୁଏ
margin ଦ୍ୱାରା ହବାଇ
voltage diss create ହୁଏ

କୌଣ ଦେଇ parameter ଏବୁ ତେଣୁ threshold depend କରିବ ।

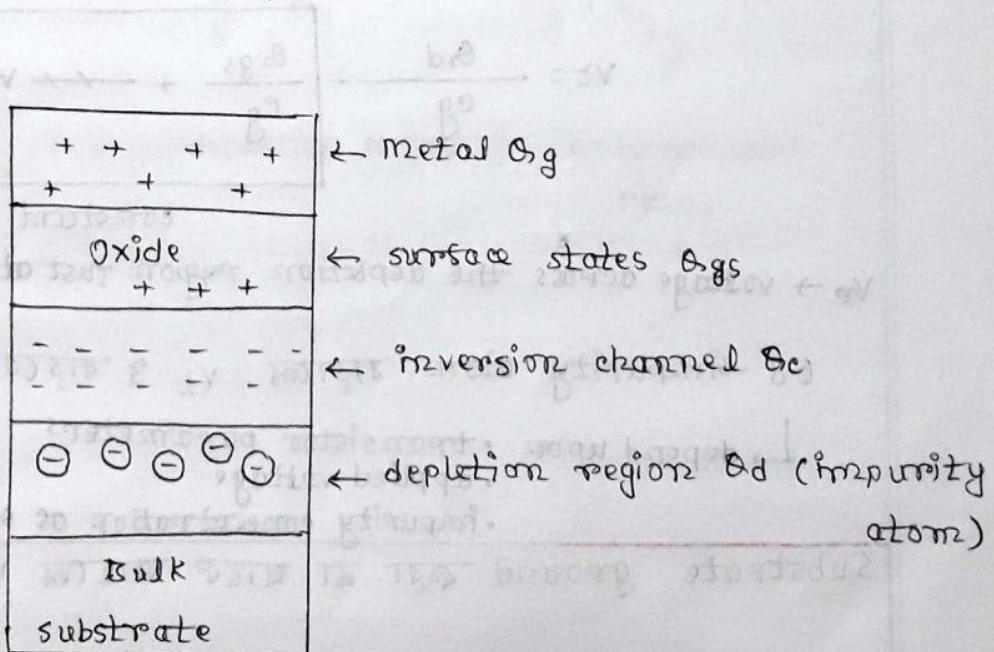


Fig: Excess charge within conducting NMOS transistor.

$$\Theta_{SS} + \Theta_g = \Theta_c + \Theta_d$$

channel create କ୍ଷେତ୍ର ଆଗେ ଘୂର୍ହିଛି $\Theta_c = 0$

$$\Theta_{SS} + \Theta_g = \Theta_d$$

charge = capacitance \times voltage

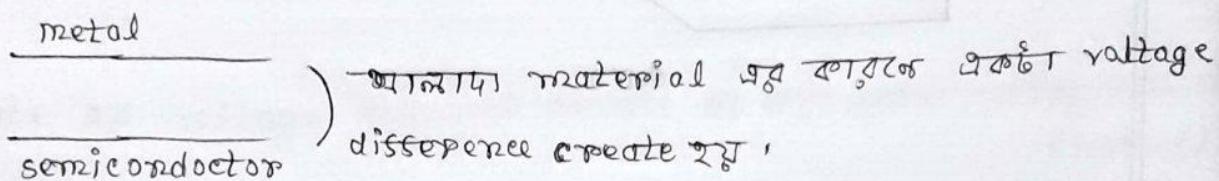
$$\theta_g = \epsilon_g V_d$$

$$= C_g V_d$$

voltage diss

$$V_d = \frac{\theta_g}{C_g} = \frac{\theta_d - \theta_{gs}}{\epsilon_g}$$

(capacitance across the insulator)



$$V_d = \frac{\theta_d}{\epsilon_g} - \boxed{\frac{\theta_{gs}}{\epsilon_g} + V_{dis} + V_{po}}$$

constant होने वाला है

V_{po} → voltage across the depletion region just at the point of inversion.

θ_d → impurity atom वाले V_d के बारे में,

- ↳ depend upon
 - transistor parameters
 - applied voltage
 - impurity concentration of semi

Substrate ground की तरफ आके ताकि V_d में कोई effect नहीं हो।

गढ़े एक body effect होते।

$$\rightarrow 0 \text{ इसके } V_d = V_{to}$$

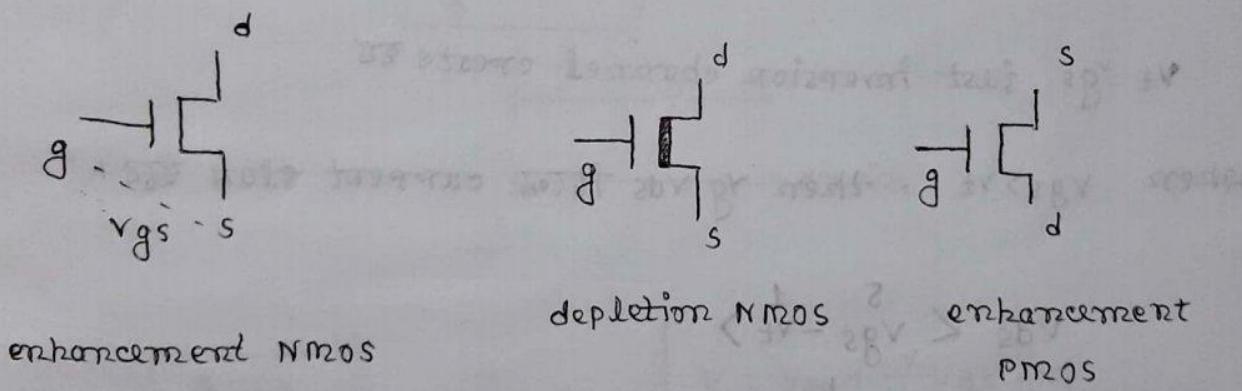
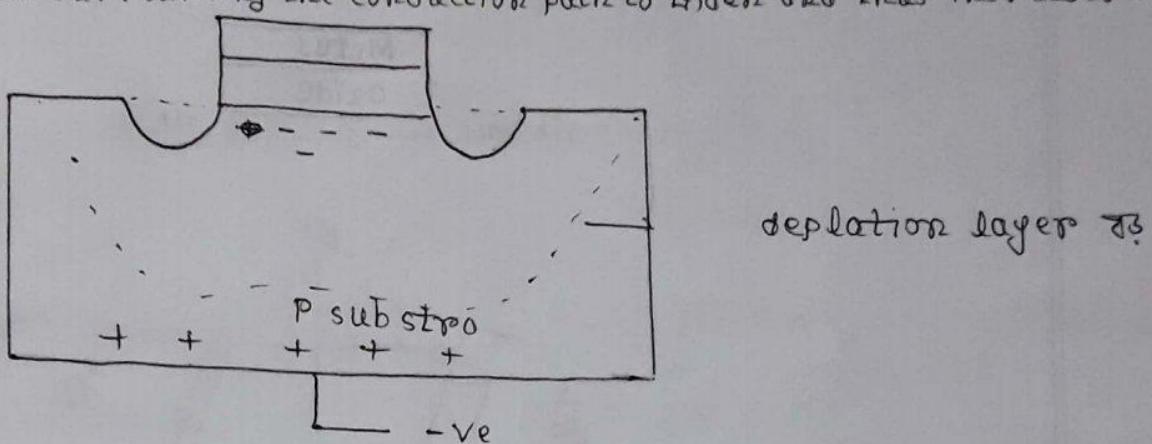
$$V_d = V_{to} + \gamma \sqrt{V_{sb}}$$

↳ bulk

$$\gamma \rightarrow 0.3 \sim 0.7$$

$$\gamma = 0.5 \text{ (default)}$$

In NMOS devices, taking the substrate voltage negative or source causes the depletion region surrounding the conduction path to widen and thus increases θ_d .



$$V_{gs} > V_t$$



when $V_{GS} < V_t$ the transistor is off, regardless of drain voltage

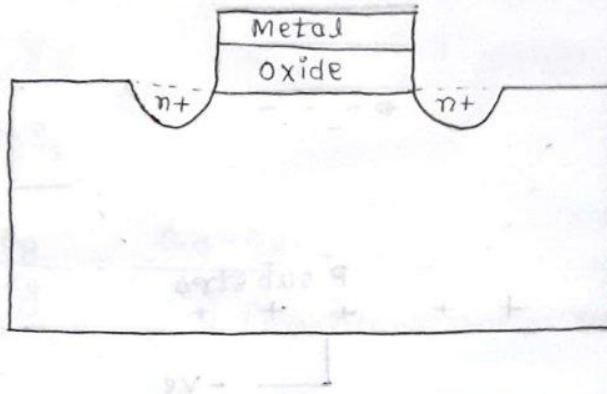
3A

$V_{GS} > V_t$ the device conduct

constant I_{DS} \leftarrow resistive region
saturation \rightarrow

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2.4 I_{DS} versus V_{DS} characteristic for NMOS Devices



$V_t = V_{GS}$ just inversion channel create \rightarrow

When $V_{GS} > V_t$, then $V_{GS} - V_t$ current flows \rightarrow

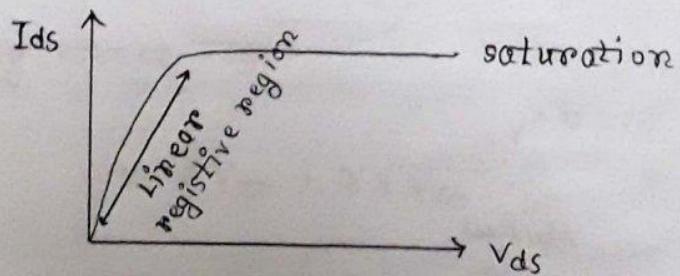
$$V_{DS} < V_{GS} - V_t$$

\hookrightarrow channel to create \rightarrow 4 volt \rightarrow , then

1 volt V_{DS} from exponential

$$V_{DS} > V_{GS} - V_t$$

V_{DS} vs I_{DS}



(a) Resistive Region

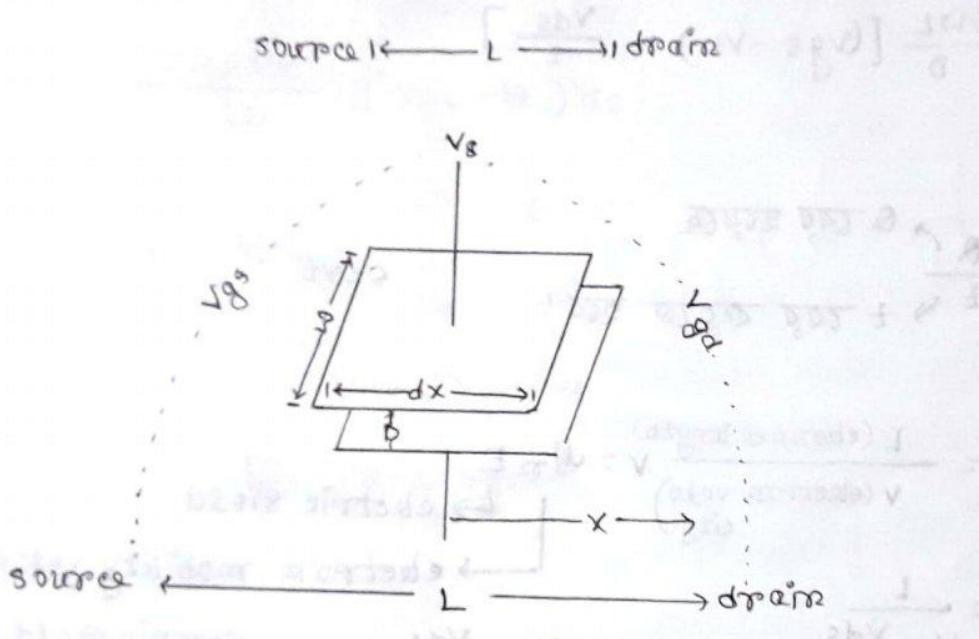
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$$I_{ds} = \frac{V}{L}$$

ϵ is the permittivity of insulation in farads/metre
 D is the thickness of oxide in metres



$$q = CV$$

$$C = \frac{\epsilon A}{D}$$

$$= \frac{\epsilon W dx}{D}$$

$$V = V_{gd} + \frac{x}{L} V_{ds} - V_t$$

$$= V_{gs} - V_{ds} + \frac{x}{L} V_{ds} - V_t$$

$$\textcircled{2} q = \frac{W \epsilon dx}{D} \cdot V$$

$$= \frac{W \epsilon dx}{D} \left(V_{gs} - V_{ds} + \frac{x}{L} V_{ds} - V_t \right)$$

$$Q = \int_0^L \frac{\epsilon W}{D} \left(V_{gs} - V_{ds} + \frac{x}{L} V_{ds} - V_t \right) dx$$

$$= \frac{\epsilon W L}{D} \left[V_{gs} [x]_0^L - V_{ds} [x]_0^L + \frac{V_{ds}}{L} \left[\frac{x^2}{2} \right]_0^L - V_t [x]_0^L \right]$$

$$= \frac{\epsilon W}{D} \left[V_{gs} L - V_{ds} L + V_{ds} L / 2 - V_t L \right]$$

$$= \frac{\epsilon W L}{D} \left[(V_{GS} - V_T) L - \frac{V_{DS} L}{2} \right]$$

$$= \frac{\epsilon W L}{D} \left[(V_{GS} - V_T) - \frac{V_{DS}}{2} \right]$$

$$I_{DS} = \frac{Q}{t} \quad \text{ব্যবহৃত হচ্ছে}$$

$t = \frac{L}{v}$

$v = \mu_n E$

↳ electric field

↳ electron mobility velocity per electric field

$$t = \frac{L \text{ (channel length)}}{v \text{ (electron velocity)}} \quad v = \mu_n E$$

$$= \frac{L}{\mu_n \frac{V_{DS}}{L}} \quad = \mu_n \frac{V_{DS}}{L}$$

$$= \frac{L^2}{\mu_n V_{DS}}$$

$$\text{so, } I_{DS} = \frac{Q}{t}$$

$$= \frac{\frac{\epsilon W L}{D} \left[(V_{GS} - V_T) - \frac{V_{DS}}{2} \right]}{\frac{L^2}{\mu_n V_{DS}}}$$

$$= \frac{\mu_n V_{DS} \epsilon W L}{D L^2} \left[(V_{GS} - V_T) - \frac{V_{DS}}{2} \right]$$

$$= \frac{\epsilon W \mu_n}{LD} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

V_{ds} ৰ এৰ দিয়ে ছোটৰ বা অন্তৰ কম হলে $\frac{V_{ds}}{2}$ negligible

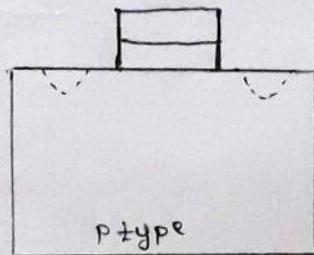
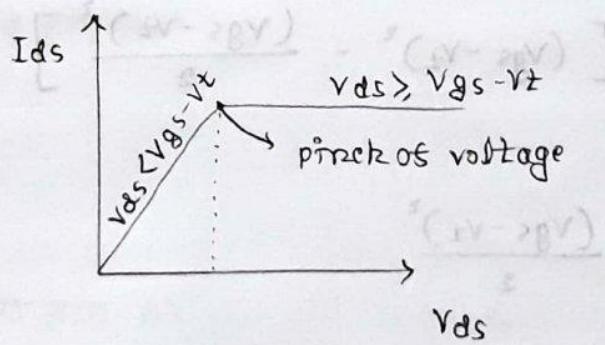
$$I_{ds} = \frac{C_{HdMn}}{LD} (V_{gs} - V_t) V_{ds}$$

$I_{ds} \propto V_{ds}$

$$V_{ds} < V_{gs} - V_t \rightarrow$$

এবং $V_{ds} > V_{gs} - V_t$

(3e)

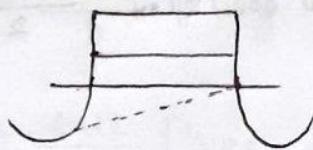


$$V_{ds} = V_{gs} - V_t$$

5 1

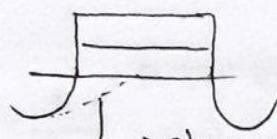
active 4 volt (ex)
open circuit

$$V_{GS} - V_T = 4$$



मात्रा $V_{DS} = 4$

active voltage $V_{GS} - V_T$



$V_{DS} = 6$

strong electric

V_{DS} drop
acti

Field create इयू फोर्स एंड जुम्प ड्रॉप नाही ।

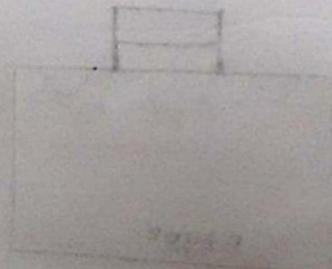
Pinch off voltage 5

$$I_{DS} = \frac{e \mu n W}{L D} \left[(V_{GS} - V_T) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$$= \left[(V_{GS} - V_T)^2 - \frac{(V_{GS} - V_T)^2}{2} \right]$$

$$= \frac{e \mu n W}{L D} \frac{(V_{GS} - V_T)^2}{2}$$

constant



2.5 Characteristics for PMOS

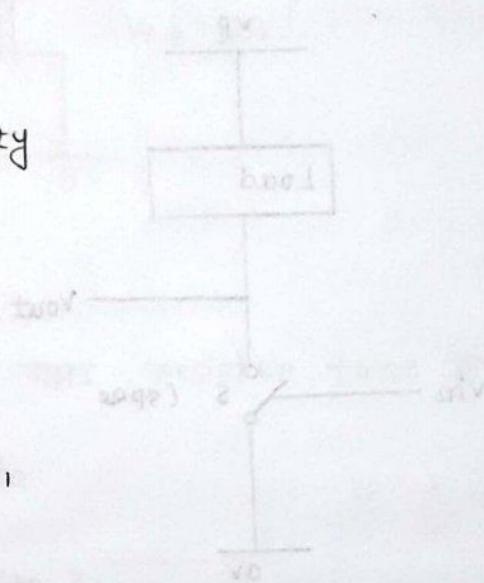
n
 d-s p
 g-s → s → d
 s → g

$\mu_p \rightarrow$ hole mobility

$$\mu_p = \frac{1}{2} \mu_n$$

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e - আর ও নাম্বার ।



Assignment

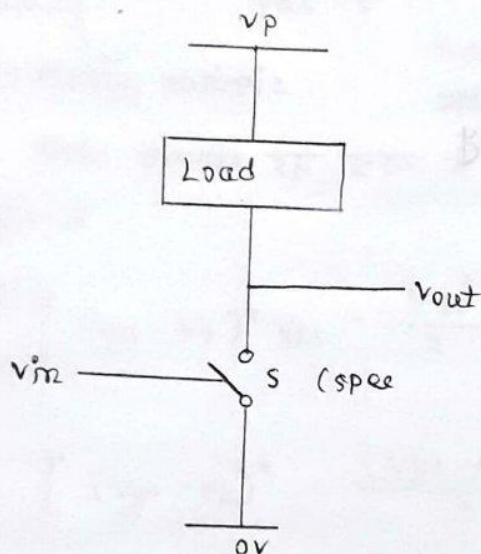
এব তাৰিখ রাত ১২

c, excel file

26 Principles of Inverter

high input \rightarrow low

low input \rightarrow high



V_{in} (high) \rightarrow connection active \rightarrow ground ଏବୁ ମାଧ୍ୟେ attach \rightarrow

$$V_{out} (\text{low}) = 0$$

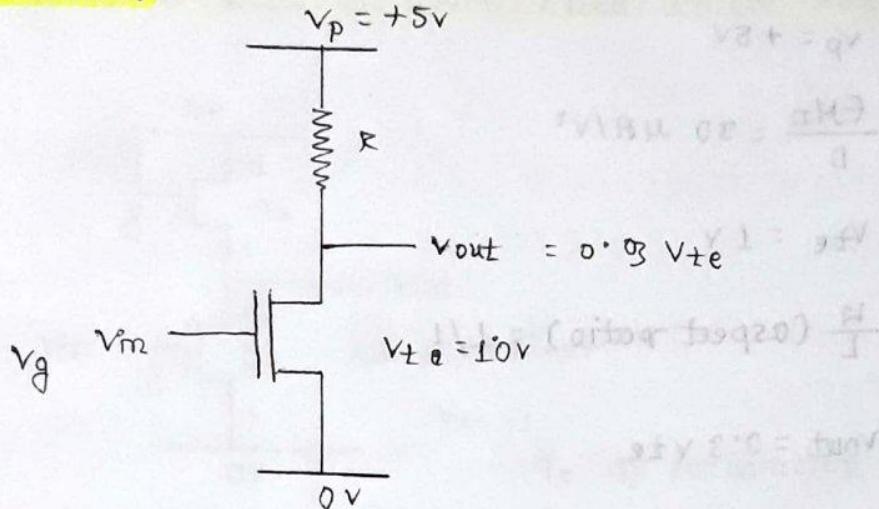
V_{in} (low) \rightarrow connection / switch open $\rightarrow V_{out} = V_p$ (high)

enhancement mode NMOS କୁ ସ୍ଵିଚ୍ କରନ୍ତି?

threshold voltage ଏବୁ ଚାପ୍ଯ ସହ V_{gs} ଏଣ୍ଟି ଚନ୍କେ କିମ୍ବା ଓପର
ଶ୍ରୀ ଥିଲ୍ କ୍ରିଏଟିଭ୍ କମ୍ପ୍ୟୁଟର୍ କମ୍ପ୍ୟୁଟର୍

With Resistor Load

2.7 NMOS Inverter



$V_{out} = 0.3 V_{te}$ হলে যার জন্য resistor time করা হচ্ছে।

↳ noise margin

কেন '0' না হয়ে $0.3 V_{te}$?

Noise margin is the amount of noise, that a circuit could withstand without compromising the operation of circuit.

$V_{out} = 0.3 V_{te}$ হওয়া হলে circuit চিকিৎসা করা হচ্ছে।

$$V_p = +5V$$

$$\frac{eMn}{D} = 30 \text{ mA/V}^2$$

$$V_{TE} = 1V$$

$$\frac{W}{L} (\text{Aspect ratio}) = 1/1$$

$$V_{DS} = 0.3 V_{TE}$$

$$V_{DS} = 0.3 \times 1 - 0 = 0.3V$$

$$V_{GS} = 5V$$

$$V_{DS} < V_{GS} - V_{TE}$$

Linear

$$R = \frac{V}{I}$$

$$= \frac{5 - 0.3}{I_{DS}}$$

$$= \frac{5 - 0.3}{34.7}$$

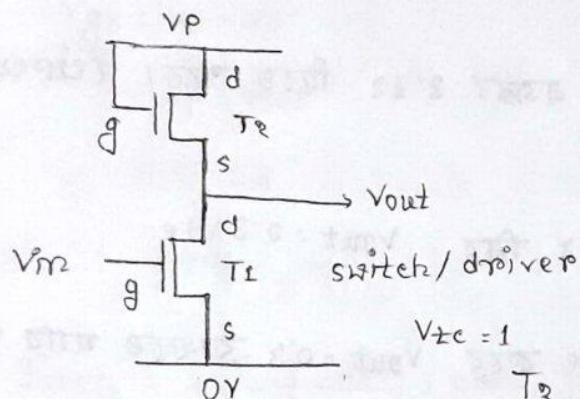
$$= 135.4 k\Omega$$

$$I_{DS} = \frac{eMnW}{LD} [(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}]$$

$$= 30 \left[(5 - 1) \times 0.3 - \frac{0.3^2}{2} \right] \text{ mA}$$

$$= 34.7 \text{ mA}$$

2.8 NMOS Inverter with an NMOS Enhancement Transistor Load.



(body effect)

$$V_m = 0 \text{ VDC} \quad V_{out} = \text{high}$$

 T_2 এর saturation প্রের জন্য T_1 এর মধ্যে দিয়ে শারীর প্রবাহন current, leakage, যদি T_1 conduction mode এ নেই, T_2 এর ক্ষেত্রে,

$$V_{gs} = V_{ds}$$

$$V_{ds} > V_{gs} - V_{Tc}$$

$$V_{ds} = V_{Tc} - V_t$$

$$V_{out} = V_p - V_{Tc}$$

$$= V_p - [V_{Tc0} + \gamma \sqrt{(V_{sb})}]$$

$$V_{sb} = V_s - V_b \\ = V_s - 0$$

$$= 5 - [1 + 0.5 \sqrt{V_{out}}]$$

$$V_{out} = 5 - [1 - 0.5 \sqrt{V_{out}}]$$

$$V_{out} = 3.12 \quad \checkmark$$

$$\Rightarrow V_{out} = 4 - 0.5 \sqrt{V_{out}}$$

$$V_{out} = 5$$

$$\frac{\sqrt{V_{out}}}{2} = 4 - V_{out}$$

$$\Rightarrow \sqrt{V_{out}} = 8 - 2V_{out}$$

$$\Rightarrow V_{out} = 64 - 32V_{out} + 4V_{out}^2$$

body effect ଏହି ଜନ୍ମ ବାଟୁ କରେ ଗଲାକୋ ।

$$\text{high voltage} = 3.12$$

high input ହିଟରେ ଏତଙ୍କା 3.12 ଦିଇ ଥିଲେ, (current ଏହି property)

$$\text{Desired } V_{out} = 0 \text{ ହାଲେ } 2 \text{ କିମି } V_{out} = 0.3 V_{te}$$

$\frac{W}{L}$ ratio measure କରେ $V_{out} = 0.3$ ହାଲେ ଗଲାକି ।

ଆଶ୍ୱର୍ତ୍ତାବ କଣାହେ R ଏହି value measure କରା ଥିଲାଛିଲୋ ।

→ ଏଥାଳେ R ଏହି ଲାଭିବାର transistor NMOS.

$$T_2 \text{ ଏହି କଣାହେ, } V_{gs} = V_g - V_s \\ = 3.12 - 0 \\ = 3.12$$

$$V_{ds} = 0.3 - 0 \\ = 0.3$$

$$V_{ds} < V_{gs} - V_{te} \quad \text{linear / resistive}$$

$$I_{ds} = 30 \left(\frac{W_1}{L_1} \right) \left[(3.12 - 1) 0.3 - \frac{0.3^2}{2} \right]$$

$$= 17.73 \left(\frac{W_1}{L_1} \right) \text{mA}$$

→ aspect ratio

T_2 saturation region

$$V_{GS} = V_P - V_S$$

$$= V_P - V_{out}$$

$$= 5 - 0.3$$

$$= 4.7 \text{ V}$$

$$I_{DST_2} = \frac{50}{2} \left[\frac{292}{L_2} \right] (4.7 - 1)^2$$

$$= 205.4 \left(\frac{292}{L_2} \right) \text{ mA}$$

resistive region of I का रेत।

$$I_{DST_1} = I_{DST_2}$$

$$\Rightarrow 17.73 \frac{291}{L_1} = 205.4 \frac{292}{L_2}$$

$$\Rightarrow \frac{291}{L_1} = \frac{205.4}{17.73} \frac{292}{L_2}$$

$$\Rightarrow \frac{\frac{291}{L_1}}{\frac{292}{L_2}} = 11.58 \approx 12$$

→ inverter ratio

Aspect ratio: individual transistor

Inverter n: NOT transistor

$$K = \frac{8/I}{1/4}$$

प्रोतीव always 12 but कुर्हार size एवं डेसिग तावत्तड्डे हैं

चिक नहूं। एमनडाई Design करते हैं यह चेन्स always

क्यों एंहेंन्मोस इसे करता है?

Drawback :

$$\begin{array}{l} 0 \rightarrow 3.12 \\ (\text{Vout}) \quad 0 \rightarrow 3.0 \quad (\text{V}_m) \end{array} \quad | \quad \text{If } V_m = 0.3$$

0 इसे करने पर V_{GS}

body effect एवं जन्स threshold होते यादे, at same time, V_{GS} 3

करते आके, एंडेन्स current घूर्हे कर होते हैं इसे tends to zero

$$I_{DSL} = I_{DOL}$$

$$\frac{3.12}{3.12 + 0.3} = \frac{3.12}{3.42} = 0.904$$

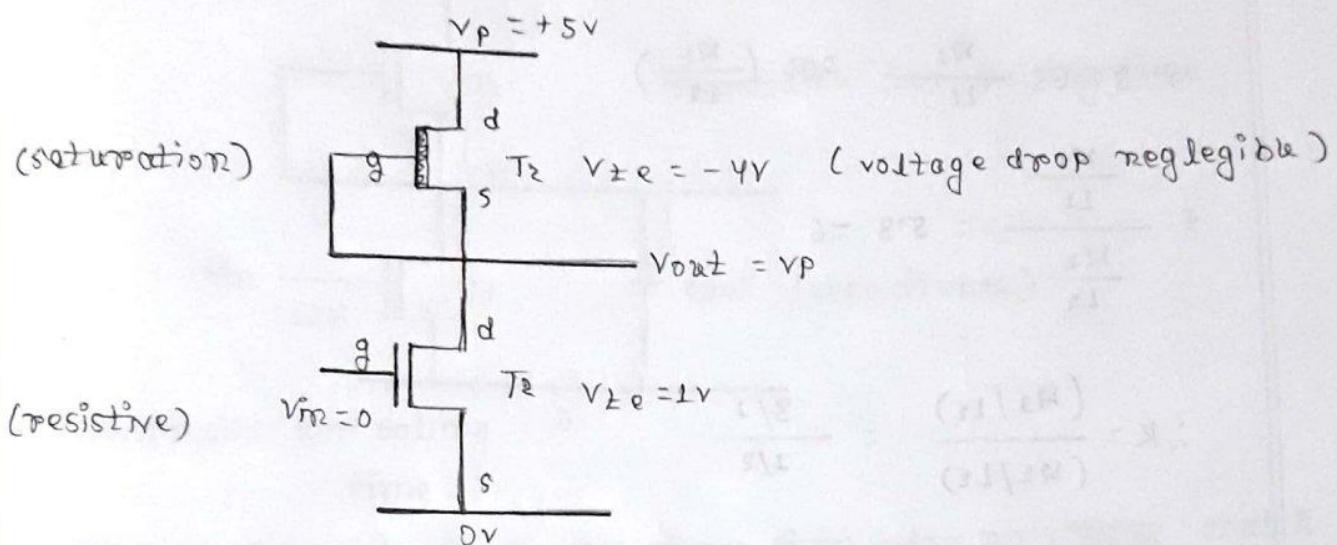
$$\frac{3.12 - 0.3}{3.12 + 0.3} = \frac{2.82}{3.42} = 0.824$$

$$\frac{0.3}{3.12 + 0.3} = \frac{0.3}{3.42} = 0.087$$

Defects निम्नलिखि

Retirement insulation
Retention rate

2.9 NMOS Inverter with OT NMOS Depletion Transistor Load.



$T_2 \rightarrow$ saturation region of OT65 ,

$$V_{IN} = 5V \quad V_{OUT} = 0.3 V_{ZD}$$

$$V_{DS} \quad V_{GS} - V_T$$

$$I_{DS} \text{ of } T_1 = 30 \left(\frac{W_1}{L_1} \right) \left[(5-1)^{0.8} - \frac{0.3^2}{2} \right] = 34.65 \left(\frac{W_1}{L_1} \right) \mu A$$

$$I_{DS} \text{ of } T_2 \text{ if } |V_{DS}| > V_{GS} - V_T$$

$$5 - 0.3 > (V_G - V_S) - V_T \\ 4.7 > (0.3 - 0.3) - (-4)$$

$$\Rightarrow 4.7 > 4$$

→ satisfied

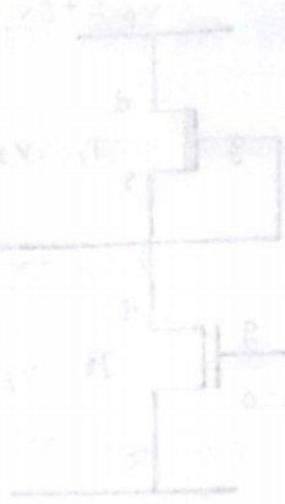
$$I_{DS} \text{ of } T_2 = 200 \left(\frac{W_2}{L_2} \right) \mu A$$

$$I_{DS T_1} = I_{DS T_2}$$

$$\Rightarrow 34.65 \cdot \frac{W_1}{L_1} = 200 \left(\frac{W_2}{L_2} \right)$$

$$\Rightarrow \frac{\frac{W_1}{L_1}}{\frac{W_2}{L_2}} = 5.8 = 6$$

$$\therefore K = \frac{(W_2/L_2)}{(W_1/L_1)} = \frac{3/2}{1/2}$$



voltage drop: २५ म्व, output ५V.

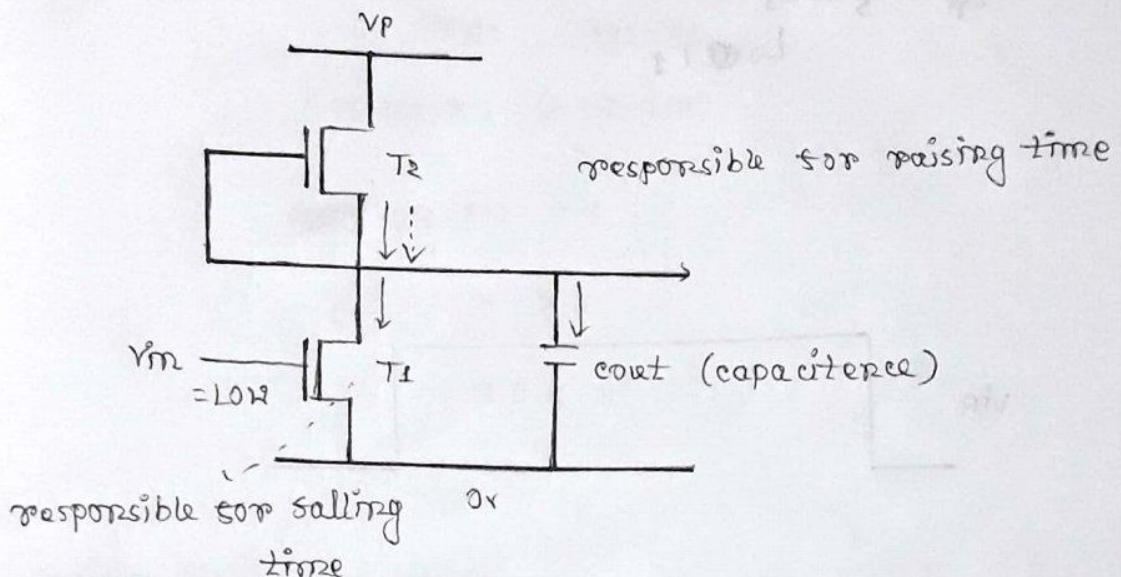
rising time, falling time T_T

2.10 Edge time for NMOS inverter with a Depletion Load.

Property calculation.

transistor & capacitance property $\frac{\text{metal}}{\text{insulator}} \frac{\text{insulator}}{\text{metal}}$

edge time indicate \rightarrow maximum speed of operation and the factors upon which the speed is dependent.



likeage current for T_1 एवं डिट्रॉफ्ट फॉलो इट, फॉलो C_{out} की

चमा इन्हें।

$$V_m = \text{High} \quad T_1, T_2 \quad \text{or} \quad \uparrow \text{out}$$

(*) $I_{DS} \text{ of } T_2 = 200 \left(\frac{W_2}{L_2} \right) 4A$

saturation state of component.

$$I_{DS} \text{ of } T_2 \text{ in saturation, } = \frac{30}{2} \left(\frac{W_2}{L_2} \right) (5-1)^2$$

$$= 240 \left(\frac{W_2}{L_2} \right) 4A$$

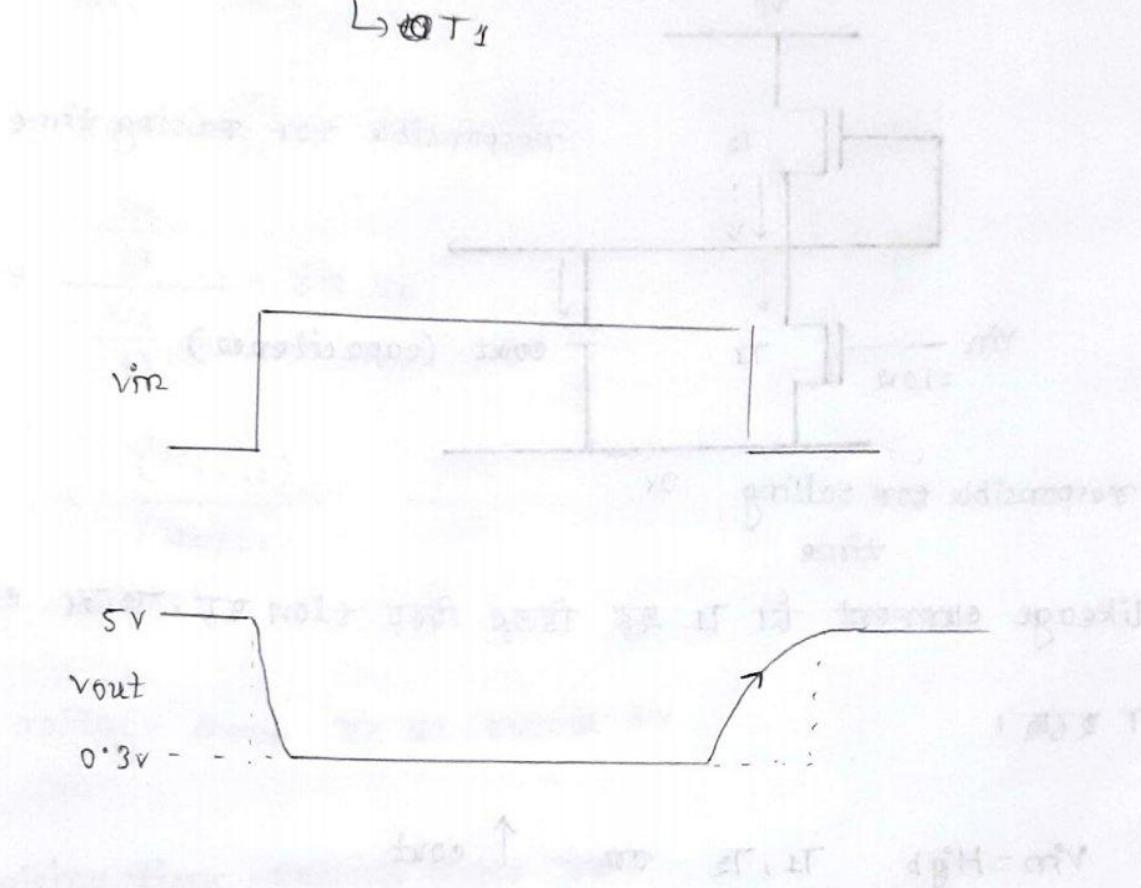
T_1 के time falling time.

$$\frac{\text{Max } I_{DS} \text{ of } T_2}{\text{Max } I_{DS} \text{ of } T_1} = \frac{6 \left(\frac{W_2}{L_2} \right)}{5 \left(\frac{W_2}{L_2} \right)} = \frac{6}{5}$$

or

$$t_r = \frac{6}{5} k Z_f$$

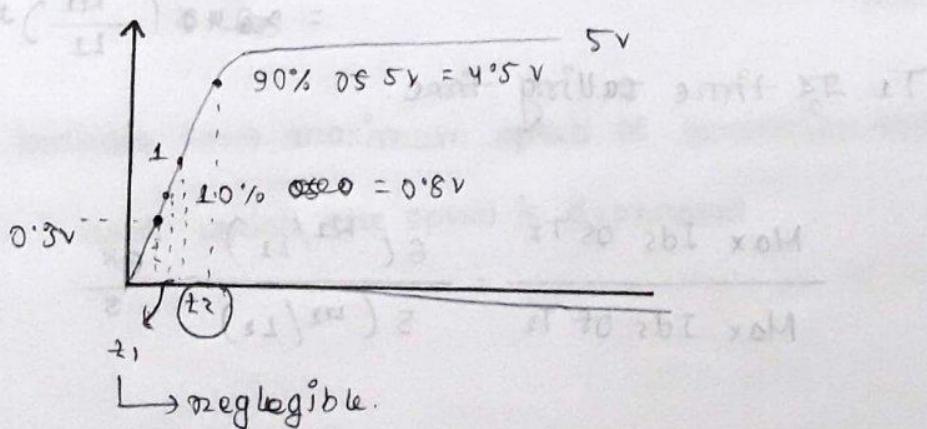
↳ T_1



Rising time वर्ते राह्य:

It is usual to calculate edge times from the 10% to 90% points on the O/P waveform. ($0.3V \rightarrow 5V$)

O/P



$$\begin{array}{r} 0.5 \\ - 0.3 \\ \hline 0.8 \end{array}$$

$$V_{ds} = V_{gs} - V_t$$

$$(0.75 - 0.3) 4.7 > 0 - (-4)$$

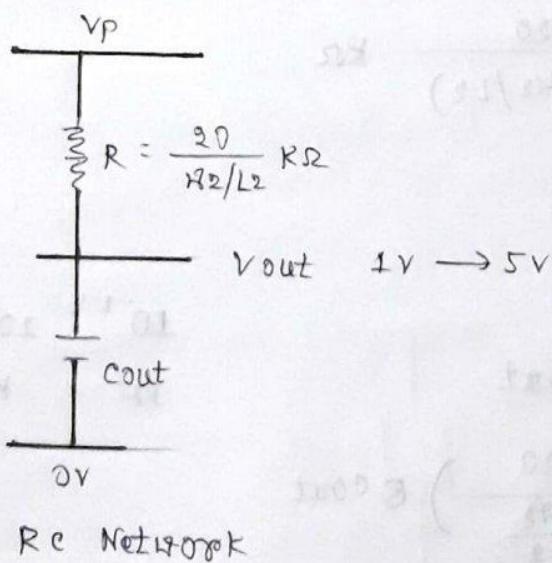
$$(0.45 - 0.8) 4.1 > 4$$

$$(-5 - 4) > 4$$

$$-3.9 < 4$$

raising time : resistive

transistor का represent करने का resistor है।



$$V_{out} = V_p - (V_p - V_I) e^{-\frac{t}{R C_{out}}}$$

$$4.5 = 5 - (5 - 1) e^{-\frac{t}{R C_{out}}}$$

$$4.5 = 5 - 4 e^{-\frac{t_2}{R C_{out}}}$$

$$4.5 = 5 - 4 e^{-\frac{t_2}{R C_{out}}}$$

$$4e^{-\frac{t_2}{R C_{out}}} = \frac{1}{2}$$

$$\text{or, } e^{-\frac{t_2}{R C_{out}}} = \frac{1}{8}$$

$$\text{or, } \frac{-t_2}{R C_{out}} = \ln 2 - \ln 8$$

$$\text{or, } t_2 = -\frac{t_2}{R C_{out}} = \ln 8$$

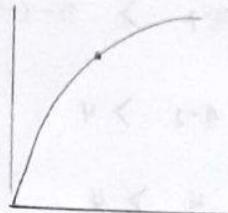
$$\Rightarrow t_2 = 2.08 R C_{out}$$

$$V = IR$$

$$R = \frac{V}{I}$$

$$= \frac{\text{Pinch of volt}}{\text{Pinch of cap}}$$

$$= \frac{(v_{gs} - v_t)}{\frac{eHn}{2D} \left(\frac{W}{2}\right) (v_{gs} - v_t)^2}$$



$$R = \frac{1}{\frac{eHn}{2D} \left(\frac{W}{2}\right) (v_{gs} - v_t)}$$

$$= \frac{1}{\frac{25}{2} \left(\frac{W}{L}\right) (0 - (-4)) \frac{mA}{V}} = \frac{1}{50 \frac{mA}{V}} M\Omega$$

$$= \frac{20}{(L_2/L_1)} K\Omega$$

$$10^{-12} \quad 10^3 = 10^{-9}$$

PF KΩ ns

$$t_2 = 2.08 R_{\text{cout}}$$

$$= 2.08 \left(\frac{20}{L_2/L_1} \right) R_{\text{cout}}$$

$$t_2 = \frac{42 C_{\text{out}}}{(L_2/L_1)} \text{ ns}$$

$$\alpha = \rho V$$

$$RC = \frac{V}{A} \cdot \frac{\alpha \theta_0}{V}$$

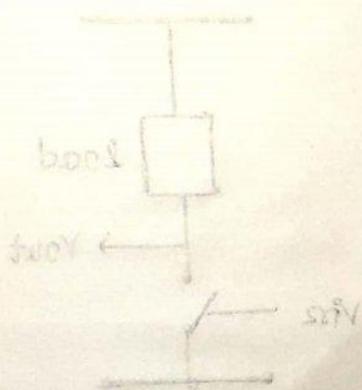
$$= \frac{\theta_0}{A} = \frac{A - 5}{A} =$$

$$t_r = t_2 = \frac{42 \text{ cout}}{L_2 / L_1} \text{ ns}$$

$$t_s = \frac{5}{6} t_r$$

$$= \frac{5}{6} \times \frac{42 \text{ cout}}{L_2 / L_1} \cdot \left(\frac{L_2 / L_1}{L_1 / L_2} \right)^{\frac{1}{K}}$$

$$= \frac{35 \text{ cout}}{L_1 / L_2}$$



4E

Ratioed circuit : aspect ratio.

2.11 Ratioed and Ratioless Design

$$t_{RP} = \frac{42 C_{out}}{2L_2/L_1} \text{ ns}$$

edge time.

$$t_{R} \propto \frac{1}{2L_2/L_1} \text{ ns}$$

$$t_F = \frac{35 C_{out}}{2L_1/L_2} \text{ ns}$$

$$t_F \propto \frac{1}{2L_1/L_2} \text{ ns}$$

aspect ratio রাশিটে time কমবোৰ, speed বৃদ্ধি !

$$I_{DS} \text{ of } T_2 = 240 \left(\frac{2L_2}{L_1} \right)$$

$$I_{DS} \text{ of } T_2 \propto \left(\frac{2L_2}{L_1} \right)$$

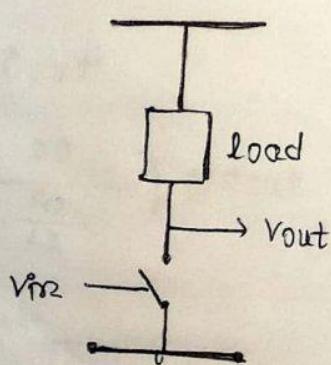
$$n \quad T_L \propto \frac{2L_1}{L_2}$$

Ratioed এবং Problem: Power consumption

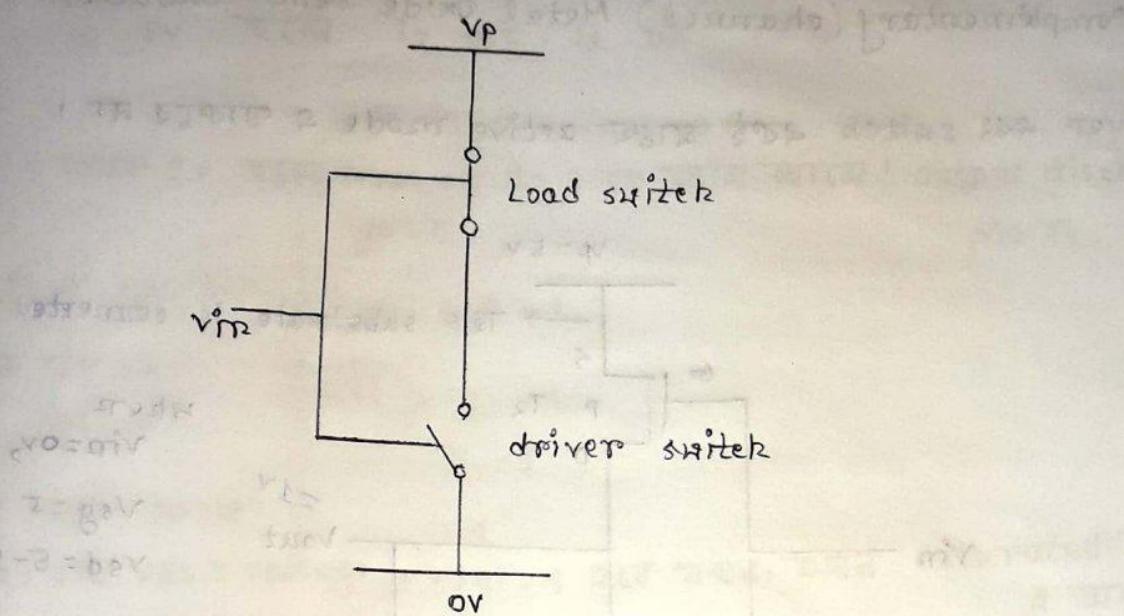
$$P = VI$$

$$\rightarrow I \propto \frac{2L_1}{L_2}$$

তাই চার্জের aspect ratio আসামা
ক্ষমতা কম !



এখন time of driver and load connected থাকবো না !



at a time एकोटाम्यात चिकित्सा जुहे:

एकोरंगुर्दू चालू जुहे का, aspect ratio measure कर्न्हाटे इसो का, no static power dissipation,

$$V_{DSR} = bEV$$

$$V_{DS} = 0 - bEV$$

$$bEV > E - bEV$$

1.

$$V_T = V_T$$

2. Following edge V_D of $V_S = mV$ अस्ति, जब अविवाह नि रि एक

3.

V_T अस्तिहार त्रिभुवन एक लिम्न बताउन्नो हि एक

4.

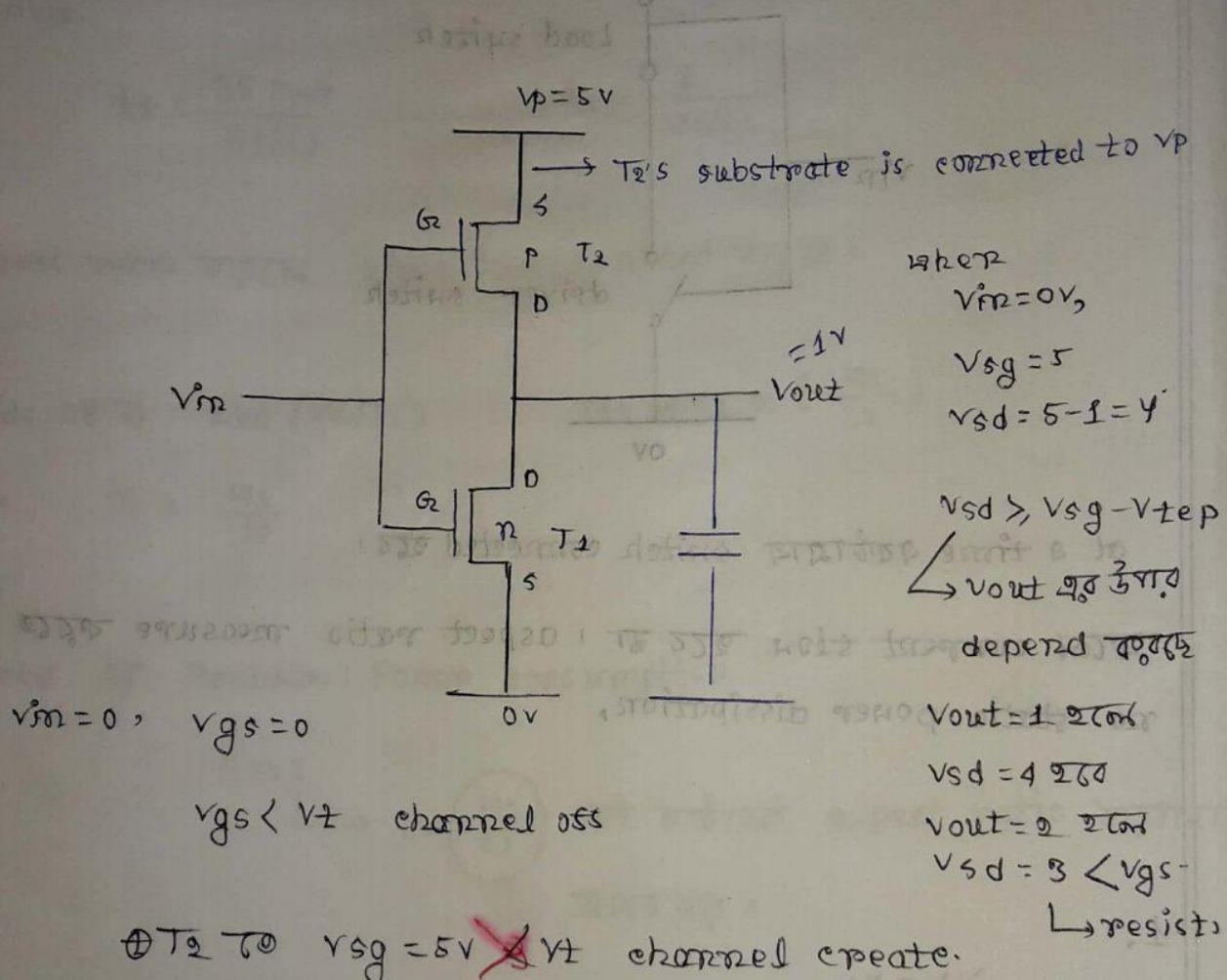
(लिम्निगान गोर्ख सप्तर) $V_S = mV$

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CMOS Characteristics

Complementary (channel) Metal Oxide semi-conductor.

Driver एवं switch एवं वाट्ट्य active mode ए घाकरे ना।



The current flowing through T_2 is the leakage current of T_1 which is very small.

T_2 is in resistive mode. When $V_m = 5V \approx 0V$, capacitor charge

$V_{out} \approx 5V$ in resistive mode,

T_2 is saturated until the output reaches 1V.

$V_m = 0$ capacitance ↑

$V_{out} = 5V$ (voltage drop negligible)

$V_{in} = 5V$ എന്നു T_2 off, T_1 on.

ടാഡ് ദോർ, $V_{out} = 0V$

$V_{in} = 0$ എന്നു 5V എന്നു $V_{out} = 5 \pm 0.2$ ന്റെയോ ആയോ, output discharge എന്ന്

T_1 എന്ന് v_{gs} fixed

ഇഷ്യൻ $V_{in} = 5V$,

$$v_{gs} = 5V$$

But V_{out} change

$$v_{gs} = 5V$$

$$v_{ds} = 4 - 0 = 4$$

$$v_{ds} \geq v_{gs} - V_t$$

$$5 - 1$$

$$= 4$$

via T_1 .

ഇല്ലെങ്കിൽ, താഴെ v_{ds} ചെരുപ്പു ചെയ്യുന്നതു, ഫയൻ saturated എന്നു resistive എന്നു ആയാൽ,

$$\frac{eU_{n2}}{2D} \left(\frac{w_2}{L_1} \right) (5-1) = \frac{eU_p}{2D} \left(\frac{w_2}{L_1} \right) (5-1)^2$$

$$\text{or } \frac{\frac{w_2}{L_1}}{\frac{w_2}{L_2}} = \frac{w_p}{U_n} = \frac{15}{30} = \frac{1}{2}$$

$$\text{or, } \frac{w_2}{L_2} = 2 \left(\frac{w_1}{L_1} \right)$$

$$\text{In saturation, } I_{ds} = \frac{eU_{n2}}{2D} \left(\frac{w_2}{L_1} \right) (v_{gs} - V_t)^2$$

$$w_1 : L_1 = 1 : 1$$

ഡൈ ഡാലോറ്റ് - സ്പെൻ പാ എസ് ടെസ്റ്റ് എൻ റി

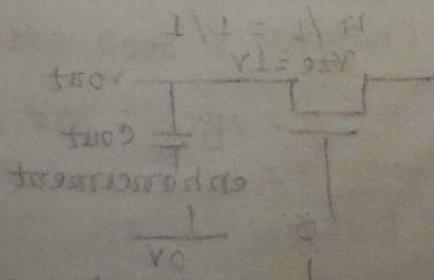
$$w_2 : L_2 = 2 : 1$$

ബൈറ്റേഡ് എന്നു ഭാഗം വിവരിക്കുന്നതുണ്ട്.

• ഫെറ്റു രി ഒ ബി ഫീറ്റു

ഫൈറ്റു ഡൈസ് - റി - പ്രൈസ്റ്റ് എൻ റി

ഡൈസ്



20 ഗോഡ് ലോറ്റ് സ്പെൻ ലോറ്റ്

T_1, T_2 എക്സ് type state നിംബന്മാൻ \rightarrow ടോർ active

T_L

saturation ശീൽഡ് മിനിമു ഇല്ല

channel inactive

ശ്രദ്ധാനാഭരീ യഥാന മിനിമു ഇല്ലെങ്കിൽ ചേയ്യാൻ

$V_{m2} = 2.5$ ടുട്ടി ഫീഡ് mode നിംബന്മാൻ

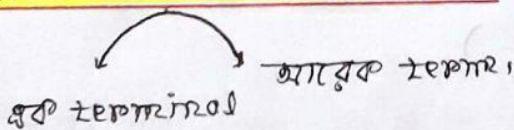
പ്രാഥാന്ത കുറഞ്ഞ ശൃംഗാര

33.8

SE

Basic Gate/Device:

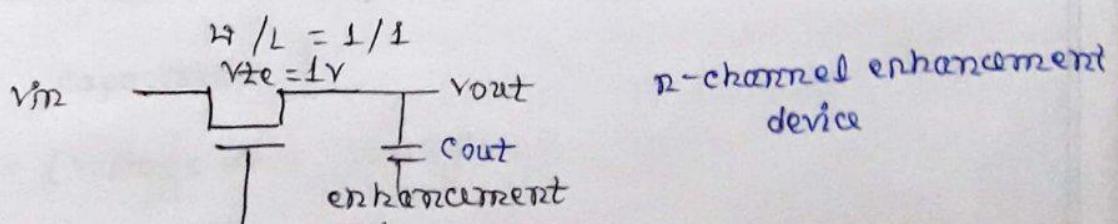
2.13 NMOS Pass Transistor



A device that acts as a voltage-controlled switch

• allows the device input to be selectively

transmitted to its output.



n-channel enhancement device

control voltage controls state of the switch.

applied voltage এর উপর ফিল্ড করে :

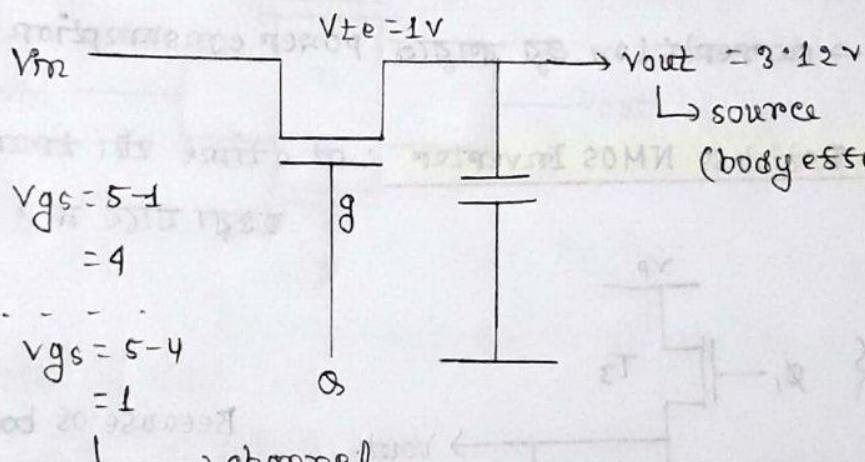
high \rightarrow drain

low \rightarrow source

initially $\phi = 0V$ এলে channel off, V_{out} remains at its existing voltage because V_{out} maintained, capacitor charged. (leakage current এর কারণে)
 অনেক discharge হলে যাবে $\frac{V_{out}}{2}$ না আসবে $\frac{V_{out}}{2}$ অভিভাবত

$$n/L = 1/1$$

$$V_{BE} = 1V$$



$S = 5V$ এলে voltage diff $\neq 0$ transistor T on, action depends on V_{in} , V_{out}

a. $V_{in} = 0V$, initial $V_{out} = 0V$ [No current $\neq 0$ because $V_{ds} = 0$]

b. $V_{in} = V_p$, $n = 0V$ [$V_{in} \rightarrow$ drain, $V_{out} \rightarrow$ source = 0
 $= V_p$, gate = 5V]

current flows from V_{in} to V_{out} .

$$V_{gs} = 5 - 0 = 5V$$

current $\neq 0$ হবে তবে $V_{gs} - V_{BE} = 0$

বাস্তু V_{out} raise হচ্ছে (becz C_{out} is charged) V_{out} change হওয়ার

কারণ V_{gs} বের হচ্ছে, $V_{gs} = V_g - V_s$

$$= 5 - V_{out}$$

$$= 5 - 0 | 5 - 1 | 5 - 2$$

$$V_{ds} =$$

c. $V_{in} = V_{out}$, initial $V_{out} = V_p - V_{te}$

$\rightarrow 3.12$

d. $V_{in} = 0V$, " $V_{out} = V_p - V_{te}$

→ drain, source change

$$V_{gs} = 0$$

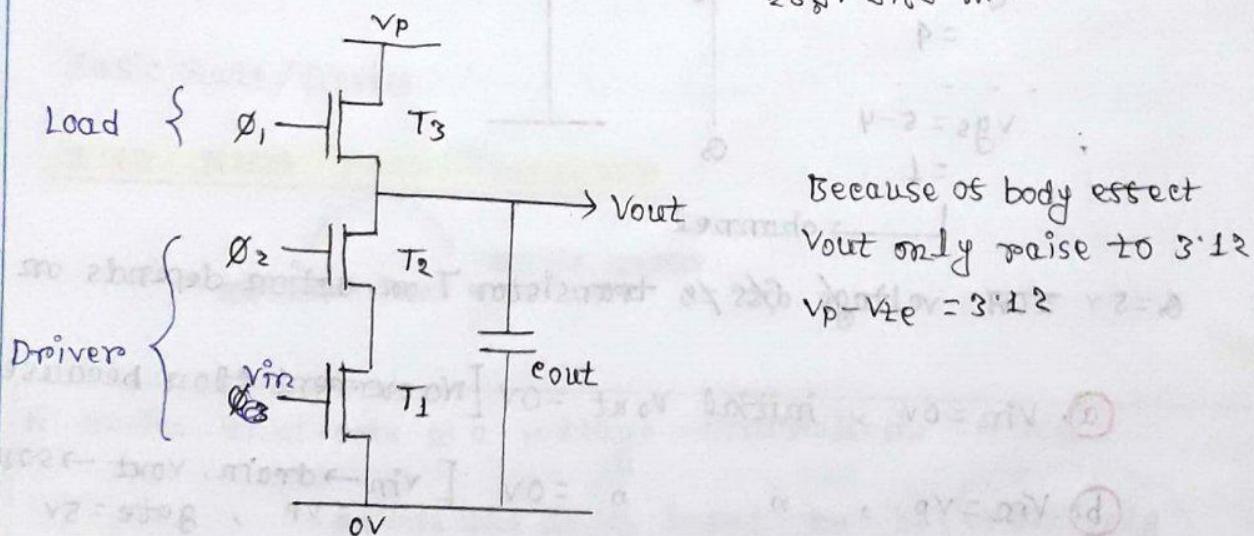
छायोग्नि discharge हो

कौन ratio का problem?

→ ये अपरिवर्ती एवं उत्तर रास्ते power consumption हैं

2.14) Next : Ratioless NMOS Inverter : at a time एक transistor open

इतना होता है



- Φ_1 high, Φ_2 low तो T_3 open, T_2 off, so T_1 याकि बंद हो जाएगा

No path between V_{out} and $V_{in}=0$

V_{out} एवं उत्तर याकि बंद हो जाएगा। V_{out} raise because of capacitor (charged via T_3)

- Φ_1 high, Φ_2 high तो V_{in} एवं उत्तर depend

$[V_{in}=0 \text{ तो } V_{out}=3.1, \text{ but no path between } V_{out} \text{ and } V_{in}=0]$

$V_{in}=\text{high}$ तो याकि repeat हो चर्ज, discharge

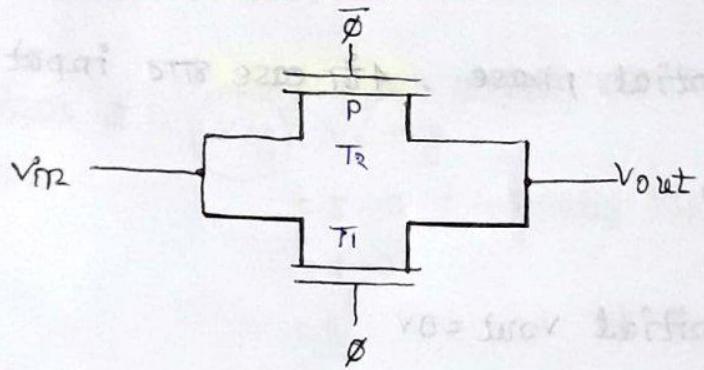
C_{out} discharge होते हैं; $V_{out} = 10V$ होते हैं।

परिवर्तन करने? एक यादें फिर से लगाएं तो उसका अवधारणा होता है।

→ nmos, pmos नहीं होते हैं।

2.15 CMOS Pass Gate /

CMOS transmission gate



• ϕ low अब $\bar{\phi}$ high

→ T_1, T_2 नहीं होते हैं।

$$\text{NMOS } V_{gs} = V_g - V_s \neq 0 - 0 = 0 \quad) \text{ both नहीं होते हैं.} \\ = 0 - 5 = -5$$

PMOS

$$V_{sg} = V_s - V_g \\ = 0 - 5 = -5$$

$$I = 0.5 - 5 = 0$$

so कोनता conduction path नहीं।

- \bar{Q} high, \bar{Q} low both devices turn on.

NMOS

$$V_{GS} = V_g - V_s$$

$$= 5 - 0 = 5$$

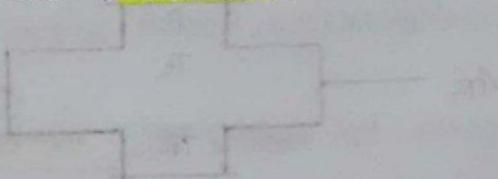
PMOS

$$V_{SG} = V_s - V_g$$

$$= 5 - 0 = 5$$

Turn on, initial phase. **4th case** ~~all~~ input, output एवं

चारों फिल्ड रखें।



a) $V_m = 0 \text{ V}$, initial $V_{out} = 0 \text{ V}$

volt diff = 0, no current flow

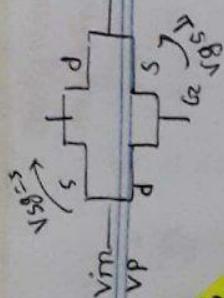
drain of T_1 and source of T_2

b) $V_m = V_p$, initial $V_{out} = 0 \text{ V}$

NMOS फिल्ड current द्वारा $V_{out} = V_p - V_{t2}$

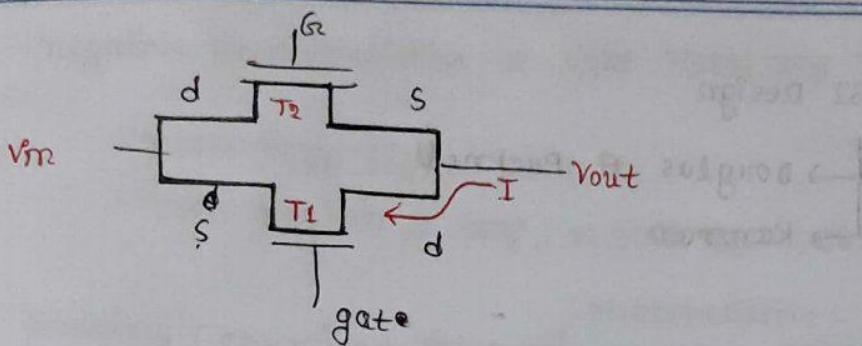
the NMOS turn off द्वारा यादे थर्ड

PMOS फिल्ड 5V (voltage drop नहीं) gain रखते,



c) $V_m = V_p \Rightarrow V_{out} = V_p$, volt diff = 0, no flow, $V_{out} = V_p$ remain

d) $V_m = 0$, $V_{out} = V_p$



nmos \rightarrow s and gate constant, so $V_{gs} = 5$ remain same during fall.
 $V_{gs} = 5$, channel create, s charge

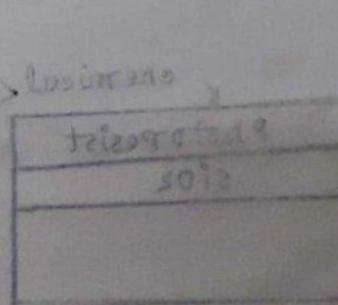
drain to source current fall voltage drop as out discharges.

but PMOS \rightarrow $V_{sg} = V_s - V_g$

$$\begin{aligned}
 &= 5 - 0 \quad [\text{initially } V_{sg} = V_p] \\
 &= 4 - 0 \\
 &= 3 - \dots = \dots = 1 - 0 = 1
 \end{aligned}$$

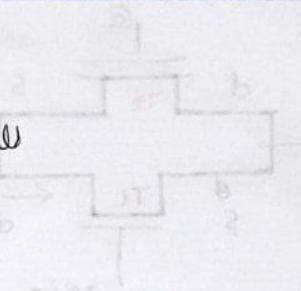
$V_{out} = V_{sg} = 1 = V_{tp}$ pmos device turns off

and V_{out} continues to fall to 0V via T_1 .



বই : Basic VLSI Design

→ Douglas A Pucknell
→ Kammer

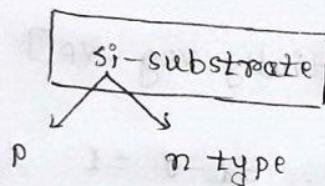


Fabrication

→ NMOS fabrication

Fabrication:

Process of manufacturing semiconductor devices, typically the metal oxide semiconductor (MOS) devices used in the Integrated chips



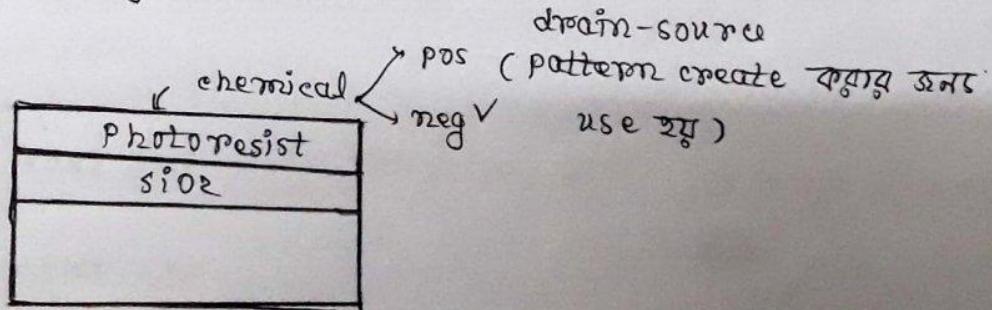
NMOS এর জন্য p type substrate . . . [বই এর signature দ্বারা কৃত
করে]

Si - substrate এর diameter $75 - \frac{150}{500} \text{ mm}$
thickness 0.44 mm

doping $10^{15}/\text{cm}^3$ to $10^{16}/\text{cm}^3$



p-type substrate



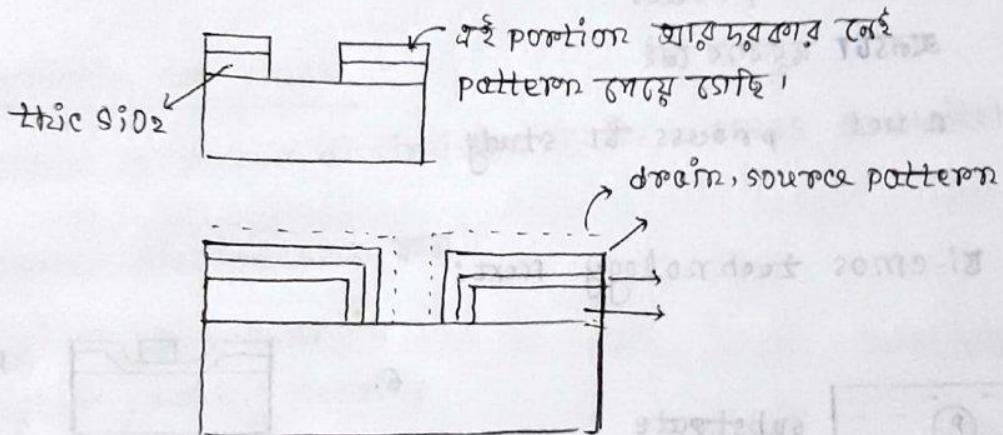
negative photoresistive or light गुड़ने का इयो मार्ग ।

- mask परियों light देना है ।
- देने वाली region का, उसके द्वारा mask determined

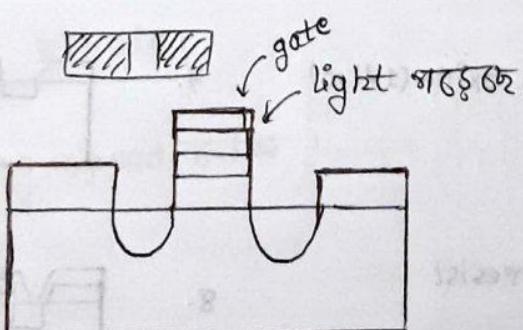
Etching (chemical परियों soft portion शुरू करना)

mask-1 : आकृत्याने light गुड़वे ना ।

silicon portion वाले छड़ियों वाले etching (HF acid परियों)



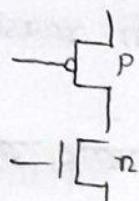
mask-2 use



Describe the process with figure (मेरी तरफ से)

CMOS fabrication : self study

↳ NMOS + PMOS



\checkmark n well process

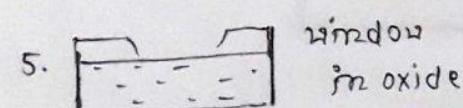
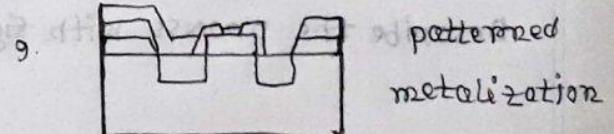
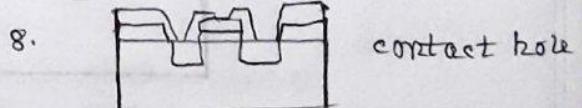
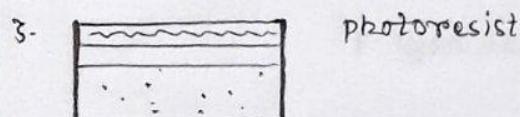
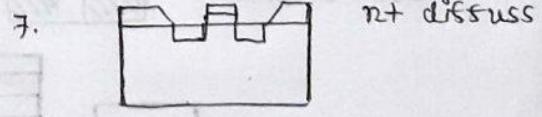
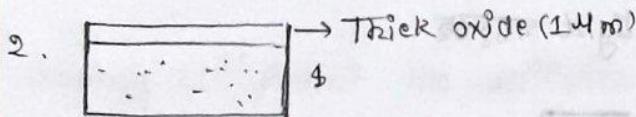
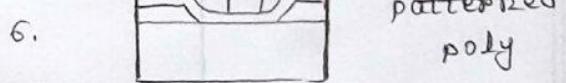
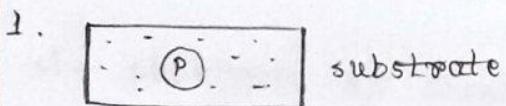
\checkmark p well process

ଅନ୍ତର୍ଭାବ କରି

n well process to study



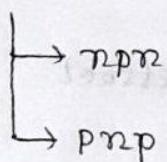
Bi-CMOS technology next:



Trans (BJT \rightarrow Bipolar Junction Transistor
CMOS \rightarrow

BJT and CMOS এর advantage কে এবং ক্ষয়ার জন্য BiCMOS.

BJT: base, collector, emitter



characteristics of CMOS

- NMOS এ power dissipation কম, CMOS এ switch এর বাস্তুতে power dissipation কম।
- Higher noise margin
- Higher packing density
- High yield.

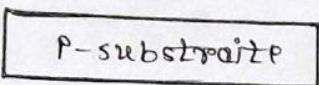
characteristics of Bipolar

- switching speed কম।

BICOMOS କୁଣ୍ଡାଏ ଥେବାରେ better.

SiCOMOS Fabrication :

1.



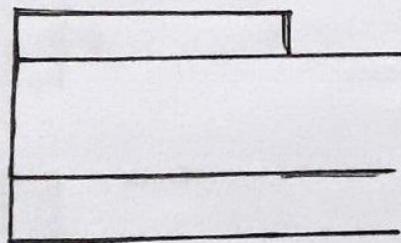
2. Oxide layer (ତ୍ୟ ଅପରେସନ ଗୁଣେ କମ୍ପା ହେଉଥାଏ effect)

3.

4. Buried layer (ନିଚେଯ ଧର୍ଯ୍ୟ କୁର୍ରାତର ମିଳାଦର୍ଥ ଲାଗେ)

5. Epitaxy : some layer ଏବଂ ତୀର୍ତ୍ତ ଯାହେକାଟା layer

6.

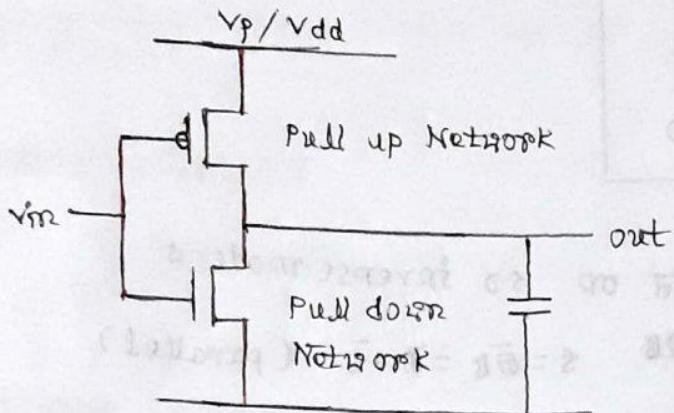


Step 19: Pucknell ଏବଂ ବର୍ଷ ଥେବେ figure ଦେଖେ ନିତେ ହୋ।

Pull-Up and Pull-Down Networks

CMOS गेट एक संयोजन है। यह पुल-अप और पुल-डाउन क्रियों का संयोजन है। P-MOS द्वारा डाउन चार्ज किया जाता है और P-MOS द्वारा अप चार्ज किया जाता है।

N-MOS द्वारा डाउन चार्ज किया जाता है और N-MOS द्वारा पुल-डाउन किया जाता है।



Pullup एवं PMOS कैसे हैं?

$$V_{gs} > V_t$$

body effect एवं source जैसा है।

Pullup एवं NMOS याकरण source, V_{ds} एवं याकरण connected.

V_{out} बढ़ते हैं तब तक source voltage change, so threshold change.

एवं highest १.२५V गई है। Full voltage माझे याद ना,

■ The function of Pull up Network is to provide a connection between V_{dd} and V_{out} to pull V_{out} to logic '1' (charge up)

■ Pull up, pull down both connected हैं, power rails would be short

If neither connected, output would float (tristate logic)

PMOS is conducting with low input
 $p(\bar{x}_1, \bar{x}_2, \dots) = s(x_1, x_2, \dots)$

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NAND $s = (\bar{A} \cdot \bar{B})$, pull

A	B	$\bar{A} \cdot \bar{B}$
0	0	1
0	1	1
1	0	1
1	1	0

Pull up : zero वाले OR से inverse mode में

$$s = \bar{A} \cdot \bar{B} = \bar{A} + \bar{B} \quad (\text{parallel})$$

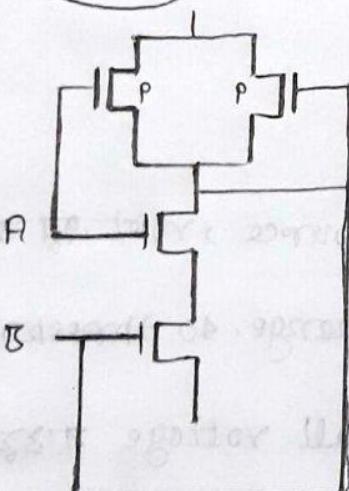
Pull down:

"function तरीके में नहीं"

$$\begin{aligned} s &= \bar{A} \cdot \bar{B} \\ &= \bar{A} + \bar{B} \end{aligned}$$

$$\bar{s} = A \cdot B$$

(series)



यादृच्छिक CMOS नामांकन

त्रिविधु

सेट करना

त्रिविधु

NOR gate.

$$f = \overline{(A+B)}$$

*

$$\textcircled{f} = \overline{(A+B) \cdot c}$$

$$\text{pullup} = \overline{(A+B)} \cdot c$$

$$= (\overline{A+B}) + \overline{c}$$

$$\text{pull down } f = (A+B) \cdot c$$

यदि $f = (A+B) \cdot c$ देखा शारण ठाएने

Let $f = (\overline{A+B}) \cdot c$ को नियम हो, तो वह अंकों का बदला नियम हो।

0 → 1
1 → 0

0 → 0
1 → 1

0 → 1
1 → 0

0 → 0
1 → 1

Color Plate Stick diagram and Design Rules

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Blue \rightarrow cable connection

Rule 1:

একই color cross করতে connection হবে নোর

Rule 2:

অন্যান্য color cross করতে normally connection হবে

Rule 3:

ফিল্ম (polisilicon + diff \rightarrow transistor) \rightarrow contact shown হলে
diffusion not a transistor

connection দিতে চাইলে explicitly দিতে হবে।

Rule 4:

In CMOS,

is drawn to avoid touching p-diss
 \nearrow with n-diss

pull up

- - - demarcation (metal আর polysilicon)

pull down

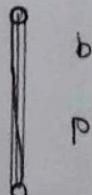
কাস্ট

cross করতে নাহিবে

* depletion হোমানোর জন্য yellow দিতে হবে।

Stick diagram এর মধ্যে main circuit ও আকতের পরিসর দেখা

green \rightarrow NMOS



blue \rightarrow metal

yellow \rightarrow PMOS

poly \rightarrow red

Stick Diagram: is means of capturing topography and layer information through color codes.

Design Rule: series of parameters provided by semiconductor manufacturer that enable the designer to verify the correctness of a mask set.

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Page :

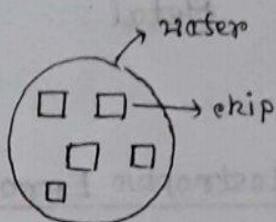
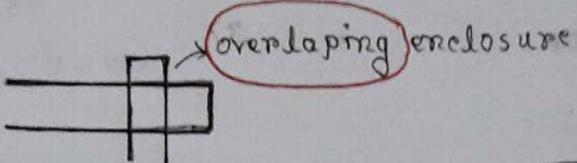
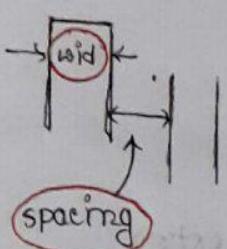
8A

Design Rules

stick diagram & measurement घटके हैं।

circuit design के तर्ज पर measurement provide

Basic DRC



DRC (Design Rules checking) determines whether the physical layout of a particular chip

satisfy rule.

satisfy rule.

- optimize ~~area~~ yield (percentage of good chip)
- minimize the
- reliable

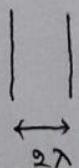
Yield: Unclustered

clustered (defect का बाजे होते)

2 major approaches:

• Micror:

• λ rules: scalable → बड़ा हो, कमाने याए \times



* Exam: Design -----

λ based (MOSIS) Design Rules:

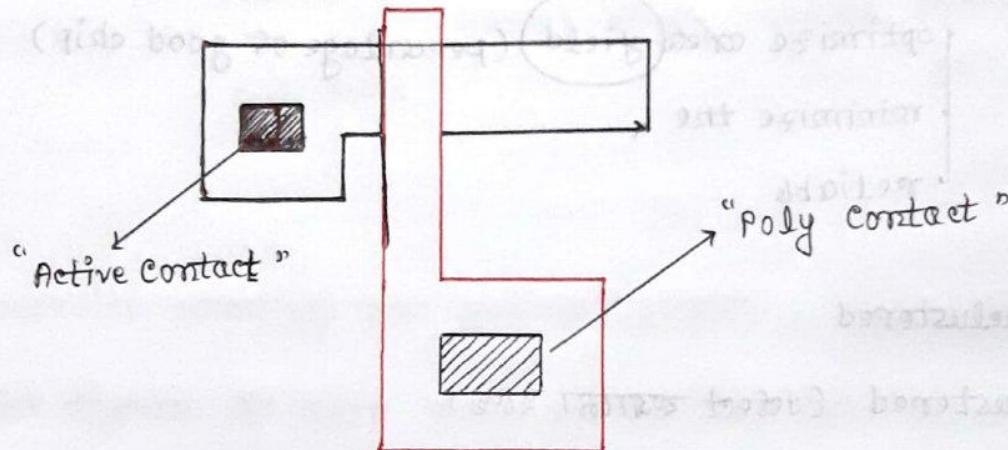
Poly+silicon: minimum 2λ

Diffusion: 3λ

Metal:

catastrophic Errors: overlapping & enclosure extra

NT problem create $\frac{1}{2}\lambda$



Micron: constant

Adder

half adder:

$$e_0 = ab$$

$$\text{sum} = \bar{a}b + a\bar{b}$$

CMOS fig of half adder... + stick diagram

Full Adder:

$$e_0 = ab + bc + ac$$

$$\text{sum} = a \oplus b \oplus c$$

CMOS fig design

Shifter: (Circular)

→ pass transistor / CMOS fig convert

0 shift] same
 n n

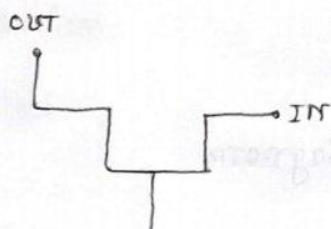
k bit right shift = $n-k$ left shift

$0 \rightarrow n-1$ पर्याप्त शिफ्ट

4×4 shifter (matrices എന്നും)

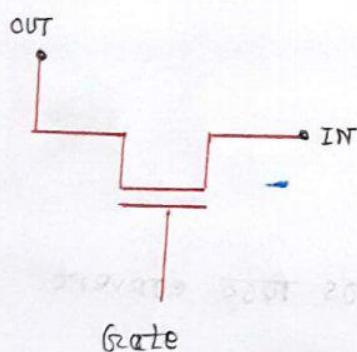
Right shifter (self)

shifter



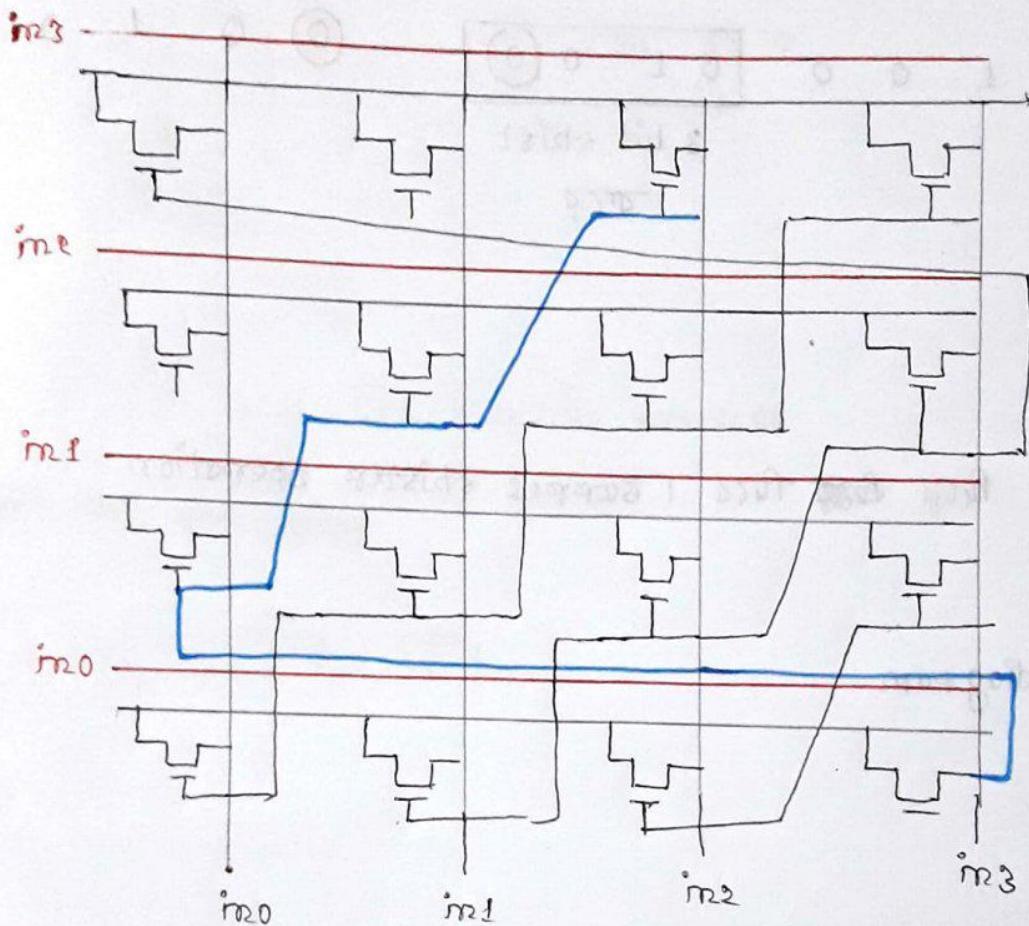
switch

- * Crossbar switch: 4×4 shifter \rightarrow 4×4 barrel shifter.



switch (nmos pass)

ഏറ്റവും 16 ടി സ്വിച്ച് നി ഉണ്ടാക്കാൻ പറ്റിയാണ്.

4x4 Tapped shifter

Switches are mutually exclusive (এখন্তা এক কলে বাঁকী পুলে) ACTIVE
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left shifter

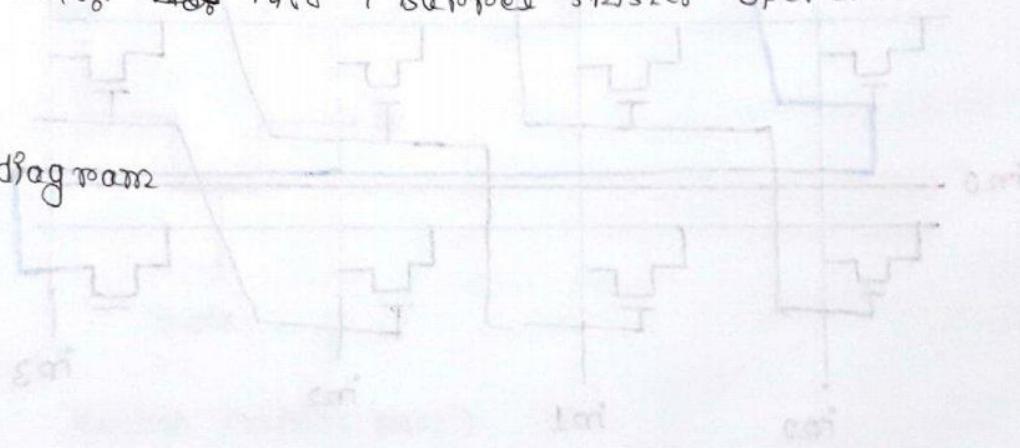
50/54	S3	S2	S1	i3	i2	i1	i0	03	02	01	00
1	0	0	0	0	1	0	0	0	1	0	0
0	1	0	0	0	1	0	0	0	0	1	0

3 bit shift

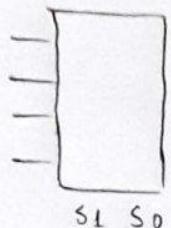
বাটো

Input দিয়ে আঙুল দিয়ে । Parallel shifter operation

stick diagram



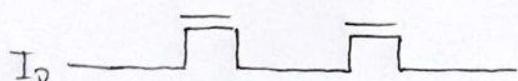
Multiplexer (Data selector)



S_1	S_0	I_o
0	0	

$$I_o = I_0 \bar{S}_1 \bar{S}_0 + I_1 \bar{S}_1 S_0 + I_2 S_1 \bar{S}_0 + I_3 S_1 S_0$$

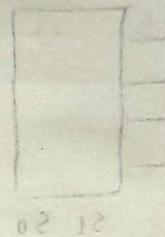
NMOS Pass Transistor



Design Representation

Design can be of any level:

Highlevel - fabrication



Intermediate

Lowlevel : Backend.

$$02121I + \bar{0}2121I + 02\bar{1}21I + \bar{0}2\bar{1}20I = S$$

Front level शब्द

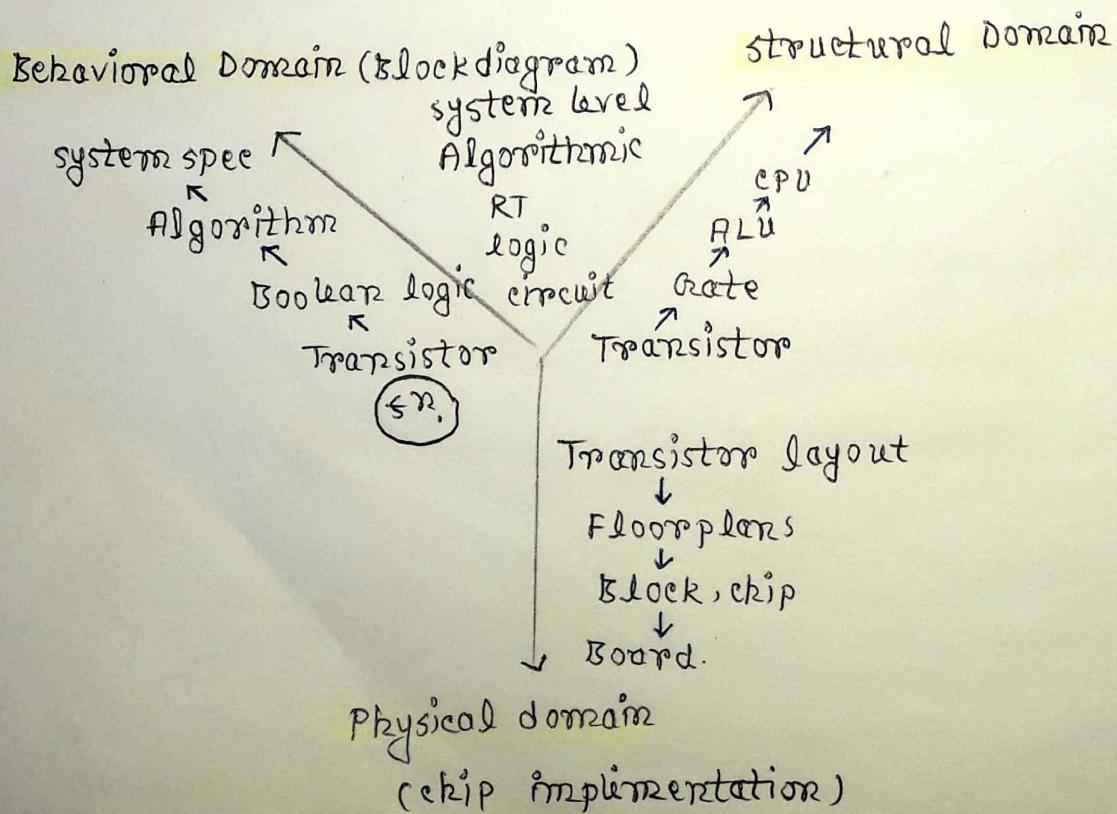
orofasemart 2209 20H3

Behavioral: input फॉर्म फॉर output नाही !



structural: को को वर्तनेवे component निये होते, IO, CPU, peripheral device

physical: core level, (memory-chip), circuit.



Outer shells are generalisations.

ডিট্রোর ফিল্ম পৰ্যে এমন level, abstract, physical না।

Alternative Y-chart (কাষেলের মত) helix shape

এটাৰও ডিট্রোর ফিল্ম manufacturing level.

Locsys19

Behavioral Represent (how a design should respond to given input)
specified by,

- Boolean equation : and, OR

- truth table

- Algorithms written in standard HLL like C.

- Hardware level language (Verilog or VHDL)

↳ VHDL

VHDL : Hardware Description Language.

VHSIC : Very High speed Integrated Circuits.

• Cell Struct

network का क्रम इवे component कि कि?

प्रैक्टिक (प्रैक्टिक) त्रैया, नियम

लेखनालोगिक, कर्ता संस्कृती

Physical

fabrication, masking

(तुम्हारी)

Preparation Reel

RC, bias : असाधारण

○ Physical Design Flow

Physical design converts a circuit description into a geometric description.

Circuit Partitioning

complex system के smaller module / subsystem.

module बीचेरे मध्ये येणा connection कर इये, minimize interc.

cut size = connection

size 1 = 15 व्हा गाने के cut ए 15 का component.

■ Each subsystem का be designed independently.

o Floor Planning

module কোনো কিছির place ? কিছির connection ?

- determine rough position

কোনটাৰ গুৱা কোনটা দিলে optimal হবে ?

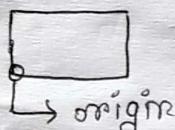
- shapes of block

- pin locations of the blocks

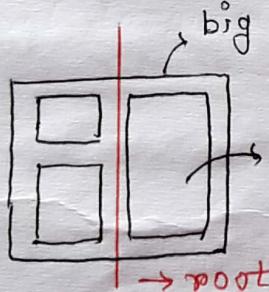
■ Find approximate locations of a set of modules that need to be placed on a layout surface.

→ Available region typically considered rectangular.

Floor Plan Specification

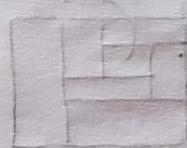


modules, area, rotation



big rectangle (vertically, horizontally dissect)

slicing tree → skewed
↓ non skewed



V → vertical

lest এৰ মুলো least node

H → Horizontal

নিচেৰটা বামে, উগাবোঢ়া কৰে

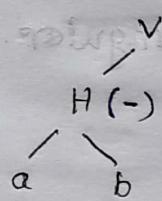
^{right}
skewed parent and child node কাষণটি কোনে থাবে না'



$H \backslash H$ → non-skewed (চোখে না portion এ
থাবে নেই non-skewed)

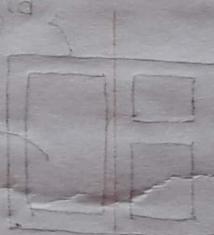
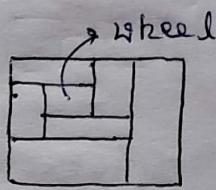
LRR

Left, Right, Root



tree থেকে floor plane

Non slicing Floor Plane:



↳ hierarchical

Non slicing যখন slicing এর মধ্যে চাল আয়ে, তখন গ্রেট

A hierarchical Floor plan

Introspective H

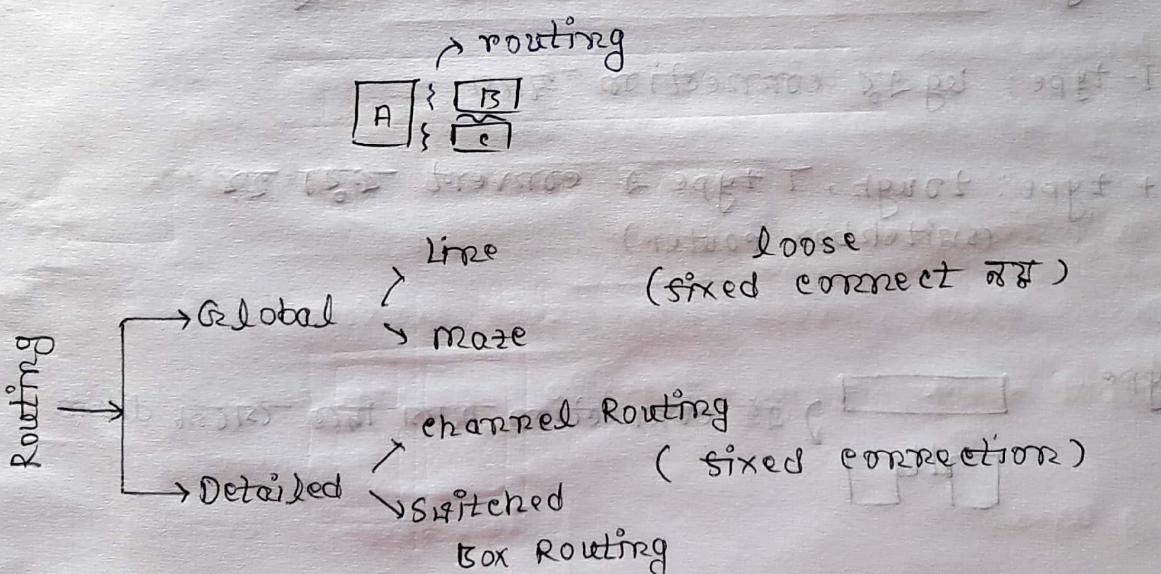
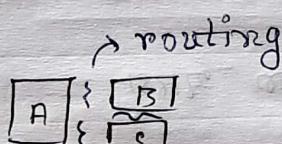
Diss of floor planning and Placement:

Floorplanning → flexible, pin connection ^{not} fixed, routing area.

Placement: geometrical shape, with defined pin location, separate space for routing.

o Routing

cable connection/generating metal wires to connect the pins



↳ desired

Routing Region: Through which inter connecting wires are laid.

Horizontal: top and bottom pin connection

Vertical: (left, right) pin connection

Switchbox (मार्गदर्शक pin)

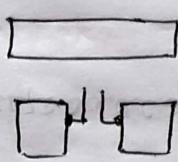
channel junctions:

channel routers } L-type: board एवं corner एवं, ordering is not important

T-type: leg एवं connection आठों

+ type: tough, T type एवं convert करना शक्ति
(switchbox router)

T-type



प्रत्येक आठों परिवर्तन की दिक्कत

Graph models used in Global Routing

graph problem.

1. grid based

2. checker

3. channel Intersection: Most suitable for global routing

Two-stage routing method is a powerful technique.

Floating terminal: 2 side থেকে connection possible

তথ্যন 2 side থেকে connection করে করে হাস্যা হয়।



* Order of Routing Regions

Slicing

Non-slicing (switchbox)

Detailed Routing (geometric)

Placement

global Routing

Detailed Routing

Routing layer:

কর্তব্যজনোয় metal/color

1 layer: 1st, metal connection

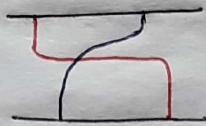
3 layer: vertical deep blue

মধ্যে vertical অন্য color

Models for Multi-layer Routing

Unsolved: Layer এর color: ১) Horizontal, vertical ২)

color আসাদা হয় ১) ২) ৩) ৪) ৫) ৬) ৭) ৮) ৯) ১০)



wavy portion to grab

Determine the presence of fault

o Testing of VLSI circuit

because there are so many environmental variations possible

Fallacy (সব যেন ঘটিত কিন্তু ঘটত নয়) (Testing is used to guarantee that a chip is fault-free). Testing only increases confidence

Difference between Testing and Verification

Verification:

Design check, measurement check, performed once

Testing:

Output check, trial, tries to guarantee the correctness of the manufactured chip/circuit

Testing level:

chip level

board level

system level

Two steps in testing:

① Test Generation

upper level & testing cost দুটি,

দ্রোপ অন্তরে কাটা।

accidentally some dissensual polysilicon layers might

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Date:

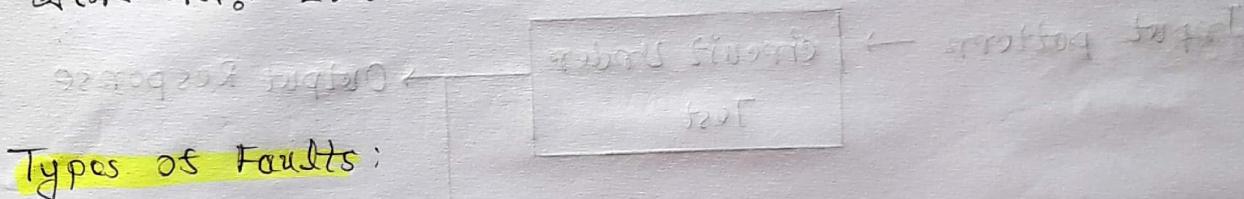
Page:

Source of Faults:

- during fabrication process : surface এবং উপরের rectangular pattern
- Defects in material(s) :
- Because of ages :
- During packaging :

parasitic Transistor, NMOS, PMOS এবং capacitance দ্বারা হয়,

অনেক মধ্যে Transistor



Types of Faults:

Permanent : ক্ষতি দ্বারা ; time independent, easier to detect

Nonpermanent : loose connection



Intermittent (charge particle)

nonenvironmental

(0.733)

0.09433

(1 - FC)

$\frac{1}{199} (199 - 53)$

$$DL = 1 - Y$$

$$1 - (0.73)^{0.09} \quad FC = \frac{48}{53} = 0.905$$

Some Terminology:

Fault coverage : $FC = \frac{\text{detected fault}}{\text{Total no. of faults}}$, determines the quality of set of test vectors

$(1 - FC)$ means faults not been covered

Defect Level:

yield (যদি অংশ good, 0-1 এর মধ্যে)

Fault coverage : কতটুকু detect করতে পেরেছি

Basic Testing Principle:

golden response (output standard)

