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| Combinational Circuit Design |
| Section 1,Group 7 |
| Fall 2017 |

Submitted to-

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**Specification**

Input: 3 bit of Input ( X ,Y,Z )

X being the most significant bit and Z least significant bit

Output: Sequence of letters at the 7-segment display one by one

Functional Operation: For each certain combination, one certain output will be displayed i.e. for 0 0 0,the output will be C .

**Formulation**

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | X | Y | Z | a | b | c | d | e | f | g |
| C | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| S | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| E | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 2 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 3 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| - | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 7 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |

Figure : Truth table of circuit

**Optimization**

For the multiplexer circuit ,

|  |  |  |  |
| --- | --- | --- | --- |
| X | Y | Z | b |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

|  |  |  |  |
| --- | --- | --- | --- |
| X | Y | Z | a |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

|  |  |  |  |
| --- | --- | --- | --- |
| X | Y | Z | c |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

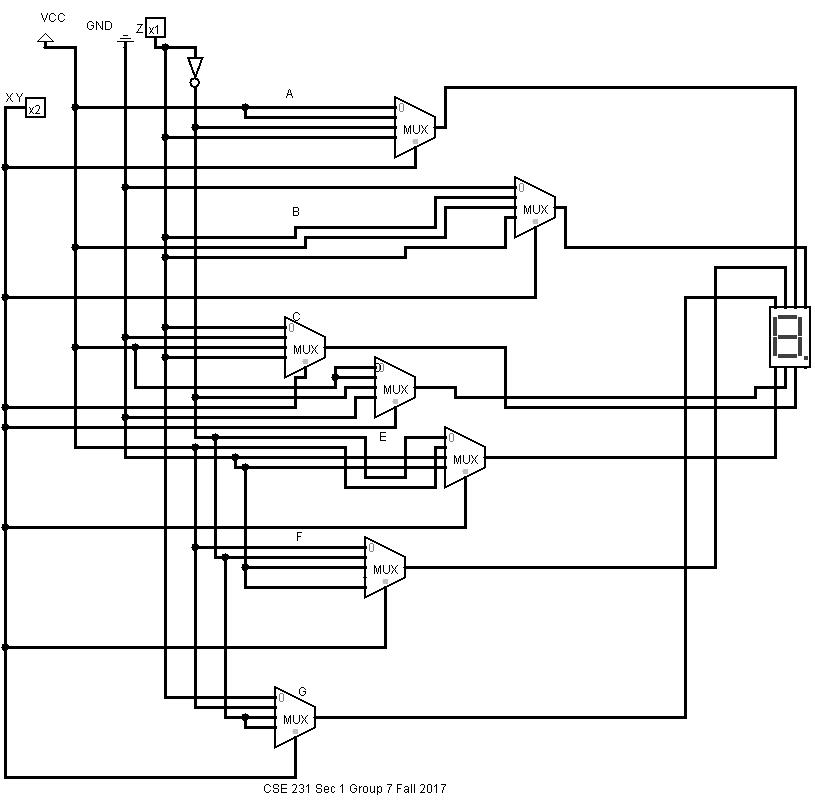
|  |  |  |  |
| --- | --- | --- | --- |
| X | Y | Z | d |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 |

|  |  |  |  |
| --- | --- | --- | --- |
| X | Y | Z | e |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 |

|  |  |  |  |
| --- | --- | --- | --- |
| X | Y | Z | f |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 |

|  |  |  |  |
| --- | --- | --- | --- |
| X | Y | Z | g |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

**Logic Diagram**



**Circuit Cost**

Literal cost :

Gate input :

Gate input with inverter :

Total number of apparatus : Multiplexers – 7 , Inverter – 1 ,Ground -1, Power -1,Pin-2

**Decoder :**

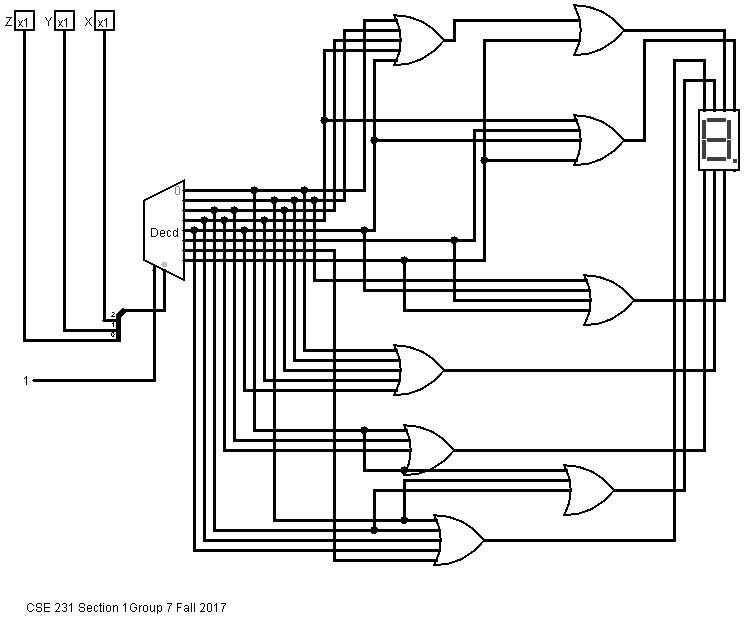
|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | a | b | c | d | e | f | g |
| D0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| D1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| D2 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| D3 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| D4 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| D5 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| D6 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| D7 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |

**Functional Operation :**

For respective 7 segment display , the necessary minterms are added through an OR gate and this output is connected in the display segments.

The enable switch is kept in active high mode and the inputs are connected through the selector bit input

**Logic Diagram :**



**Circuit Cost**

Literal cost :

Gate input :

Gate input with inverter :

Total number of apparatus :

Basic Gates

We will reduce the number of gates using K map over the table here .

A

|  |  |  |  |
| --- | --- | --- | --- |
|  |  |  |  |
|  |  |  |  |

B

|  |  |  |  |
| --- | --- | --- | --- |
|  |  |  |  |
|  |  |  |  |

C

|  |  |  |  |
| --- | --- | --- | --- |
|  |  |  |  |
|  |  |  |  |

D

|  |  |  |  |
| --- | --- | --- | --- |
|  |  |  |  |
|  |  |  |  |

E

|  |  |  |  |
| --- | --- | --- | --- |
|  |  |  |  |
|  |  |  |  |

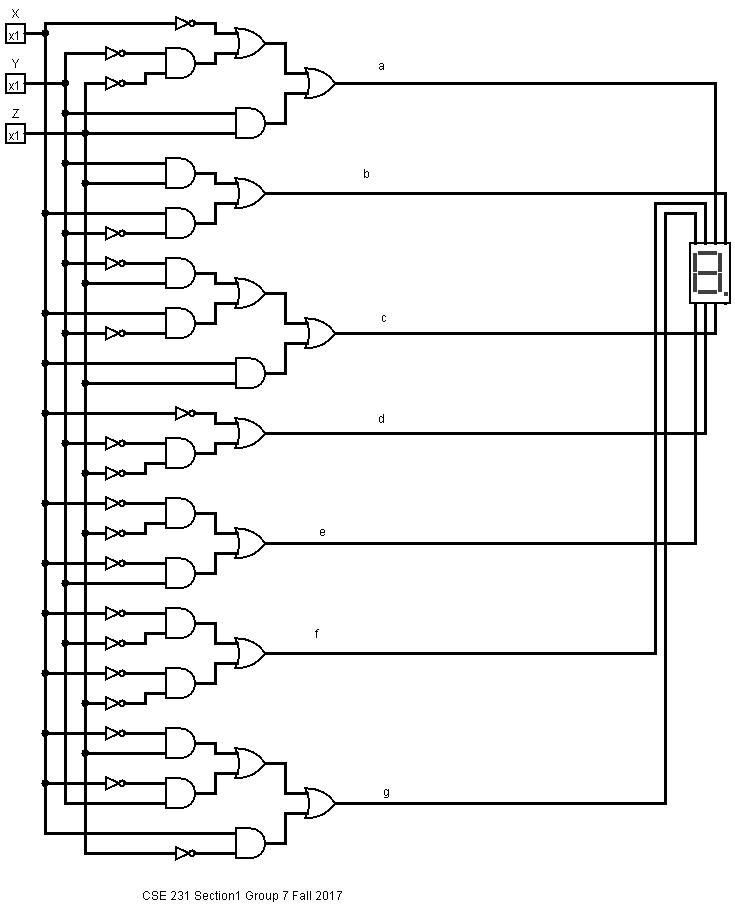
F

|  |  |  |  |
| --- | --- | --- | --- |
|  |  |  |  |
|  |  |  |  |

G

|  |  |  |  |
| --- | --- | --- | --- |
|  |  |  |  |
|  |  |  |  |

**Logic Diagram :**



**Circuit Cost for Basic Gates**

Literal cost :

Gate input :

Gate input with inverter :

Total number of apparatus :

**Circuit Cost for Universal gates**

Literal cost :

Gate input :

Gate input with inverter :

Total number of apparatus :

**Universal gates :**

