TASK : 08

cont. Embedded Systems Concepts

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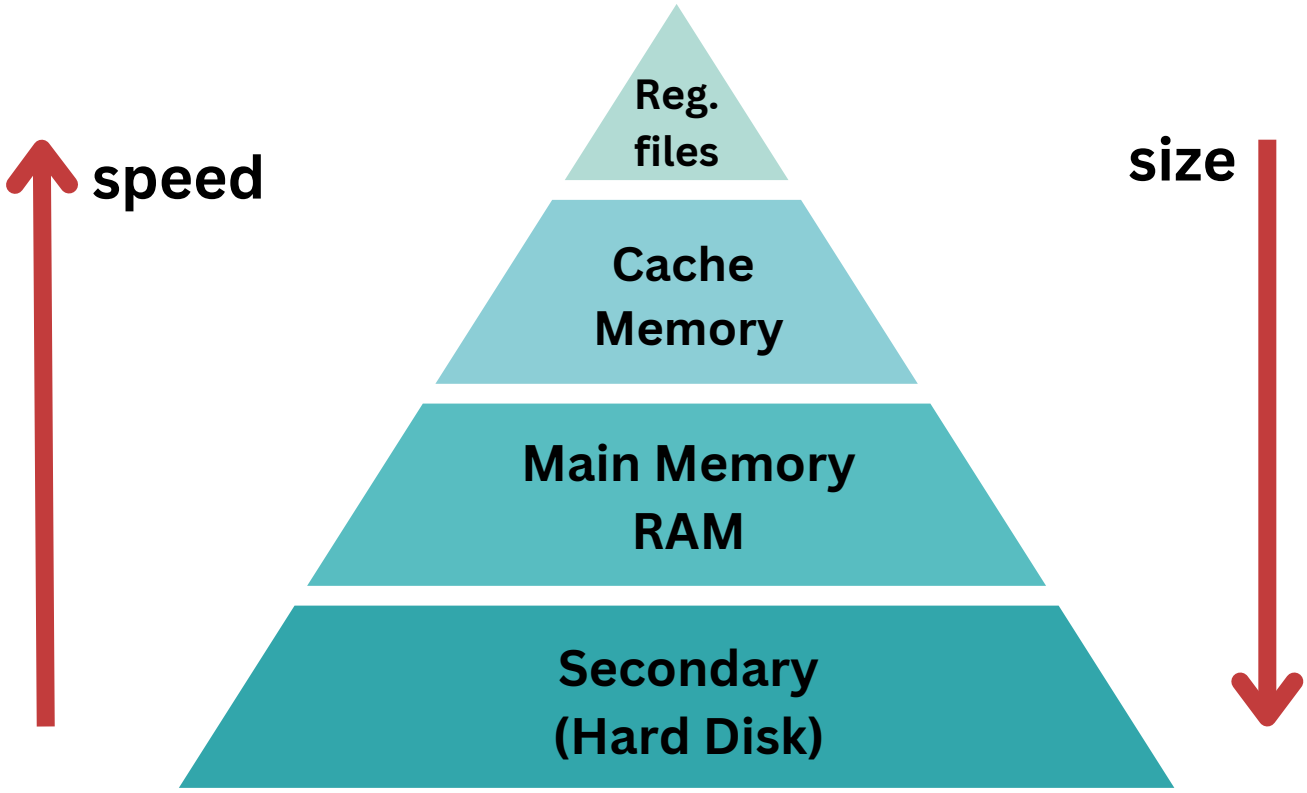
Cache Memory:

- Cache memory is a small, high-speed type of volatile computer memory that is used to temporarily store frequently accessed data and instructions.
- There are levels of cache: once it more near to core, it has more speed.

CPU ⟷ Cache ⟷ RAM

Cache Coherence:

It protocols ensure that the data stored in different caches remains consistent across all cores or processors.



FPU:

Floating Point Unit is a specialized hardware component that is dedicated to performing arithmetic and mathematical operations on floating point numbers.

MPU:

Memory Protection Unit, Its primary function is to protect the memory regions of a system by controlling the access permissions for different areas of memory.

MMU:

Memory Management Unit, that is responsible for translating virtual memory addresses used by the CPU into physical memory addresses. The MMU plays a crucial role in modern computer systems by enabling the efficient use of memory resources and providing memory protection and virtual memory support.

Types of Architecture:

VON NEUMANN

- **In the Von Neumann architecture, both instructions and data are stored in the same memory space.**
- **The CPU accesses instructions and data from memory sequentially, fetching instructions one after another.**
- **It employs a single shared bus for both data and instructions, which can lead to potential bottlenecks and limited parallelism.**

HARVARD

- In Harvard architecture, separate memory spaces are used for instructions and data, providing simultaneous access to both.
- This separation allows the CPU to fetch instructions and data concurrently, which can improve performance by reducing bottlenecks.
- It typically employs separate buses for instructions and data, enhancing parallelism and throughput.

I/O in Harvard Architecture:

1- Memory Mapped

- I/O devices are treated as if they were memory locations.
- The same address space is used for both memory and I/O devices, with each device assigned a range of addresses.
- When the CPU needs to perform I/O operations, it accesses the I/O device by reading from or writing to specific memory addresses associated with that device.

2- Port Mapped

- In port-mapped I/O, separate address spaces are used for memory and I/O devices.
- I/O devices are accessed through dedicated I/O ports, which are separate from memory addresses.
- Special instructions or CPU commands are used to access I/O ports, distinct from memory access instructions.

Pipeline:

- It refers to a technique used to enhance the performance and efficiency of a processor by breaking down the execution of instructions into a series of sequential stages. Each stage in the pipeline performs a specific operation on the instruction or data, and multiple instructions are processed simultaneously, with each instruction advancing through the pipeline stages.
- RISC is supported pipeline but CISC doesn't.

MIPS:

Million Instructions Per Second, can be used as a unit of measurement to indicate the computing performance of a system, specifically the number of instructions a processor can execute in one second. However, this usage is less common in contemporary discussions compared to its other meanings.

Clock:

It represented as a square wave, is a periodic electrical signal used in digital systems to synchronize the operation of various components, such as processors, memory units, and input/output devices.

Clock Systems

Electrical

RC - Oscillator

EX: Timer 555

Mechanical

Material

- **Ceramic Resonate**
- **Crystal Oscillator**

	RC	Ceramic	Crystal
Cost	Low	In - Between	High
Accuracy	Low	In - Between	High
Setting Time	High	In - Between	Low
Noise Immunity 1- Temp.	Low	High	High
2- EMI	Low	High	High
3- Vibration	High	Low	Low

Bus bridges:

They are hardware components used in computer systems to connect two or more separate buses, allowing them to communicate with each other. These bridges play a crucial role in system architecture by enabling interoperability between different types of buses, which may have different protocols, speeds, or architectures.

Hardware Parts:

1- Master

- **The master device is typically the primary or controlling component in a system.**
- **It often initiates and coordinates actions or operations performed by other devices or components.**
- **The master device may have priority access to system resources and can often control the timing and sequence of operations.**

2- Slave

- **The slave device is typically subordinate to the master device and follows the instructions or commands issued by the master.**
- **It may perform specific tasks or functions in response to commands received from the master device.**
- **The slave device may have limited autonomy and relies on the master for coordination and control.**