CSE306 (Computer Architecture Sessional)
July 2023 Term
All Lab Section

December 19, 2023

1 Problem Description

In this assignment, you are required to design a floating point adder circuit which takes two floating points as inputs and provides their sum, another floating point as output. Each floating point will be 32 bits long with following representation:

Sign	Exponent	Fraction
1 Bit	11 Bits	20 Bits

- You have to implement your design in any simulator software of your choice. Please note that, if your chosen simulator does not provide support for 32-bit ALU, you can construct one by cascading a number of smaller ALUs. Moreover, since construction of ALU is not the major focus of this assignment, you can take help from the Internet or other sources (or even use someone else's implementation) for the 32 bit ALU part only.
- The shifter circuit provided by the simulator software tool may be used as needed. Alternatively, you may implement them yourselves.
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- I . Ro (There is no need to involve clock pulses if you do one-step rounding. Alternatively, you may decide to do it in one clock pulse.)
- The rest of the circuit design and implementation must be done by you.
- It is advised that you prepare separate sub modules instead of one complex circuit.

For this assignment, you will work in a group (same as the group for assignment on ALU). T
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2 Submission

Deadline For all sections: January 14, 2023 (Sunday) at 11:55 PM.
A submission link will be opened on Moodle for submitting your simulation. Make a folder containing all your simulation project files, zip it, and submit it following the naming format. The naming format should be your section name followed by your group id (e.g., $B1\_Group7$). Please ensure a single submission from each group (only a single member of the group should submit).