Xingyu (Tom) Wang

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EDUCATION

University of British Columbia Vancouver, Canada

Bachelor of Applied Science in Computer Engineering, CGPA: 4/4.33 *08/2021 – 09/2025(expected)*

- Related Courses: **Computer Architecture**, **Digital and Microsystem design**, **Computing System**, Error Control Coding, Algorithm and Data structure, Machine Learning, Software Construction

SKILLS SUMMARY

Programming Languages	Engineering skills	Programming skills
• Java, Python, C, C++	• FPGA, Digital design	• Software Hardware Interface
• System Verilog, Assembly	• Microprocessor and system buses	• Embedded Programming
• Bash, Makefile	• Memory Hierarchy	• Deep Learning Algorithms
• Latex, Markdown	• Cache and Page Prefetching	• Git, GDB, Linux environment

WORK EXPERIENCE

Full-time Student Research Assistant *May, 2024 – Aug, 2024*

UBC Systopia Lab *Vancouver, BC*

- **Aim**: Investigate the applicability of the Learned Relaxed Belady (LRB) machine-learning model for cache and page pre-fetching.
- **Methods**: Collect SPEC 2017 traces with PIN, and apply Learning Memory Access Pattern methods.
- **Progress**: Tune LSTM model Add Attention Layer. Analyze trace. Experiment with heuristic methods. Hardware-Software Codesign for Prefetching
- **Supervision under**: Shaurya Patel, Prof. Alexandra Fedorova.

PROJECTS

Microsystem Design with Microprocessor *Jan 2024 - April 2024*

- Build **memory, data bus, various I/O** around a M68K CPU on FPGA. Interact with CPU using embedded C programming.
- Implemented components include **DRAM controller, Cache Controller, SPI, Canbus, I2C, ADC/DAC**, and Simple RTOS usage with multi-threading and priority interrupts.
- Integrate the above components with VGA and Voice modules, and map addresses accordingly both in RTL design and C programming to produce a Tetris game with the M68K CPU.

ECC Performance Analysis on FPGA *Mar 2024 – April 2024*

- RTL design of simple decoder and encoder for both **Hamming** code and **LDPC** code on FPGA.
- Analyze and compare performance on decode/encode cycle, combinational logic length, maximal frequency, gate usage, efficiency, and ease of use on DE1-SOC FPGA board.

RC4 Cracking on FPGA *June 2023*

- Encryption and Decryption of RC4 using System Verilog on FPGA. Leveraging **on-chip memory** with multiple **FSM**.
- Multi-core system to brute force cracking RC4 Encryption. Parallel processing to accelerate execution. Communication between cores. The number of cores can adapt according to the Hardware Resources.

Supervised Learning on Audio Files *Nov 2023 – Dec 2023*

- Collect Audio files, and process with Fourier Transform to get frequency data from Audio waveform. Apply PCA to reduce the dimension. Label data
- Supervised learning with Support Vector Machine and Neural Network, comparing the performance, memory usage, and efficiency of training and predicting.

AWARDS

- Dean’s Honors List 2021 - 2024
- NSERC Awards May 2024