Summary of ELEC 402

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1 Fabrication of ICs

1.1 Digital Circuits

1.1.1 Packaging

- Packaged or covered with epoxy resin (plastic) or ceramic
- Wire bonding: connect the chip to the package
- PADS: connect the package to the PCB

IO buffer: connect the chip to the package

- change the voltage level
- remove noise
- improve rise/fall time
- protect the chip from ESD
- provide a constant current source

Driving PADs:

- connect the package to the PCB
- provide a constant current source
- remove noise
- protect the chip from ESD

1.2 Wafer Fabrication

Built in a clean room.

Wafer: a thin slice of semiconductor material.

- Silicon
- Gallium Arsenide
- Silicon Carbide

Growing a Silicon Crystal:

- Czochralski process
- Float zone process
- Epitaxial growth

1.3 MOSFET

MOSFET (Metal Oxide Semiconductor Field Effect Transistor):

- NMOS: n-channel MOSFET
- PMOS: p-channel MOSFET
- CMOS: complementary MOSFET

1.4 Lithography

- Photolithography: use light to transfer a geometric pattern from a photomask to a light-sensitive chemical (photoresist) on the substrate.
- Etching: remove the unwanted material
- Ion implantation: change the electrical properties of the material

1.4.1 N/P-Well CMOS Process

2 RLC Circuits

2.1 Circuits Review

2.1.1 Resistor

- $V = IR$
- $P = IV = I^2R = \frac{V^2}{R}$

2.1.2 Capacitor

- $I = C\frac{dV}{dt}$
- $V = \frac{1}{C}\int Idt$
- $P = IV = CV\frac{dV}{dt} = \frac{V^2}{R}$

2.1.3 Inductor

- $V = L\frac{dI}{dt}$
- $I = \frac{1}{L}\int Vdt$
- $P = IV = LI\frac{dI}{dt} = \frac{I^2}{R}$

2.2 RLC Circuits

2.2.1 Series RLC Circuit

Wires have resistance, inductance and capacitance. Thus the circuit is not ideal.

For a change of voltage to propagate through the wire, it takes time.

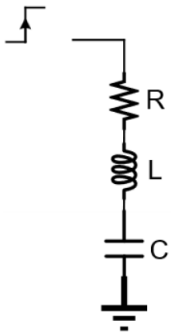

Figure 1: RLC Circuit

2.2.2 Rise/Fall Time

Rise time is the time it takes for the voltage to rise from 10% to 90% of the final value.

Fall time is the time it takes for the voltage to fall from 90% to 10% of the final value.

If there is no inductance, then the time of fall $t_f = RC \times \ln(9) = 2.2RC$.

Let $\tau = RC$, then $t_f = 2.2\tau$. If τ is too large, the signal will converge given a fluctating input since it never reaches the final value before the next fluctuation.

3 MOSFET

3.1 Structure

The given image shows a MOSFET with P-type boday and N-type source and drain. This is a NMOS transistor. Voltage applied to gate will allow current to flow from source to drain.

- **Polysilicon**: Silicon formed from many small silicon crystals.
- **Gate Oxide**: Insulating layer between the gate and the channel.
- Source and Drain are doped with N-type impurities. PMOS has P-type impurities with body as N-type.
- **Bulk**: Body of the transistor.

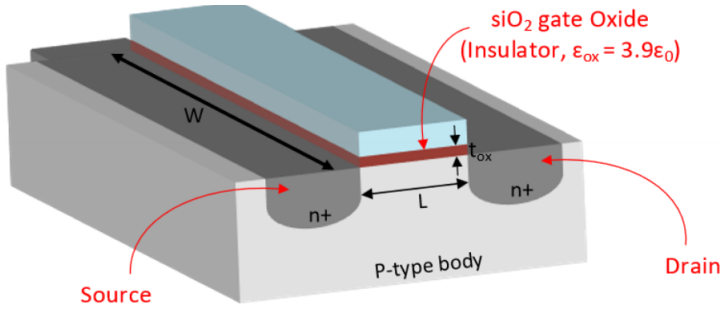

Figure 2: MOSFET

3.2 NMOS and PMOS

Drain-Source current is controlled by the gate-source voltage.

- **NMOS**: When $V_{GS} > V_{th}$, the transistor is on. When $V_{GS} < V_{th}$, the transistor is off.
- **PMOS**: When $V_{GS} < V_{th}$, the transistor is on. When $V_{GS} > V_{th}$, the transistor is off.

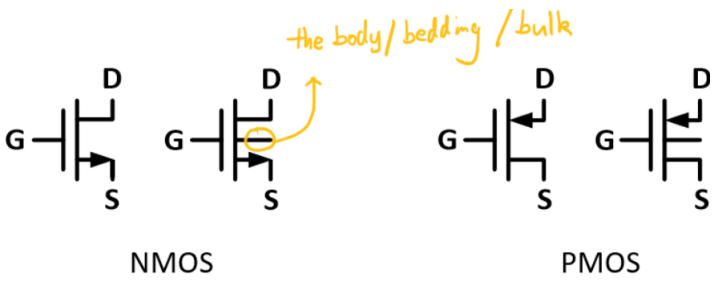

Figure 3: MOSFET