

Summary of ELEC 402

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1 Fabrication of ICs

1.1 Digital Circuits

1.1.1 Packaging

- Packaged or covered with epoxy resin (plastic) or ceramic
- Wire bonding: connect the chip to the package
- PADS: connect the package to the PCB

IO buffer: connect the chip to the package

- change the voltage level
- remove noise
- improve rise/fall time
- protect the chip from ESD
- provide a constant current source

Driving PADS:

- connect the package to the PCB
- provide a constant current source
- remove noise
- protect the chip from ESD

1.2 Wafer Fabrication

Built in a clean room.

Wafer: a thin slice of semiconductor material.

- Silicon
- Gallium Arsenide
- Silicon Carbide

Growing a Silicon Crystal:

- Czochralski process
- Float zone process
- Epitaxial growth

1.3 MOSFET

MOSFET (Metal Oxide Semiconductor Field Effect Transistor):

- NMOS: n-channel MOSFET
- PMOS: p-channel MOSFET
- CMOS: complementary MOSFET

1.4 Lithography

- Photolithography: use light to transfer a geometric pattern from a photomask to a light-sensitive chemical (photoresist) on the substrate.
- Etching: remove the unwanted material
- Ion implantation: change the electrical properties of the material

1.4.1 N/P-Well CMOS Process

2 RLC Circuits

2.1 Circuits Review

2.1.1 Resistor

- $V = IR$
- $P = IV = I^2R = \frac{V^2}{R}$

2.1.2 Capacitor

- $I = C \frac{dV}{dt}$
- $V = \frac{1}{C} \int I dt$
- $P = IV = CV \frac{dV}{dt} = \frac{V^2}{R}$

2.1.3 Inductor

- $V = L \frac{dI}{dt}$
- $I = \frac{1}{L} \int V dt$
- $P = IV = LI \frac{dI}{dt} = \frac{I^2}{R}$

2.2 RLC Circuits

2.2.1 Series RLC Circuit

Wires have resistance, inductance and capacitance. Thus the circuit is not ideal.

For a change of voltage to propagate through the wire, it takes time.

2.2.2 Rise/Fall Time

Rise time is the time it takes for the voltage to rise from 10% to 90% of the final value.

Fall time is the time it takes for the voltage to fall from 90% to 10% of the final value.

If there is no inductance, then the time of fall $t_f = RC \times \ln(9) = 2.2RC$.

Let $\tau = RC$, then $t_f = 2.2\tau$. If τ is too large, the signal will converge given a fluctuating input since it never reaches the final value before the next fluctuation.

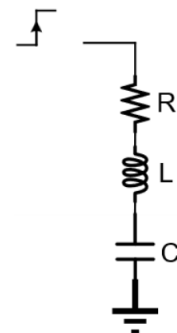


Figure 1: RLC Circuit

3 MOSFET

3.1 PN Junction Diode

- **P-type:** Doped with acceptor impurities. Holes are majority carriers. Electrons are minority carriers.
- **N-type:** Doped with donor impurities. Electrons are majority carriers. Holes are minority carriers.
- **Depletion Region:** Region where the majority carriers are depleted. The region is charged. Depleted means the region is charged by the ions.

3.2 Structure

The given image shows a MOSFET with P-type body and N-type source and drain. This is a NMOS transistor. Voltage applied to gate will allow current to flow from source to drain.

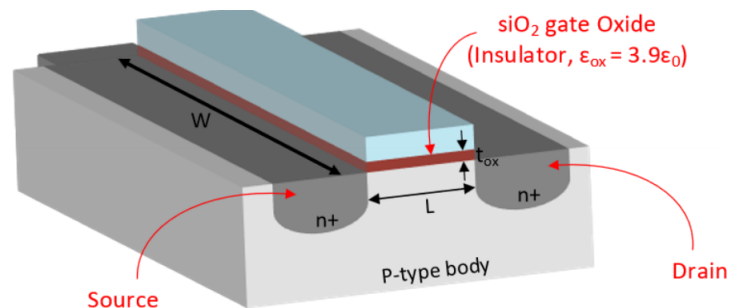


Figure 2: MOSFET

- **Polysilicon:** Silicon formed from many small silicon crystals.
- **Gate Oxide:** Insulating layer between the gate and the channel.
- Source and Drain are doped with N-type impurities. PMOS has P-type impurities with body as N-type.
- **Bulk:** Body of the transistor.

3.2.1 Gate-body Structure

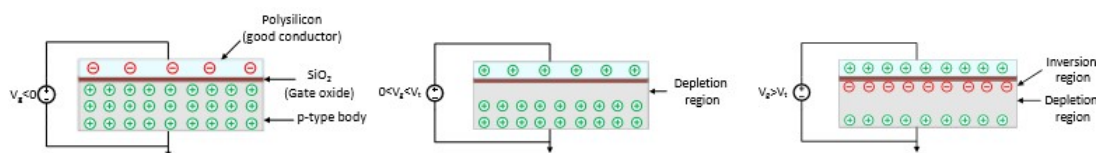


Figure 3: Gate-body Structure

1. Accumulation mode: Gate voltage is negative or zero. Holes are attracted to the gate thus forming a channel. Low resistance.

2. Depletion mode: Gate voltage is positive but less than threshold voltage. Holes are repelled from the gate. High resistance.
3. Inversion mode: Gate voltage is greater than threshold voltage. Electrons are attracted to the gate thus forming holes at the body. Low resistance.

3.3 NMOS and PMOS

Drain-Source current is controlled by the gate-source voltage.

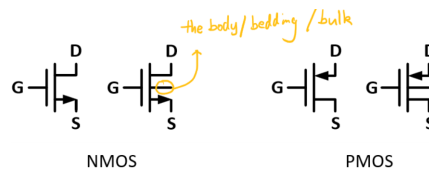


Figure 4: MOSFET

NMOS: When $V_{GS} > V_{th}$, the transistor is on. When $V_{GS} < V_{th}$, the transistor is off.

PMOS: When $V_{GS} < V_{th}$, the transistor is on. When $V_{GS} > V_{th}$, the transistor is off.

3.3.1 nMOS modes

Source and drain are symmetric diffusion terminals. For nMOS, source is the terminal at lower voltage ($V_{ds} > 0$)

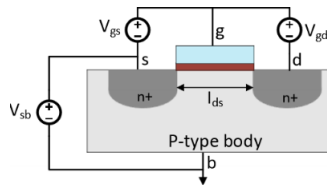


Figure 5: nMOS modes

- Cutoff: $V_{GS} < V_{th}$, $I_{DS} = 0$. It is the depletion mode.
- Triode/Linear: $V_{GS} > V_{th}$, $V_{DS} < V_{GS} - V_{th}$. It is the linear mode.
 - Conductivity is proportional to $V_{GS} - V_{th}$. The larger the $V_{GS} - V_{th}$, the larger the conductivity, the smaller the resistance.
 - Current flow from D to S. Electrons flow from S to D.
- Saturation: $V_{GS} > V_{th}$, $V_{DS} > V_{GS} - V_{th}$. It is the saturation mode.
 - Channel is pinched off at the drain end. The current is independent of V_{DS} .

3.4 MOSFET Characteristics

Carrier velocity is proportional to the electric field. $v_d = \mu_n E$. μ_n is the carrier mobility of the electrons.

Electric field is proportional to the voltage gradient. $E = \frac{dV}{dx}$. Can approximate as $E = \frac{V}{L}$ where L is the length of the channel.

Thus time it takes for the electron to travel from source to drain is $t = \frac{L}{v_d} = \frac{L}{\mu_n E} = \frac{L^2}{\mu_n V}$.

C_{ox} is the capacitance of the oxide layer. $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$. With W as the width of the channel, L as the length of the channel, $C_{ox} = \frac{\epsilon_{ox}WL}{t_{ox}}$.

Let $\beta = \mu_n C_{ox} \frac{W}{L}$ be the gain factor.

- Cut-off: $I_{DS} = 0$.
- Triode: $I_{DS} = \beta(V_{GS} - V_{th} - \frac{V_{DS}}{2})V_{DS}$.
- Saturation: $I_{DS} = \frac{\beta}{2}(V_{GS} - V_{th})^2$. independent of V_{DS} .

For a fixed V_{ds} and $V_{GS} > V_{th}$, the current is proportional to:

- L : The length of the channel. The longer the channel, the longer the time it takes for the electron to travel from source to drain.
- W : The width of the channel. The wider the channel, the more electrons can flow through.
- V_{th} : The threshold voltage. The larger the threshold voltage, the larger the current.
- ϵ_{ox} : The permittivity of the oxide layer. The larger the permittivity, the larger the current.
- t_{ox} : The thickness of the oxide layer. The thinner the oxide layer, the larger the current.
- μ_n : The carrier mobility of the electrons. The larger the carrier mobility, the larger the current.

$$- \mu_n = 500 \text{cm}^2/\text{V} \cdot \text{sec} \approx 2.5\mu_p. \mu_p = 180 \text{cm}^2/\text{V} \cdot \text{sec}.$$

- Thus need to increase the size of pmos to match the current of nmos.

For small V_{DS} , the transistor is viewed as a linear resistor.

$$R_{on} = \frac{1}{\beta(V_{GS} - V_{th})}.$$

3.4.1 Region of Operation

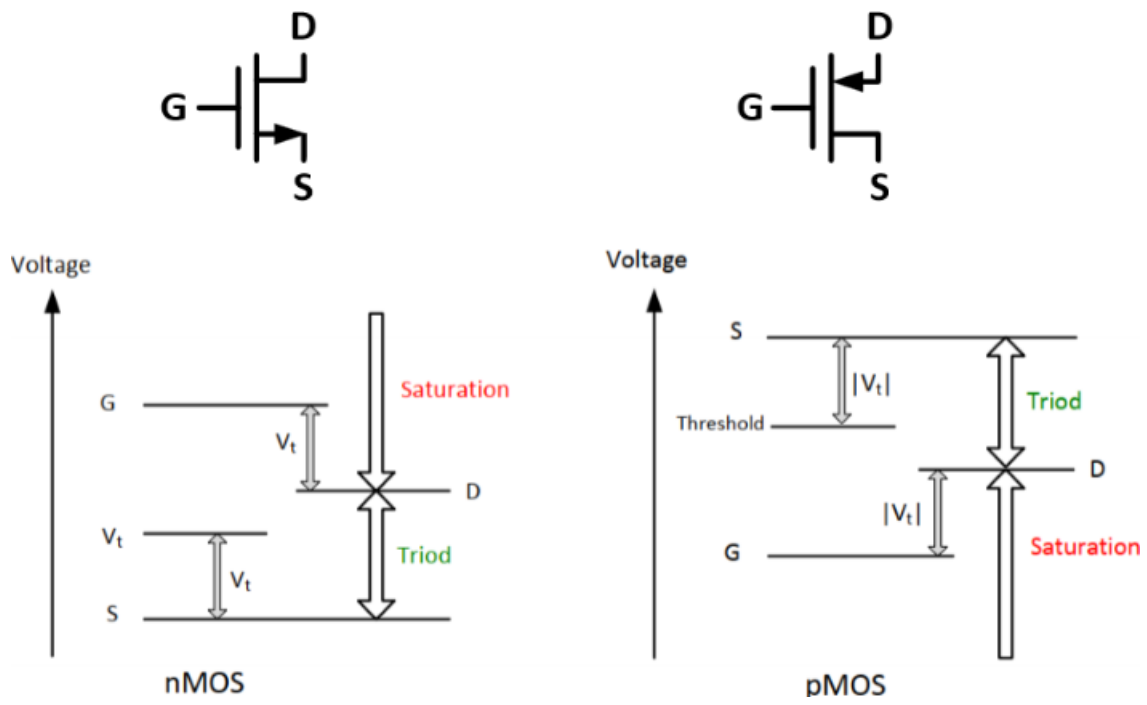


Figure 6: Region of Operation