Challenge_0007: Pipelined RV32IMC Processor

The purpose of this challenge is to design, implement, and verify a complete pipelined RV32I processor core in SystemVerilog. This is a straight extension of the **rv32i** processor that we designed in **challenge_0005**. Except top module name (which will now be **rv32imc_top**), **Everything else stays the same**: same ports as before, same tracer usage, same local and evaluation flows, same submission format, same disqualifiers. The top module name will now be **rv32imc_top**. Your job is simply to add full support for **RV32M** (MUL/MULH/MULHSU/MULHU/DIV/DIVU/REM/REMU) and **RV32C** (all compressed 16-bit instructions) on top of your existing RV32I pipeline. No interface changes, no new signals, no alternate build flags.

- **Scope:** RV32I **+ M + C** fully supported. Previously excluded ops (ECALL, EBREAK, FENCE, FENCE.TSO, PAUSE) remain **illegal**.
- **Reset/Tracer:** Unchanged from Task #1. Keep your tracer exactly as you wired it before.
- **Submission:** Same ZIP with RTL and `rtl.f` at root. No TB/tracer/mem models.
- **Synthesis/Flow:** Same Yosys/OpenLane (sky130A) requirement. Tracer excluded from synthesis as before.
- **Functionality Gate: 100%** match vs Spike required; anything less ⇒ **overall score = 0**.
- **Scoring Weights: Functionality 50%**, **Performance 30%**, **Area 20%**, **Power 0%**.
- **Disqualify if:** Wrong top name/ports, missing (or nonworking) tracer, unsynthesizable RTL, or functionality < 100%.