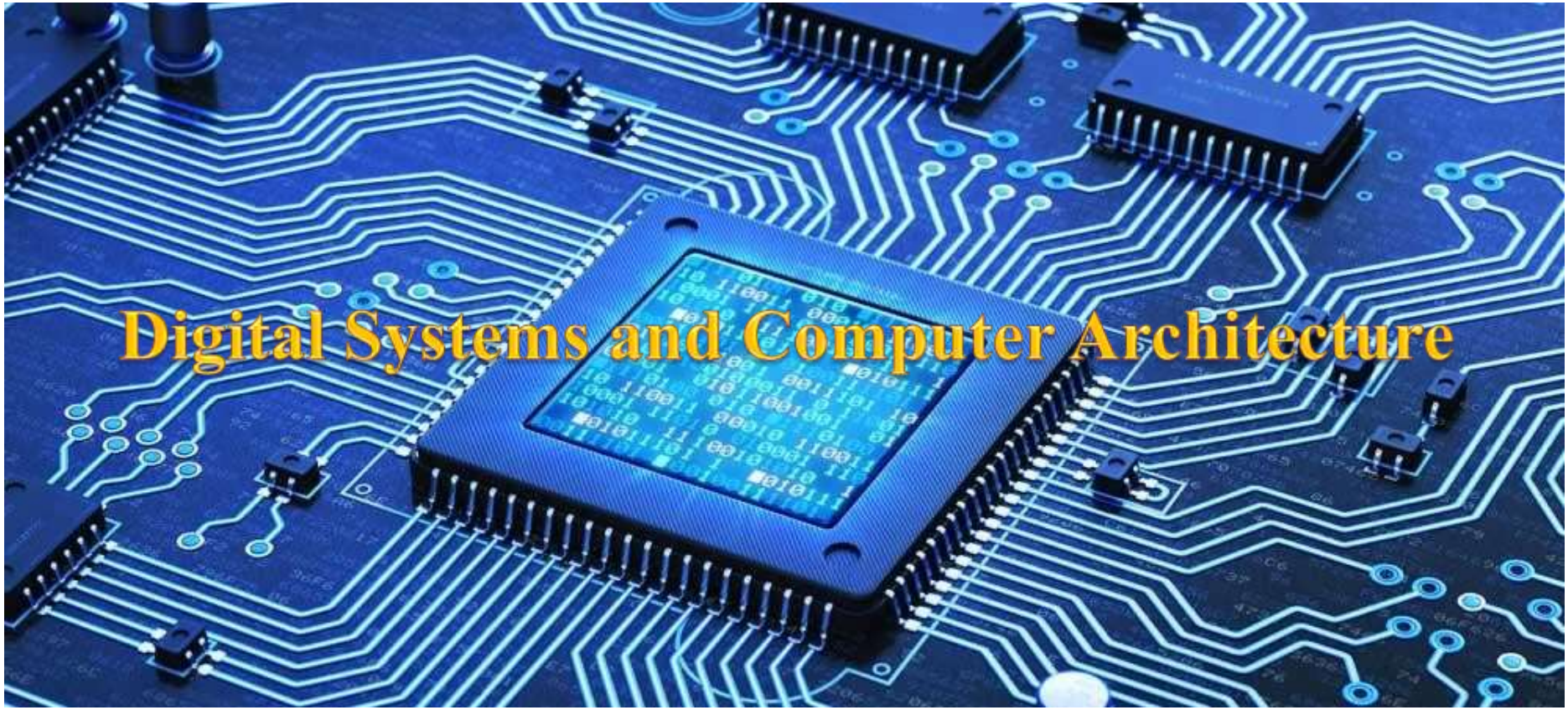


Session 2.12

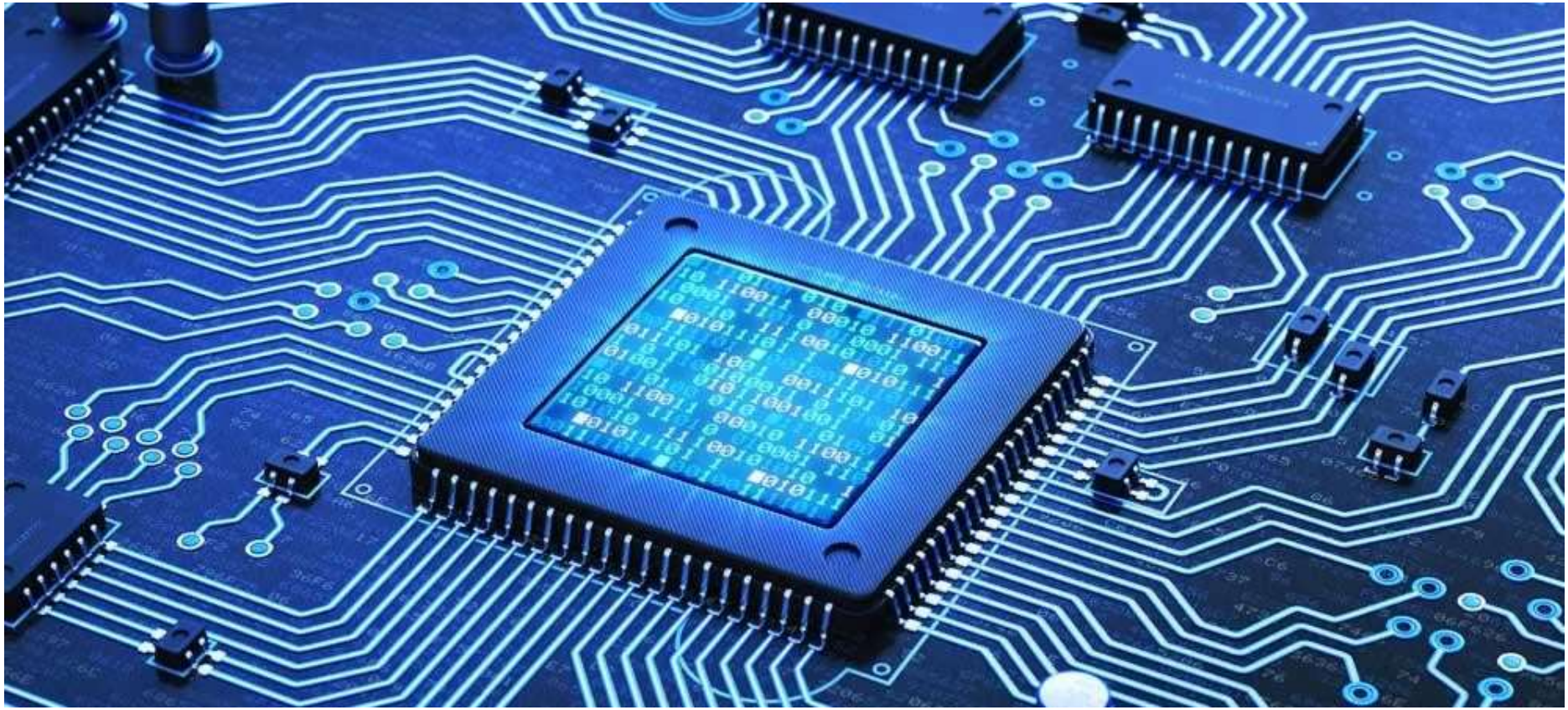
Module 2

Mouli Sankaran

JK and T Flip-flops

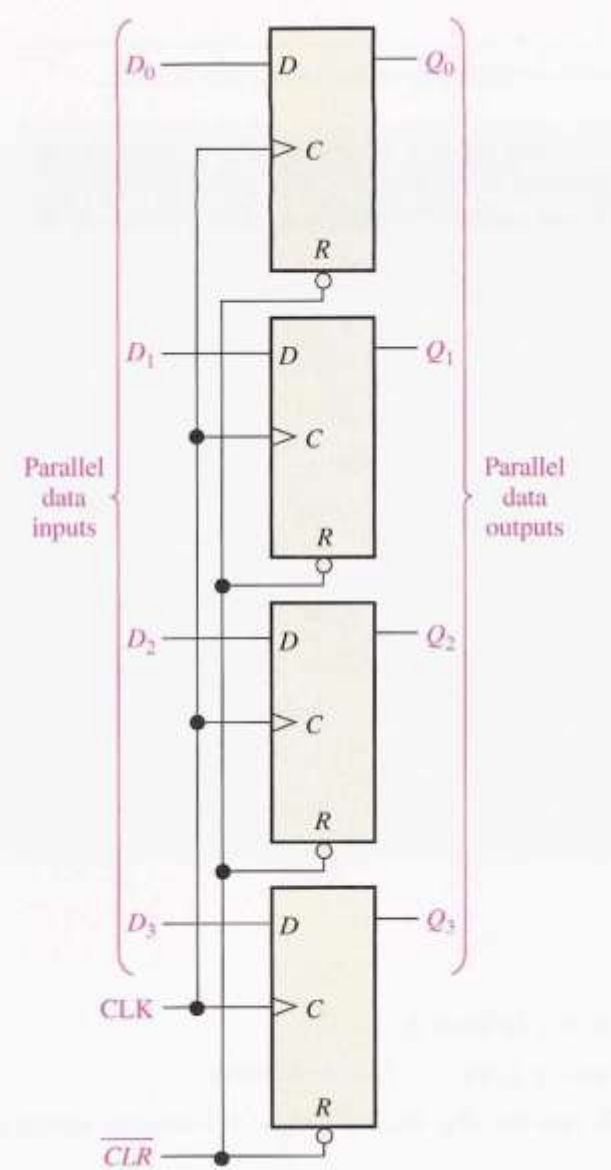
Session 2.12: Focus

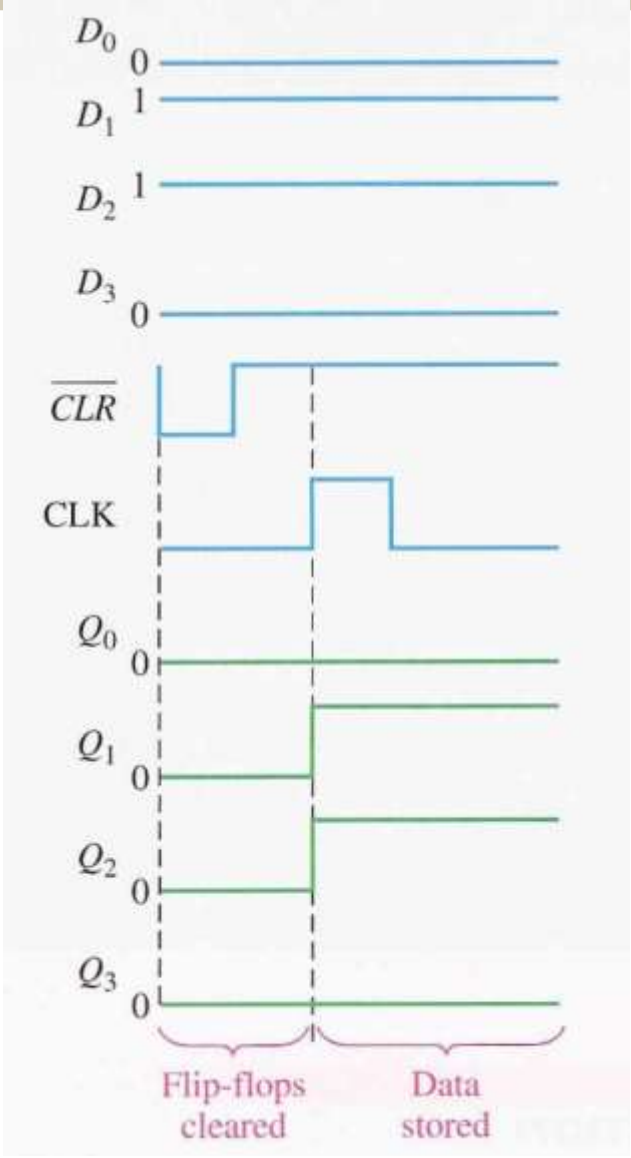
- Applications using D Flip-flop
  - 4-bit Asynchronous Up counter
  - 4-bit Asynchronous Down counter
  - Serial to Parallel Data Converter



Applications using D-Flip-flops

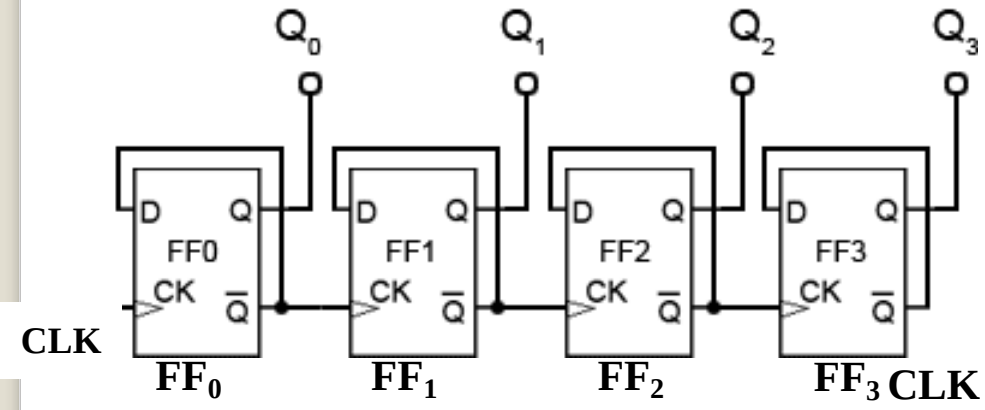
Quiz 1: What does this circuit do?





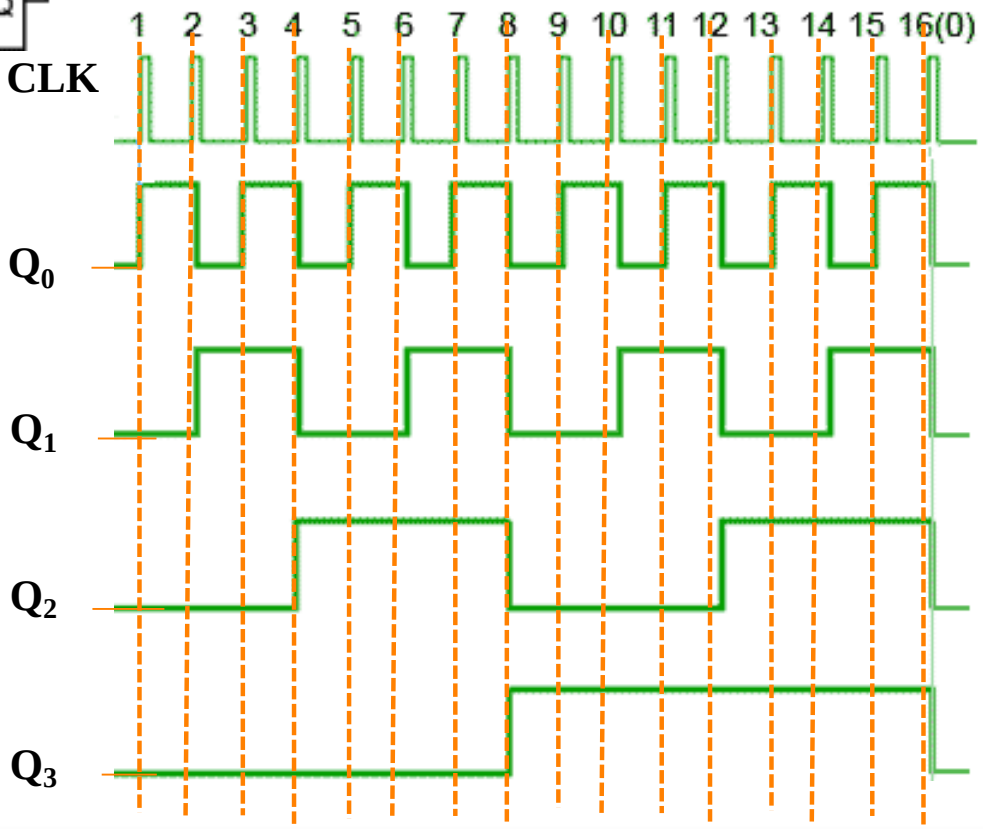
4-bit Data storage

Example 1: 4-bit Asynchronous Up Counter

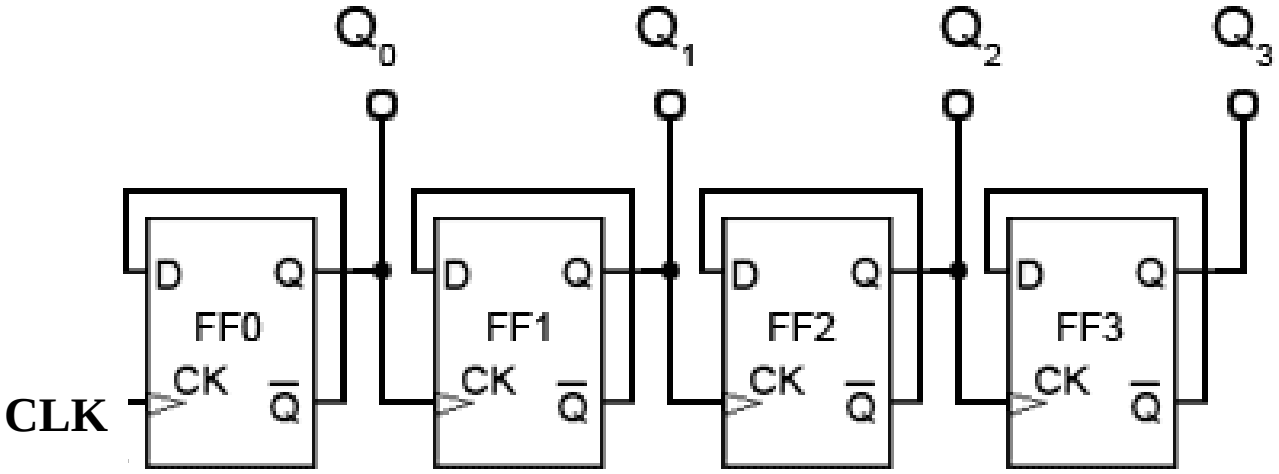


All are **+ve edge triggered D flip-flops**
Initially all **D Flip-flops** are **cleared**
$Q_3Q_2Q_1Q_0 = 0000$
CLK is clock input

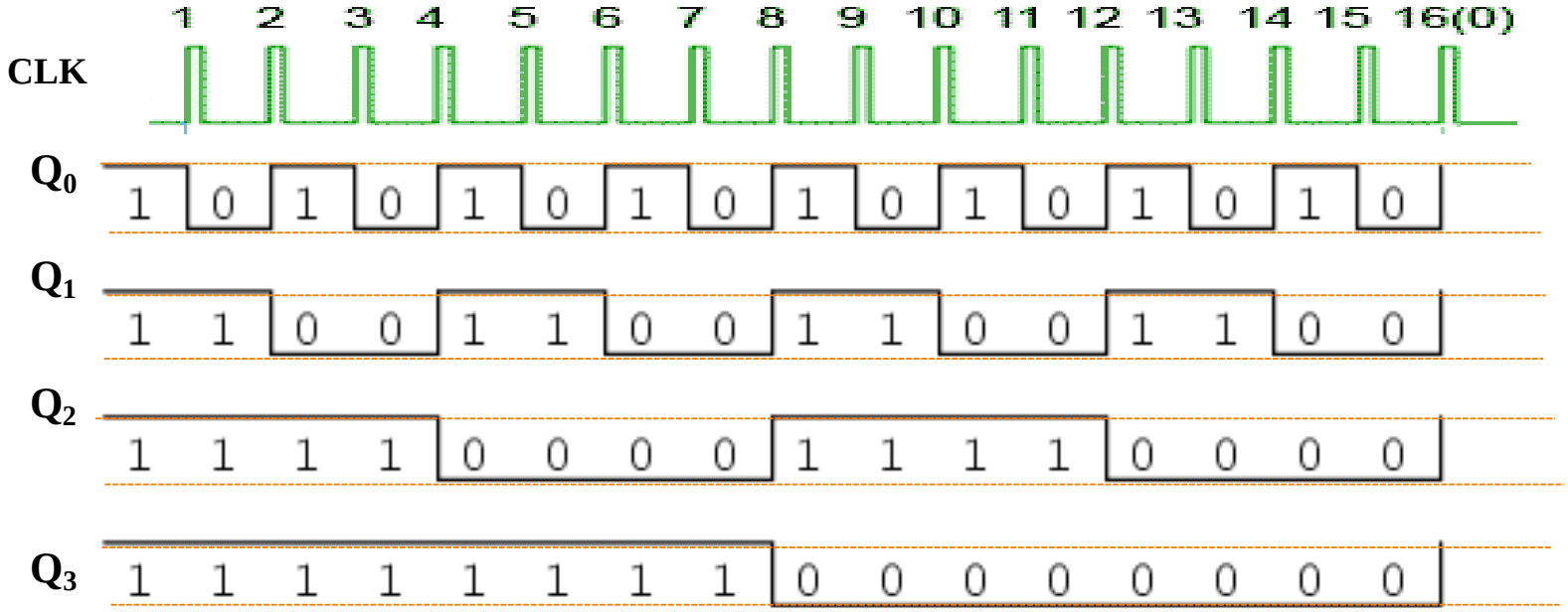
- It **counts** the **clock pulses** from **0000** to **1111**
- **Q'** of **previous** stage is **fed as clock** to the **next** stage **flip-flop**
- Since the **transitions** of **flip-flops** are **not happening** based on the **same clock pulse**, this is an **asynchronous counter**



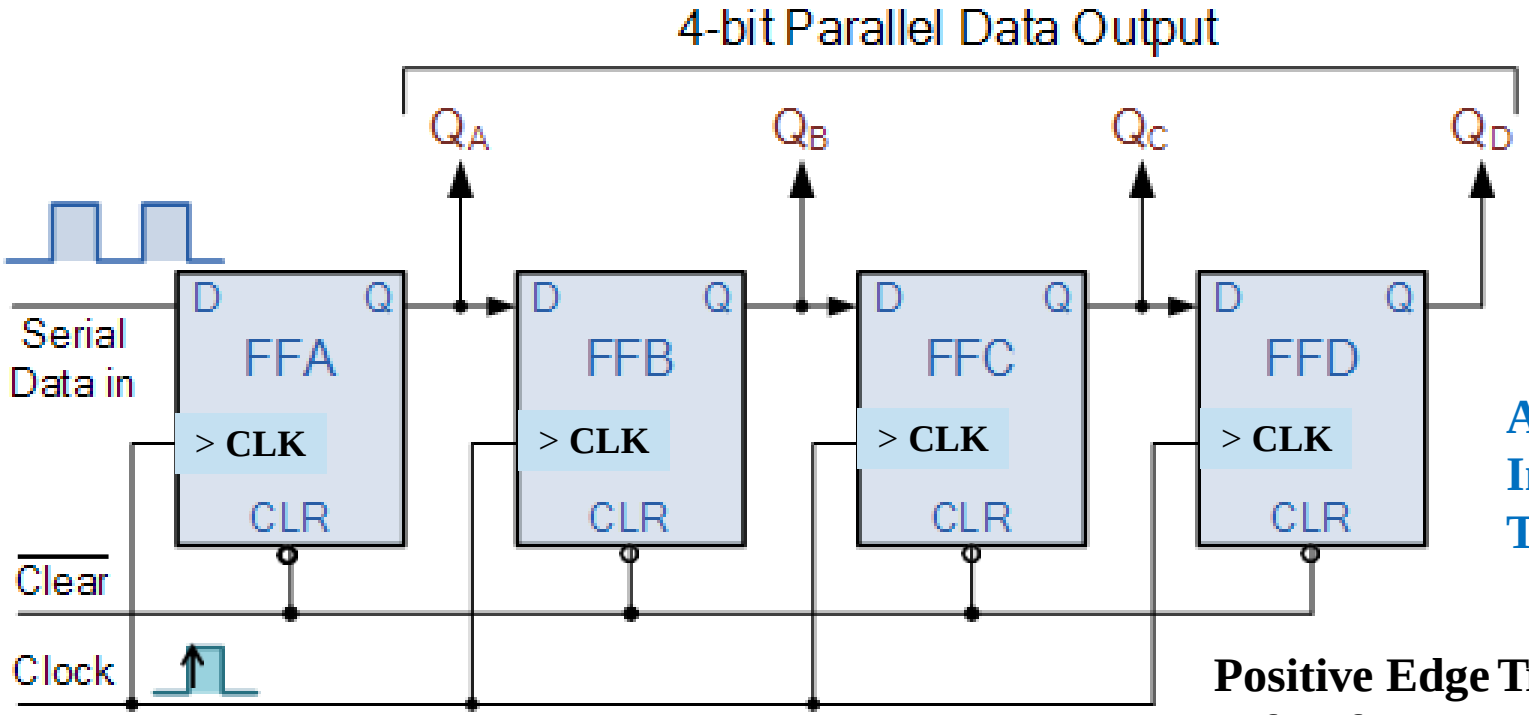
Example 2: 4-bit Asynchronous Down Counter



- **Initially** all **D Flip-flops** are **set** to **1111**
- It **down counts** the **clock pulses** from **1111** to **0000**



Example 3: Serial to Parallel Data Converter



- **Serial to parallel data converter**
- The **serial data** is **shifted in at the positive edge of** every **clock pulse**
- **After four clock pulses** the **parallel data** is available at **$Q_3Q_2Q_1Q_0$**

Session 2.12: Summary

- Applications using D Flip-flop
  - 4-bit Asynchronous Up counter
  - 4-bit Asynchronous Down counter
  - Serial to Parallel Data Converter