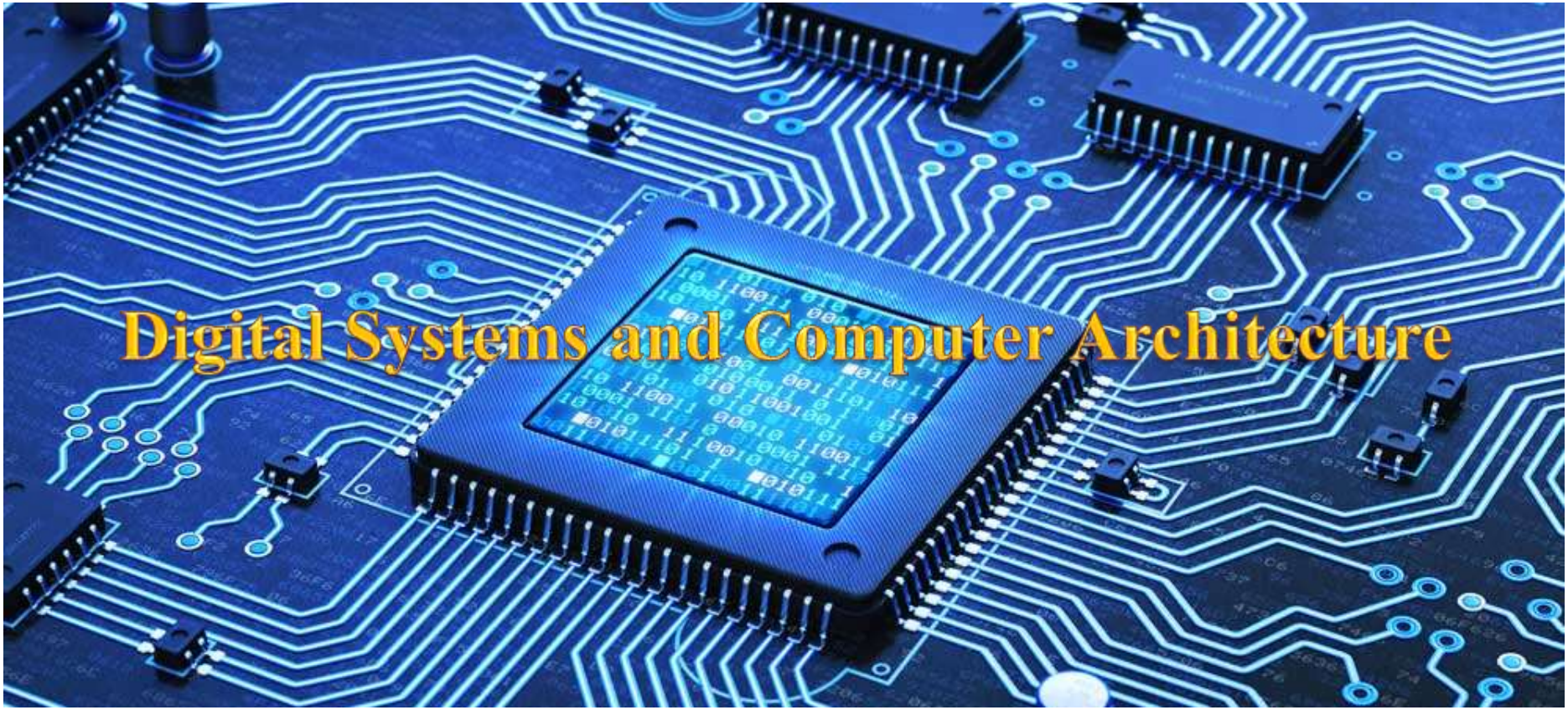


Session 2.11

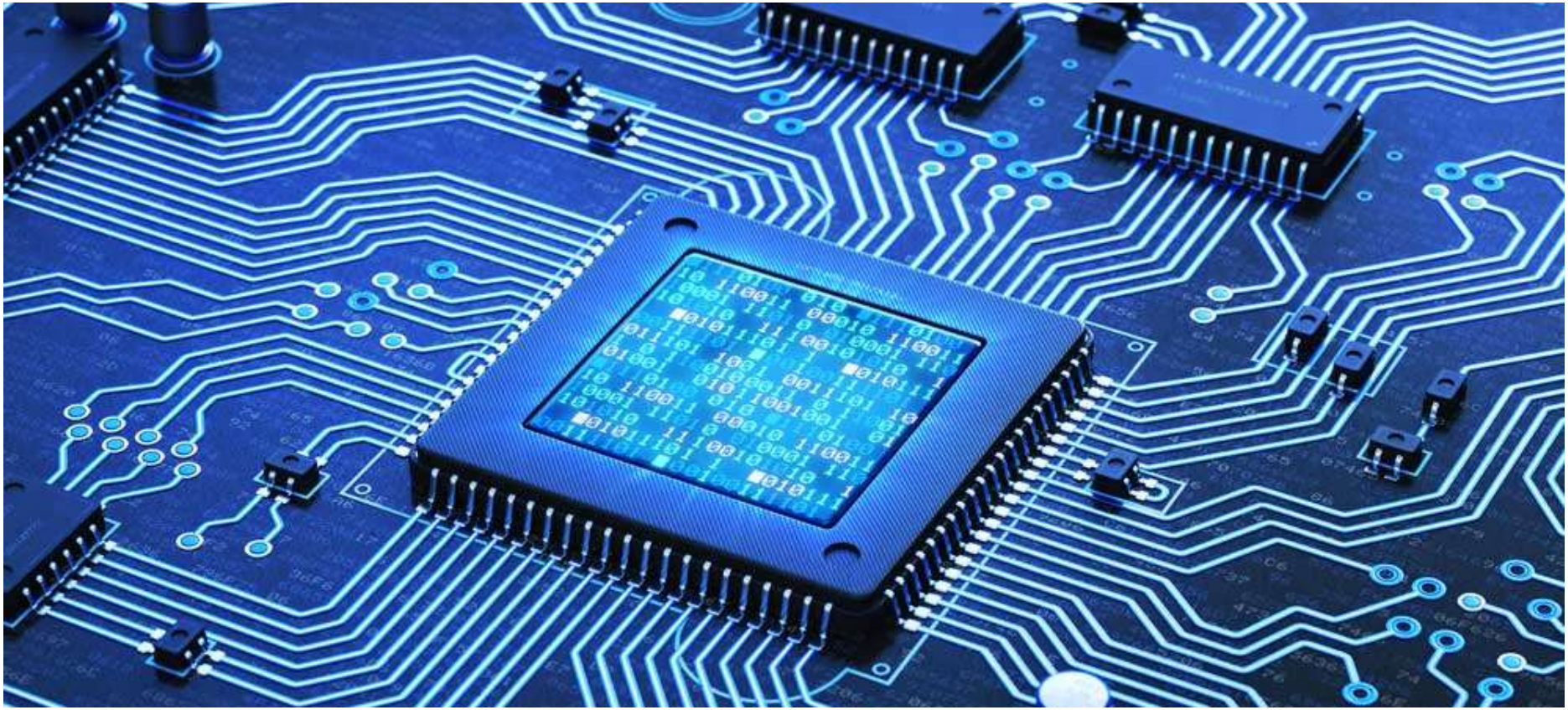
Module 2

Mouli Sankaran

JK Flip-flops

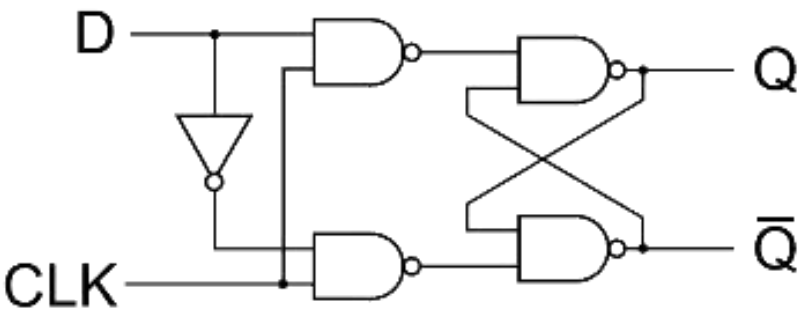
Session 2.11: Focus

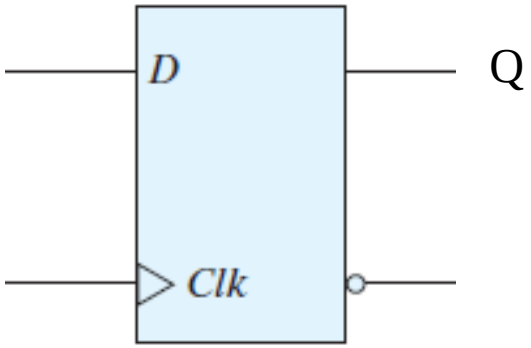
- Latches and Flip-flops
  - Level and Edge-triggered clocks
  - Clock edges (+ve and –ve)
- Edge-triggered D Flip-flops
  - Positive edge-triggered D Flip-flop Implementation
  - Logic Symbol
- JK Flip-flop
  - Implementation



Positive Edge-triggered D Flip-flop

D Flip Flop

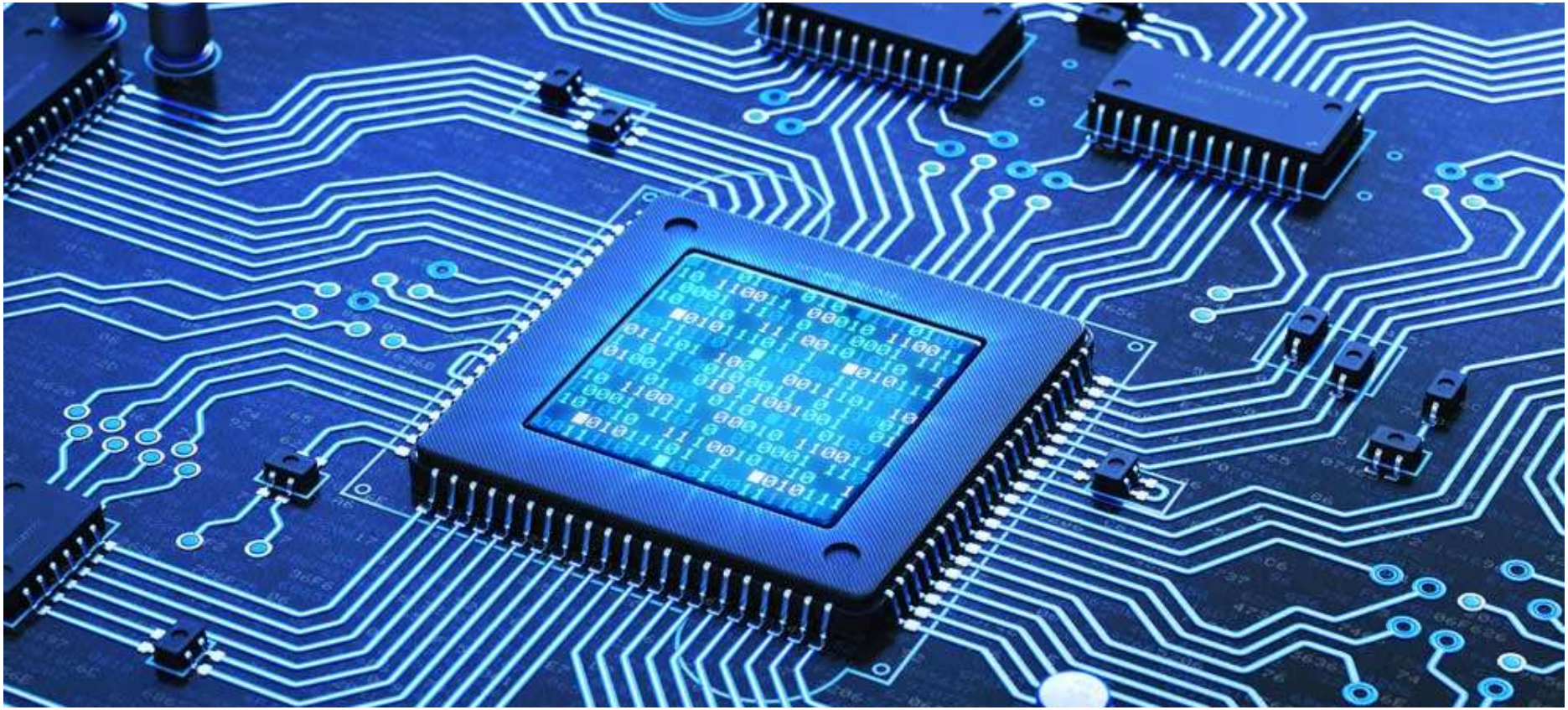




D Flip-Flop

D	Q(t + 1)	
0	0	Reset
1	1	Set

- The value that is produced at the output (**Q**) of the flip-flop is the **value** that was **stored** in the **master** stage **immediately before** the **positive edge occurred**
- The logic symbol of the positive edge-triggered D-flip-flop is give above

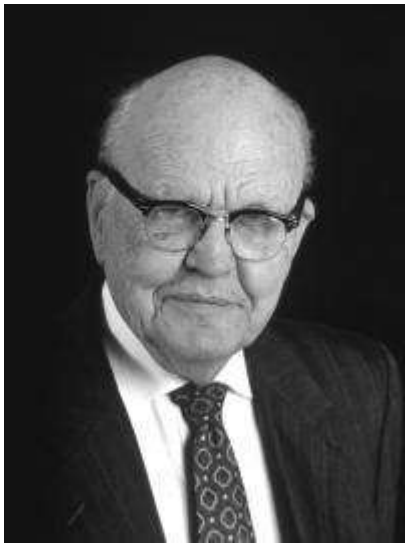


JK Flip-flop

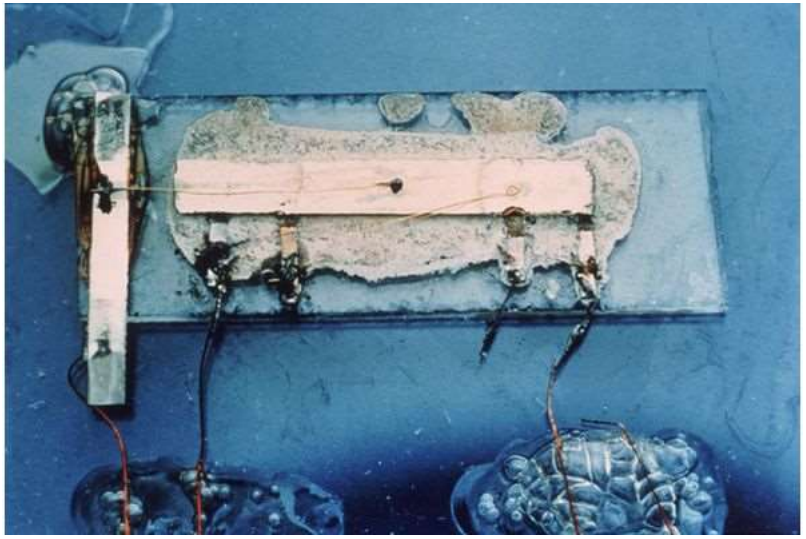
Other Flip-flops with D Flip-flop

- D Flip-flop is the simplest flip-flop that can be built with a less number of logic gates
- In a typical Integrated Chip has millions of logic gates and flips-flops inside them
- Other types of flip-flops are built using the D flip-flop
  - J-K Flip-Flop
  - T Flip-flop

Why is JK Flip-flop named so?

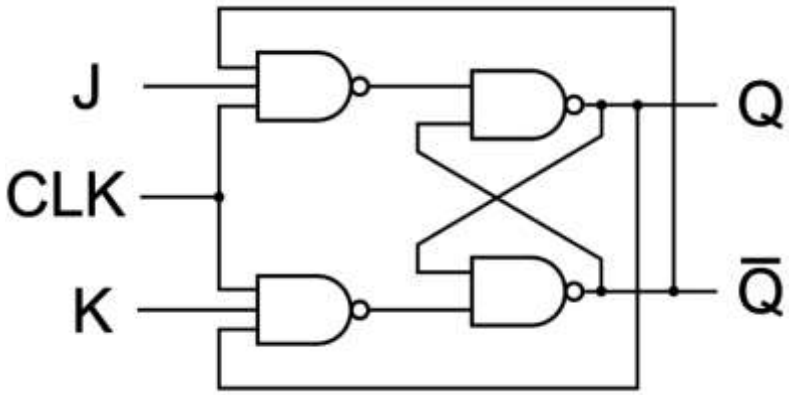


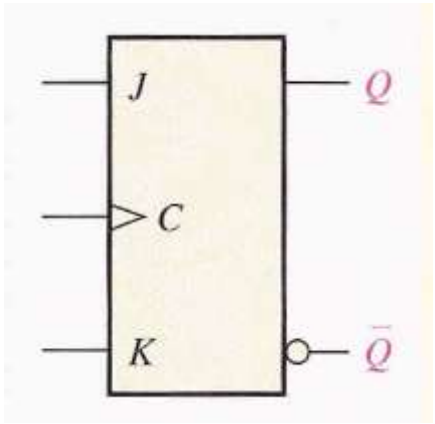
The first IC built by JK in 1958



- The choice of the letters "**JK**" in the **JK flip flop** do have significance.
- The **JK flip flop** was **named** after **Jack Kilby**, the **Texas Instruments (TI)** engineer that **invented** the **integrated circuit (IC)** in **1958**. Won **Noble prize** in **physics** in **2000**.
- The **modified RS circuit** that **eliminated race conditions** was named **JK** in **his honour**.

- JK Flipflop

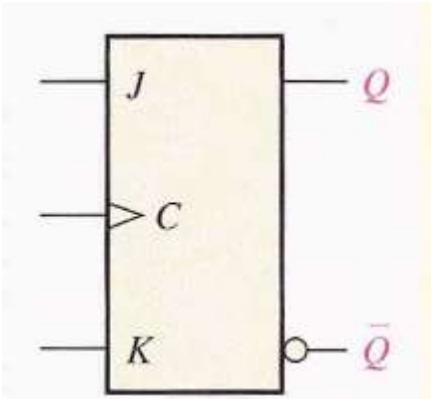




JK Flip-Flop

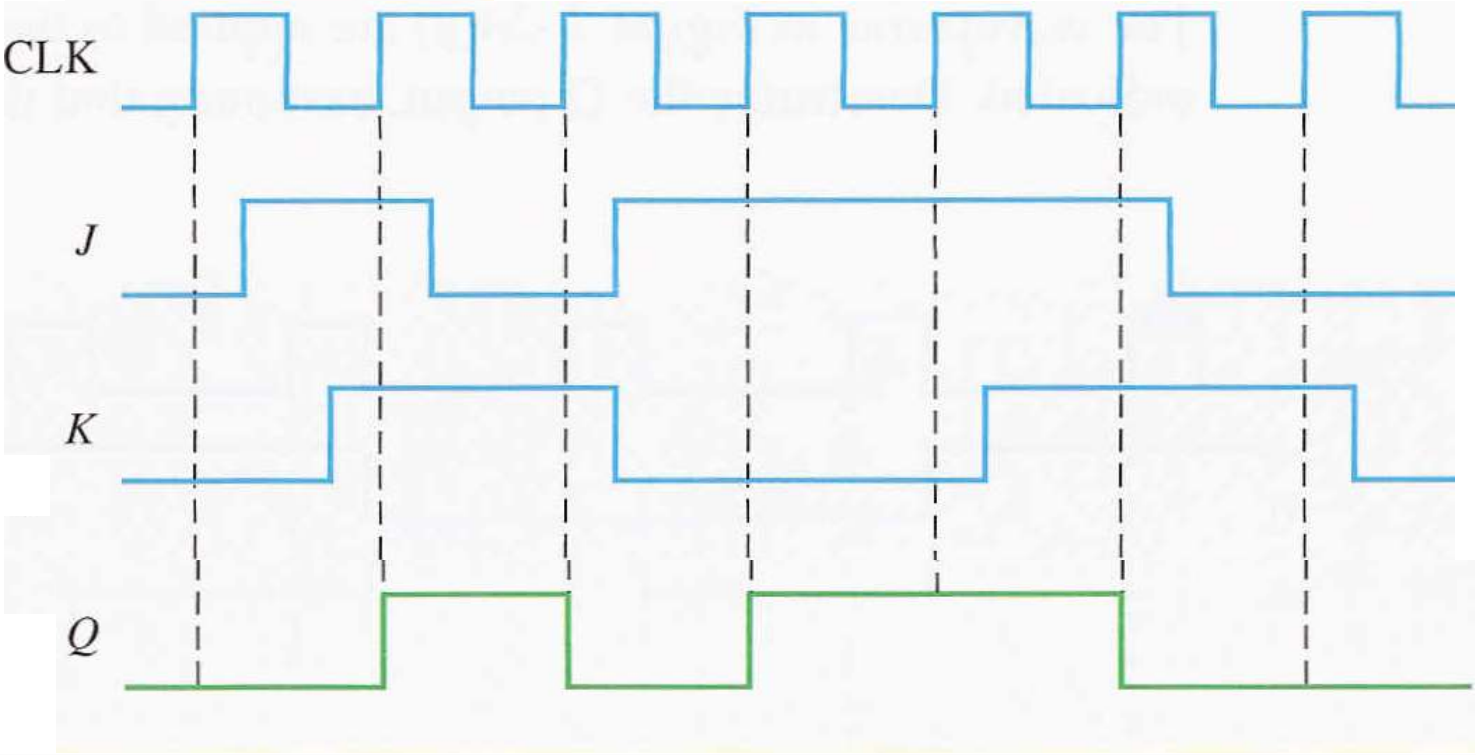
J	K	Q(t + 1)	
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$Q'(t)$	Complement

Quiz 1: Draw the output (Q) waveform

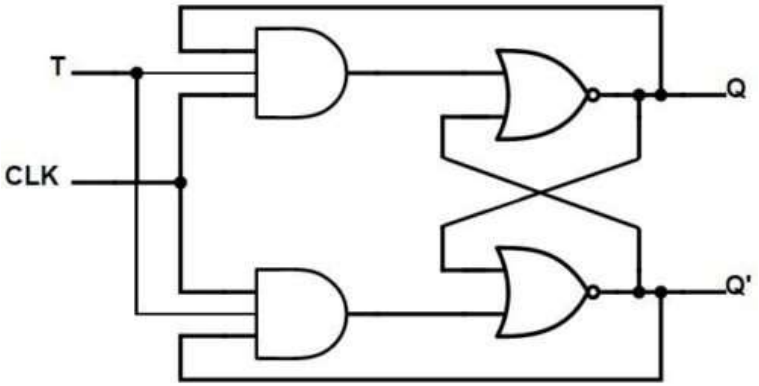


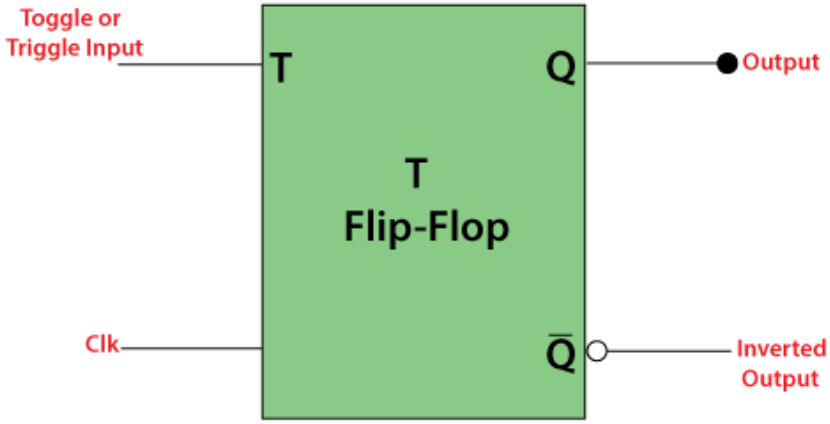
Assume that the flip-flop is initially **RESET**

This is **Positive** edge-triggered



• T flip flop





CLK	T	Q(n+1)	State
| +ve edge	0	Q	NO CHANGE
| +ve edge	1	Q’	TOGGLE

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