EAST WEST UNIVERSITY

Course Title:Electrical Circuits
Course: CSE251
Lab Report (7)
Section:5
Date: 12.1.22

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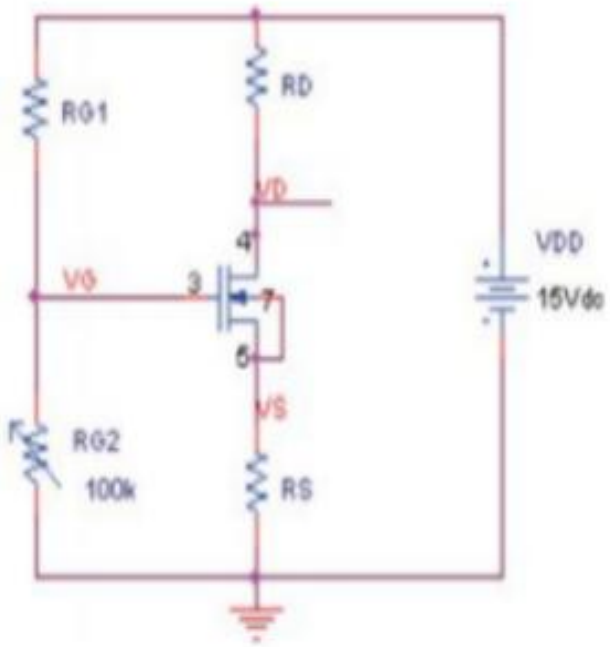
Experiment No: 7

Title: Biasing of a Common-Source Voltage Amplifier.

Objectives:
1.Identify an appropriate DC operation point for a NMOS transistor.

Circuit Diagram:



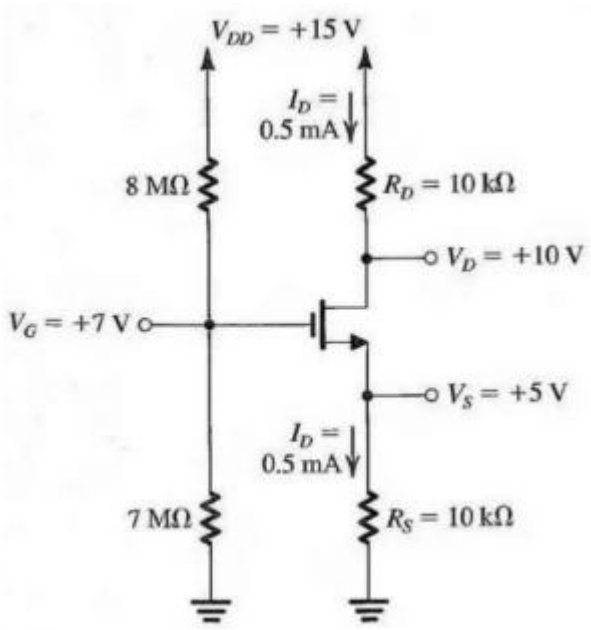
Here,
I_D = 0.5 mA, VDD = 15V, VD = 10V, VS = 5V,

We know,
$I_D = 0.5 * k_n * V_{ov}^2$
So, V_{ov}=1V

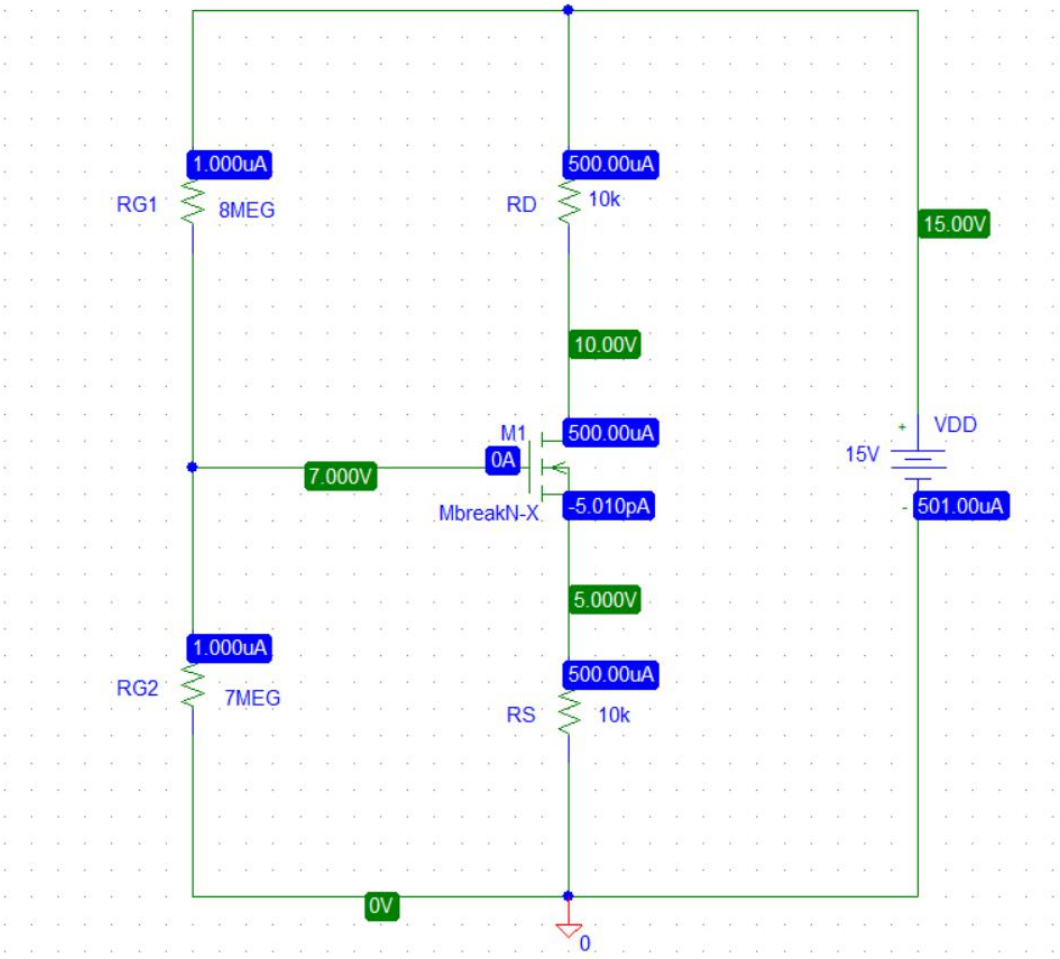
VGS = V_{ov} + Vth = 1+1 = 2V.
VG – VS = 2;
∴ VG = 5 + 2 = 7V.

Drain Resistance, RD =((VDD-VD)/ I_D)
= ((15-10)/0.5) Ω
= 10 Ω
Drain Resistance, RD =((VS-0)/ I_D)
= ((5-0)/0.5) Ω
= 10 Ω

Circuit of Example:



Pspice Simulation:



In the Experimental data sheet,
I_D = 0.6 mA, VDD = 15V, VD = 10V, VS = 4V,
We know,
$I_D = 0.5*k_n*V_{ov}^2$

So, V_{ov}=1.3V
VGS = V_{ov} + Vth = 1.3+1.2 = 2.5V
VG – VS = 2.5;
∴ VG = 4 + 2.5 = 6.5V.

Drain Resistance, RD =((VDD-VD)/ I_D)
= **((15-10)/0.6)** ***k*Ω**
= **8. 33** ***k*Ω**
Drain Resistance, RD =((VS-0)/ I_D)
= **((4-0)/0.6)** ***k*Ω**
= **6.67** ***k*Ω**

Pspice Simulation: