Department of Computer Science & Engineering
CSE 251– Electronic Circuits
Semester Final Exam

Course Code: CSE 251 | **Semester**: FL 21
Teacher's Initial: SMRC | **Section**: 5 (Five)
Time: 90 Mins | **Full Marks:** 50

All the questions must be answered. Symbols have their usual meanings.

Question 1 [CO_1, 20]

Determine the drain current (I_D), gate-source voltage (V_{GS}) and the drain-source voltage (V_{DS}) at the Q-point of the following circuits. Also mention their operational modes (linear/saturation). [Given for both MOSFETs, $V_{TH} = 0.75$V and $\mu_n C_{ox} W/L = 1.28$ mA/V^2. Ignore the short channel effect.]

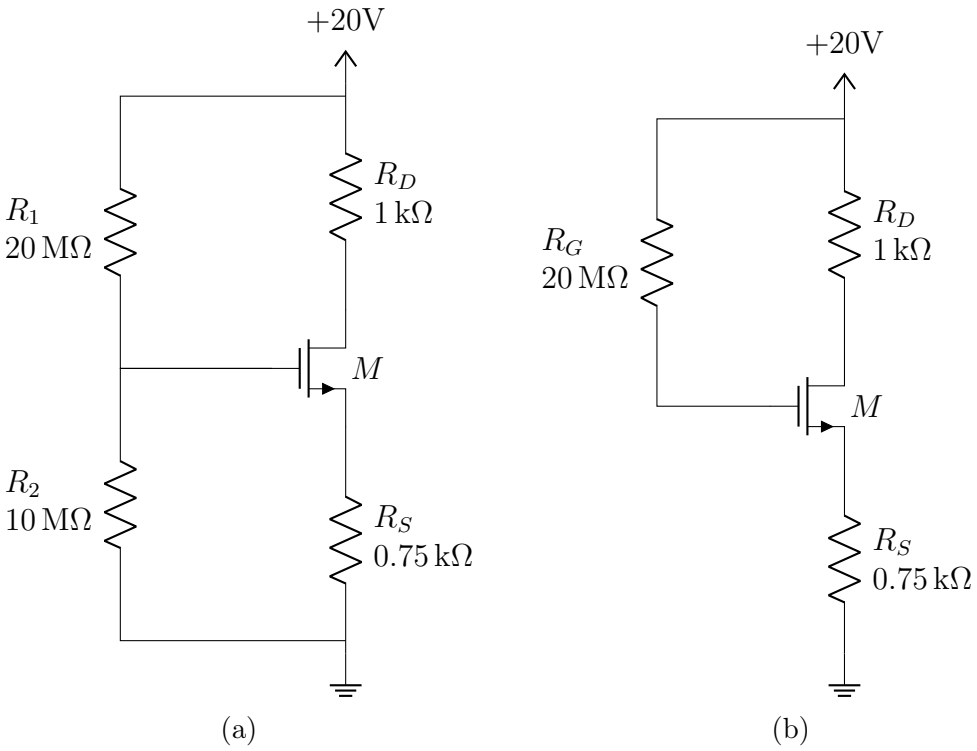

Figure Q.1: Circuit Diagrams for Question-1.

Question 2 [CO_2, 15]

Choose a suitable bias circuit working in saturation mode from Figure Q.1, along with the associated Q-point values. Draw a Source Follower amplifier configuration by connecting proper input and output terminals to the bias circuit. Now determine, g_m, Z_{in}, Z_{out}, A_{v0}, A_v, G_v and v_{out} of the Source Follower circuit. [Take, input source, $v_{sig} = 1.5$V peak sinusoid, source impedance, $R_{sig} = 888$ kΩ, load impedance, $R_L = 0.8$ kΩ and the CLM parameter, $\lambda = 25$ μS]

Question 3 [CO_2, 7]

Using the small signal model of MOSFET, derive the expression of the input impedance (Z_{in}) of the following amplifier circuit.

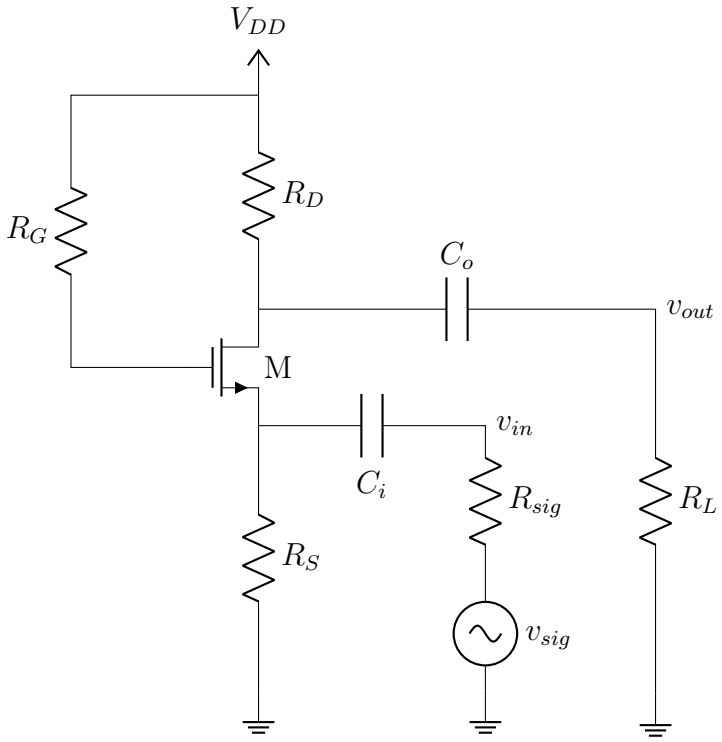

Figure Q.3: Circuit Diagram for Question-3.

Question 4 [CO_2, 8]

Design CMOS logic circuit for the logic function, $F(x, y, z) = \overline{x + y.z}$