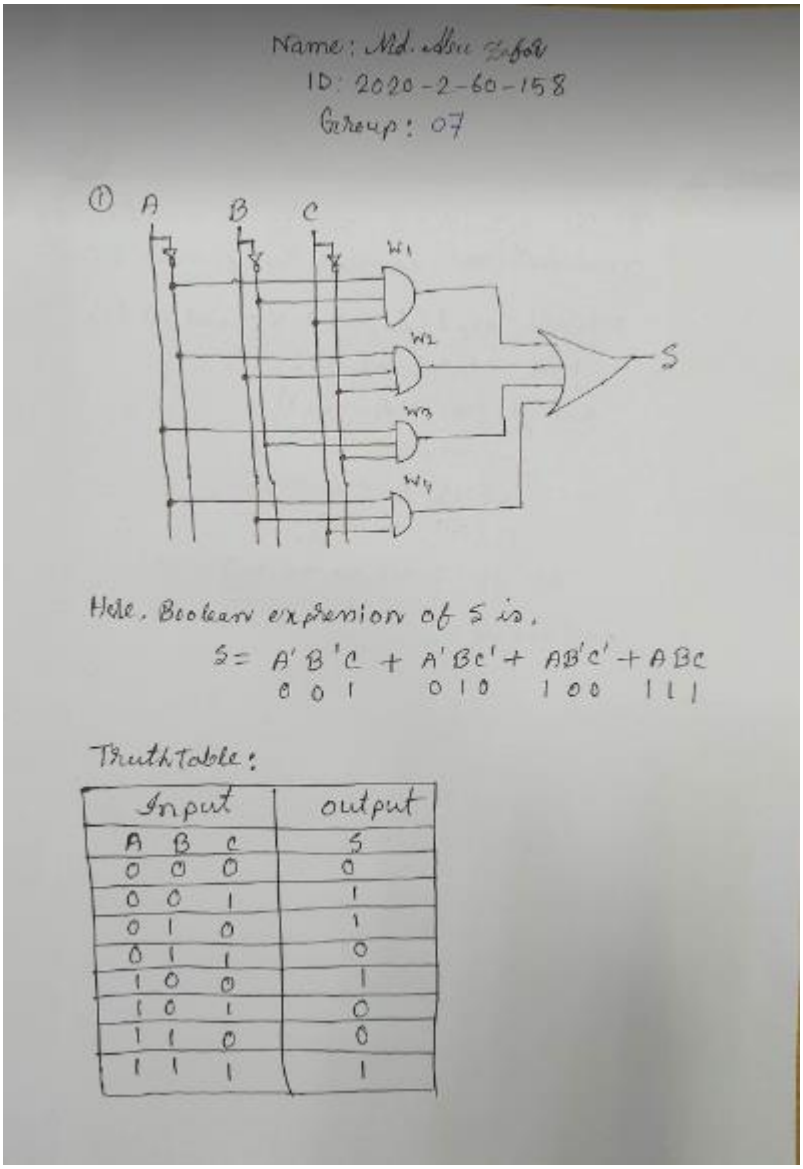
EAST WEST UNIVERSITY

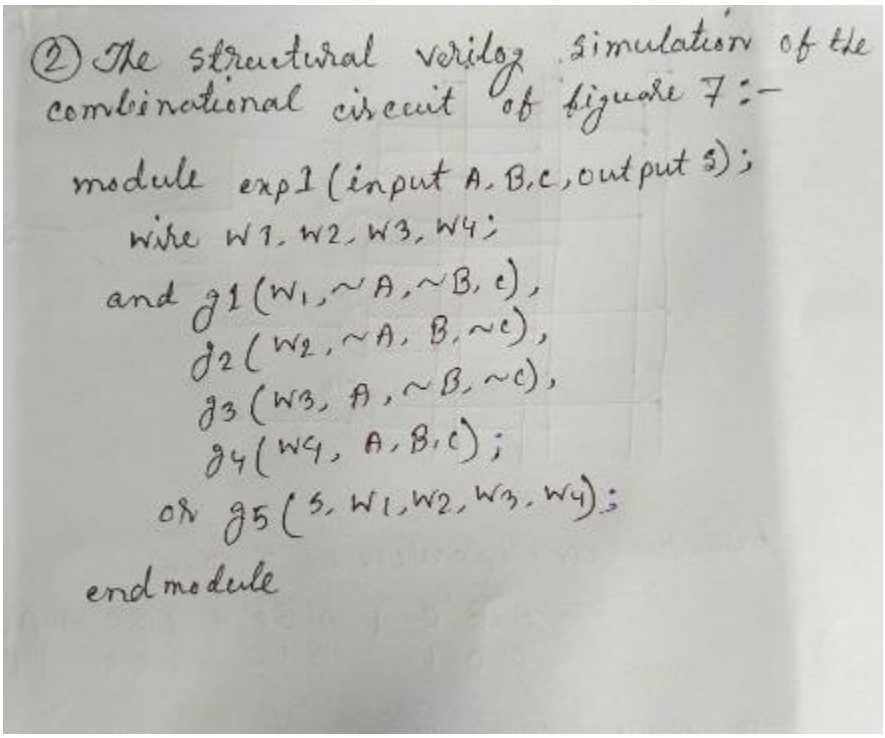
Expt-1 Prelab and Lab Work

Expt-1 Prelab

1.



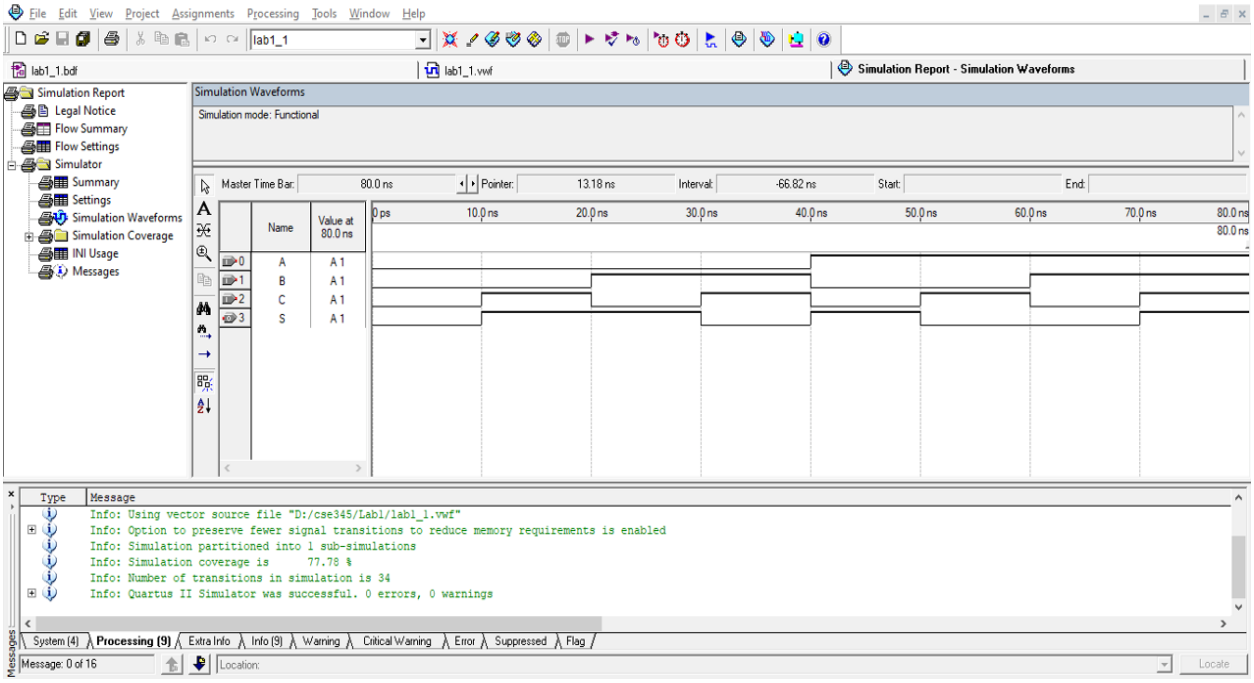
2.



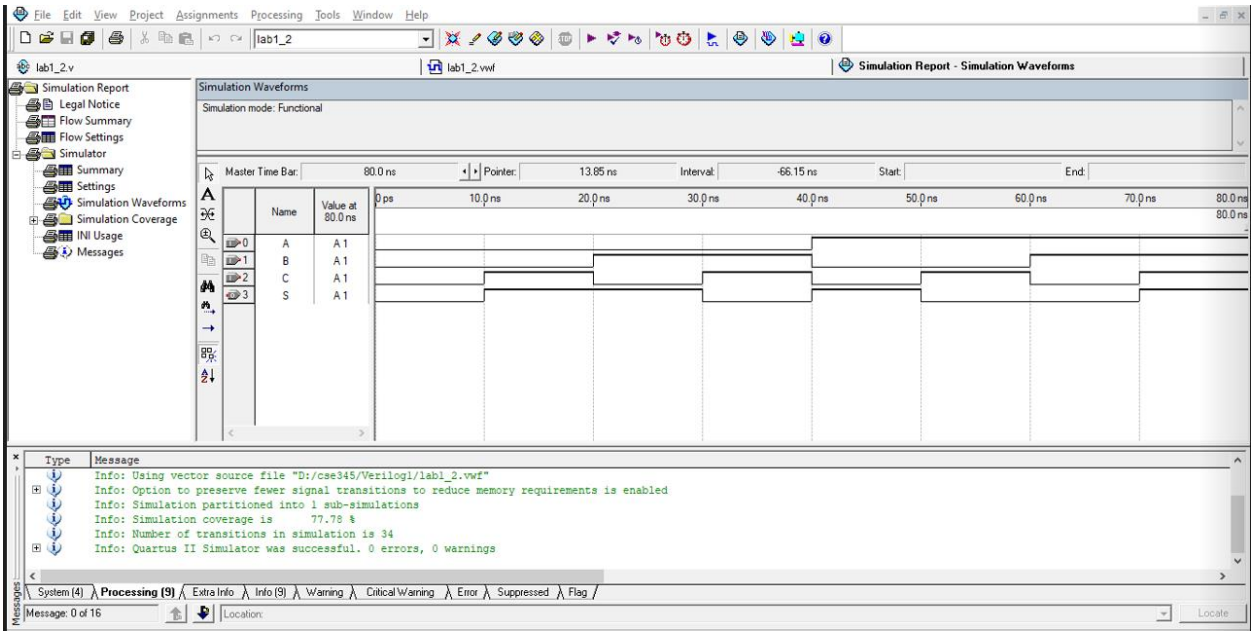
(2) The structural verilog simulation of the combinational circuit of figure 7:-

```
module exp1 (input A, B, C, output S);
  wire W1, W2, W3, W4;
  and g1 (W1, ~A, ~B, C),
      g2 (W2, ~A, B, ~C),
      g3 (W3, A, ~B, ~C),
      g4 (W4, A, B, C);
  OR g5 (S, W1, W2, W3, W4);
end module
```

Lab work:
Circuit Simulation:



Verilog:


File Edit View Project Assignments Processing Tools Window Help
lab1_2
lab1_2.v
lab1_2.vwf
Simulation Report - Simulation Waveforms
Simulation Report
Legal Notice
Flow Summary
Flow Settings
Simulator
Summary
Settings
Simulation Waveforms
Simulation Coverage
INI Usage
Messages
Simulation Waveforms
Simulation mode: Functional
Master Time Bar: 80.0 ns
Pointer: 13.85 ns
Interval: -66.15 ns
Start:
End:
Name
Value at 80.0 ns
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
50.0 ns
60.0 ns
70.0 ns
80.0 ns
0 A A 1
1 B A 1
2 C A 1
3 S A 1
Type
Message
Info: Using vector source file "D:/cse345/Verilog1/lab1_2.vwf"
Info: Option to preserve fewer signal transitions to reduce memory requirements is enabled
Info: Simulation partitioned into 1 sub-simulations
Info: Simulation coverage is 77.78 %
Info: Number of transitions in simulation is 34
Info: Quartus II Simulator was successful. 0 errors, 0 warnings
System (4)
Processing (9)
Extra Info
Info (9)
Warning
Critical Warning
Error
Suppressed
Flag
Message: 0 of 16
Location:
Locate