East West University
Department of Computer Science and Engineering
Course Outline
Spring 2023 Semester

Course: CSE345 Digital Logic Design (Sections 2 & 3)

Credits and Teaching Scheme

	Theory	Laboratory	Total
Credits	3	1	4
Contact Hours	3 Hours/Week for 13 Weeks + Final Exam in the 14th Week	2 Hours/Week for 13 Weeks	5 Hours/Week for 13 Weeks + Final Exam in the 14th Week

Prerequisite

CSE251 Electronic Circuit

Instructor Information

Instructor: **Musharrat Khan**
Senior Lecturer, Department of Computer Science and Engineering
Office: Room # 636
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TA: TBA

Class Routine and Office Hour

Day	08:30-10:00	10:10-11:40	11:50-01:20	01:30-03:00	03:10-04:40
Sunday		**CSE345(2) Room: FUB-303**	**Office Hour**	**CSE345(3) Room: 359**	
Monday		**CSE209(3) Room: FUB-401**	**Office Hour**		
Tuesday		**CSE345(2) Room: FUB-303**	**Office Hour**	**CSE345(3) Room: 359**	
Wednesday		**CSE209(3) Room: FUB-401**	**Office Hour**		
Thursday		**CSE345LAB(2) Room: 634**	**Office Hour**	**CSE345LAB(3) Room: 634**	**Office Hour**

Course Objective

This course introduces the fundamental concepts and practices of gate-level and MSI-level design of digital circuits. This course also emphasizes computer-aided design of digital circuits using Verilog Hardware Description Language (HDL). Knowledge of this course will be needed as prerequisite knowledge for future courses such as CSE360 Computer Architecture, CSE442 Microprocessors and Microcontrollers, and CSE490 VLSI design.

Knowledge Profile

K3: Theory-based engineering fundamentals
K4: Forefront engineering specialist knowledge for practice
K5: Engineering design

Learning Domains

Cognitive - C2: Understanding, C3: Applying, C4: Analyzing, C6: Creating
Psychomotor - P2: Manipulation, P3: Precision
Affective - A2: Responding

Program Outcomes (POs)

PO1: Engineering Knowledge
PO2: Problem Analysis
PO3: Design/Development of Solutions

Complex Engineering Problem Solution

EP1: Depth of knowledge required
EP2: Range of conflicting requirements

Complex Engineering Activities

None

Course Outcomes (COs) with Mappings

After completion of this course students will be able to:

CO	CO Description	PO	Learning Domains	Knowledge Profile	Complex Engineering Problem Solving/ Engineering Activities
CO1	**Interpret** and **apply** binary number system and Boolean algebra for design and analysis of combinational and sequential digital circuits.	PO1	C2, C3	K3	EP1
CO2	**Analyze** combinational and sequential circuits for determining output behavior of digital circuits.	PO2	C4	K3, K4	EP1

CO3	**Apply** Boolean algebraic and state transition techniques; and **design** combinational and sequential circuits for constructing practical digital circuits.	PO3	C3, C6	K4, K5	EP1, EP2
CO4	**Use** analytical, software, and hardware tools and techniques; **design** circuits; p**erform** and **demonstrate** skills; and **write** report for constructing and testing practical digital circuits.	PO3	C3, C6 P2, P3 A2	K4, K5	EP1, EP2

Course Topics, Teaching-Learning Method, and Assessment Scheme

Course Topic	Teaching-Learning Method	CO	EP/ EA	Mark of Cognitive Learning Levels				CO Mark	Exam (Mark)
				C2	C3	C4	C6		
Binary number system, binary arithmetic, and Binary codes	Lecture, Class Discussion, Discussion outside class with Instructor/TA	CO1		4				4	Midterm Exam I (20)
Boolean algebra, Logic gates, Minimization of Boolean functions using K-map	Do	CO1	EP1	6	10			16	
Analysis of combinational circuit using Boolean algebraic technique	Do	CO2	EP1			4		4	Midterm Exam II (20)
Design of combinational circuit using Boolean algebraic technique	Do	CO3	EP1, EP2		3			3	
Design and use of MSI-level combinational circuits: parallel adder and	Do	CO3	EP1, EP2		3		6	9	

subtractor; encoder and decoder; multiplexer and demultiplexer									
Design of Combinational circuits using Verilog HDL	Do	CO3	EP1, EP2				4	4	
Flip-Flops, Representation and analysis of sequential circuits	Do	CO2	EP1			4		4	Final Exam (20)
Design of sequential circuit using state transition techniques	Do	CO3	EP1, EP2		4			4	
Design of MSI-level sequential circuits: registers, counters	Do	CO3					8	8	
Design of sequential circuits using Verilog HDL	Do	CO3	EP1, EP2				4	4	

Laboratory Experiments and Assessment Scheme

Experiment	**Teaching-Learning Method**	**CO**	**Mark of Cognitive Learning Levels**		**Mark of Psychomotor Learning Levels**		**Mark of Affective Learning Levels**	**CO Mark**
			C3	C6	P2	P3	A2	
Schematic and Structural Verilog Simulation of Combinational Logic Circuits	Preparing Pre-Lab Report, Lab Experiment, Result Analysis , and Post-Lab Report	CO4						
Design and Implementation of a	Do	CO4						

Combinational Logic Circuit								
Behavioral Verilog Simulation of a Combinational Logic Circuit	Do	CO4						
Binary Adder and Subtractor	Do	CO4						
Decoder and Its Use in Combinational Logic Implementation		CO4						
Multiplexer and Its Use in Combinational Logic Implementation	Do	CO4						
Verilog Simulation of a sequential circuit	Do	CO4						
Counters	Do	CO4						
Lab Exercise Total		CO4	1	4	1	1	1	8
Lab Exam	Individual Lab Exam	CO4	3	3	1	0	0	7
Total			**4**	**7**	**2**	**1**	**1**	**15**

Mini Project

Mini Project	**Teaching-Learning Method**	**CO**	**EP/ EA**	**Mark of Cognitive Learning Level**		**Mark of Psychomotor Learning Levels**		**Mark of Affective Learning Level**	**CO Mark**
				C3	**C6**	**P2**	**P3**	**A2**	
Lab-based Mini Project including Report and Presentation	Group-based moderately complex digital circuit design project with report writing and oral/poster presentation	CO4	EP1, EP2	2	5	1	1	1	10

Overall Assessment Scheme

Assessment Area	CO				Other	PO Marks		
	CO1	CO2	CO3	CO4		PO1	PO2	PO3
Class Participation					5			
Class Test/Quiz					10			
Midterm-I Exam	20	0	0	0		20	0	0
Midterm-II Exam	0	4	16	0		0	4	16
Final Exam	0	4	16	0		0	4	16
Laboratory Performance and Lab Exam	0	0	0	15		0	0	15
Mini Project	0	0	0	10		0	0	10
Total	**20**	**8**	**32**	**25**	**15**	**20**	**8**	**57**

Teaching Materials/Equipment

Text book:
Md. Mozammel Huq Azad Khan, *Digital Logic Design*, Bangladesh University Grants Commission, 2006.

Lab Manual:
Lab manual will be provided.

Project Description:
Project description will be provided.

Equipment/Software:
Digital circuit design board, SSI and MSI level ICs, and Quartus II software.

Grading System

Marks (%)	Letter Grade	Grade Point	Marks (%)	Letter Grade	Grade Point
97-100	A+	4.00	73-76	C+	2.30
90-96	A	4.00	70-72	C	2.00
87-89	A-	3.70	67-69	C-	1.70
83-86	B+	3.30	63-66	D+	1.30
80-82	B	3.00	60-62	D	1.00
77-79	B-	2.70	Below 60	F	0.00

Exam Dates

Section	Term I	Term II	Final
2	12.03.2023	09.04.2023	14.05.2023
3	12.03.2023	09.04.2023	14.05.2023

Academic Code of Conduct

Academic Integrity:
Any form of cheating, plagiarism, personification, falsification of a document as well as any other form of dishonest behavior related to obtaining academic gain or the avoidance of evaluative exercises committed by a student is an academic offence under the Academic Code of Conduct and **may lead to severe penalties as decided by the Disciplinary Committee of the university.**

Special Instructions:

- Students are expected to attend all classes and examinations. A student MUST have at least 80% class attendance to sit for the final exam.
- Students will not be allowed to enter into the classroom after 20 minutes of the starting time.
- For plagiarism, the grade will automatically become zero for that exam/assignment.
- Normally there will be **NO make-up exam**. However, in case of **severe illness, death of any family member, any family emergency, or any humanitarian ground**, if a student miss any exam, the student MUST get approval of makeup exam by written application to the Chairperson through the Course Instructor **within 48hours**of the exam time. Proper supporting documents in favor of the reason of missing the exam have to be presented with the application.
- For **final exam**, there will be NO makeup exam. However, in case of **severe illness, death of any family member, any family emergency, or any humanitarian ground**, if a student miss the final exam, the student MUST get approval of **Incomplete Grade** by written application to the Chairperson through the Course Instructor **within 48 hours** of the final exam time. Proper supporting documents in favor of the reason of missing the final exam have to be presented with the application. **It is the responsibility of the student to arrange an Incomplete Exam within the deadline mentioned in the Academic Calendar in consultation with the Course Instructor**.
- All mobile phones MUST be turned to silent mode during class and exam period.
- There is **zero tolerance for cheating** in exam. Students caught with cheat sheets in their possession, whether used or not writing on the palm of hand, back of calculators, chairs or nearby walls; copying from cheat sheets or other cheat sources; copying from other examinee, etc. would be treated as cheating in the exam hall. The only penalty for cheating is **expulsion for several semesters as decided by the Disciplinary Committee of the university**.