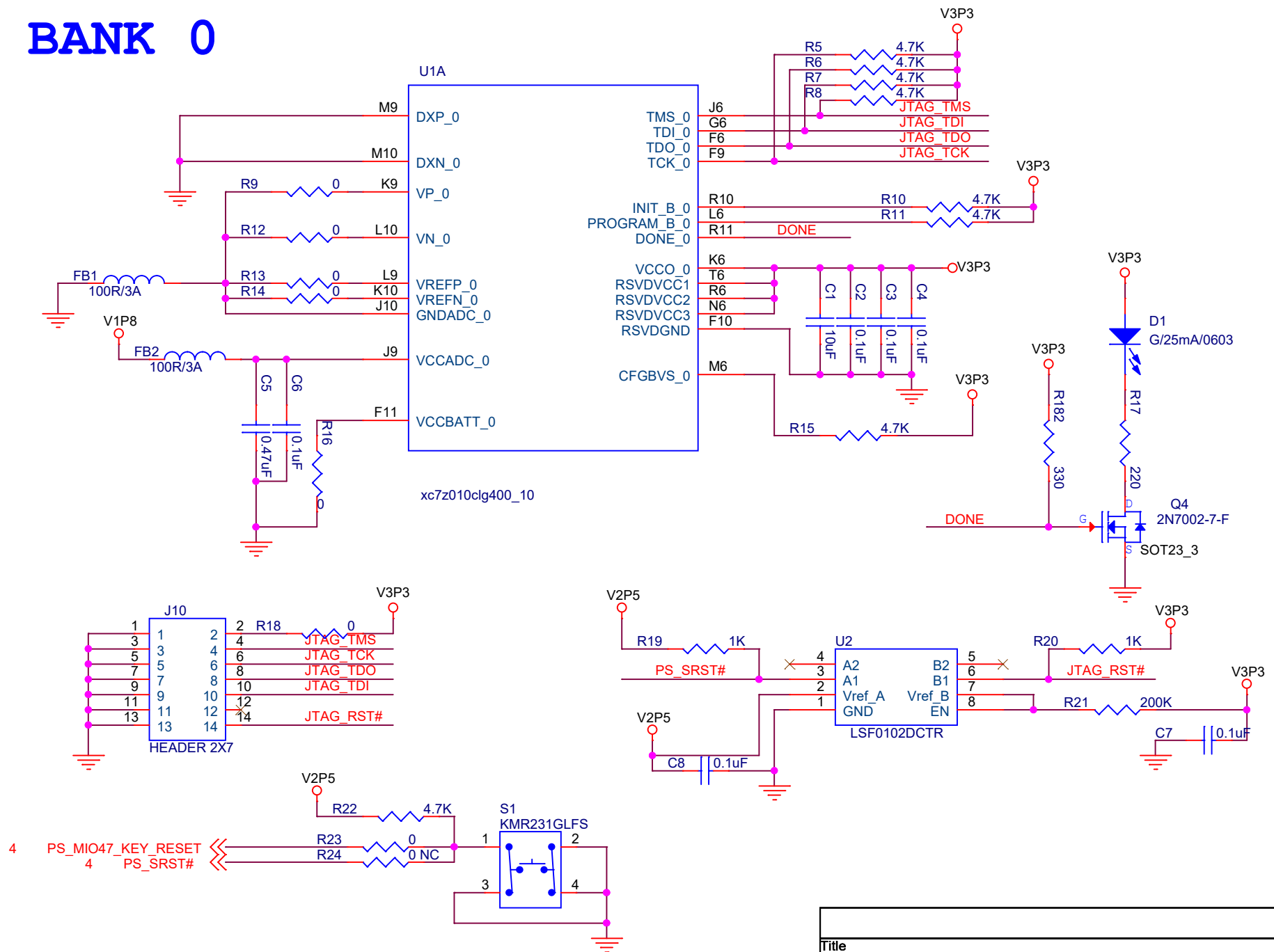


Boot Mode	JP1	JP2	JP3	JP4
Cascade JTAG	0	0	0	0
TF Card	0	1	0	1
QSPI Flash	0	0	0	1
NOR Flash	0	0	1	0
NAND Flash	0	1	0	0

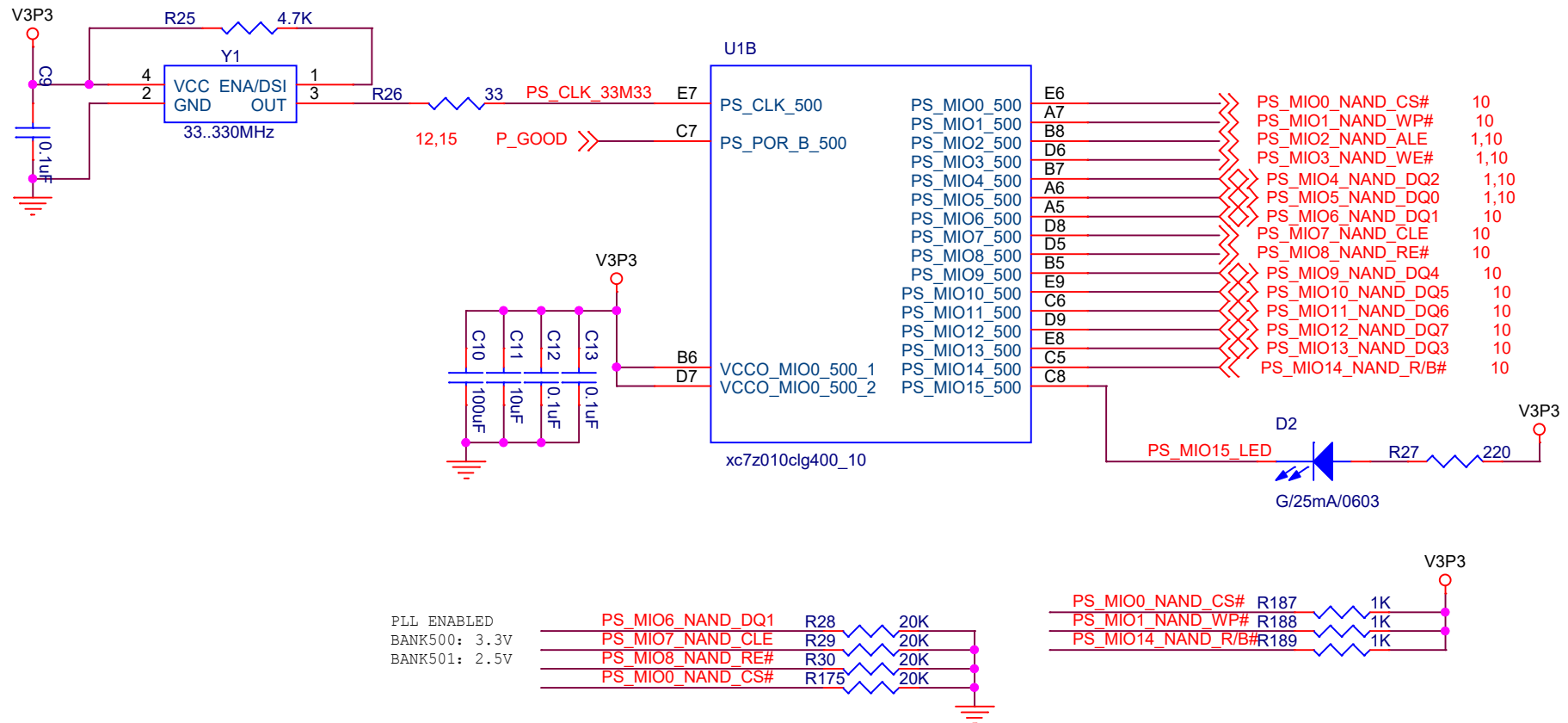
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# BANK 0



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# BANK 500

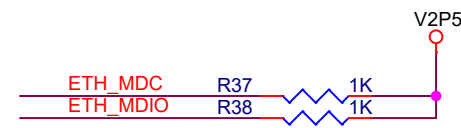
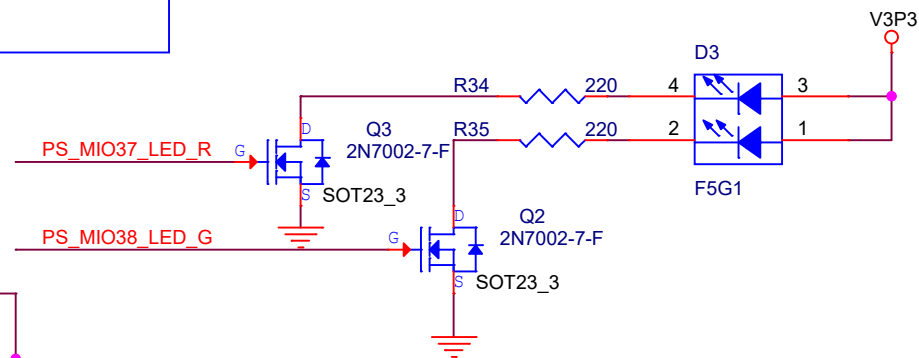
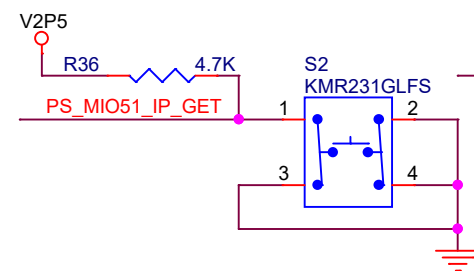
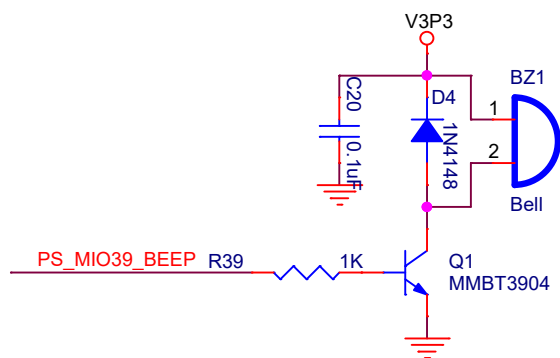
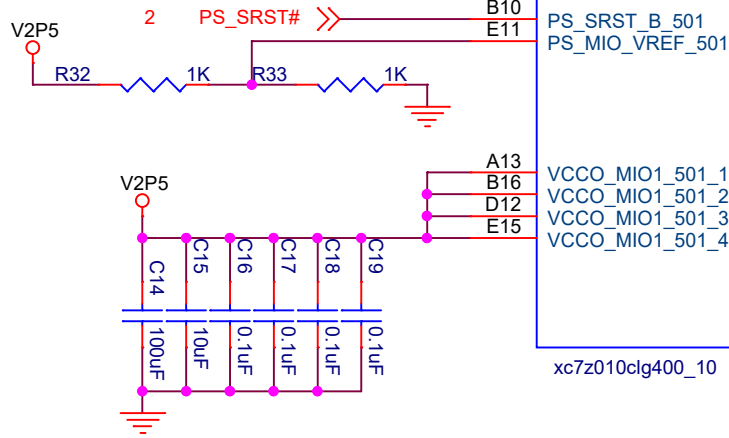
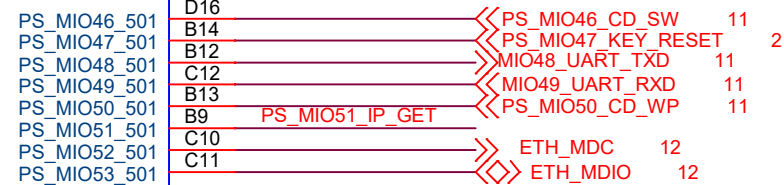
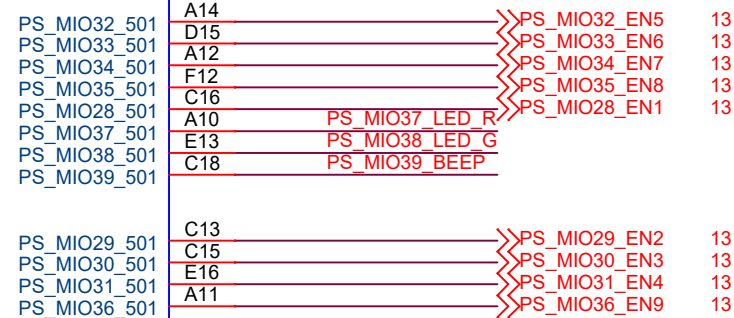
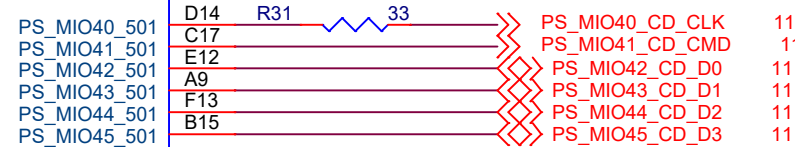
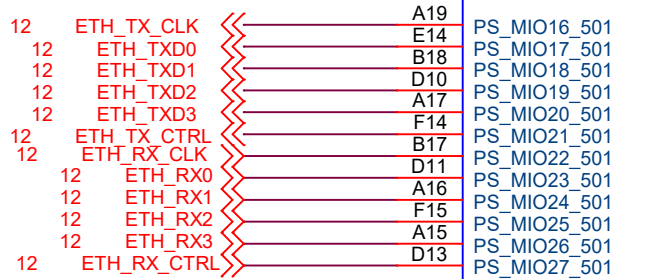


PLL ENABLED  
BANK500: 3.3V  
BANK501: 2.5V

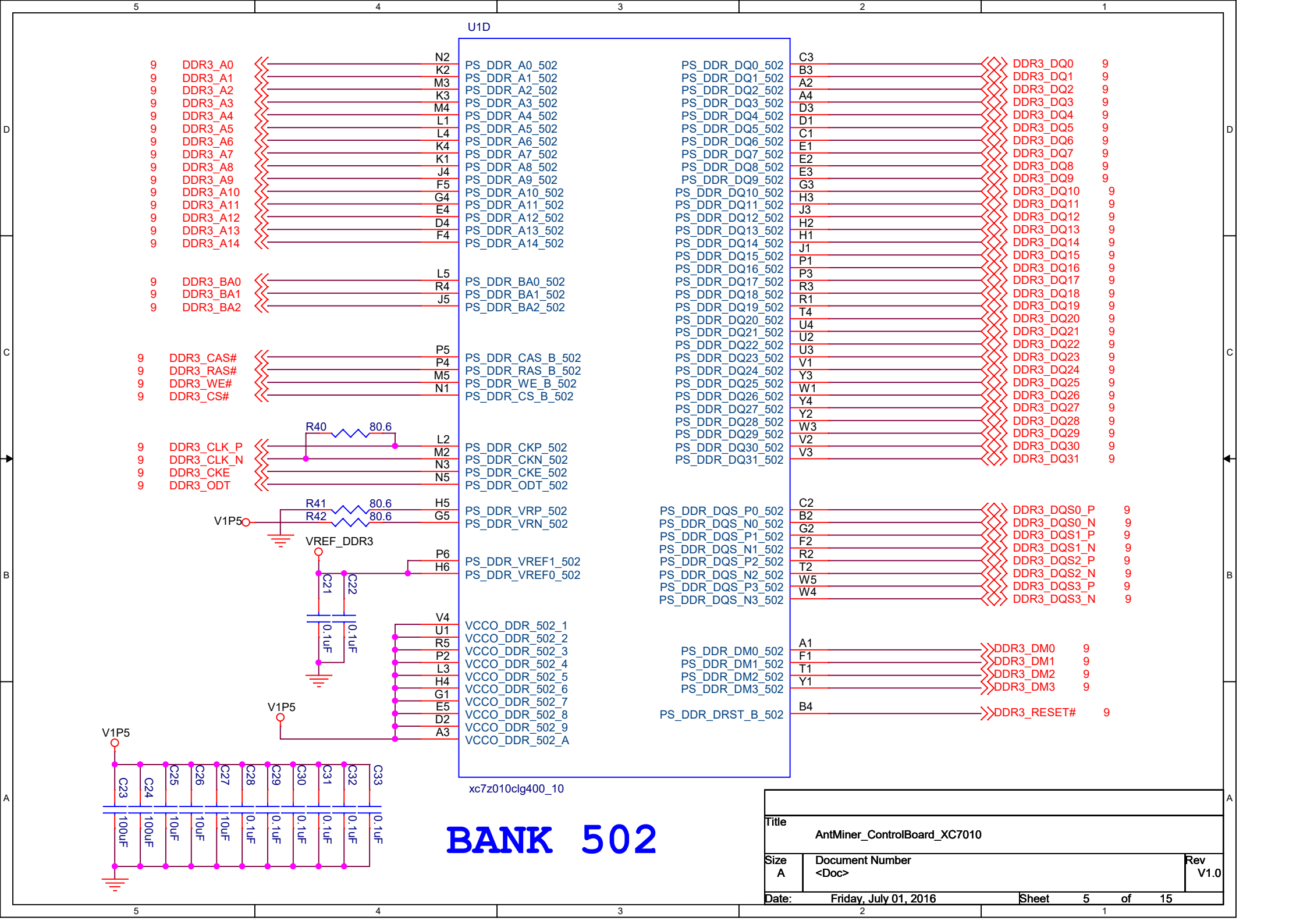
During an SD memory card boot sequence, the BootROM reads the logic level on the MIO pin 0 as an SD Card Detect. MIO pin 0 must be Low during the SDIO boot process.

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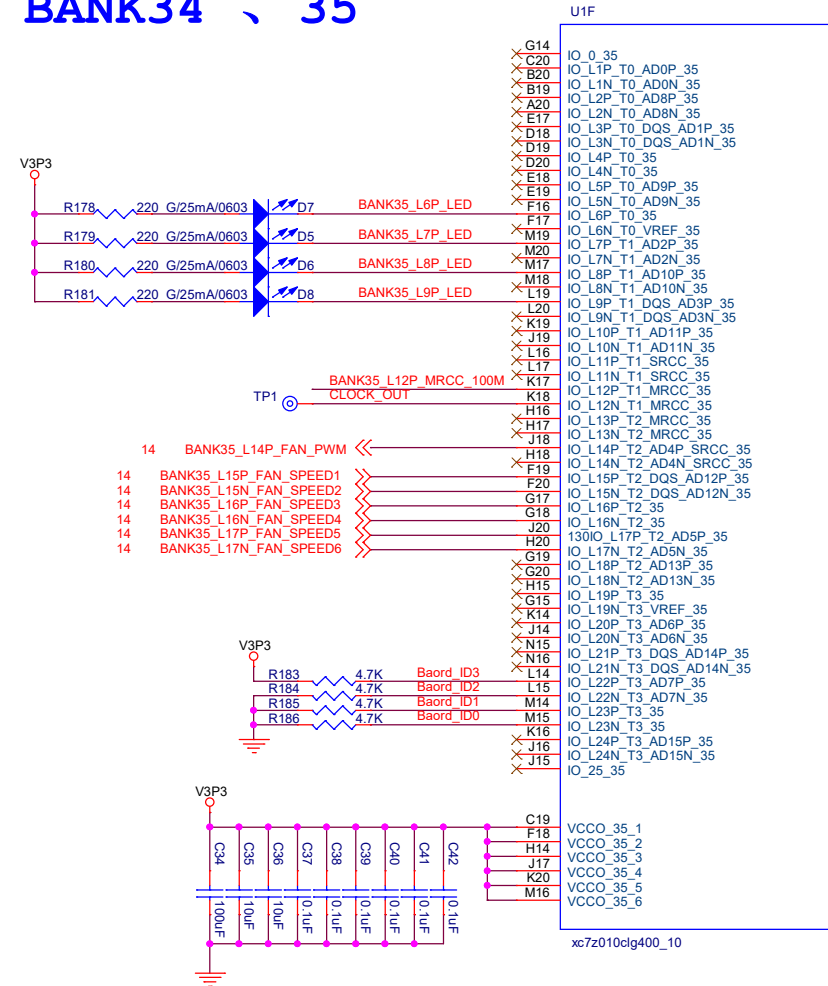
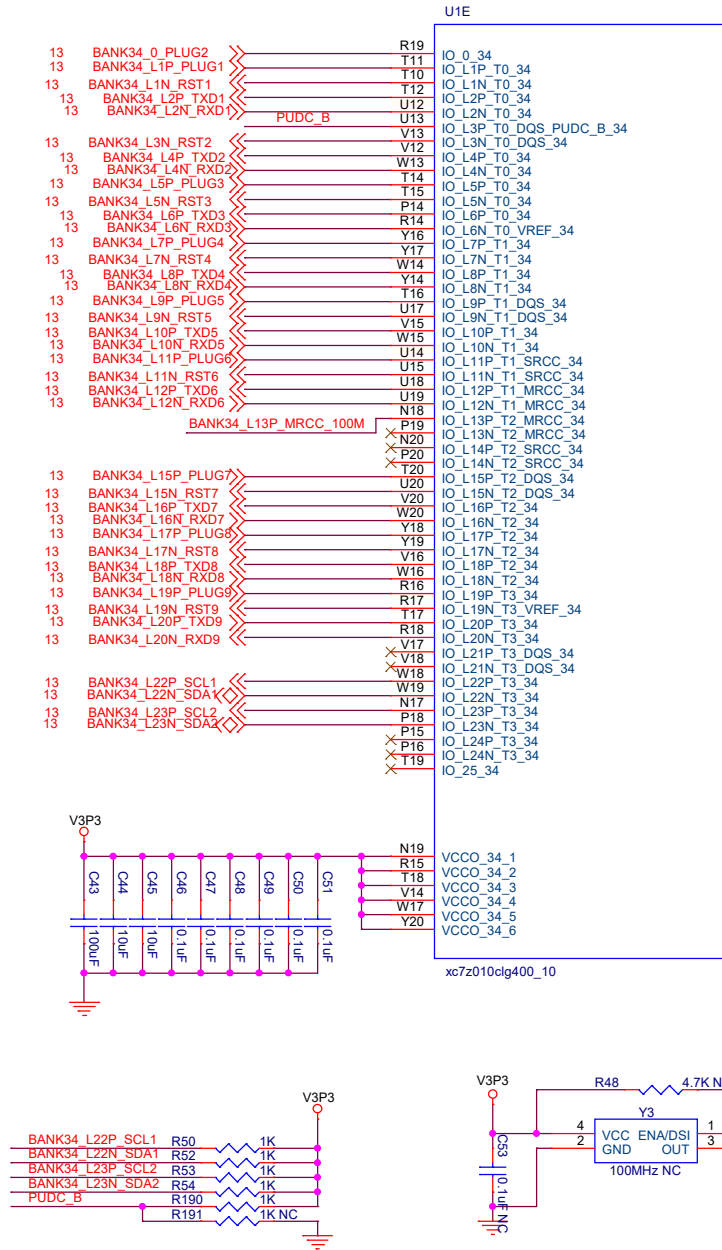
# BANK 501



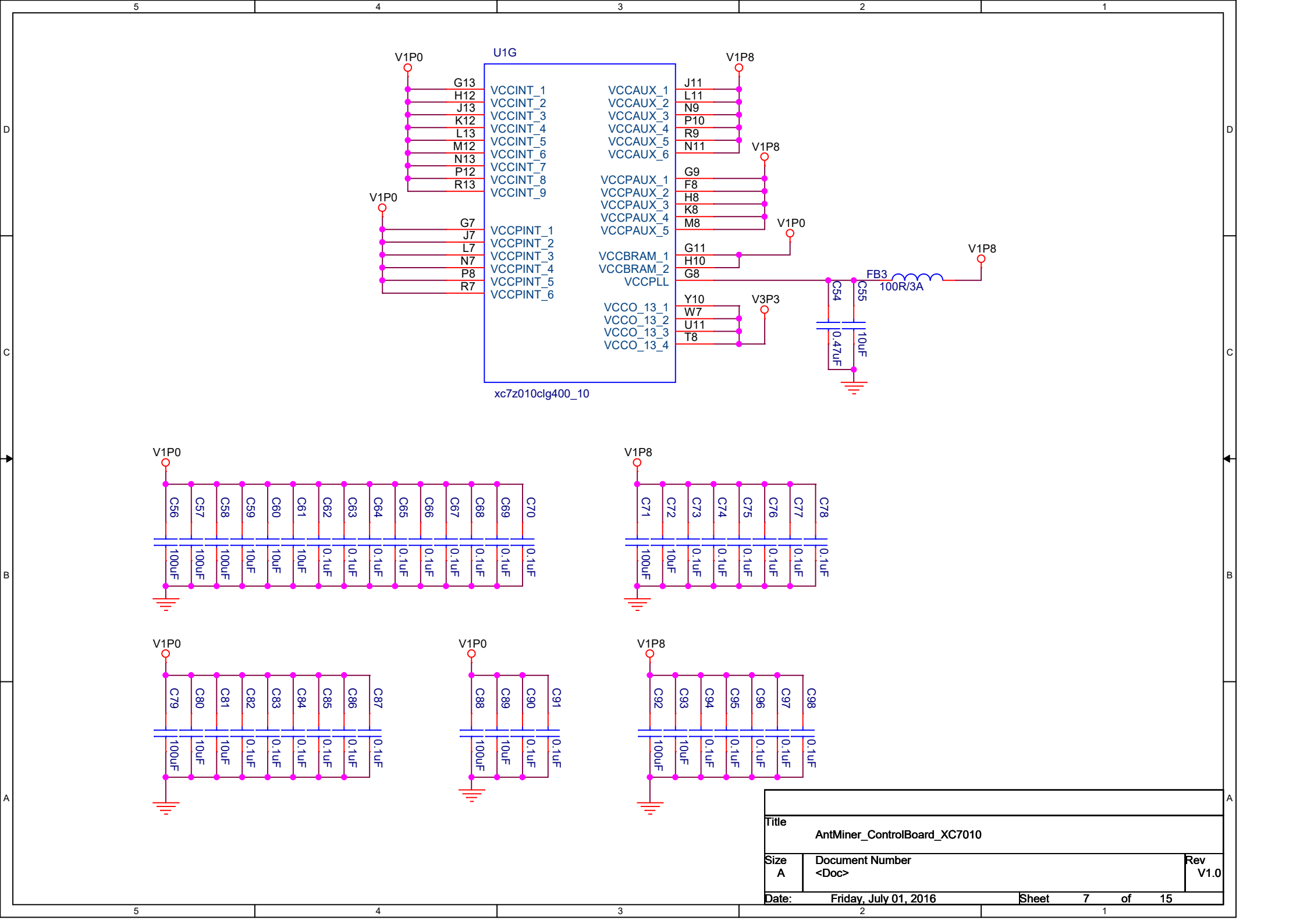
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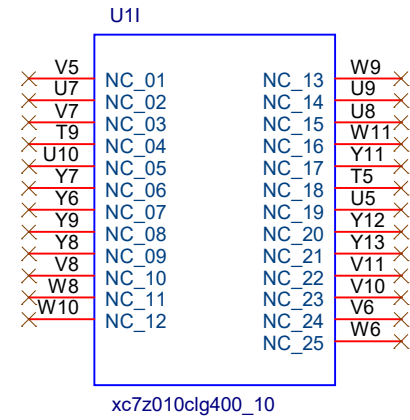
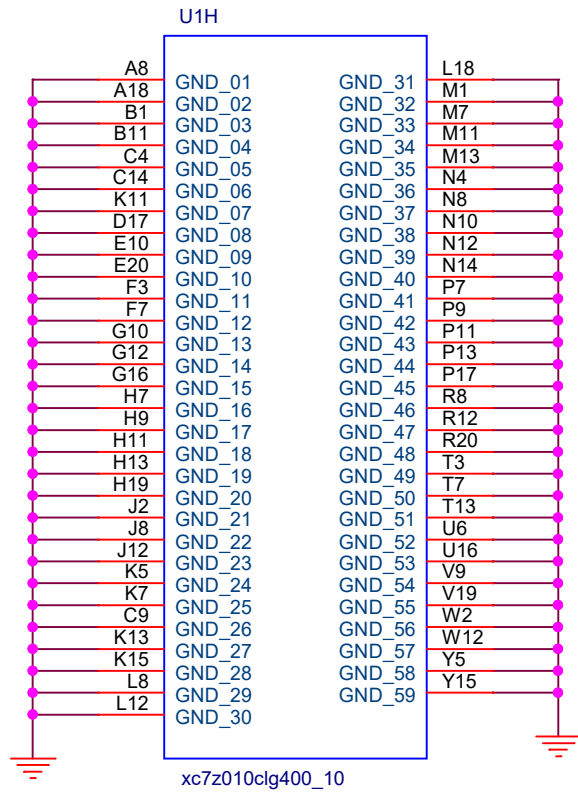


# PL BANK34 、 35



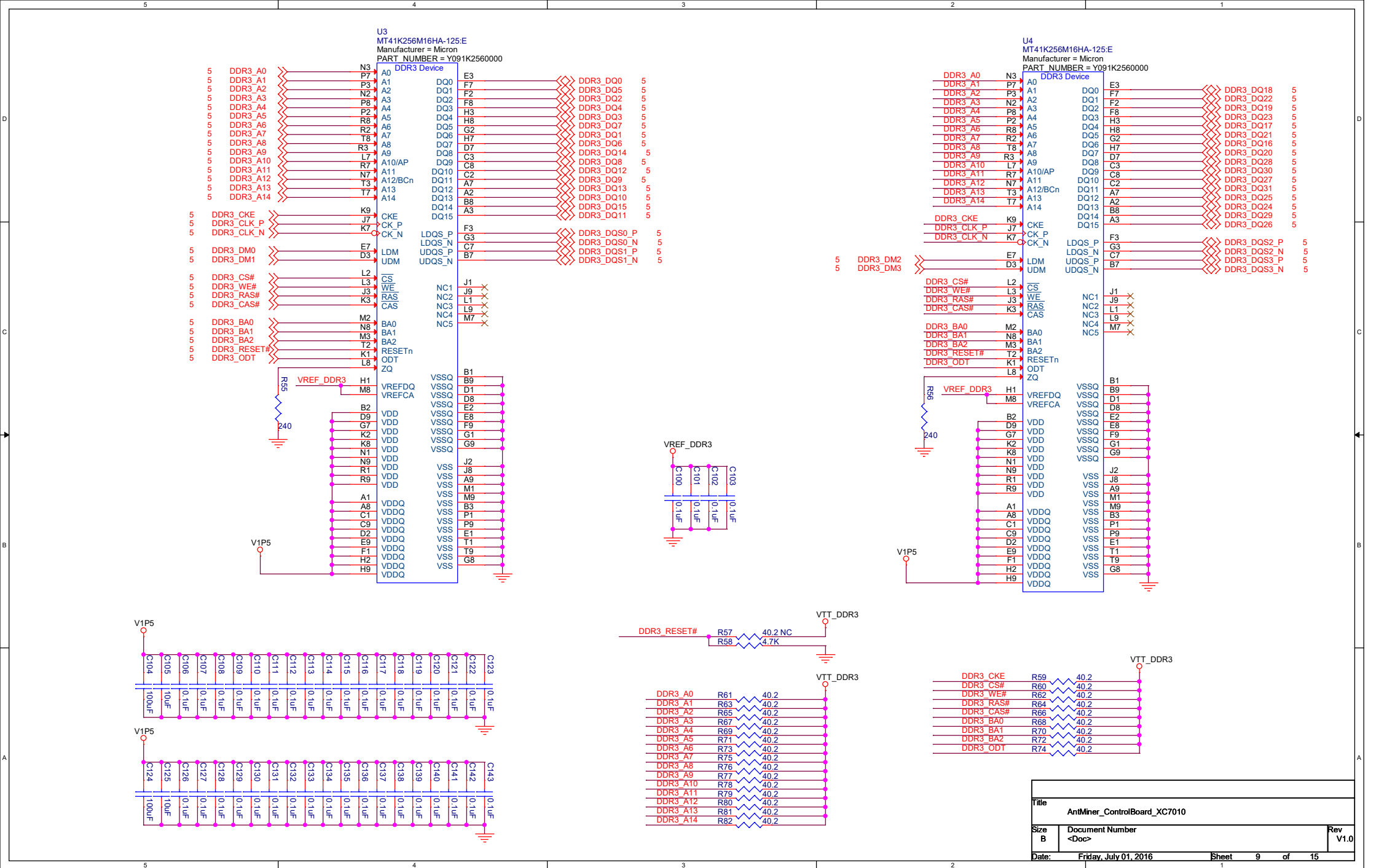
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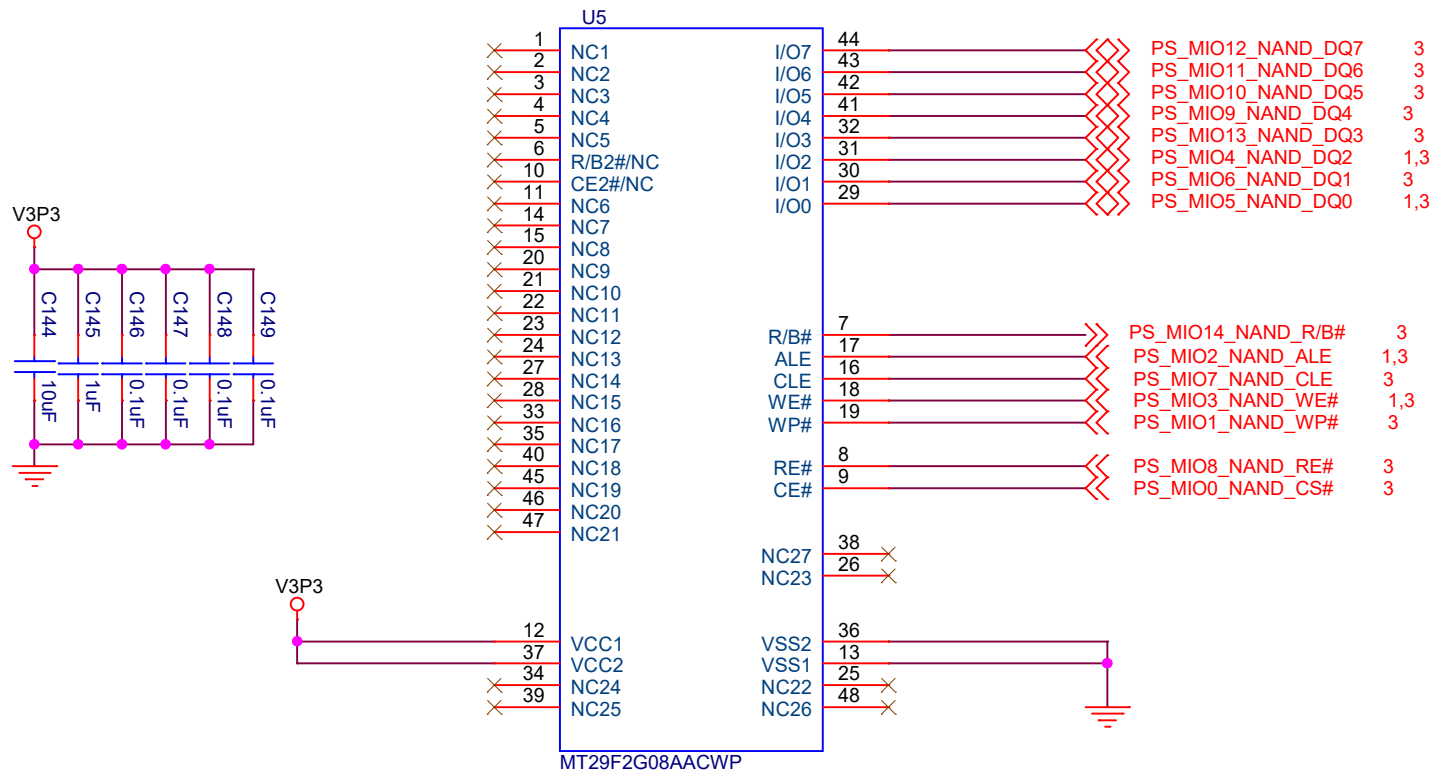


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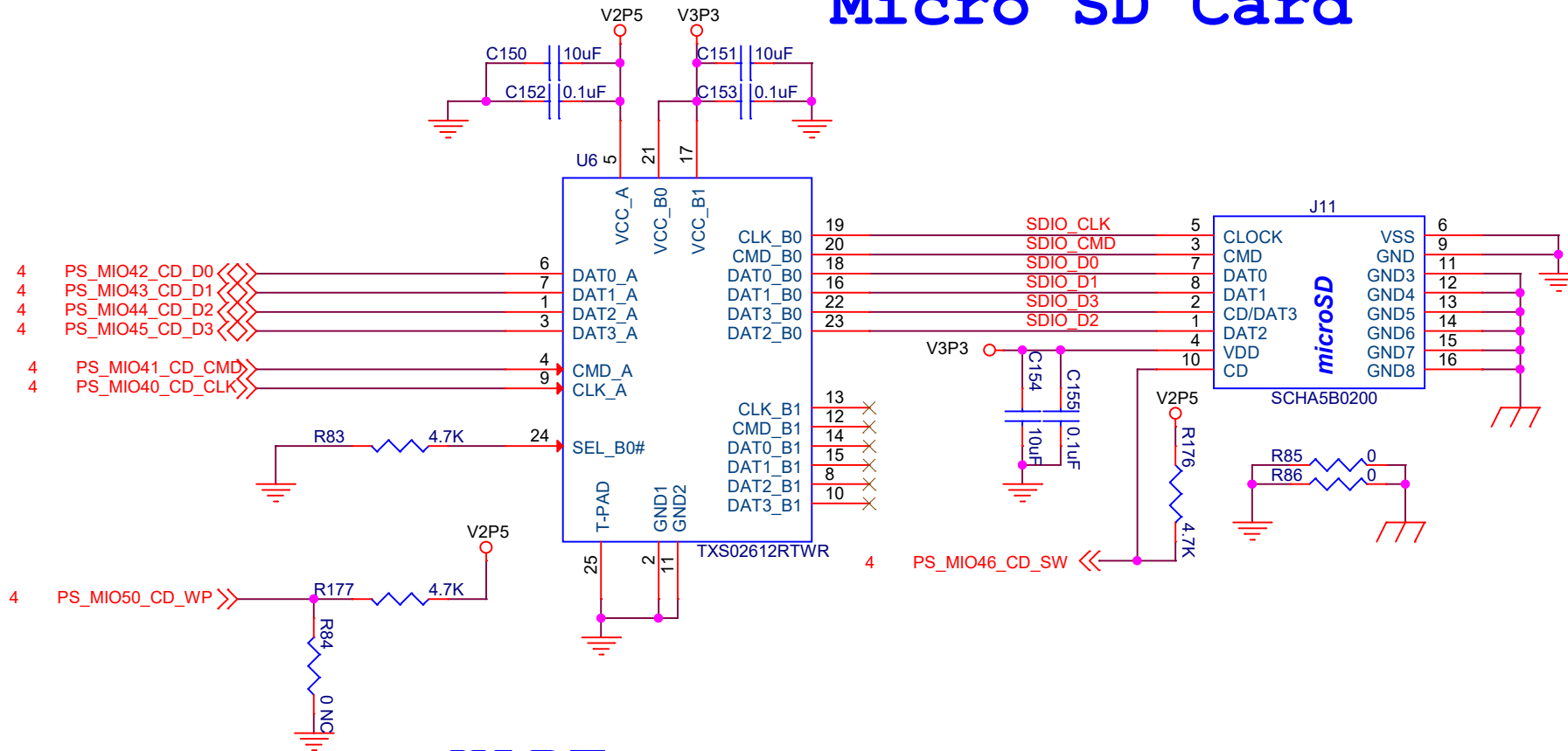


# NAND FLASH

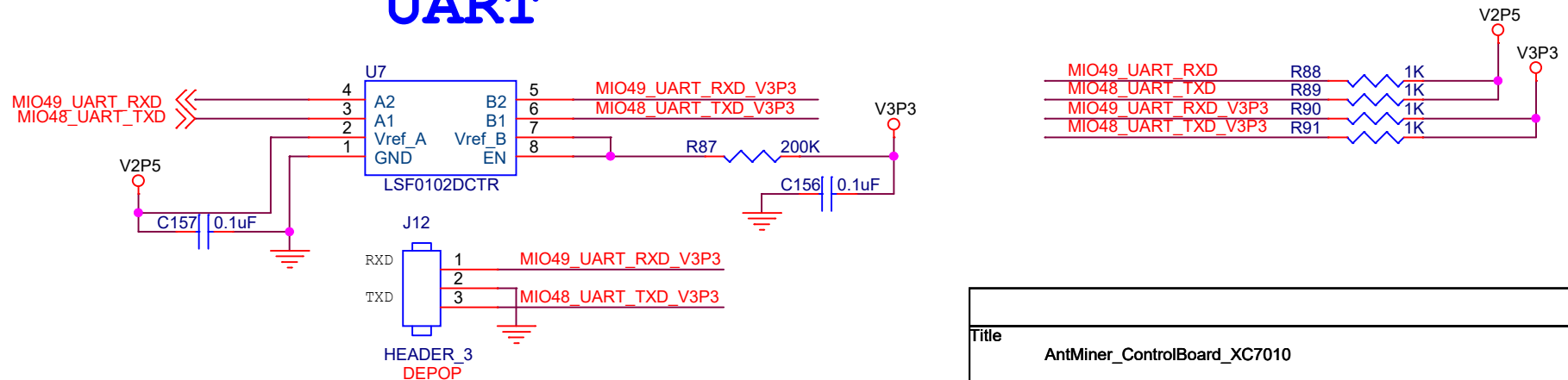


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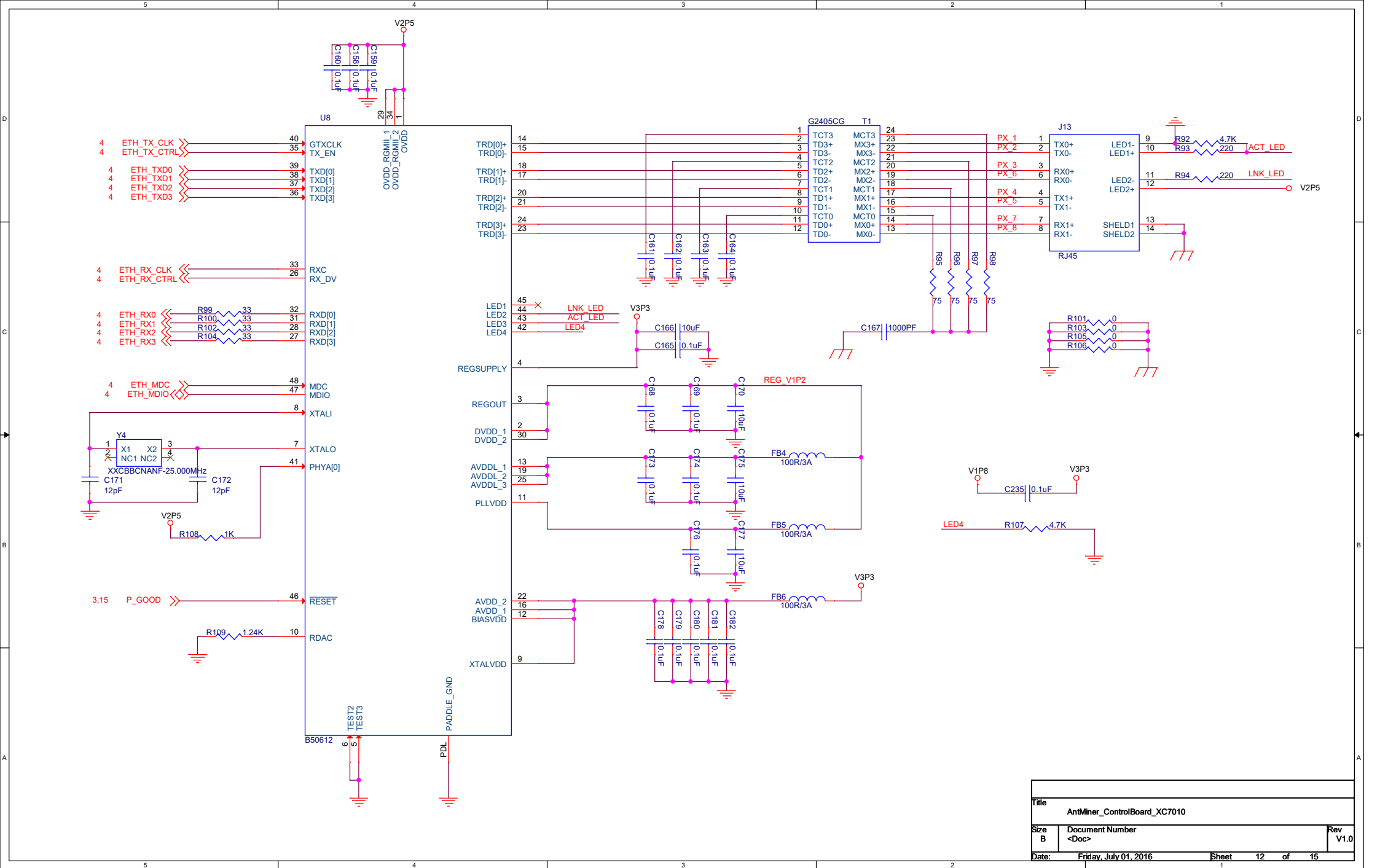
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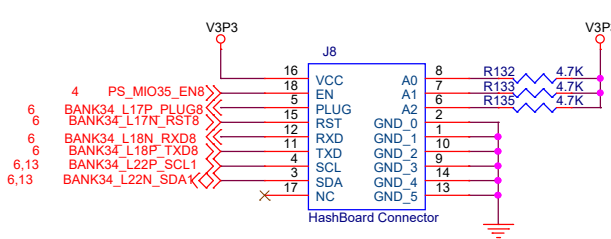
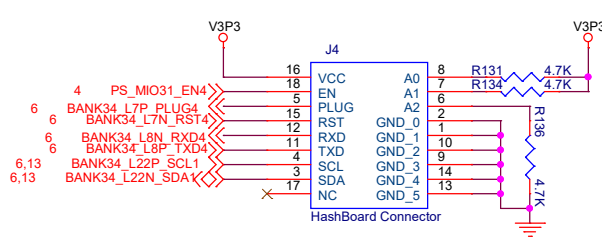
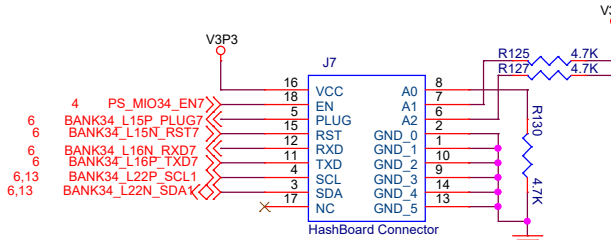
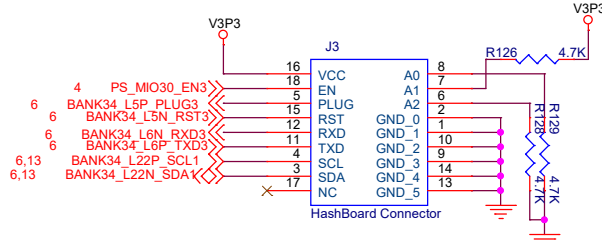
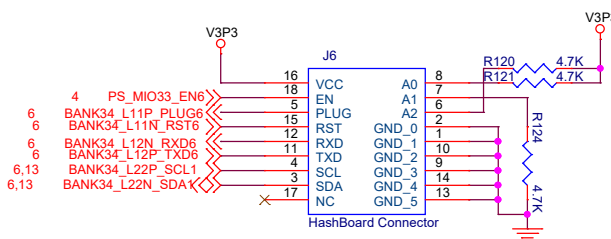
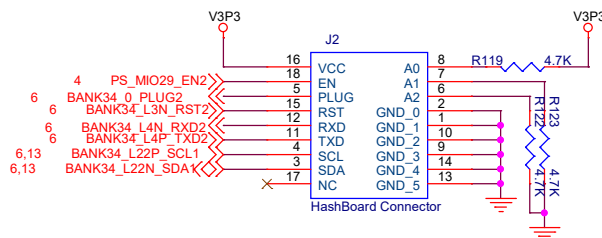
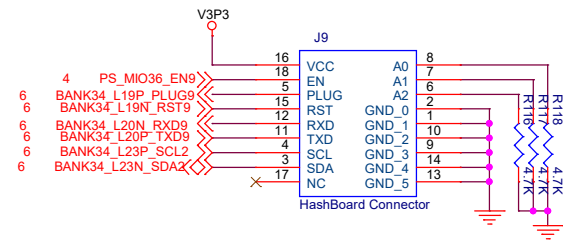
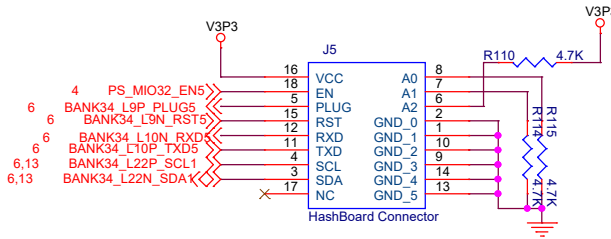
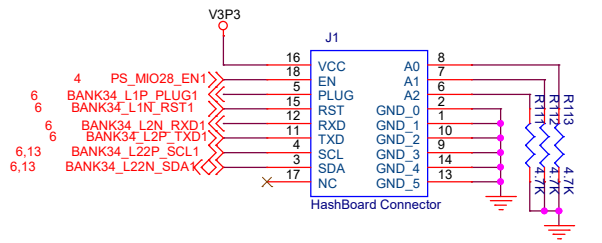
## UART



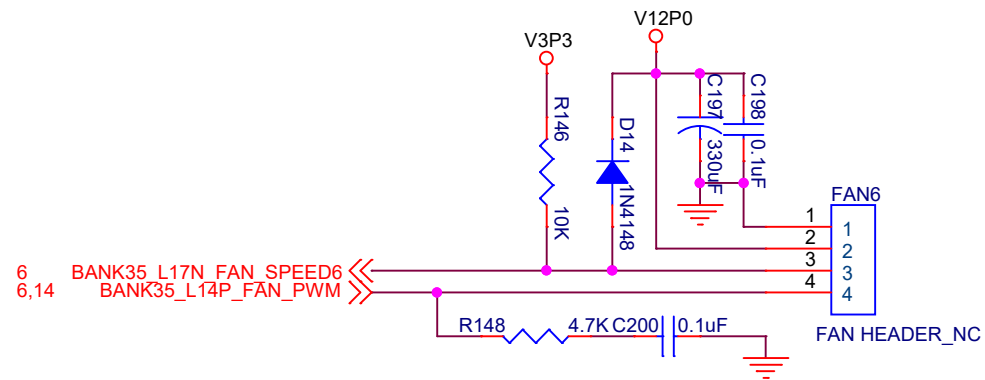
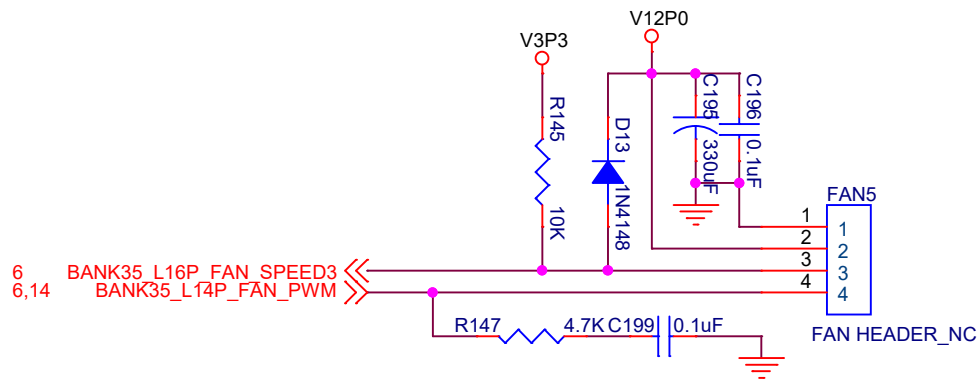
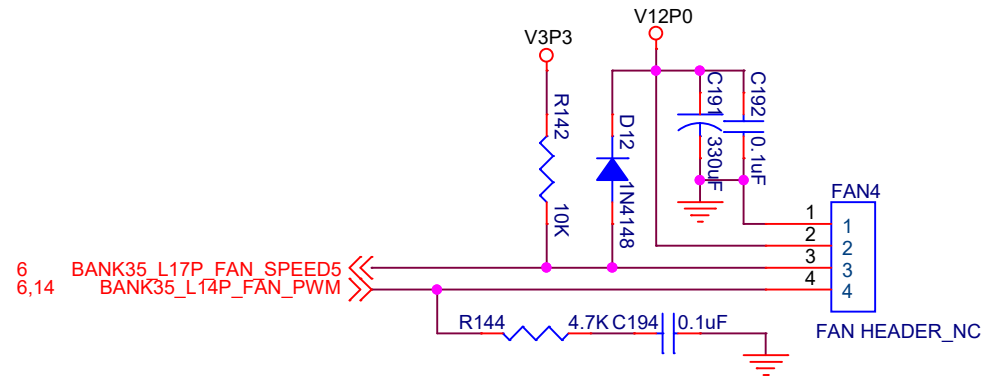
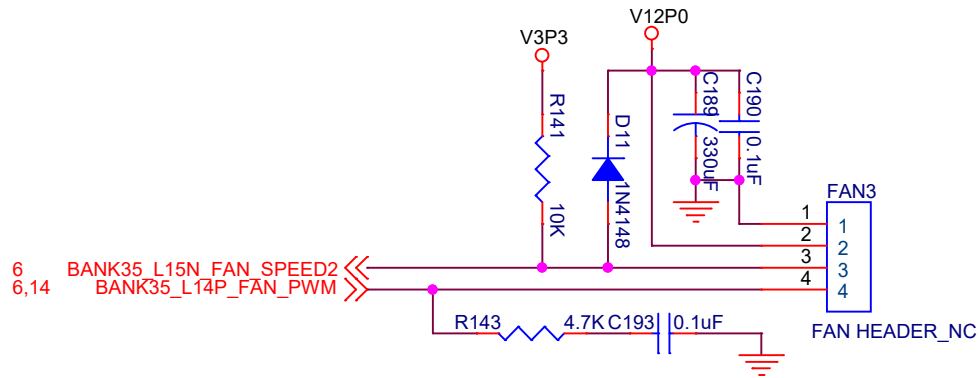
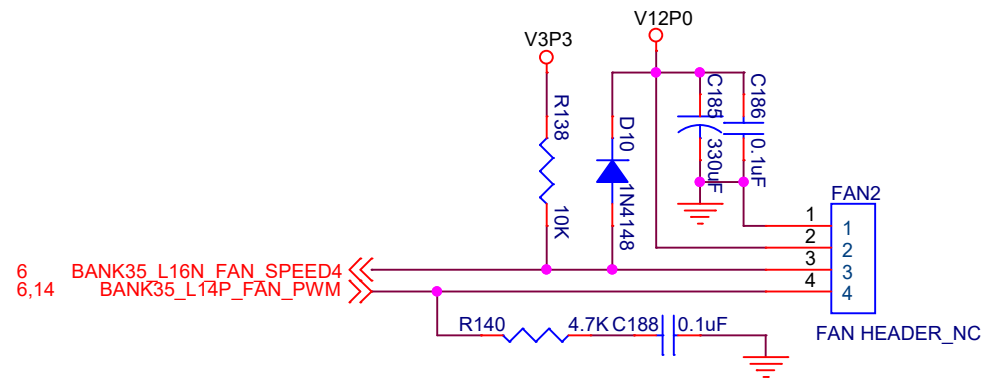
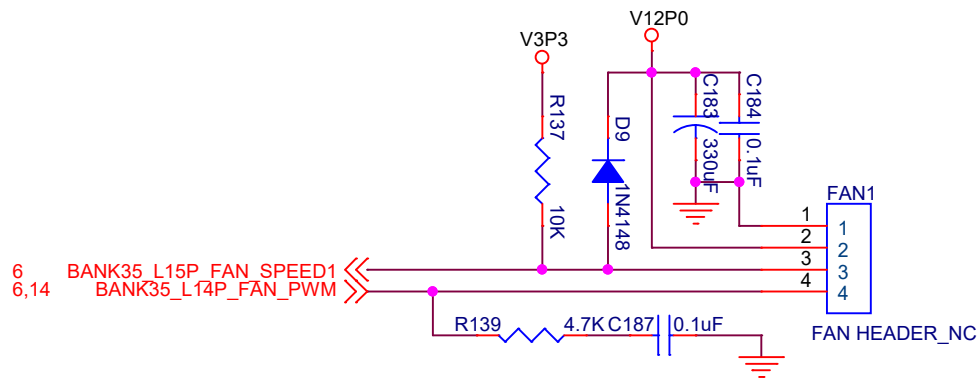
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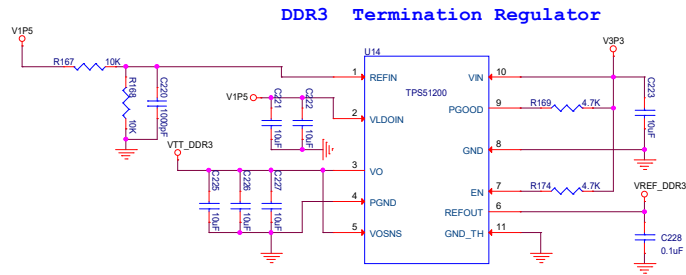
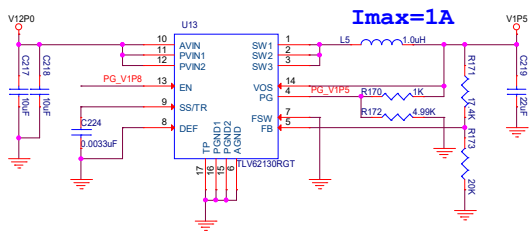
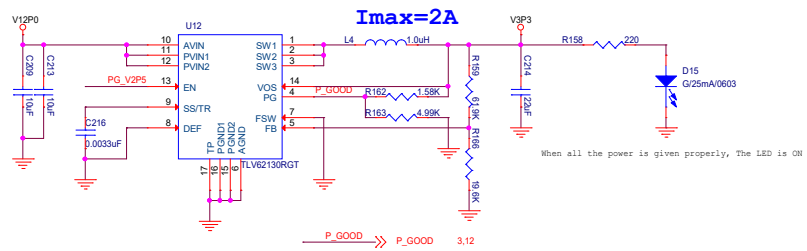
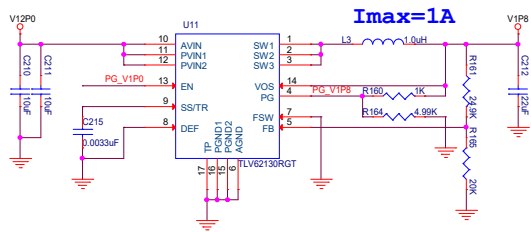
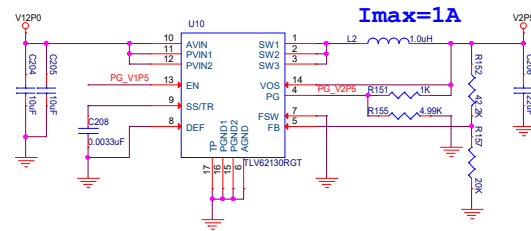
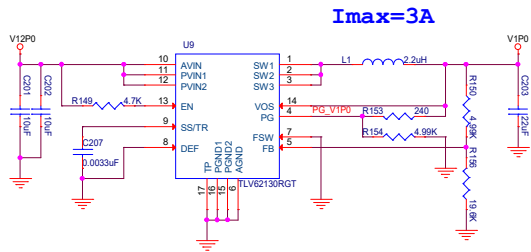
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- BANK34\_L1P\_PLUG1
- BANK34\_L1N\_RST1
- BANK34\_L2P\_TXD1
- BANK34\_L2N\_RXD1
- PS\_MIO29\_EN2
- BANK34\_0\_PLUG2
- BANK34\_L3N\_RST2
- BANK34\_L4P\_TXD2
- BANK34\_L4N\_RXD2
- PS\_MIO30\_EN3
- BANK34\_L5P\_PLUG3
- BANK34\_L5N\_RST3
- BANK34\_L6P\_TXD3
- BANK34\_L6N\_RXD3
- PS\_MIO31\_EN4
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- BANK34\_L7N\_RST4
- BANK34\_L8P\_TXD4
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### 12V Power CONN

