DEPARTMENT OF INFORMATION TECHNOLOGY

NATIONAL INSTITUTE OF TECHNOLOGY SRINAGAR

Microprocessor Lab Assignment

Note:

- Use hardware description languages such as Verilog or VHDL to complete the following assignments.
- A maximum of two students are allowed to form a group for the assignment.
- However, if any of the students in the group is not able to explain the work done, he/she will get zero marks.

Submission Timeline:
Part 1 and 2 - 14/11/2024 (group B) and **15/11/2024 (group A)**
Part 3: Will be informed.

Part 1:

1) Design a 4-bit equality comparator circuit that has two 4-bit binary inputs (A and B) and outputs a logic-1 if both inputs are equal.
2) Design a 4-bit adder.
3) Design the circuits for multiplication.
4) Design the circuits for division.

Part 2:

1) Implement an Arithmetic Logic Unit (ALU).

   Required: Develop an ALU that takes two 8-bit inputs A and B, and executes the following six instructions: **add, sub, and, or, xor, nor**.

The ALU generates an 8-bit output that we call ‘Result’ and an additional 1-bit flag ‘Zero’ that will be set to ‘logic-1’ if all the bits of ‘Result’ are 0.

Note: Draw a block diagram that will implement the ALU operations listed above.

Part 3:

1) Design an in-order processor, in which the main execution unit , that is , ALU is at least able to perform functions listed in Part 2 of the assignment.