Verification Report

[Project Name]

# Verification Plan

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| **No.** | **Feature** | **Test Description** | **Ref.** | **Type** | **Result** | **Comments** |
| 1 | **HREADY** signal high/low. | The HREADY signal indicates whether the transfer is pending or complete. | IHI0033.pdf/Sec.1.2/ pg. no. 1-5  IHI0033.pdf/Sec.4.1/ pg. no. 4-2 | Transfer  T | **HREADY** is HIGH, it indicates no wait state or indicating that the current transfer is completing.  **HREADY** is LOW, it indicates wait state. | A slave can request that the master extends the data phase by using HREADY. This signal, when LOW, causes wait states to be inserted into the transfer and enables the slave to have extra time to provide or sample data. |
| 2 | Enable or Disable the **HWRITE** | HWRITE controls the direction of data transfer to or from the master. | IHI0033.pdf/Sec.3.1/ pg. no. 3-2 | Transfer  T | **HWRITE** is HIGH, it indicates a write transfer and the master broadcasts data on the write data bus, **HWDATA[31:0]**  **HWRITE** is LOW, a read transfer is performed and the slave must generate the data on the read data bus, **HRDATA[31:0]** | For write operations the master holds the data stable throughout the extended cycles.  For read transfers the slave does not have to provide valid data until the transfer is about to complete. |
| 3 | Assert the **HMASTLOCK** | If the master requires locked accesses then it must also assert the HMASTLOCK signal. | IHI0033.pdf/Sec.3.3/ pg. no. 3-7 | Locked transfer  A | This signal indicates to any slave that the current transfer sequence is indivisible and must therefore be processed before any other transactions are processed. | Ensuring that the slave does not perform other operations between the read and write phases of a microprocessor SWP instruction.  After a locked transfer, it is recommended that the master inserts an IDLE transfer. |
| 4 | Four-beat wrapping burst, WRAP4 | A write transfer using a four-beat wrapping burst, with a wait state added for the first transfer. | IHI0033.pdf/Sec.3.5.3/  pg. no. 3-11 | Burst operation  T | The transfer to address 0x3C is followed by a transfer to address 0x30 | The burst is a four-beat burst of word transfers, the address wraps at 16-byte boundaries, and the transfer to address 0x3C is followed by a transfer to address 0x30. |
| 5 | Four-beat incrementing burst, INCR4 | A read transfer using a four-beat incrementing burst, with a wait state added for the first transfer. | IHI0033.pdf/Sec.3.5.3/  pg. no. 3-12 | Burst operation  T | The address 0x3C is followed by a transfer to address 0x40. | The address does not wrap at a  16-byte boundary and the address 0x3C is followed by a transfer to address 0x40. |
| 6 | Undefined Length Burst, INCR | Incrementing bursts of undefined length. | IHI0033.pdf/Sec.3.5.3/  pg. no. 3-14 | Burst operation  T | The first burst starting at address  0x20. These transfer addresses increment by two.  The second burst starting at address  0x5C. These transfer addresses increment by four. | We do two bursts. The first burst is a write consisting of two half word transfers starting at address 0x20. These transfer addresses increment by two.  The second burst is a read consisting of three word transfers starting at address 0x5C. These transfer addresses increment by four. |
| 7 | **HPROT[3:0]** set to b0011 | The protection control signals, HPROT[3:0], provide additional information about a bus access | IHI0033.pdf/Sec.3.7/  pg. no. 3-22 | Protection control  A | non-cacheable,  non-bufferable, privileged, data access | The HPROT control signals have exactly the same timing as the address bus. |
| 8 | Default Slave | default slave to provide a response when any of the non-existent address locations are accessed | IHI0033.pdf/Sec.4.1.1/  pg. no. 4-2 | Address decoding | Default slave provides an **ERROR** response  and  **IDLE** or **BUSY** transfers. | IDLE or BUSY transfers to non-existent locations result in a zero wait state OKAY  Response. |
| 9 | **HRESP** is 0. | The transfer has either completed successfully or additional cycles are required for the slave to complete the request. | IHI0033.pdf/Sec.5.1/  pg. no. 5-2 | R | **OKAY** | The HREADY signal indicates whether the transfer is pending or complete. |
| 10 | **HRESP** is 1. | An error has occurred during the transfer. | IHI0033.pdf/Sec.5.1/  pg. no. 5-2 | R | **ERROR** | The error condition must be signalled to the master so that it is aware the transfer has been unsuccessful.  A two-cycle response is required for an error condition with HREADY being asserted in the second cycle. |

## Explanation of Different Fields

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| **No.** | The serial number of the test. |
| **Feature** | The feature which the current test is verifying in full or partially. The feature is usually on the abstraction level of a user. |
| **Test Description** | A detailed description of the test case being performed. You can be as verbose as you want. |
| **Ref.** | Reference to the section in the related standard document. The section number as well as page numbers should be described here. |
| **Type** | Type of the test. Whether the test is an assertion (A) or a transaction (T) type or a response (R). |
| **Result** | Pass (P) or Fail (F). |
| **Comments** | Any other comments about the test or its results that you want to mention. |