Verification Report

[Project Name]

# Verification Plan

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| **No.** | **Feature** | **Test Description** | **Ref.** | **Type** | **Result** | **Expected Outcome** | **Comments** |
| 1 | **HREADY** signal high. | **HREADY** is HIGH, it indicates no wait state or indicating that the current transfer is completing. | IHI0033.pdf/Sec.1.2/ pg. no. 1-5  IHI0033.pdf/Sec.4.1/ pg. no. 4-2 | T | Current transfer is complete. |  |  |
| 2 | **HREADY** signal low. | **HREADY** is LOW, it indicates wait state. | IHI0033.pdf/Sec.1.2/ pg. no. 1-5 | T | Transfer Pending. |  |  |
| 3 | Write transfer. | **HWRITE** is HIGH, it indicates a write transfer and the master broadcasts data on the write data bus, **HWDATA[31:0]** | IHI0033.pdf/Sec.3.1/ pg. no. 3-2 | T | Write successfully. |  | For write operations the master holds the data stable throughout the extended cycles.  HRESP should be low and HREADY should be high. |
| 4 | Read transfer. | **HWRITE** is LOW, a read transfer is performed and the slave must generate the data on the read data bus, **HRDATA[31:0]** | IHI0033.pdf/Sec.3.1/ pg. no. 3-2 | T | Read successfully. |  | For read transfers the slave does not have to provide valid data until the transfer is about to complete.  HRESP should be low and HREADY should be high. |
| 5 | Master Signal: IDLE  **HTRANS [1:0] =b00** | When the **IDLE** transfer is inserted to an address. | IHI0033.pdf/Sec.3.2/ pg. no. 3-5 | A | The transfer must be ignored by the slave. Slaves must provide a zero-wait OKAY response. |  |  |
| 6 | Master Signal  **HTRANS [1:0] =b01** | A **BUSY** transfer is inserted and the address and control signals must reflect the next burst transfer | IHI0033.pdf/Sec.3.2/ pg. no. 3-5 | A | Slaves must always provide a zero-wait state OKAY. The transfer must be ignored by the slave |  |  |
| 7 | Assert the **HMASTLOCK** | If the master requires locked accesses then it must also assert the **HMASTLOCK** signal. | IHI0033.pdf/Sec.3.3/ pg. no. 3-7 | A | This signal indicates to any slave that the current transfer sequence is indivisible and must therefore be processed before any other transactions are processed. |  | Ensuring that the slave does not perform other operations between the read and write phases of a microprocessor SWP instruction.  After a locked transfer, it is recommended that the master inserts an IDLE transfer. |
| 8 | Four-beat wrapping burst, WRAP4 | A write transfer using a four-beat wrapping burst, with a wait state added for the first transfer. | IHI0033.pdf/Sec.3.5.3/  pg. no. 3-11 | T | The transfer to address 0x3C is followed by a transfer to address 0x30 |  | The burst is a four-beat burst of word transfers, the address wraps at 16-byte boundaries, and the transfer to address 0x3C is followed by a transfer to address 0x30. |
| 9 | Four-beat incrementing burst, INCR4 | A read transfer using a four-beat incrementing burst, with a wait state added for the first transfer. | IHI0033.pdf/Sec.3.5.3/  pg. no. 3-12 | T | The address 0x3C is followed by a transfer to address 0x40. |  | The address does not wrap at a  16-byte boundary and the address 0x3C is followed by a transfer to address 0x40. |
| 10 | Undefined Length Burst, INCR | Incrementing bursts of undefined length. | IHI0033.pdf/Sec.3.5.3/  pg. no. 3-14 | T | The first burst starting at address  0x20. These transfer addresses increment by two.  The second burst starting at address  0x5C. These transfer addresses increment by four. |  | We do two bursts. The first burst is a write consisting of two half word transfers starting at address 0x20. These transfer addresses increment by two.  The second burst is a read consisting of three word transfers starting at address 0x5C. These transfer addresses increment by four. |
| 11 | **HTRANS**: Transfer type changes | Transfer type changes from **IDLE** to **NONSEQ** during waited states. | IHI0033.pdf/Sec.3.6.1/  pg. no. 3-16 | A | Successfully transfer type changed. Slaves must give the OKAY response. |  | After change, the HTRANS signal must be kept constant after the transition until HREADY is high |
| 12 | **HTRANS**: Transfer type changes | Transfer type changes from **BUSY** to **SEQ** during waited states for fixed-length bursts. | IHI0033.pdf/Sec.3.6.1/  pg. no. 3-17 | A | Successfully transfer type changed. Slaves must give the OKAY response. |  | After change, The HTRANS signal must be kept constant after the transition until HREADY is high |
| 13 | **HTRANS**: Transfer type changes | Transfer type changes from **BUSY** to **any other type** during waited states for undefined length burst, when HREADY is LOW. The burst continues if an SEQ transfer is performed but terminates if an IDLE or NONSEQ transfer is performed. | IHI0033.pdf/Sec.3.6.1/  pg. no. 3-18 | A | Successfully transfer type changed. Slaves must give the OKAY response. |  |  |
| 14 | **HPROT[3:0]** set to b0011 | The protection control signals, **HPROT[3:0],** provide additional information about a bus access | IHI0033.pdf/Sec.3.7/  pg. no. 3-22 | A | non-cacheable,  non-bufferable, privileged, data access |  | The HPROT control signals have exactly the same timing as the address bus. |
| 15 | Default Slave: **NONSEQUENTIAL** or **SEQUENTIAL** transfers | a **NONSEQUENTIAL** or **SEQUENTIAL** transfer is attempted to a non-existent address location | IHI0033.pdf/Sec.4.1.1/  pg. no. 4-2 | A | Default slave provides an **ERROR** response |  |  |
| 16 | Default Slave: **IDLE** or **BUSY** transfers | **IDLE** or **BUSY** transfers to non-existent locations | IHI0033.pdf/Sec.4.1.1/  pg. no. 4-2 | A | zero wait state OKAY  Response. |  |  |
| 17 | Slave transfer response: Done | The transfer has completed successfully when **HREADY** is high and **HRESP** is  **OKAY**. | IHI0033.pdf/Sec.5.1.1/  pg. no. 5-3 | A | Transfer completed successfully |  |  |
| 18 | Slave transfer response: Pending | Additional cycles are required for the slave to complete the request. An error has occurred during the transfer. In this case when transfer is pending **HREADY** is low and **HRESP** is  **OKAY**. | IHI0033.pdf/Sec.5.1.2/  pg. no. 5-3 | A | Transfer is pending. |  |  |
| 19 | Slave transfer response: Failed | In the first cycle, to start the **ERROR** response, the slave drives **HRESP** high to indicate **ERROR** while driving **HREADY** low to extend the transfer for one extra cycle. In the next cycle **HREADY** is driven high to end the transfer and **HRESP** remains driven high to indicate **ERROR.** | IHI0033.pdf/Sec.5.1.3/  pg. no. 5-3 | A | Transfer is failed |  | The error condition must be signalled to the master so that it is aware the transfer has been unsuccessful. |
| 20 | **HCLK** signal | A clock signal **HCLK** is generated. | IHI0033.pdf/Sec.7.1.1/ pg. no. 7-2 | A | All input signals are sampled on the rising edge of HCLK. All output signal changes must occur after the rising edge of HCLK. |  |  |
| 21 | Reset signal **HRESETn** | It is the active LOW signal and reset all bus elements. During reset all masters must ensure the address and control signals are at valid levels and that **HTRANS[1:0]** indicates IDLE and all slaves must ensure that **HREADYOUT** is HIGH. | IHI0033.pdf/Sec.7.1.2/ pg. no. 7-2 | A | Reset done |  |  |

## Explanation of Different Fields

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| **No.** | The serial number of the test. |
| **Feature** | The feature which the current test is verifying in full or partially. The feature is usually on the abstraction level of a user. |
| **Test Description** | A detailed description of the test case being performed. You can be as verbose as you want. |
| **Ref.** | Reference to the section in the related standard document. The section number as well as page numbers should be described here. |
| **Type** | Type of the test. Whether the test is an assertion (A) or a transaction (T) type. |
| **Result** | Pass (P) or Fail (F). |
| **Comments** | Any other comments about the test or its results that you want to mention. |