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# Exercise 3 Verification Report

## Component

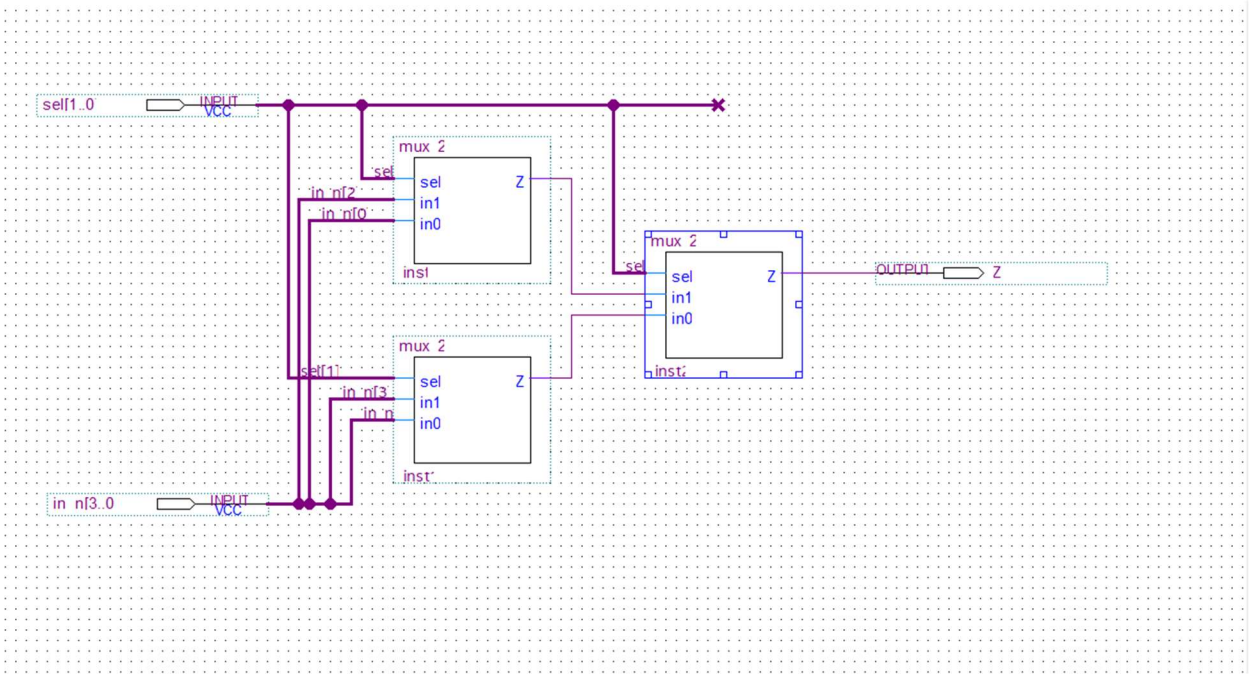



**Figure 1: Multiplexor Visual Schematic**

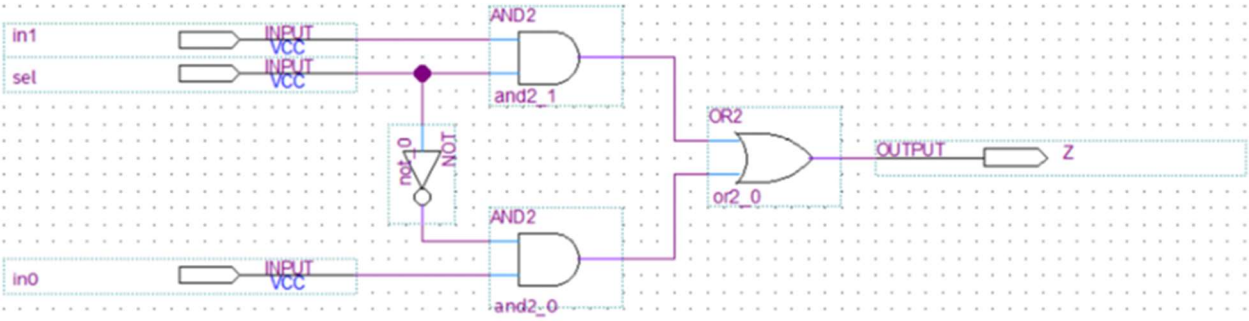



**Figure 2: Multiplexor Component Visual Schematic**

The purpose of this exercise was to create a multiplexor or MUX, a combinational circuit that connects 1 of N input signals to a single output. A MUX is a key component for designing the circuitry of a computer. For this particular exercise, a two input MUX component as shown in Figure 2: Multiplexor Component Visual Schematic was used as a component to form the main MUX as seen in Figure 1: Multiplexor Visual Schematic.

**MUX Signature**

- INPUTS:
    - Sel bus from 0 - 1
    - Input bus from 0 - 3
- OUTPUTS:
    - Z of either 0 or 1

**Verification Tests**

Port Mapping

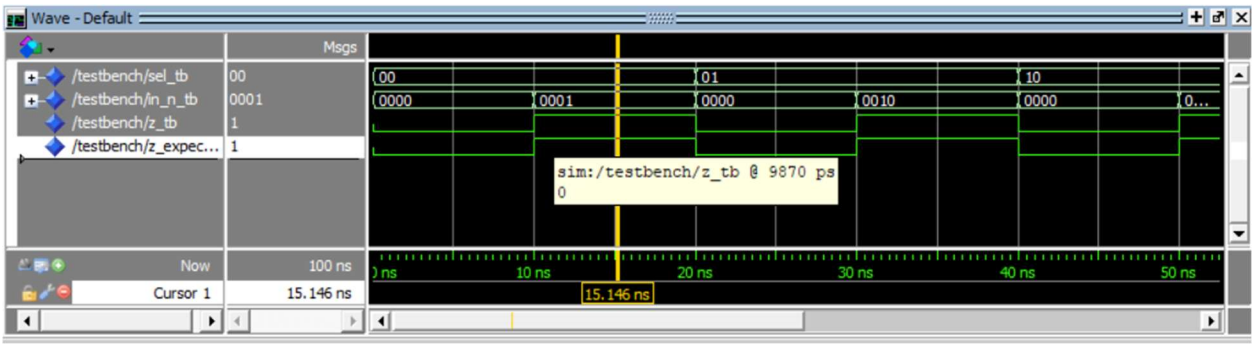
sel[0..1] => sel_tb

input_n[3..0] => in_n_tb

Z => z_tb

| sel_tb | in_n_tb | z_tb | z_expected |
|---|---|---|---|
| 00 | 0000 | 0 | 0 |
| 00 | 0001 | 1 | 1 |
| 01 | 0000 | 0 | 0 |
| 01 | 0010 | 1 | 1 |
| 10 | 0000 | 0 | 0 |
| 10 | 0100 | 1 | 1 |
| 11 | 0000 | 0 | 0 |
| 11 | 1000 | 1 | 1 |

**Figure 3: Port Mapping and Truth Table**


Wave - Default
Msgs
/testbench/sel_tb
/testbench/in_n_tb
/testbench/z_tb
/testbench/z_expec...
00
0001
1
1
sim:/testbench/z_tb @ 9870 ps
0
Now
100 ns
Cursor 1
15.146 ns
10 ns
20 ns
30 ns
40 ns
50 ns


Wave - Default
Msgs
/testbench/sel_tb
/testbench/in_n_tb
/testbench/z_tb
/testbench/z_expec...
01
0000
0
0
Now
100 ns
Cursor 1
24.846 ns
10 ns
20 ns
30 ns
40 ns
50 ns


Wave - Default
Msgs
/testbench/sel_tb
/testbench/in_n_tb
/testbench/z_tb
/testbench/z_expec...
01
0010
1
1
Now
100 ns
Cursor 1
35.142 ns
10 ns
20 ns
30 ns
40 ns
50 ns

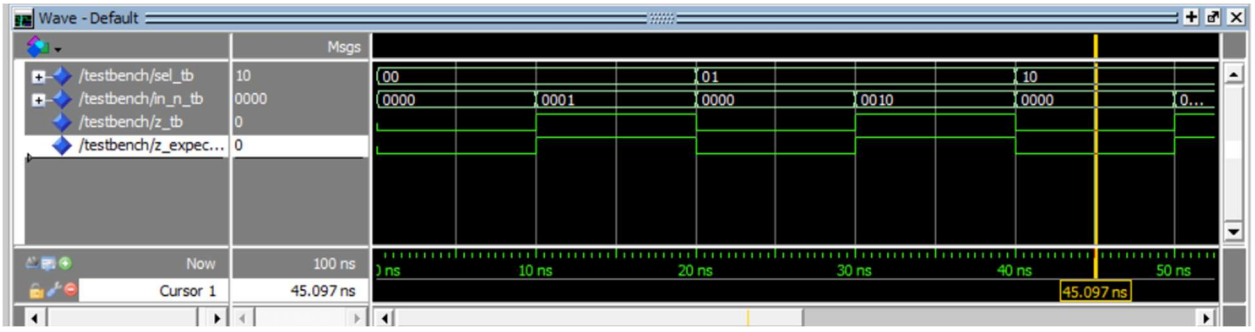

Wave - Default
Msgs
/testbench/sel_tb
/testbench/in_n_tb
/testbench/z_tb
/testbench/z_expec...
10
0000
0
0
Now
100 ns
Cursor 1
45.097 ns
10 ns
20 ns
30 ns
40 ns
50 ns


**Figure 4: Verification Test Results**

```
# ** Note: Output correct for in_n[0] = 0
#    Time: 10 ns  Iteration: 0  Instance: /testbench
# ** Note: Output correct for in_n[0] = 1
#    Time: 20 ns  Iteration: 0  Instance: /testbench
# ** Note: Output correct for in_n[1] = 0
#    Time: 30 ns  Iteration: 0  Instance: /testbench
# ** Note: Output correct for in_n[1] = 1
#    Time: 40 ns  Iteration: 0  Instance: /testbench
# ** Note: Output correct for in_n[2] = 0
#    Time: 50 ns  Iteration: 0  Instance: /testbench
# ** Note: Output correct for in_n[2] = 1
#    Time: 60 ns  Iteration: 0  Instance: /testbench
# ** Note: Output correct for in_n[3] = 0
#    Time: 70 ns  Iteration: 0  Instance: /testbench
# ** Note: Output correct for in_n[3] = 1
#    Time: 80 ns  Iteration: 0  Instance: /testbench
```

**Figure 5: Verification Test Results with Assert Statements**

Figure 3 – 5 displays the verification and testing process of the MUX schematic. The test results suggest that the verification test results from ModelSim match that of the expected output and the truth table; therefore, the MUX schematic is correct and passed all tests.