Majority Voter Simulation Results

Schematic

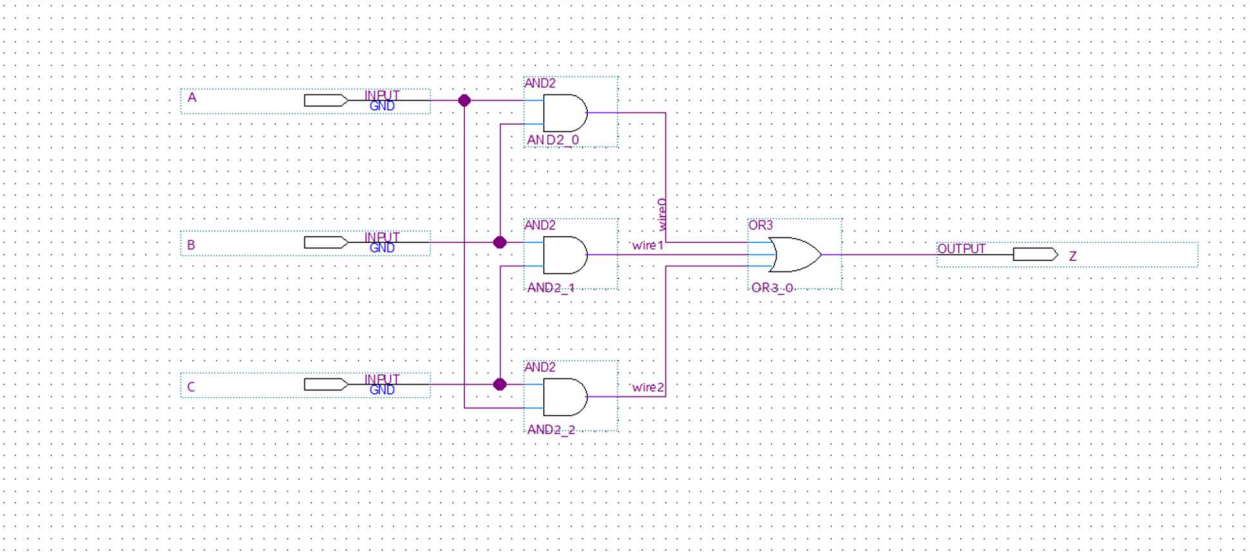
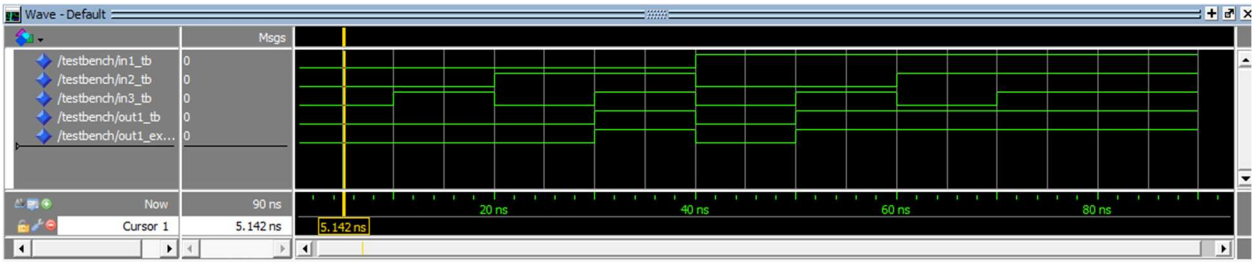
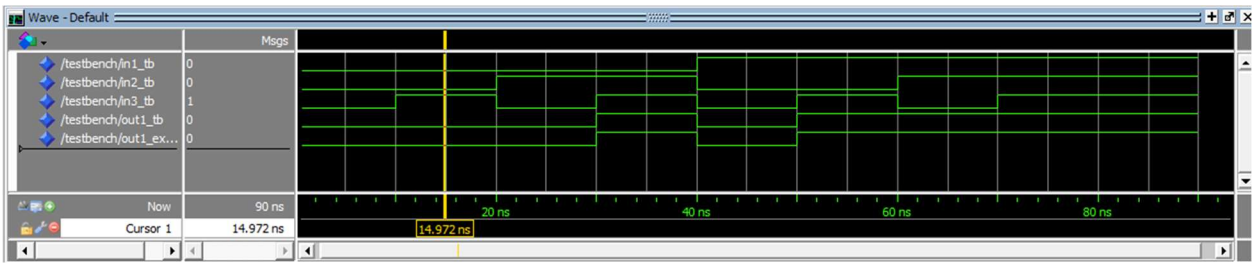


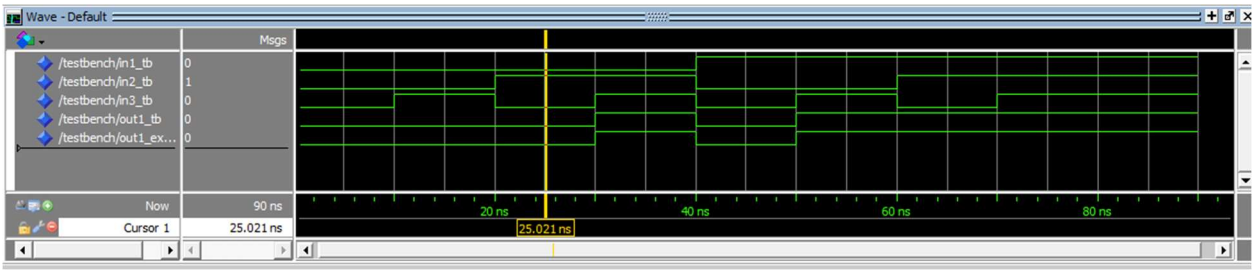
Figure 1: Majority Voter Schematic

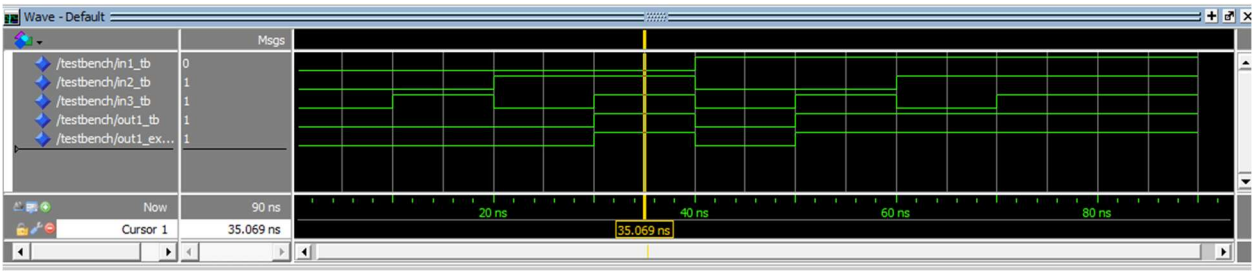
The figure above illustrates the majority voter schematic which takes in the three inputs (A, B, C) and outputs the majority value (Z). In other words, two of the three inputs were 0 and the third was 1, then the output would be a 0 and vice versa.

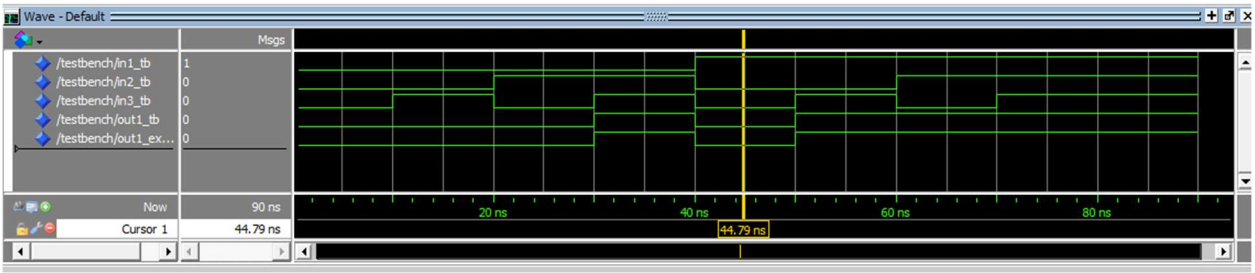
Verification Tests and Results

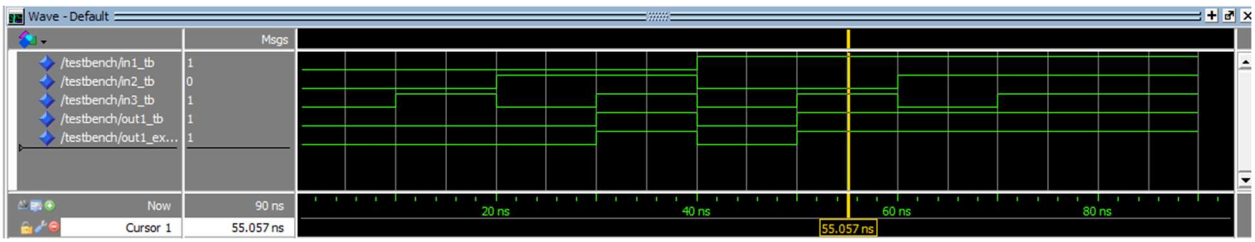


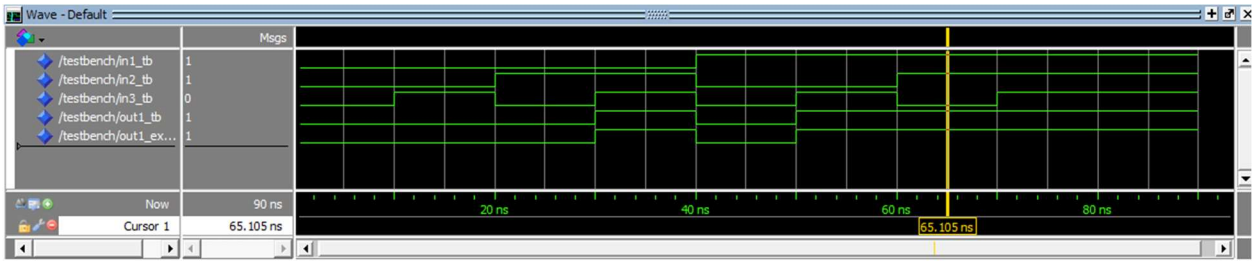



Wave - Default
Msgs
/testbench/in1_tb
/testbench/in2_tb
/testbench/in3_tb
/testbench/out1_tb
/testbench/out1_ex...
0
1
0
0
0
Now
90 ns
Cursor 1
25.021 ns
20 ns
40 ns
60 ns
80 ns
25.021 ns


Wave - Default
Msgs
/testbench/in1_tb
/testbench/in2_tb
/testbench/in3_tb
/testbench/out1_tb
/testbench/out1_ex...
0
1
1
1
1
Now
90 ns
Cursor 1
35.069 ns
20 ns
40 ns
60 ns
80 ns
35.069 ns


Wave - Default
Msgs
/testbench/in1_tb
/testbench/in2_tb
/testbench/in3_tb
/testbench/out1_tb
/testbench/out1_ex...
1
0
0
0
0
Now
90 ns
Cursor 1
44.79 ns
20 ns
40 ns
60 ns
80 ns
44.79 ns


Wave - Default
Msgs
/testbench/in1_tb
/testbench/in2_tb
/testbench/in3_tb
/testbench/out1_tb
/testbench/out1_ex...
1
0
1
1
1
Now
90 ns
Cursor 1
55.057 ns
20 ns
40 ns
60 ns
80 ns
55.057 ns


Wave - Default
Msgs
/testbench/in1_tb
/testbench/in2_tb
/testbench/in3_tb
/testbench/out1_tb
/testbench/out1_ex...
1
1
0
1
1
Now
90 ns
Cursor 1
65.105 ns
20 ns
40 ns
60 ns
80 ns
65.105 ns

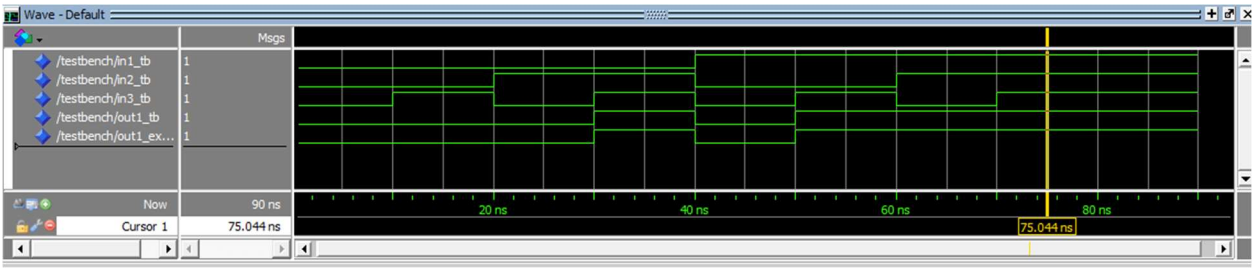


Figure 2: Simulation Results for Verification

The figure above illustrates the simulation results for the verification process. As indicated in the figure above, the actual output matches the expected output for all cases. A truth table of the majority voter schematic and the port mapping is provided below.

in1_tb	in2_tb	in3_tb	out1_tb	out1_expected
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	1	1
1	0	0	0	0
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

A = in1_tb
B = in2_tb
C = in3_tb
Z = out1_tb

Figure 3: Truth Table and Port Mapping

The figure below illustrates the verification with assert statements.

```
# vsim work.testbench
# Start time: 14:27:44 on Sep 11,2022
# Loading std.standard
# Loading std.textio(body)
# Loading ieee.std_logic_1164(body)
# Loading work.testbench(gate_level)
# Loading work.majority_voter0(bdf_type)
# ** Note: Output correct for input = 000
#    Time: 10 ns  Iteration: 0  Instance: /testbench
# ** Note: Output correct for input = 001
#    Time: 20 ns  Iteration: 0  Instance: /testbench
# ** Note: Output correct for input = 010
#    Time: 30 ns  Iteration: 0  Instance: /testbench
# ** Note: Output correct for input = 011
#    Time: 40 ns  Iteration: 0  Instance: /testbench
# ** Note: Output correct for input = 100
#    Time: 50 ns  Iteration: 0  Instance: /testbench
# ** Note: Output correct for input = 101
#    Time: 60 ns  Iteration: 0  Instance: /testbench
# ** Note: Output correct for input = 110
#    Time: 70 ns  Iteration: 0  Instance: /testbench
# ** Note: Output correct for input = 111
#    Time: 80 ns  Iteration: 0  Instance: /testbench

VSIM 3>
```

Figure 4: Simulation Results with Assert Statements