- exception level
  - EL0
    - ↳ general purpose + stack pointer register
    - ↳ STR and LDR instructions
    - ↳ only access virtual memory
  - EL1: kernel
  - EL2: virtual machines
  - EL3: Arm TrustZone
- code must run at equal or higher permission per exception

- steps given exceptions
  1. current instruction in ELR_ELx
  2. current processor state stored in SPSR_ELx
  3. CPU executes exception handler at ELx
  4. calls eret
     - ↳ eret – restores processor state + resumes execution

- sctlr_el1: configure diff. parameters of CPU when CPU operates at EL1