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AND Gate Simulation Results for Verification

AND Gate

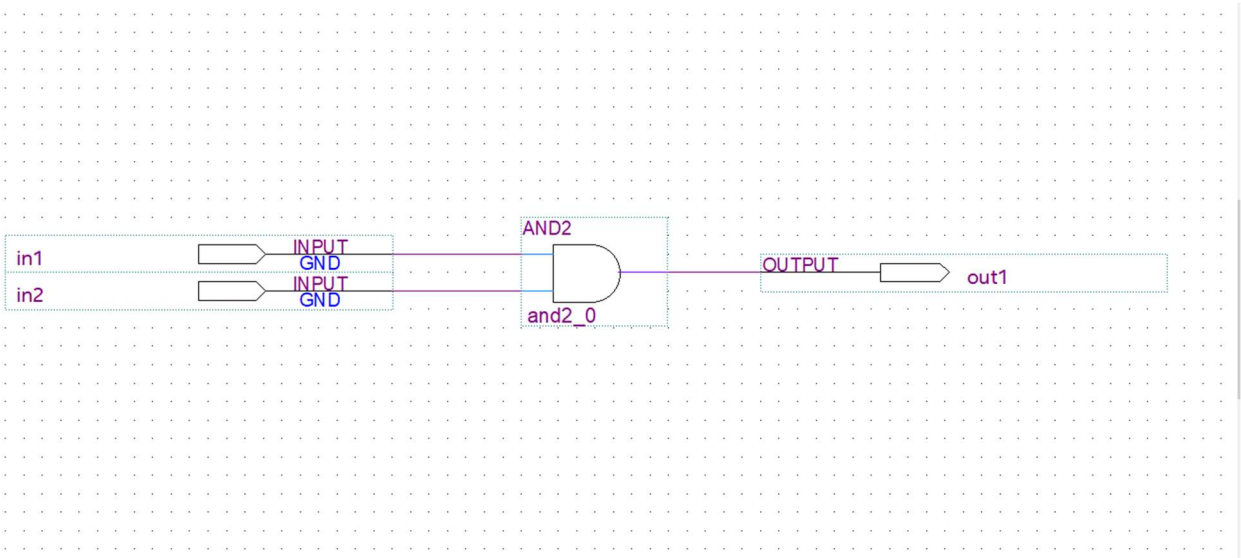

Figure 1: AND Gate

The goal was to create a simple AND gate using Quartus II that has two inputs and one output. This particular schematic has inputs “in1” and “in2” and process them through a single AND gate, “and2_0”, to provide an output “out1”.

Verification Tests

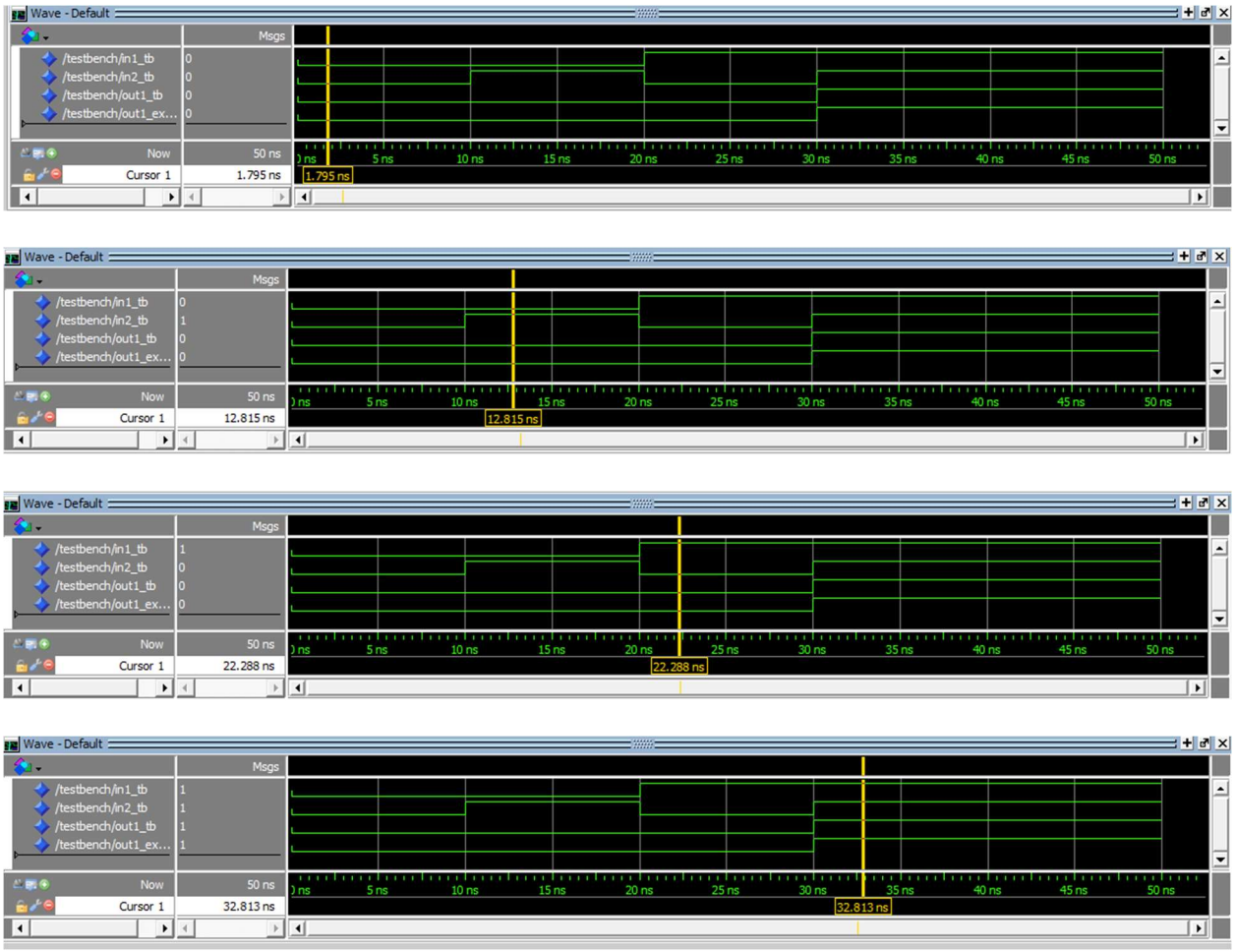

Figure 2: Simulation Results for Verification

The figure above illustrates the simulation results for the verification process. As indicated in the figure above, the actual output matches the expected output for all cases. A truth table of the AND schematic and the port mapping is provided below.

in1_tb	in2_tb	out1_tb	out1_expected
0	0	0	0
0	1	0	0
1	0	0	0
1	1	1	1

in1 => in1_tb
in2 => in2_tb
out1 => out1_tb

Figure 3: Truth Table of Verification Test Results and Port Mapping

The figure below illustrates the simulation results using assert statements.

```
# vsim work.testbench
# Start time: 14:20:58 on Sep 11,2022
# Loading std.standard
# Loading std.textio(body)
# Loading ieee.std_logic_1164(body)
# Loading work.testbench(gate_level)
# Loading work.and_2(bdf_type)
# ** Note: Output correct for input = 00
#    Time: 10 ns  Iteration: 0  Instance: /testbench
# ** Note: Output correct for input = 01
#    Time: 20 ns  Iteration: 0  Instance: /testbench
# ** Note: Output correct for input = 10
#    Time: 30 ns  Iteration: 0  Instance: /testbench
# ** Note: Output correct for input = 11
#    Time: 40 ns  Iteration: 0  Instance: /testbench

VSIM 3>
```

Figure 4: Simulation Results with Assert Statements