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**Exercise 3 Verification Report**

**Component**

A picture containing text, map, shelf

Description automatically generated

**Figure 1: Multiplexor Visual Schematic**

**Diagram, schematic

Description automatically generated**

**Figure 2: Multiplexor Component Visual Schematic**

The purpose of this exercise was to create a multiplexor or MUX, a combinational circuit that connects 1 of N input signals to a single output. A MUX is a key component for designing the circuitry of a computer. For this particular exercise, a two input MUX component as shown in Figure 2: Multiplexor Component Visual Schematic was used as a component to form the main MUX as seen in Figure 1: Multiplexor Visual Schematic.

**MUX Signature**

* INPUTS:
  + Sel bus from 0 - 1
  + Input bus from 0 - 3
* OUTPUTS:
  + Z of either 0 or 1

**Verification Tests**

Port Mapping

sel[0..1] => sel\_tb

input\_n[3..0] => in\_n\_tb

Z => z\_tb

|  |  |  |  |
| --- | --- | --- | --- |
| **sel\_tb** | **in\_n\_tb** | **z\_tb** | **z\_expected** |
| 00 | 0000 | 0 | 0 |
| 00 | 0001 | 1 | 1 |
| 01 | 0000 | 0 | 0 |
| 01 | 0010 | 1 | 1 |
| 10 | 0000 | 0 | 0 |
| 10 | 0100 | 1 | 1 |
| 11 | 0000 | 0 | 0 |
| 11 | 1000 | 1 | 1 |

**Figure 3: Port Mapping and Truth Table**

Graphical user interface

Description automatically generated

Graphical user interface

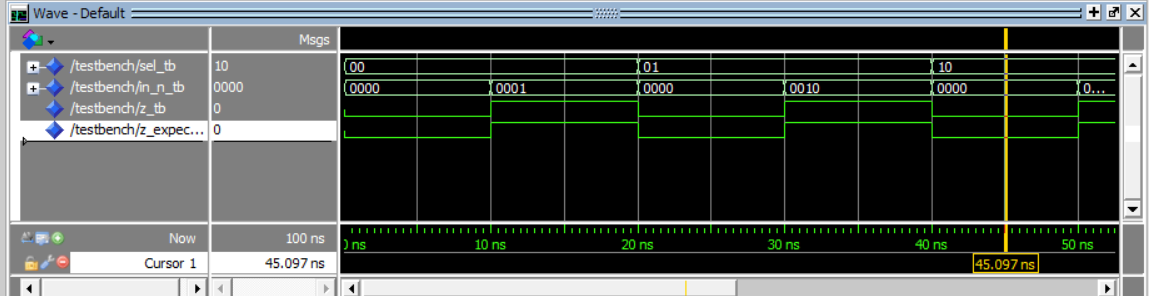
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Graphical user interface

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**Figure 4: Verification Test Results**

**Text

Description automatically generated**

**Figure 5: Verification Test Results with Assert Statements**

Figure 3 – 5 displays the verification and testing process of the MUX schematic. The test results suggest that the verification test results from ModelSim match that of the expected output and the truth table; therefore, the MUX schematic is correct and passed all tests.