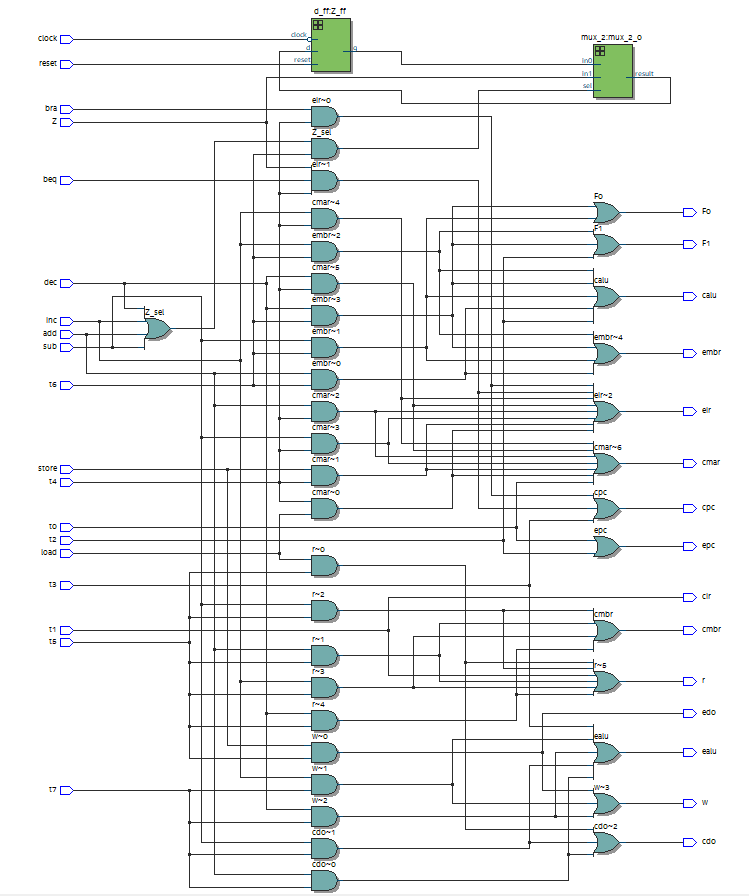
Tyler Kim

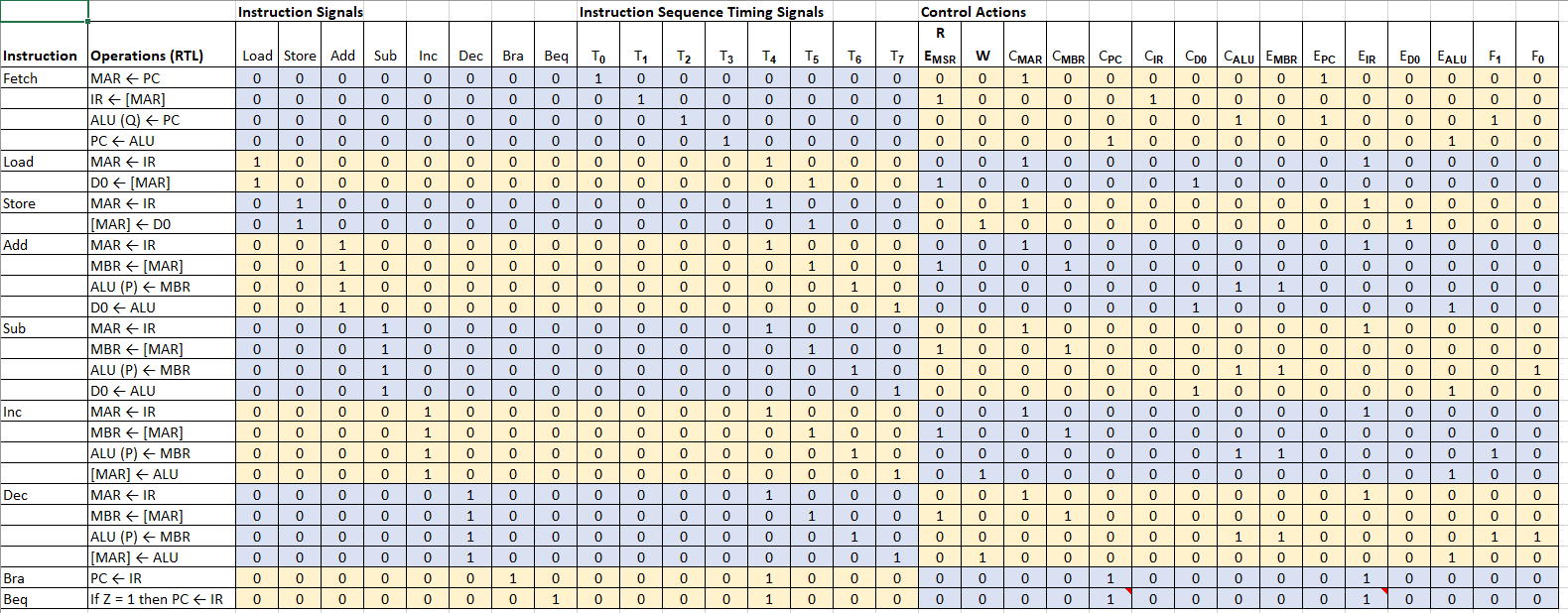
Digital Logic Design

***Control Signal Logic***

**Component**



**Figure 1: Control Signal Logic Schematic**



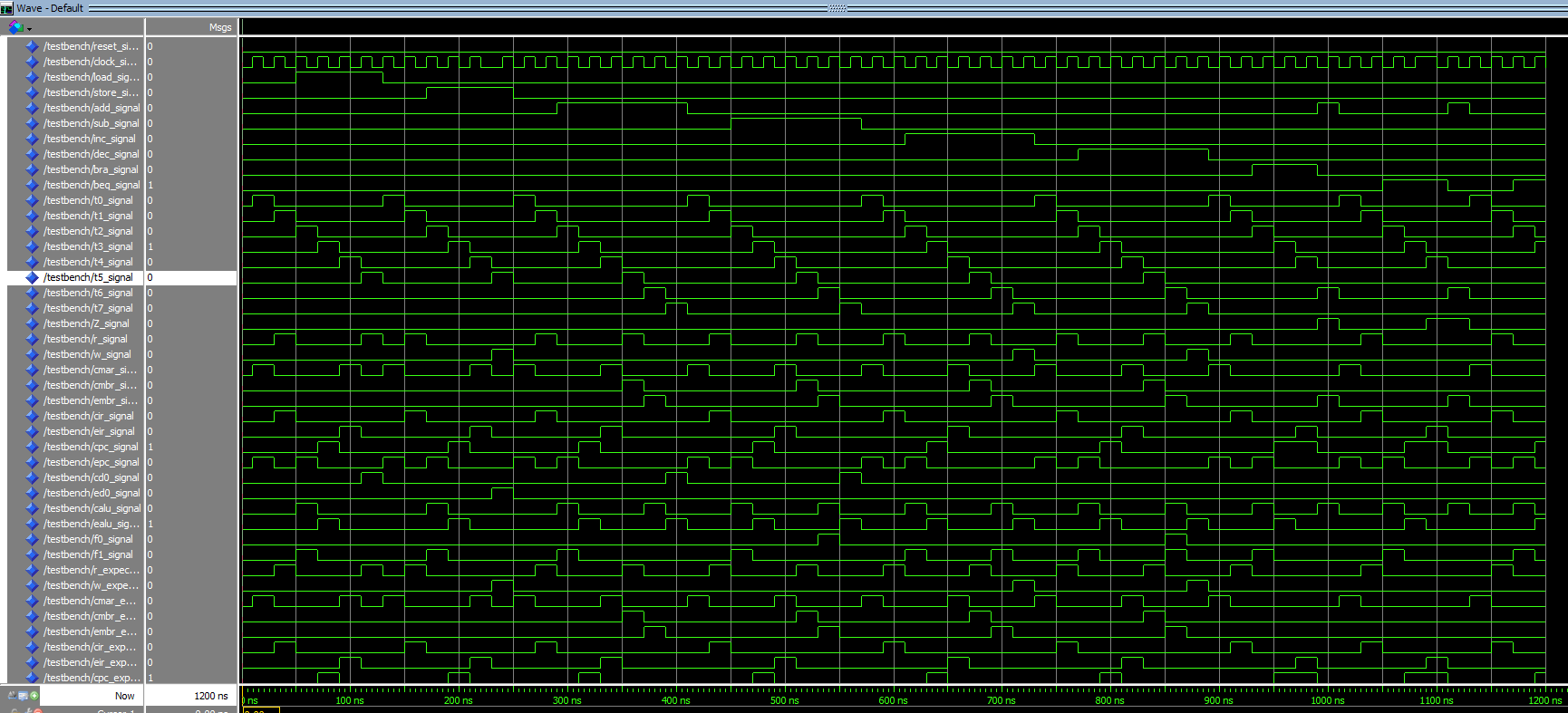
**Figure 2: Truth Table**

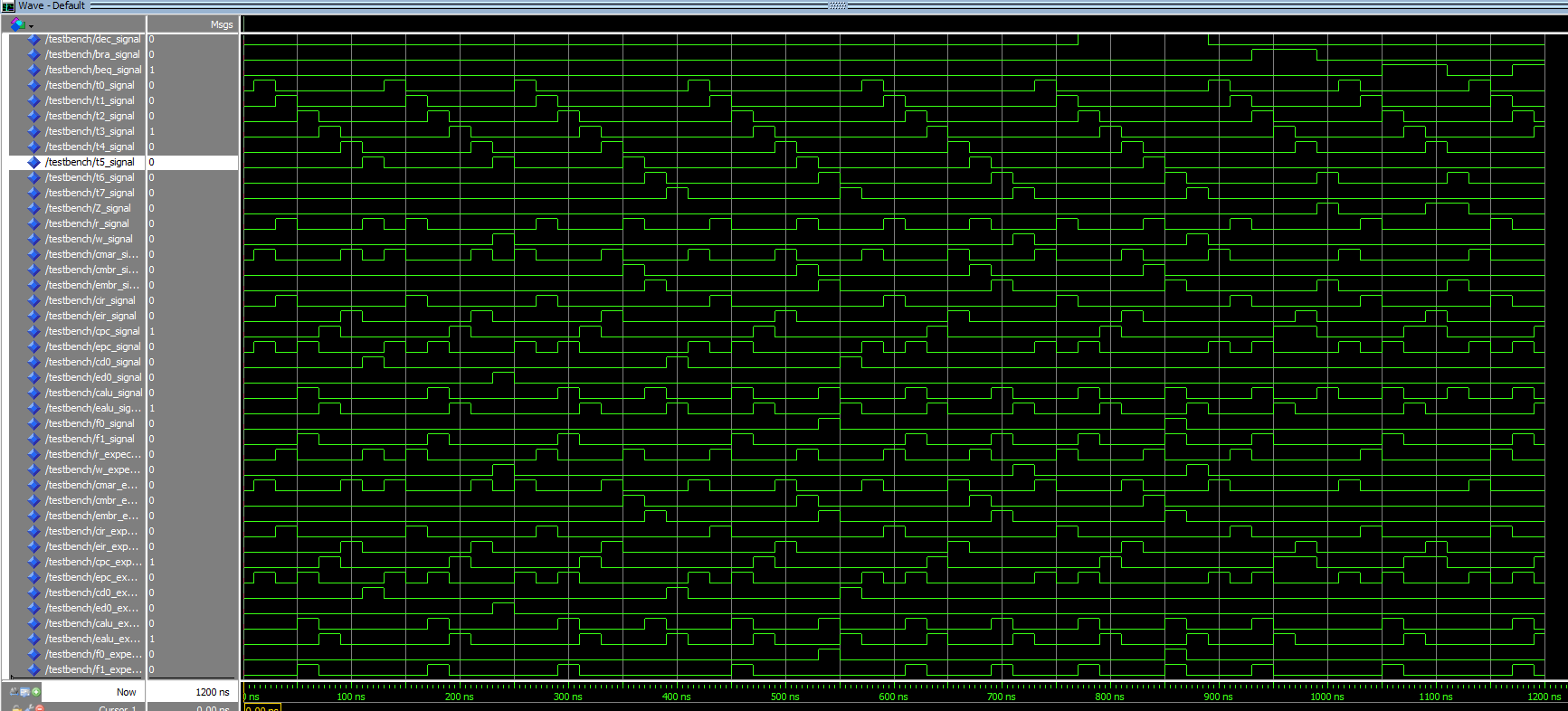
The purpose of this learning activity is to create a control signal logic encoder where it takes in 15 inputs and has 15 outputs. The 15 inputs form different combinations for each of the microinstructions of the outputs. Figure 1 illustrates the schematic and Figure 2 shows the truth table for the learning activity.

Control Signal Logic Signature

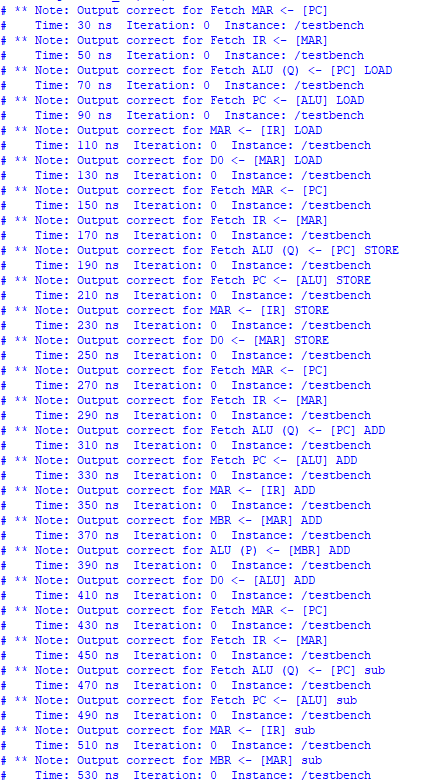
* Input
  + Instructions: *load*, *store*, *add*, *sub*, *inc*, *dec*, *bra*, *beq*
  + Instruction Sequence Timing Signals: *T0*, *T1*, *T2*, *T3*, *T4*, *T5*, *T6*, *T7*
* Output
  + *R*, *w*, *cmar*, *cmbr*, *cpc*, *cir*, *cd0*, *calu*, *embr*, *epc*, *eir*, *ed0*, *ealu*, *f1*, *f0*

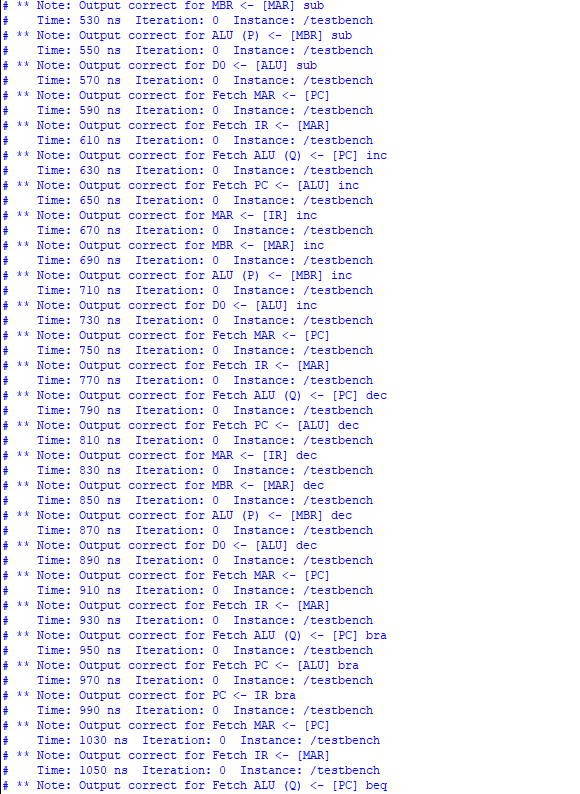
**Verification Tests**

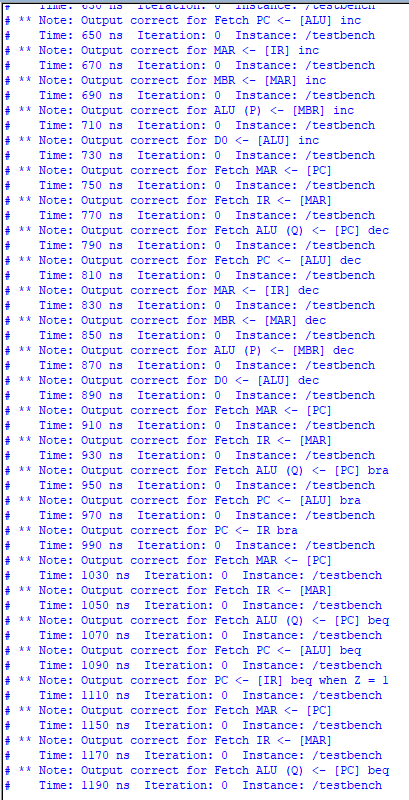




**Figure 3: Verification Tests**







**Figure 4: Verification Tests with Assert Statements**

Figures 3-4 display the verification and testing process of the control signal logic schematic. The test results indicate that the schematic passed all tests according to the verification tests and assert statements. Therefore, the control signal logic schematic is correct and successfully passed all the tests.