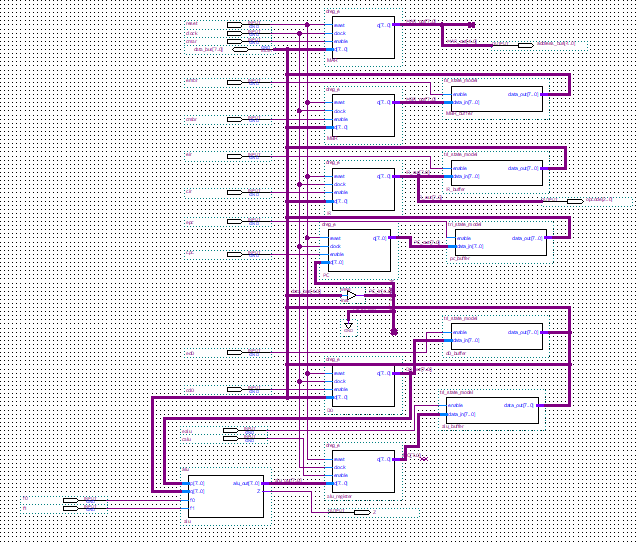
Tyler Kim

DLD

***Datapath Verification Report***

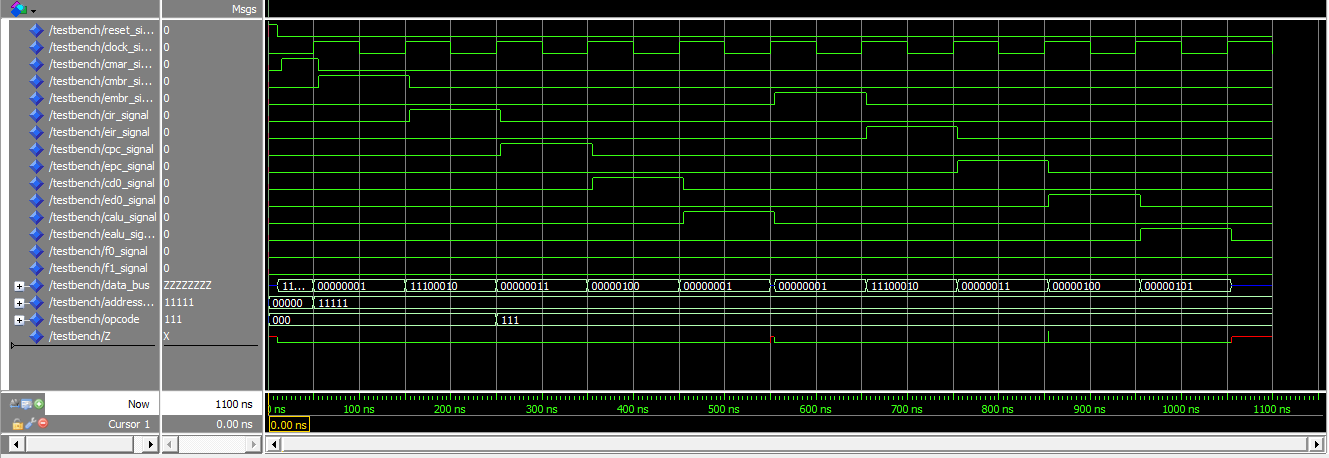
**Component**

****

**Figure 1: Datapath Schematic**

The purpose of this learning activity is to create the datapath component for the cpu. The datapath takes in 16 inputs and outputs 3 values. Among the 16 inputs, one input is the *reset* and another is the *clock*. Then the rest of the inputs of are instructions. Figure 1 highlights the datapath schematic which is composed of 6 registers with 5 tri-state components and the alu.

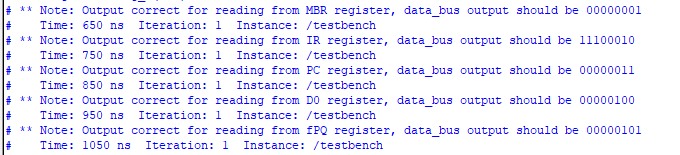
**Verification** **Tests**

****

**Figure 2: Verification Tests**

|  |  |  |
| --- | --- | --- |
| **Data Bus** | **Register** | **Read Value** |
| 11111111 | MAR | 11111111 |
| 00000001 | MBR | 00000001 |
| 11100010 | IR | 11100010 |
| 00000011 | PC | 00000011 |
| 00000001 | fPQ (ALU register) | 00000101 |
| 00000100 | D0 | 00000100 |

**Figure 3: Truth Table from Verification Tests**

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**Figure 4: Verification Tests with Assertion Statements**

Figure 2 - 4 illustrate the verification process for the datapath. I tested if I could write to and read from each register using the *data\_bus* input and output. Figure 3 illustrates the data that were loaded into each register. For fPQ, the values are loaded into the alu and alu register where *P* comes from the *D0* register and *Q* comes from the databus. In this case, *P* is 00000100 and *Q* is 00000001, so the output from the alu register should be 00000101. Since all the test cases are passed, the datapath schematic is correct.