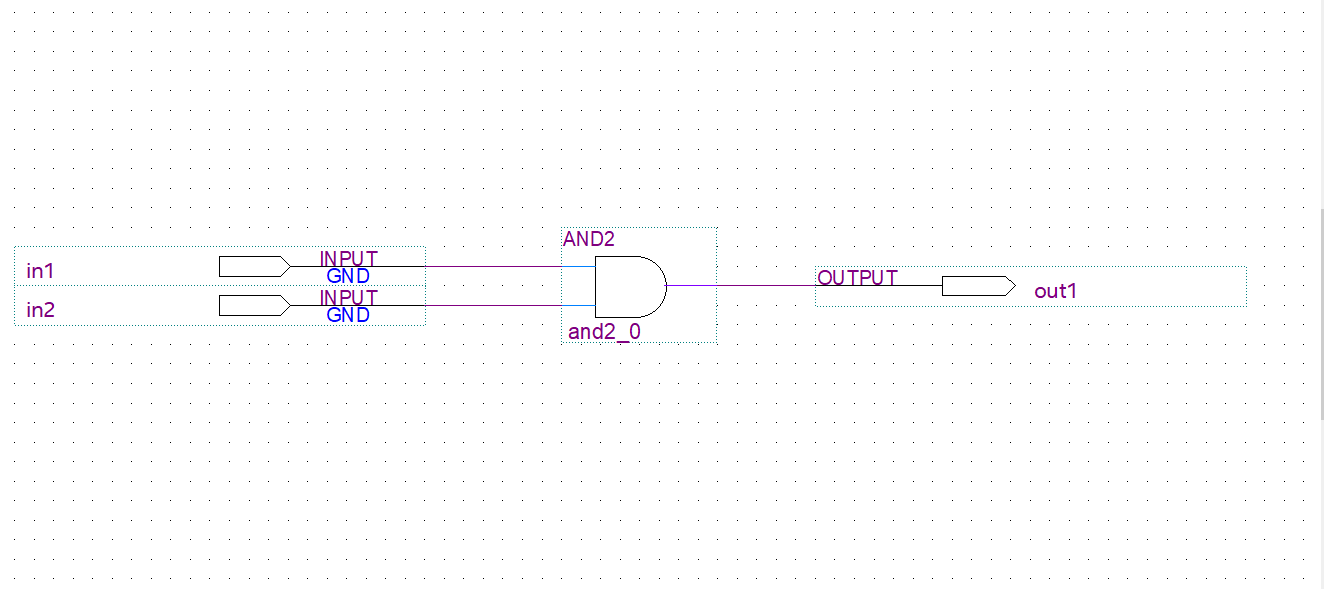
Tyler Kim

Tkj9ep

*AND Gate Simulation Results for Verification*

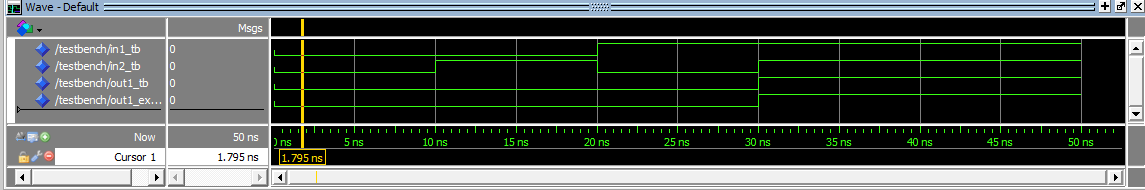
**AND Gate**

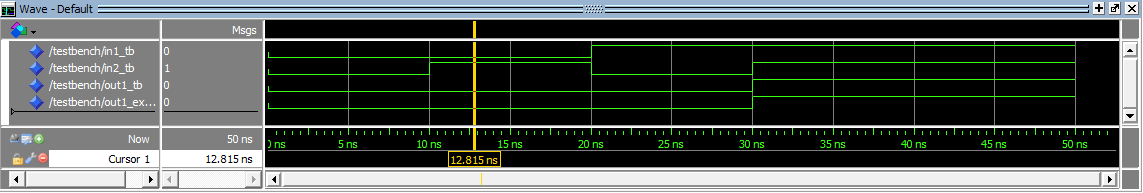
**

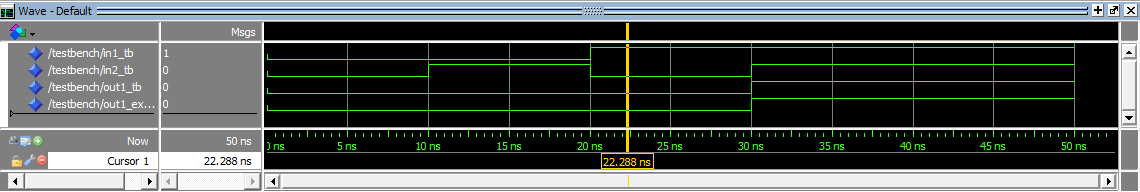
**Figure 1: AND Gate**

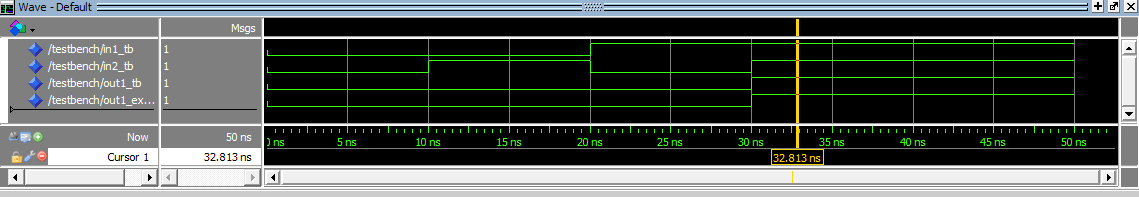
The goal was to create a simple AND gate using Quartus II that has two inputs and one output. This particular schematic has inputs “in1” and “in2” and process them through a single AND gate, “and2\_0”, to provide an output “out1”.

**Verification Tests**









**Figure 2: Simulation Results for Verification**

The figure above illustrates the simulation results for the verification process. As indicated in the figure above, the actual output matches the expected output for all cases. A truth table of the AND schematic and the port mapping is provided below.

|  |  |  |  |
| --- | --- | --- | --- |
| **in1\_tb** | **in2\_tb** | **out1\_tb** | **out1\_expected** |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 |

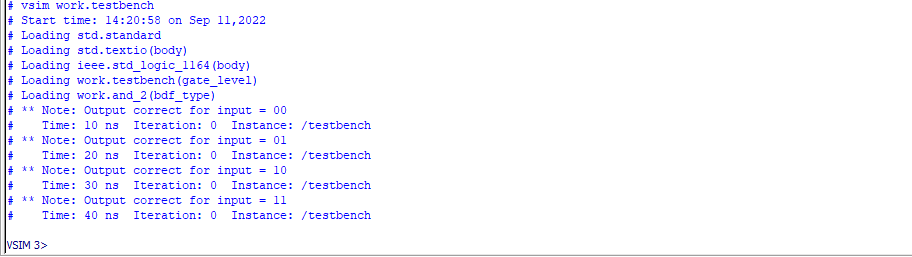
in1 => in1\_tb

in2 => in2\_tb

out1 => out1\_tb

**Figure 3: Truth Table of Verification Test Results and Port Mapping**

The figure below illustrates the simulation results using assert statements.



**Figure 4: Simulation Results with Assert Statements**