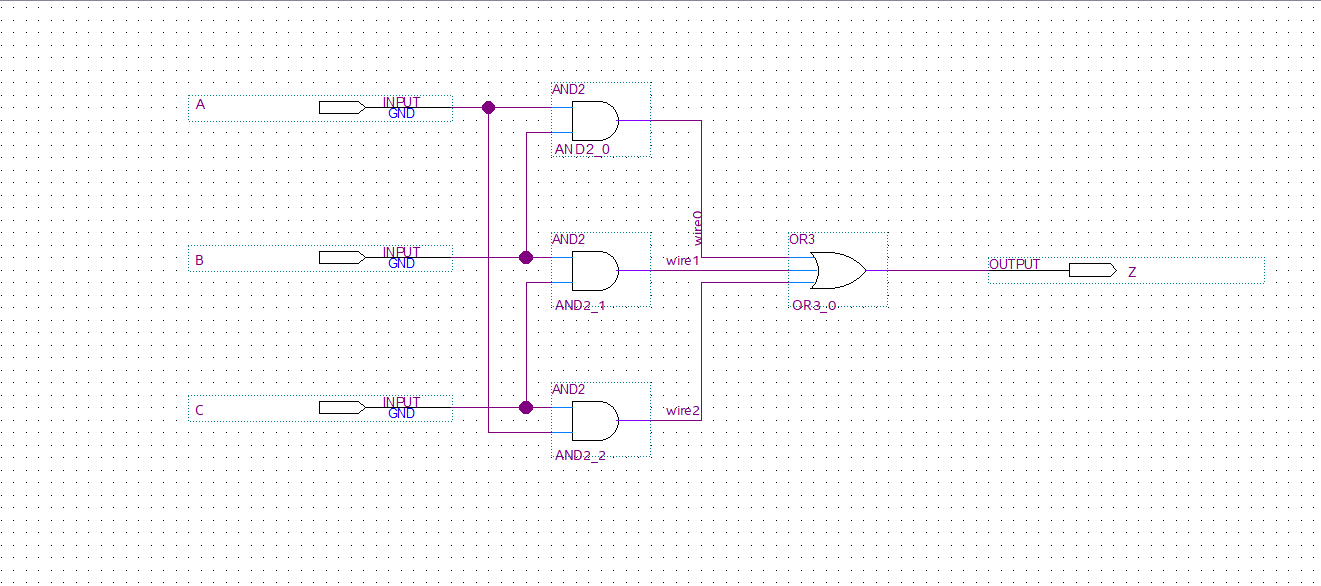
*Majority Voter Simulation Results*

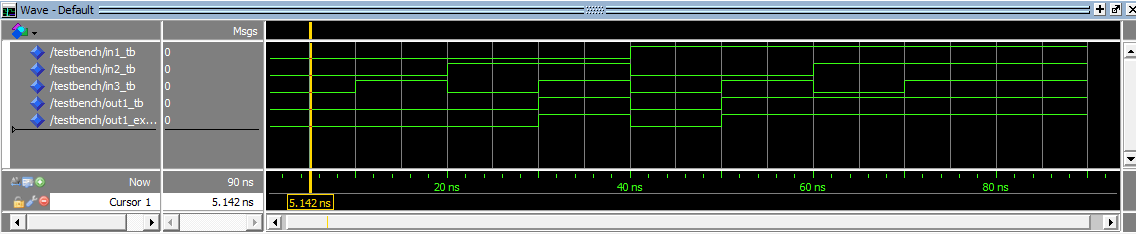
**Schematic**

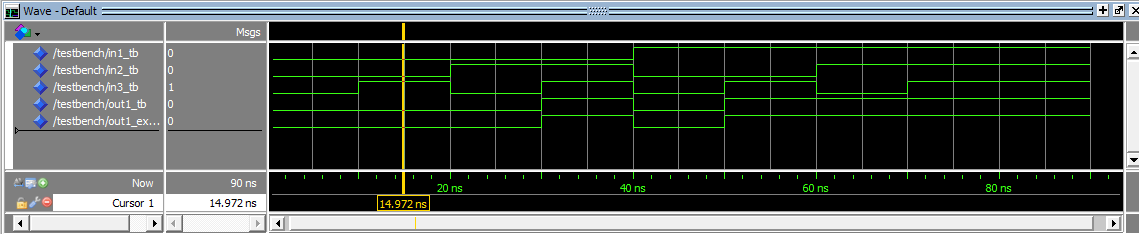


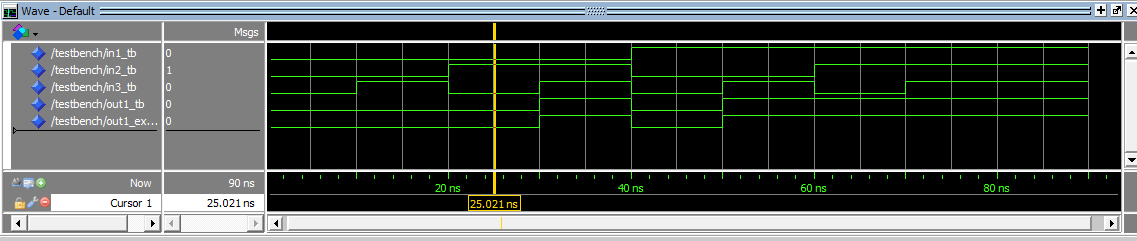
**Figure 1: Majority Voter Schematic**

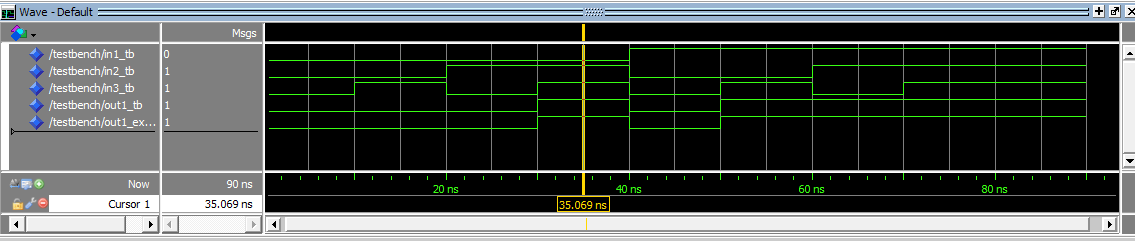
The figure above illustrates the majority voter schematic which takes in the three inputs (A, B, C) and outputs the majority value (Z). In other words, two of the three inputs were 0 and the third was 1, then the output would be a 0 and vice versa.

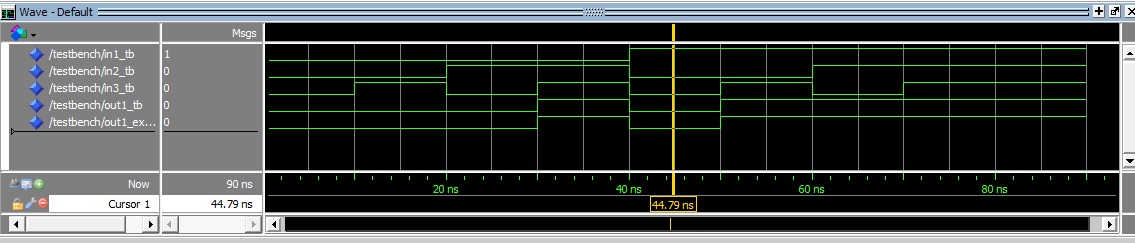
**Verification Tests and Results**

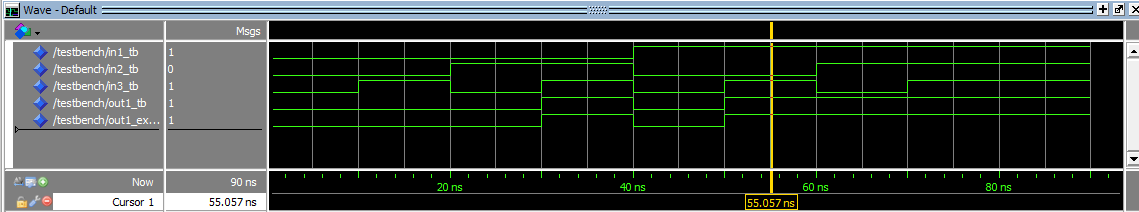


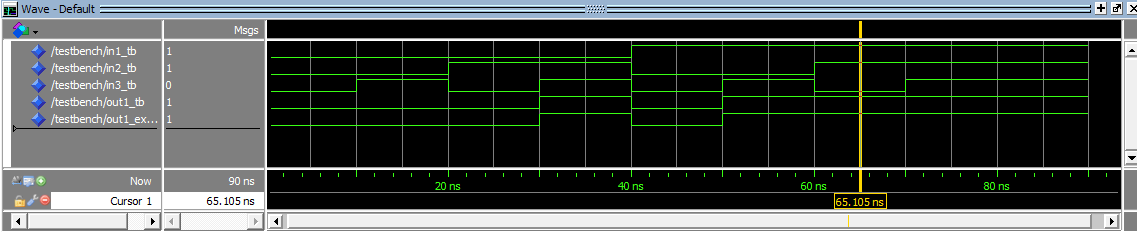


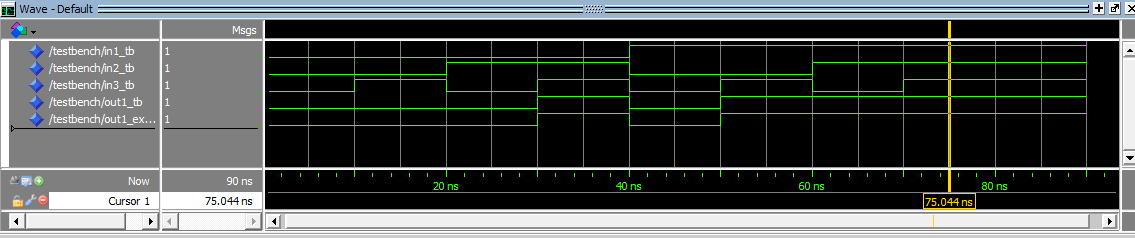












**Figure 2: Simulation Results for Verification**

The figure above illustrates the simulation results for the verification process. As indicated in the figure above, the actual output matches the expected output for all cases. A truth table of the majority voter schematic and the port mapping is provided below.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **in1\_tb** | **in2\_tb** | **in3\_tb** | **out1\_tb** | **out1\_expected** |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 |

A = in1\_tb

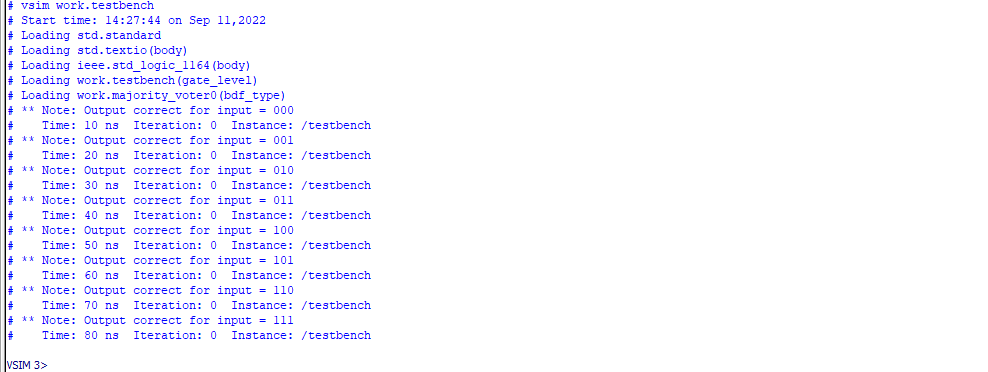
B = in2\_tb

C = in3\_tb

Z = out1\_tb

**Figure 3: Truth Table and Port Mapping**

The figure below illustrates the verification with assert statements.

****

**Figure 4: Simulation Results with Assert Statements**