

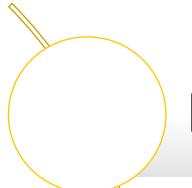
A photograph of a woman with dark hair and bangs, smiling slightly and looking towards the camera. She is wearing a light-colored, button-down shirt. The background is dark with numerous out-of-focus, glowing yellow and orange lights, suggesting a nighttime cityscape or a festive environment.

arm

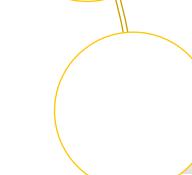
CMSIS-NN

Felix Thomasmathibalan
Staff Engineer, Machine Learning Group

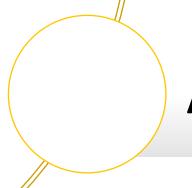
Why Target Arm Cortex-M Processors?



Enable Machine Learning on more than 52 billion* shipped units



Availability of exciting new models with lower memory footprint and MACs



Accelerate deployment of Machine Learning on edge devices



MobileNet V2

- 3.38 MB parameters
- ~ 307 million MACs

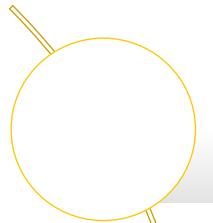


Person Detect(TFLu)

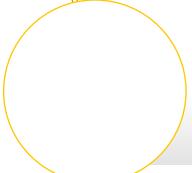
- 250 kBytes
- ~ 7 million MACs

Open Source CMSIS-NN Library

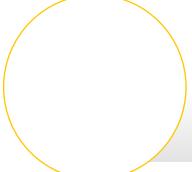
Cortex Microcontroller Software Interface Standard – Neural Networks



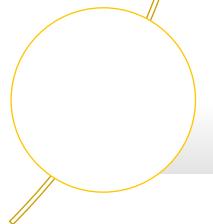
Optimized software library for key machine learning operators.



Empower and enable Cortex-M processors for tinyML applications

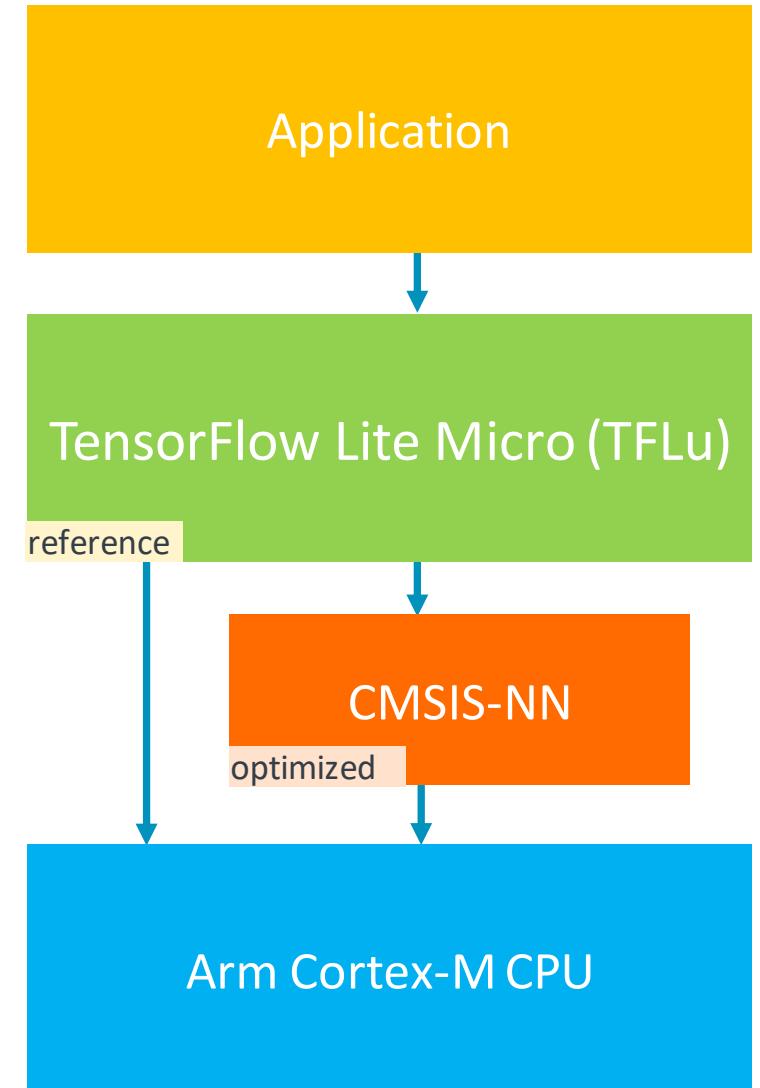
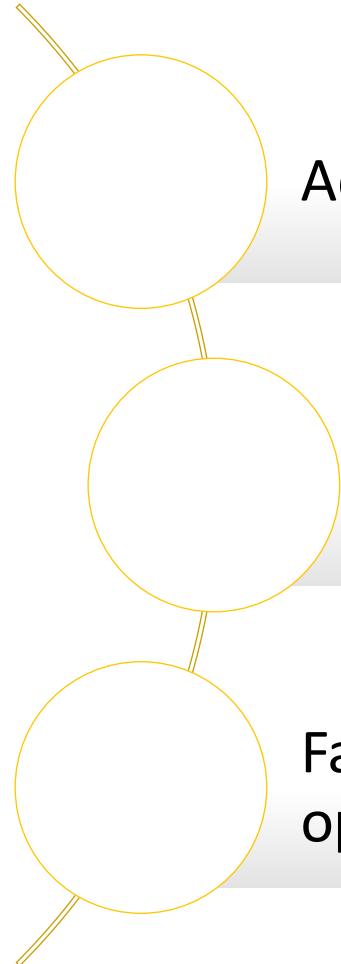


Permissive Apache 2.0 license



Supports open source framework, TensorFlow Lite for Microcontrollers.

CMSIS-NN & TensorFlow Lite for Microcontrollers



Why Optimize for tinyML ?

Power constraints

- Extend battery life of edge devices by reducing awake time.



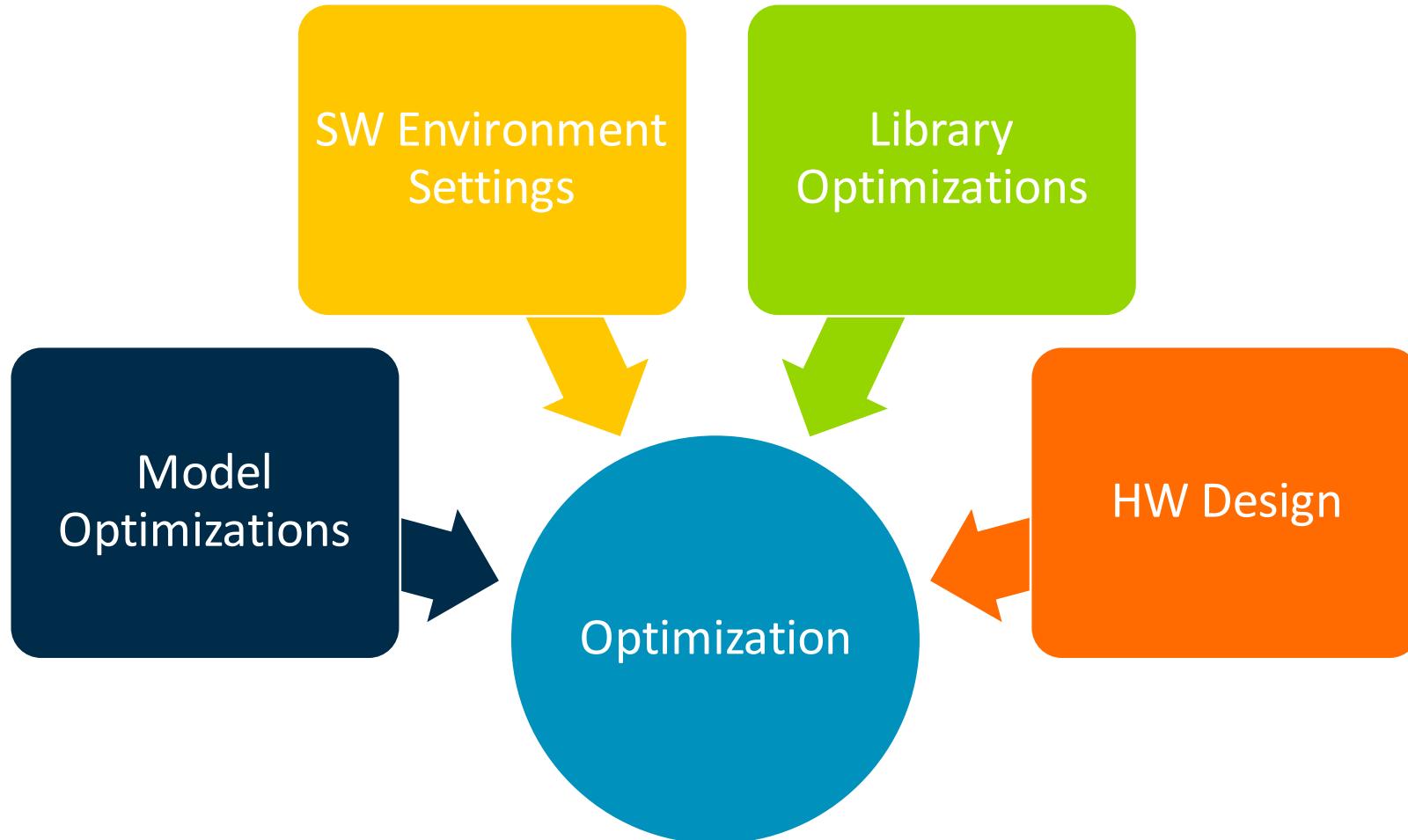
Cycle constraints

- Enable more complex models to be deployed within the inference budget.
- Meet real time latency constraints.

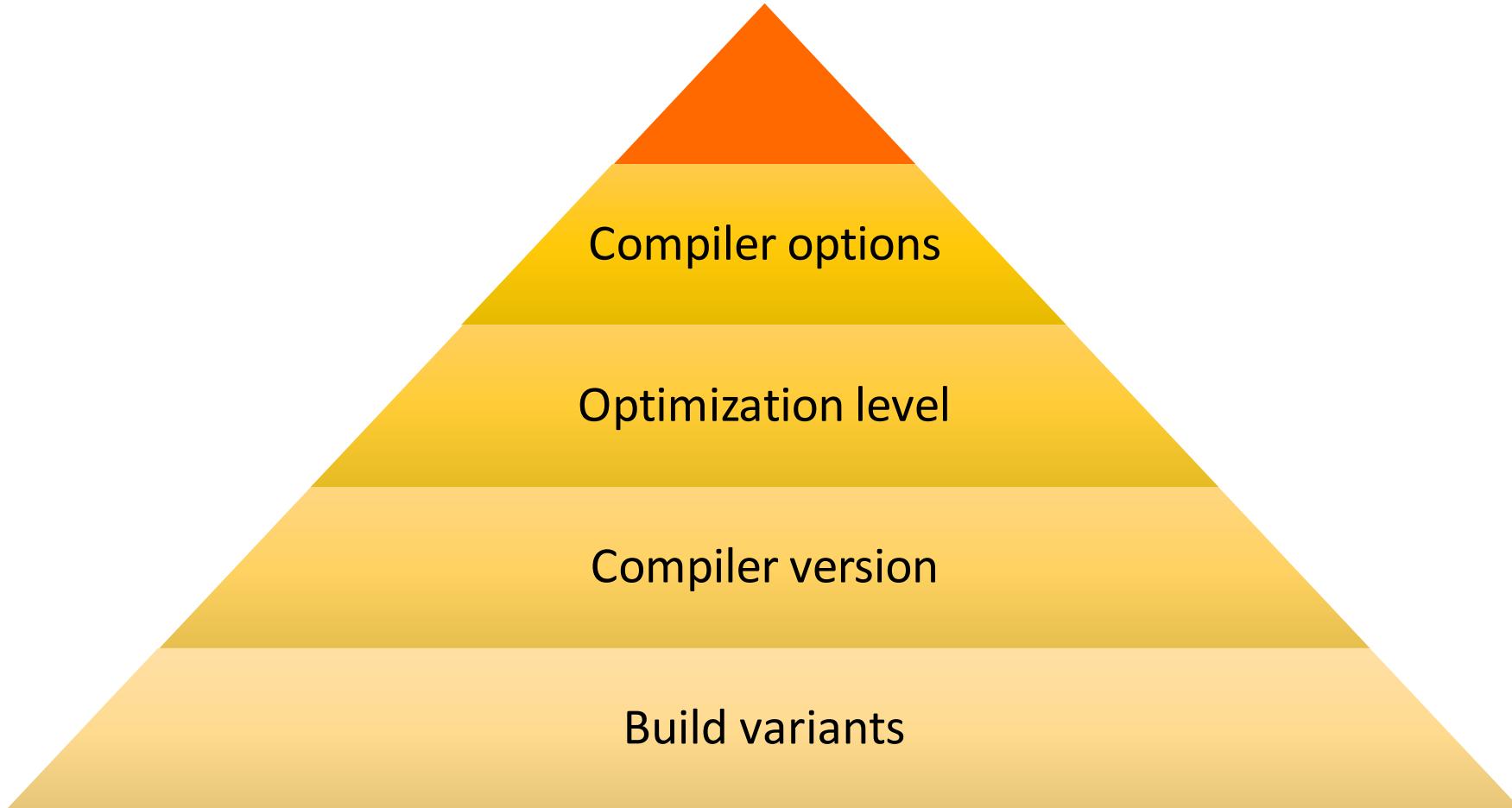


It Takes a Village to Raise a Child

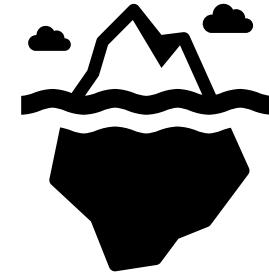
Everyone has a role to play in optimization, some more important than the other



Software Environment Foundation

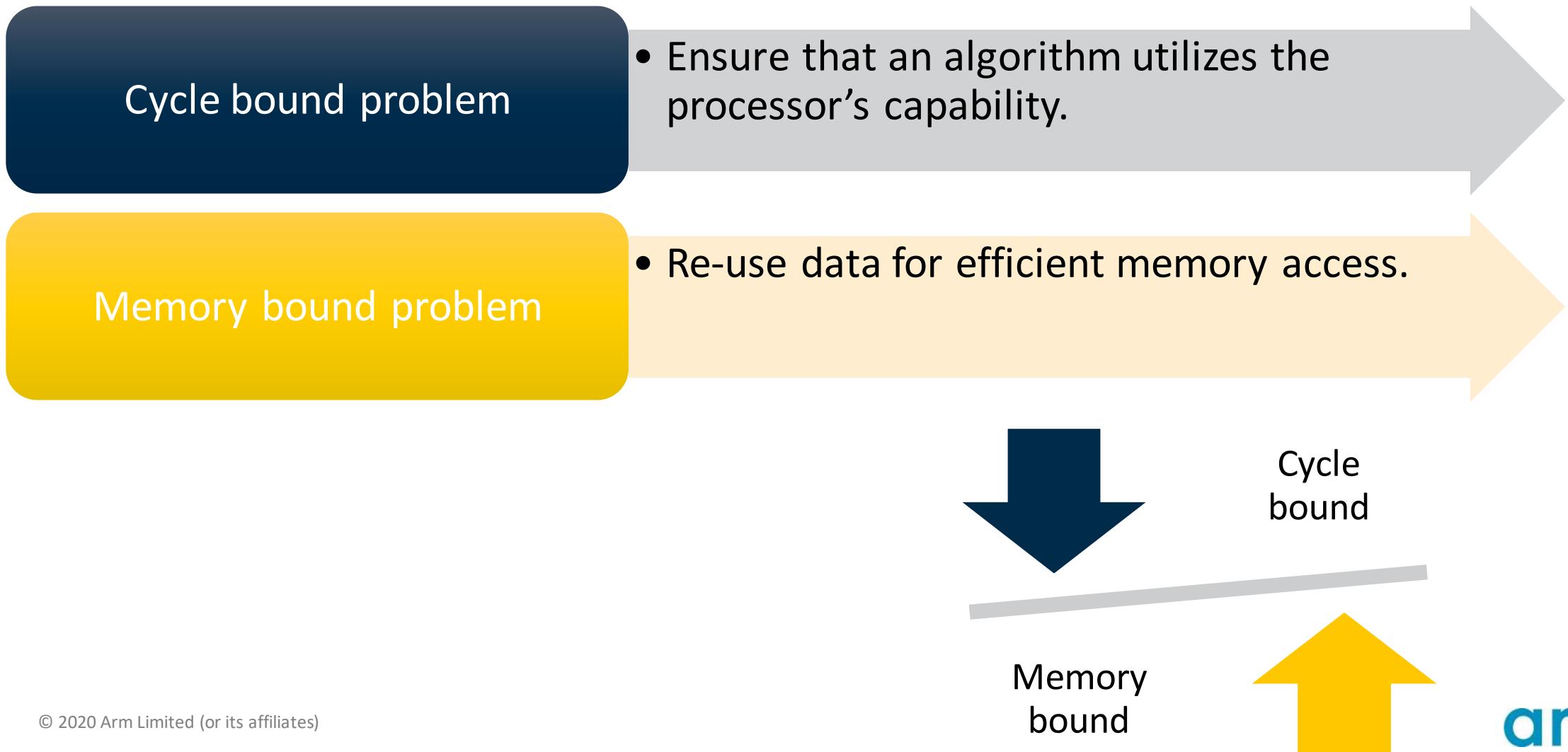


Collect reliable data
to act upon



CMSIS-NN Library Optimizations

Addresses cycle and memory bound aspects at its core



Optimization Categories

The Single Instruction Multiple Data aspect

Non-SIMD capable processors



Re-use data to improve memory access efficiency.



Reduce complexity of core processing loops.



E.g., Arm Cortex-M0, Cortex-M3

SIMD capable processors



Techniques from non-SIMD optimizations.



Utilize processor's capability to process multiple data in a single instruction.



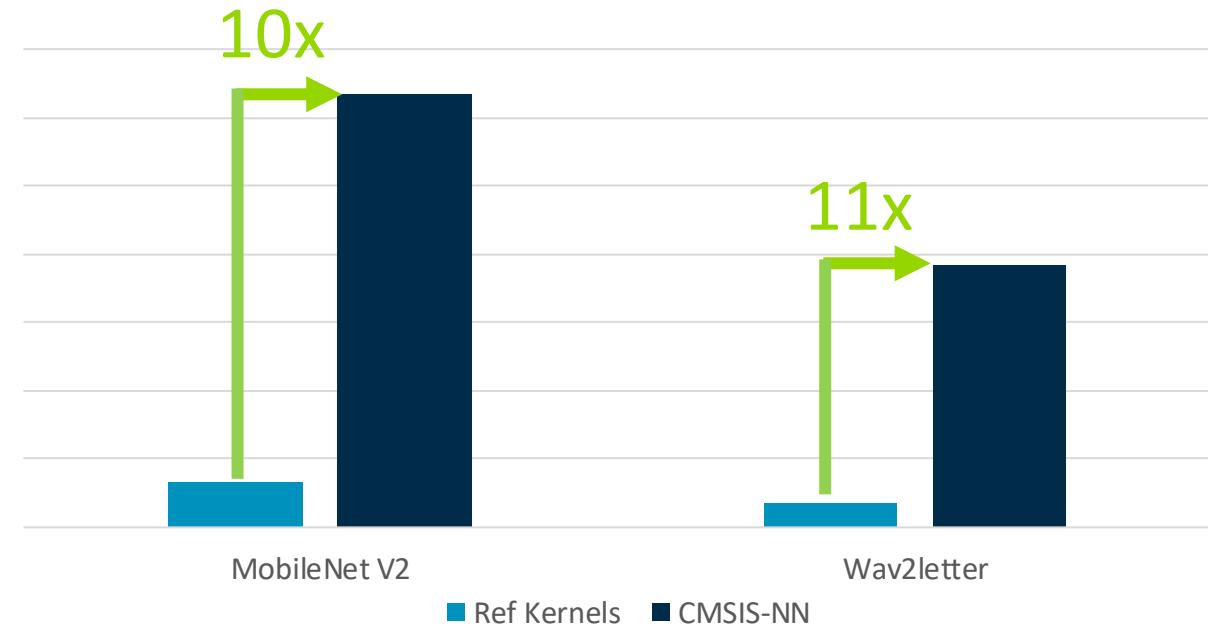
E.g., Cortex-M4, Cortex-M55 with MVE extension.

Performance Results - TFLu runtime with CMSIS-NN

Cortex-M55 system

- These numbers show current improvements on a FPGA reference system
- Continuously improving performance

CMSIS-NN performance on Cortex-M55



Model Optimizations

Shapes of tensors affect the efficacy of optimized library.

To reduce memory footprint, optimizations for all shapes is not done.

Aligned memory access is recommended for CMSIS-NN and input and output channels that are a multiple of 4 ensures that.

1x1/1xN Convolution and Fully Connected operators can act on input tensors without the need of data rearrangement resulting in better processor utilization.



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