BJT Audio Amplifier

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Table of Contents

I. Introduction

A. Objective

The objective of this experiment is to design, construct, and test a multi-stage audio amplifier circuit, capable of amplifying a low-voltage input signal to a higher voltage level suitable for driving a

load-speaker. The amplifier circuit comprises three main stages: an input buffer stage (emitter follower), a 2-stage gain stage (common-emitter), and an output buffer stage (emitter follower). The goals of the experiment include investigating the performance of each stage, analyzing the role of various components in the circuit, and fine-tuning the circuit to optimize its performance across different input frequencies while considering the non-ideal conditions of the breadboard setup. The design can be observed below in **Figure 1**.

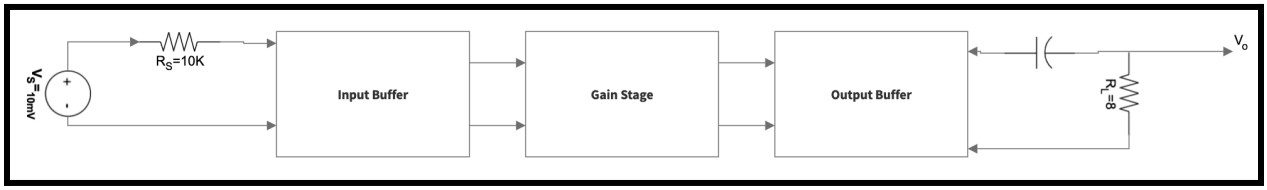

Figure 1: Audio Amplifier Circuit

B. Transistor Circuit Selection

The selection of appropriate transistor circuits is critical to achieving the desired performance of our multi-stage amplifier. Two types of transistor circuits, common-emitter (CE) and emitter-follower (EF, also known as common-collector), were utilized in this design. The common-emitter configuration is characterized by high voltage gain, making it an excellent choice for the gain stage of our amplifier. However, it has medium input and output resistances, which can lead to signal distortion or attenuation if not managed properly. This is where the emitter-follower configuration plays its role. The emitter-follower is known for its low output resistance and high input impedance, making it an ideal choice for the buffer stages in our amplifier. Its low output impedance allows it to drive loads with low resistance without significant voltage loss, while its high input impedance prevents it from drawing too much current from the signal source, thereby preserving the integrity of the input signal. By combining these two transistor configurations, we have a gain stage that amplifies the signal voltage effectively and buffer stages that ensure the signal is transferred efficiently between stages and eventually to the load. **Table 1** outlines the properties of these three transistor configurations, further elucidating their suitability for the roles they play in our multi-stage amplifier.

	Common Emitter	Emitter Follower	Common Base
Voltage Gain	$AV >> 1$	$AV \leq 1$	$AV > 1$
Input Impedance	*Medium*	Large	*Low*
Output Impedance	*Medium*	*Low*	Large
Phase Shift	180 Degrees	0 Degrees	0 Degrees

Table 1: Transistor Design Properties

C. Circuit Limitations and Assumptions

Our multi-stage amplifier design is built around the constraints and characteristics of the various components used, most notably the transistors and resistors. Each stage of the amplifier was designed with specific assumptions and limitations in mind.

Starting with the input buffer stage, the primary component is a 2N3904 NPN transistor (Q1) with a beta value of 100. This transistor is biased with resistors R1 and R2, of 155 kΩ and 282 kΩ respectively, and an emitter resistor RE1 of 6 kΩ. An assumption made at this stage is that the input resistance of the buffer stage is significantly larger than the source resistance (RS=10 kΩ), so that it doesn't load the source.

In the gain stage, two 2N3904 transistors (Q2 and Q3) are used, again with a beta value of 100. Biasing resistors R3, R4, R5, and R6 are chosen to set the quiescent collector current (ICQ) and the quiescent collector-emitter voltage (VCEQ) to suitable values for amplification. The collector resistors (RC2 and RC3) and the emitter resistors (RE2 and RE3) are chosen to provide the necessary voltage gain and to establish the desired DC operating point. Assumptions at this stage include that the transistors operate in their active regions, allowing us to use the small signal model for analysis.

The output buffer stage employs a TIP31 transistor (Q4) with a beta value of 50, and an emitter resistor RE4 of 20 Ω. The objective here is to provide a low output resistance to effectively drive the 8 Ω speaker load (RL4). We assume that the output impedance of the amplifier is much less than RL4, and that the transistor is able to supply the necessary current without going into saturation.

In the design and analysis of this multi-stage amplifier, we also assume that the base current is negligible compared to the collector and emitter currents, and that the Early effect is negligible, which simplifies calculations and analysis. These assumptions, while not entirely accurate, offer a reasonably close approximation of the real-world behavior of the transistors and the amplifier circuit as a whole. The actual performance of the amplifier may deviate slightly due to non-idealities and parasitic effects in the transistors and other components, and due to variations in component values and transistor parameters from their nominal values. These factors are taken into consideration during the testing and fine-tuning of the amplifier circuit.

D. Materials List

1. Transistors
    a) 2N3904 x 3
    b) TIP31 x 1
2. Resistors
    a) 10 KΩ (RS) x 1
    b) 155 KΩ (R1) x 1
    c) 282 KΩ (R2) x 1
    d) 6 KΩ (RE1) x 1
    e) 181 KΩ (R3) x 1

f) 69.1 KΩ (R4) x 1
g) 1.2 KΩ (RC2) x 1
h) 23.1 KΩ (RE2) x 1
i) 69.9 KΩ (R5) x 1
j) 176 KΩ (R6) x 1
k) 254 Ω (RC3) x 1
l) 25.4 KΩ (RE3) x 1
m) 20 Ω (RE4) x 1
n) 8 Ω (RL4) x 1

3. Capacitors
   a) 0.1 uF x 1
   b) 0.33 uF x 1
   c) A large capacitor for shorting across the positive and negative terminals
4. Other
   a) Breadboard
   b) Connecting Wires
   c) Power Supply
   d) Oscilloscope
   e) Function Generator
   f) Multimeter

E. Theory Notes

In this report, we utilize a three-stage transistor amplifier, consisting of an input buffer, a gain stage, and an output buffer, each playing an important role in delivering our desired output. The amplification process is complex and involves various aspects, such as loading effects, matching of source and load resistances, transistor selection, and the limitations of small signal analysis.

The loading effect is a significant consideration in amplifier design. This effect surfaces when there's a mismatch between the source and load resistances, particularly when the source resistance is substantially larger than the load resistance. In such scenarios, most of the voltage drop is experienced across the source resistance, and the voltage delivered to the load is much less than the supply voltage. To counteract this effect, one could adjust the source resistance to match the load resistance, which can boost power efficiency, even if it results in a lesser voltage being delivered to the load. Given the nature of our circuit design, our focus has been on maximizing voltage transfer, thus, we've endeavored to minimize the output resistance.

The gain stage of our amplifier, implemented with 2 common emitter configurations, is designed to provide a substantial voltage gain. Assuming an ideal scenario, an amplified stage one output of 1.284V signal inputted into an ideal emitter follower (the output buffer stage in our design) with a voltage gain of 1 will generate an AC output across the load of 1.26 V. Given our load resistance, the AC current through the load branch would then be 10 mA. This analysis is based on the understanding that the DC emitter current must be larger than the overall AC current to provide enough offset so that the current does not

swing into the negative. A negative current swing would push the transistor into the cut-off region, leading to signal clipping.

To handle larger signal voltages and corresponding higher DC currents, we employed a TIP31 power transistor in our design. While standard transistors like the 2N3904 are excellent for small signals, they would not be suitable for higher current scenarios.

In conclusion, the design and implementation of this three-stage amplifier involved carefully considering the characteristics and limitations of the components used, the effects of loading, and the requirements of small signal analysis. Refer to **Figure 1** for a comprehensive view of our circuit design.

II. AC & DC Stage Designs

A. Input Buffer Design Stage

For the design application of the input signal source and input buffer stage (emitter-follower), let's revisit the DC and AC analysis with the provided information. We will reference **Figure 2** for the DC design and **Figure 3** for the AC design in the Appendix.

Starting with the DC design, the emitter resistor RE1 is determined by the quiescent conditions. From the given conditions, we can compute RE1 as follows:

$$R_{E1} = \frac{V_{CC} - V_{CEQ1}}{I_{CQ1}} = \frac{12-6}{1mA} = 6\ K\Omega$$

Thus, RE1 is approximately 6k Ohms.
Next, we find the base-emitter resistance (rπ1), which is given by:

$$r_{\pi 1} = \frac{\beta_1 V_T}{I_{CQ1}} = 2.6\ K\Omega$$

So, rπ1 is approximately 2.6k Ohms.
Moving onto the AC design, the input impedance of the buffer stage (Ri1) is determined by the parallel combination of R1 and R2, and the sum of rπ1 and the product of (1 + β1) and RE1. This can be expressed as:

$$R_{i1} = R_1 \,||\, R_2 \,||\, [r_{\pi 1} + (1 + \beta_1) R_{E1}] = 85.9\ K\Omega$$

Thus, Ri1 is approximately 85.9k Ohms.
The small-signal voltage gain (Av1) is approximated by the following equation (assuming ro approaches infinity and neglecting the loading effect from the next stage):

$$A_{v1} = \frac{V_{o1}}{V_i} = 0.892$$

Therefore, Av1 is approximately 0.892.
Given a 10 mV peak input signal voltage, the peak voltage at the output of the buffer stage (vo1) is given by:

$$V_{o1} = A_{v1} * V_i = 8.92\,mV$$

So, vo1 is approximately 8.92 mV.
Finally, to determine the bias resistors, we find R1 to be 155k Ohms and R2 to be 282k Ohms. These resistor values are crucial for setting the correct biasing conditions for the amplifier's linear operation.

B. Gain Design Stage

The gain stage of our amplifier design is a vital component that influences the overall output of the circuit. It requires careful consideration of both DC and AC elements for effective operation. Reference **Figure 4** for the DC design and **Figure 5** for the AC design in the Appendix.
On the DC front, we have the gain stage designed to maintain the desired quiescent conditions. These conditions are critical for the amplifier's stability and its ability to handle varying input signals without distortion.

$$R_{C2} = \frac{V_{CC} - V_{C2}}{I_{CQ2}} = \frac{12-6}{5\,mA} = 1.2\,K\Omega$$
$$R_{C3} = \frac{V_{CC} - V_{C3}}{I_{RC3}} = \frac{12-6.7}{20.88\,mA} = 254\Omega$$

The base-emitter voltage, rπ2, is calculated as:

$$r_{\pi 4} = \frac{\beta_2 * V_T}{I_{CQ2}} = \frac{100*0.026}{5} = 0.52\,K\Omega$$

We also find the input resistance, Ri3:

$$R_{i3} = R_5 || R_6 || r_{\pi 3} + (1 + \beta_3) R_{E3} = 2.60\,K\Omega$$

Moving on to the AC design, the goal is to achieve the desired voltage gain. The expression for the voltage gain can be written as:

$$A_{v2} = \frac{V_{o2}}{V_{o1}} = \frac{(\beta_2)(R_{C2}||R_{i3})}{r_{\pi 2} + (1+\beta_2)(R_{E2})} = 28.8$$

Setting |Av2| equal to 28.8, we find RE2 & RE3:

$$28.8 = \frac{\beta_2(R_{C2}||R_{i3})}{r_{\pi 2}+(1+\beta_2)R_{E2}} \Rightarrow R_{E2} = 23.1\ \Omega$$

$$5 = \frac{\beta_3(R_{C3}||R_{i4})}{r_{\pi 3}+(1+\beta_3)R_{E3}} \Rightarrow R_{E3} = 25.4\ \Omega$$

Lastly, if we set R3 and R4 to be 50 kOhms, we find R3 = 181 kOhms and R4 = 69.1 kOhms.
It's important to note that this is a specific solution, and the design of such a circuit is not unique. The actual construction of this circuit with discrete components would likely require slight modifications to adjust for standard resistor values and varying transistor current gains. Furthermore, the frequency response and efficiency of the amplifier, which have not been discussed in detail here, would also be factors to consider in a comprehensive design process.

C. Output Buffer Design Stage

The design of the output buffer stage encompasses both DC and AC considerations, which are crucial for achieving the desired amplifier performance. The DC design is depicted in **Figure 6**, while the AC design is illustrated in **Figure 7** in the Appendix.
In the DC design, the output stage of our amplifier functions as an emitter-follower amplifier circuit. The 8 Ohm speaker is capacitively coupled to the amplifier's output. This configuration ensures that no DC current flows through the speaker.
The DC conditions are set to deliver an average power of 0.1 W to the load. Calculating the RMS value of the load current, we find iL(RMS) = 0.112 A using the formula PL = iL^2(RMS) * RL. For a sinusoidal signal, this leads to a peak output current of iL(peak) = 0.158 A, which in turn gives us a peak output voltage of vo(peak) = (0.158)(8) = 1.26 V.
For the transistor in the output stage, we assume a current gain of β4 = 50. We set the quiescent transistor parameters at IEQ4 = 0.3 A and VCEQ4 = 6V. The emitter resistance, RE4, is then calculated as follows:

$$R_{E4} = \frac{V_{CC}-V_{CEQ4}}{I_{EQ4}} = \frac{12-6}{0.3\ A} = 20\ \Omega$$

The quiescent collector current, ICQ4, and the input resistance to the base, rπ4, are then determined:

$$I_{CQ4} = \frac{\beta_4}{(1+\beta_4)I_{EQ4}} = \frac{50}{51} * 0.3 = 0.294\Omega$$

$$r_{\pi 4} = \frac{\beta_4 * V_T}{I_{CQ4}} = \frac{50*0.026}{0.294} = 4.42\Omega$$

Turning to the AC design, we calculate the small-signal voltage gain, Av4, which is expected to be close to unity:

$$A_{v4} = \frac{V_o}{V_{o3}} = \frac{(1+\beta_4)(R_{E4}||R_L)}{r_{\pi 4} + (1+\beta_4)(R_{E4}||R_L)} = 0.985$$

The requirement of a peak output voltage of vo = 1.26 V leads to a necessary peak voltage at the output of the gain stage, vo3 = 1.28 V.
In conclusion, the output buffer stage was designed considering both DC and AC aspects. The DC design ensures appropriate biasing and power delivery to the load. The AC design, on the other hand, guarantees the necessary gain for the signal to be amplified. These calculations facilitate the desired functioning of the output buffer stage in effectively driving the speaker load while maintaining suitable DC and AC conditions.

III. Simulations

A. Stage 1: Buffer Input (Emitter Follower)

The input buffer stage employs an NPN BJT 2N3904, a voltage divider circuit made up of resistors R1=155k and R2=282k, an emitter resistor Re1=6k, and a coupling capacitor of 0.1 μF. This stage is designed to minimize the loading effect of the 10 kΩ source resistance and to mirror the input voltage (10 mV) at the output with minimal loss. The circuit is biased with a Vcc of 12 V. The input source has a resistance Rs of 10 kΩ and a voltage Vs of 10 mV. The output Vo1 is taken from the emitter node above Re1 and is coupled to the subsequent stage via another capacitor of the same value (0.1 μF). Please refer to **Figure 8** for the schematic of the input buffer stage.

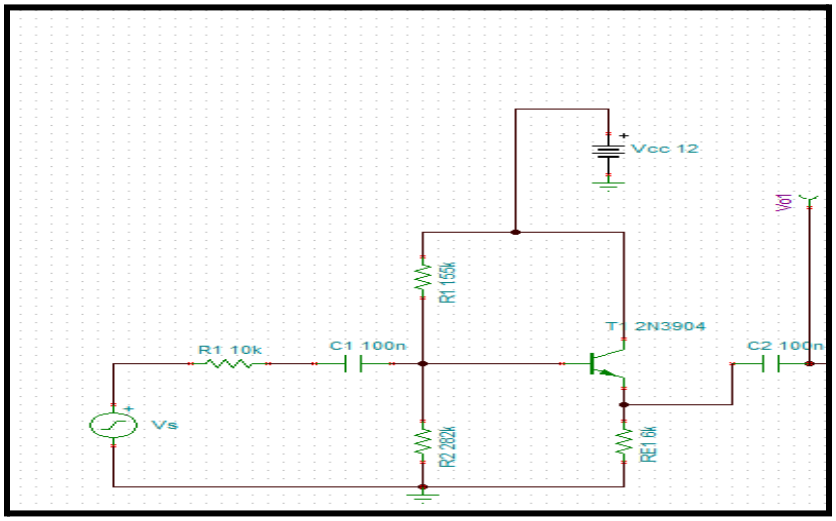

Figure 8: TINA-TI Input Buffer

B. Stage 2: Two-Stage Gain (Common-Emitter)

After the input buffer stage, the two-stage common-emitter amplifier is placed to provide the required voltage gain in the overall circuit. The first stage ensures that the input signal is neither distorted nor attenuated before it is fed into the gain stage. The two-stage common-emitter amplifier is essentially two common-emitter amplifiers connected in a series, allowing the voltage gains of each stage to be multiplied together, achieving a higher overall voltage gain. The first common-emitter stage receives the output from the input buffer stage via a coupling capacitor, which serves to block any DC voltage from the previous stage. The amplified output from the second common-emitter stage is then fed into the output buffer stage, providing the necessary current gain and low output impedance to drive the load. Refer to **Figure 9** for the schematic of the two-stage common-emitter amplifier built within TINA-TI.

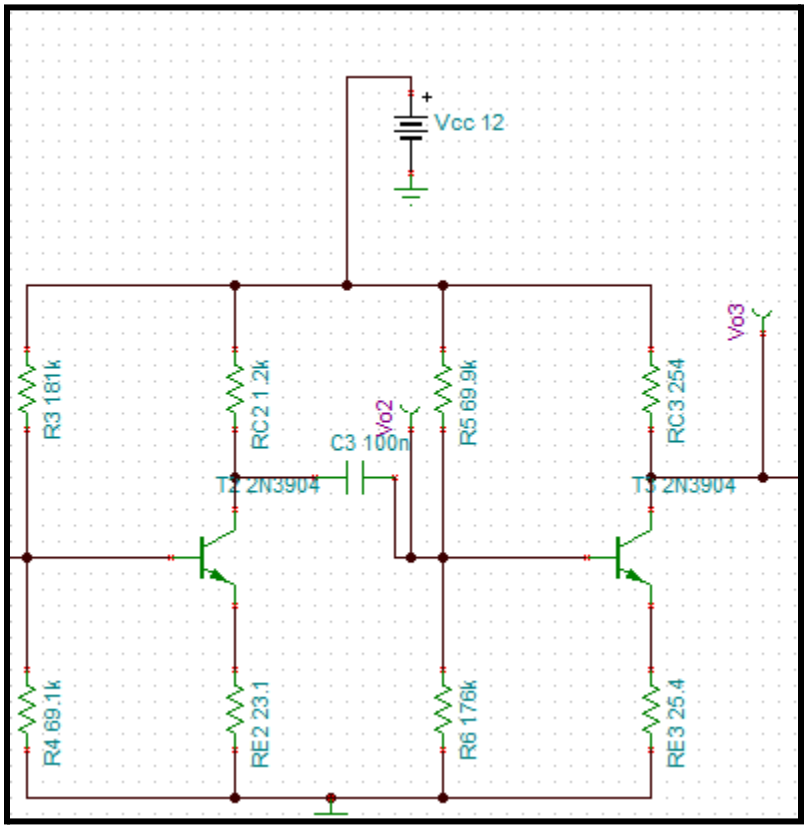

Figure 9: Two-Stage Common Emitter

C. Stage 3: Buffer Output (Emitter Follower)

The output buffer stage uses a BJT TIP31, an emitter resistor Re4=20Ω, and a coupling capacitor of 0.1 µF. This stage provides the required output current and power to drive the 8Ω speaker load. The circuit is biased with a Vcc of 12 V, and the input voltage Vs is equal to Vo3 from the previous stage. The final output Vo4 is where the speaker load is connected. Please see **Figure 10** for the schematic of the output buffer stage.

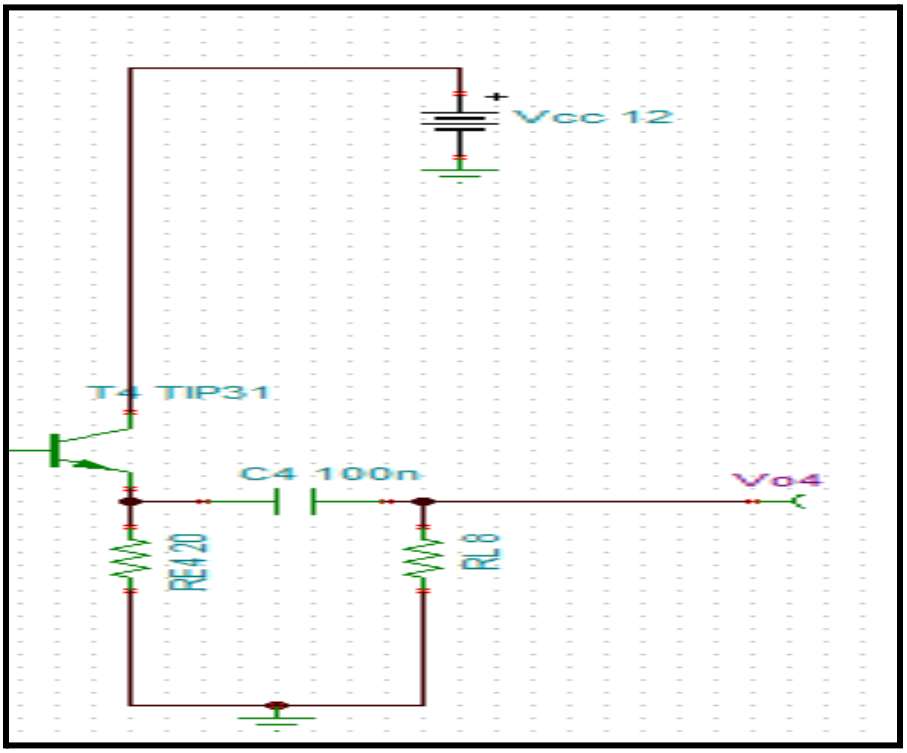

Figure 10: Output Buffer

The completed audio amplifier circuit was built and simulated using the TINA-TI software. The transient analysis output waveforms for all stages are shown in **Figure 12**. The input frequency was set to 7 kHz, which can be observed in the period of the output waveforms. Refer to **Figure 11** for the entire amplifier construction in TINA-TI.

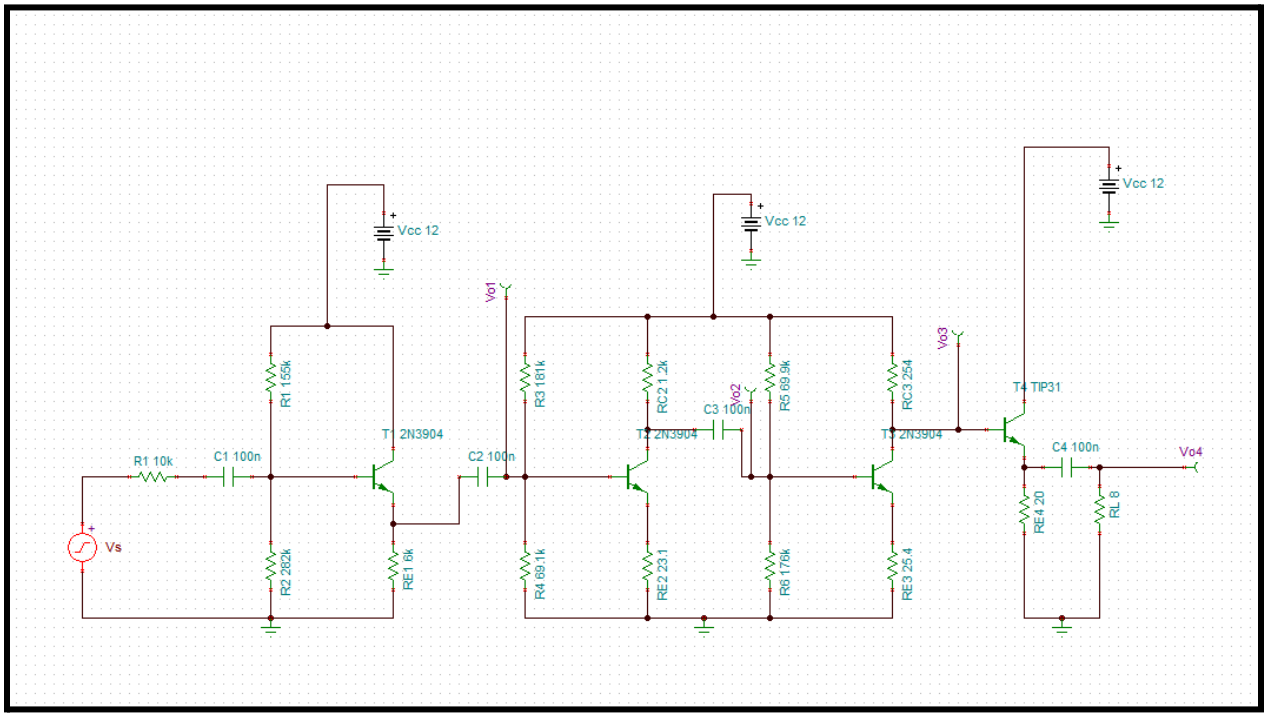

Figure 11: Total Circuit Construction

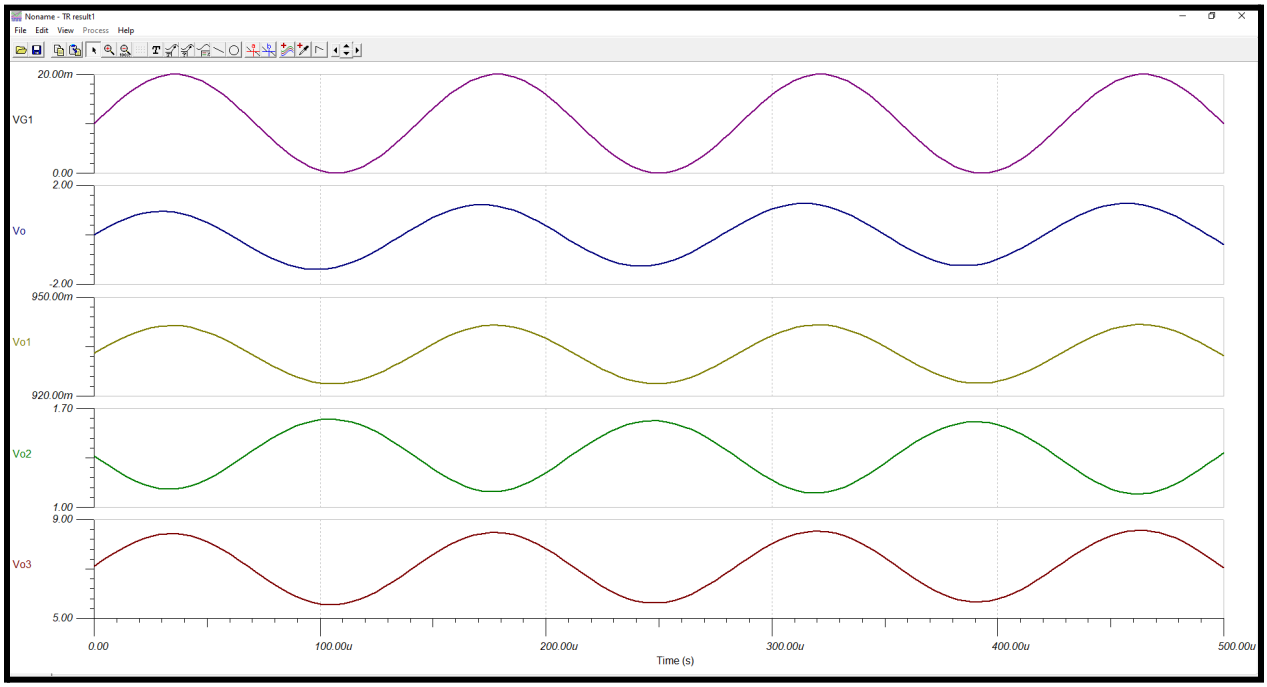

Figure 12: Transient Voltage Outputs

In this multistage amplifier, coupling capacitors are used to connect the output of one stage to the input of the next. They block any DC voltage from the previous stage, preventing it from affecting the biasing of the next stage. Only the AC signal is allowed to pass through, ensuring the subsequent stage is correctly biased and can amplify the signal as intended. In the audio amplifier circuit described, coupling capacitors

are used between the input buffer stage and the two-stage common-emitter amplifier, and between the common-emitter amplifier and the output buffer stage.

IV. Progress Report 1

A. Stage 1: Buffer Input (Emitter Follower)

1. High input impedance: Emitter followers have high input impedance, which means they draw very little current from the input source. This is beneficial when dealing with signal sources that have high output resistance or are sensitive to loading effects.
2. Low output impedance: The output impedance of an emitter follower is low, which enables it to drive loads with low resistance without significant voltage loss. This makes it ideal for driving current-demanding devices like speakers or other amplifiers.
3. Voltage buffering: Emitter followers provide unity voltage gain (the output voltage is approximately equal to the input voltage), which means they don't amplify the input signal. Instead, they provide a stable, buffered output voltage that tracks the input voltage, making them ideal for isolating stages in multi-stage amplifiers or in circuits where a stable reference voltage is needed.
4. Current gain: While the voltage gain is approximately unity, emitter followers do provide current gain. The output current can be much higher than the input current, making them suitable for driving loads that require more current than the input source can provide.
5. Power gain: Although the voltage gain is near unity, the power gain of an emitter follower can be significant due to the increased output current capability. This makes them useful in power amplifiers or other applications where power delivery is important.

The input buffer stage uses an NPN BJT 2N3904, a voltage divider circuit with resistors R1=155k and R2=282k, an emitter resistor Re1=6k, and a coupling capacitor of 0.1 µF. The purpose of this stage is to reduce the loading effect of the 10 kΩ source resistance and reproduce the same input voltage (10 mV) at the output with minimal loss. The circuit is biased with a Vcc of 12 V, and the input source has a resistance Rs of 10 kΩ and a voltage Vs of 10 mV. The output Vo1 is taken from the emitter node above Re1 and connected to the next stage through another capacitor with the same value (0.1 µF). Refer to **Figure 13** for the schematic of the input buffer stage.

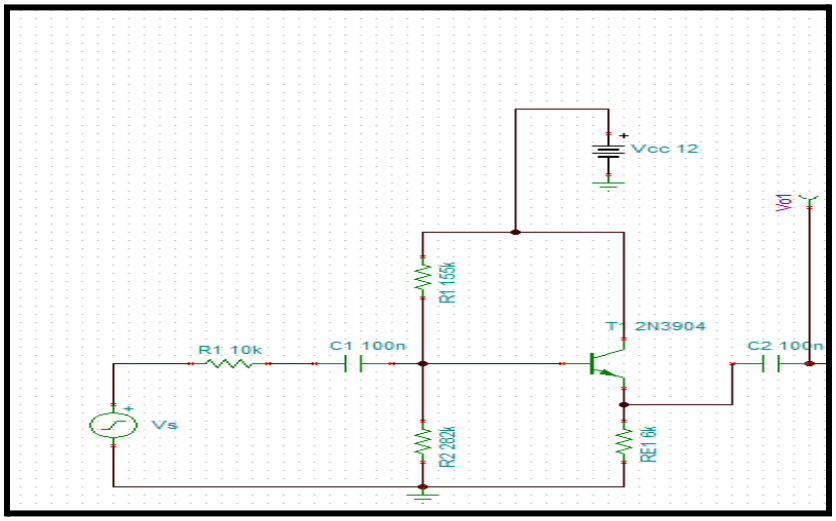

Figure 13: Tina Input Buffer

B. Stage 2: 2 Stage Gain (Common-Emitter)

The 2-stage common-emitter amplifier is used to provide the necessary voltage gain in the overall circuit. It is placed after the input buffer stage, which is an emitter follower. The input buffer stage, as mentioned earlier, provides high input impedance and low output impedance while maintaining a stable output voltage that closely follows the input voltage. This ensures that the input signal is not distorted or attenuated before being fed into the gain stage. The 2-stage common-emitter amplifier is essentially two common-emitter amplifiers connected in series. The output of the first stage is connected to the input of the second stage, allowing the voltage gains of each stage to be multiplied together, resulting in a higher overall voltage gain for the combined amplifier. This configuration is particularly useful when a large voltage gain is needed, as it allows for better control over the gain and stability of the circuit compared to using a single common-emitter stage with very high gain. The first common-emitter stage receives the output from the input buffer stage (emitter follower) through a coupling capacitor. This capacitor is used to block any DC voltage from the previous stage, preventing any DC offset from affecting the biasing of the common-emitter stages. The capacitor allows only the AC signal to pass through, ensuring that the common-emitter stages are biased correctly and can amplify the signal as intended. Each common-emitter stage consists of a transistor, a voltage divider network for biasing, and resistors connected to the emitter and collector of the transistor. The voltage divider network sets the operating point (also called the Q-point) of the transistor, which is crucial for achieving the desired voltage gain and ensuring that the transistor remains in the active region during amplification. The amplified output from the second common-emitter stage is then fed into the output buffer stage (another emitter follower), which provides the necessary current gain and low output impedance to drive the load, such as a speaker. Refer to **Figure 14** for the schematic of the 2-stage common-emitter amplifier built within Tina.

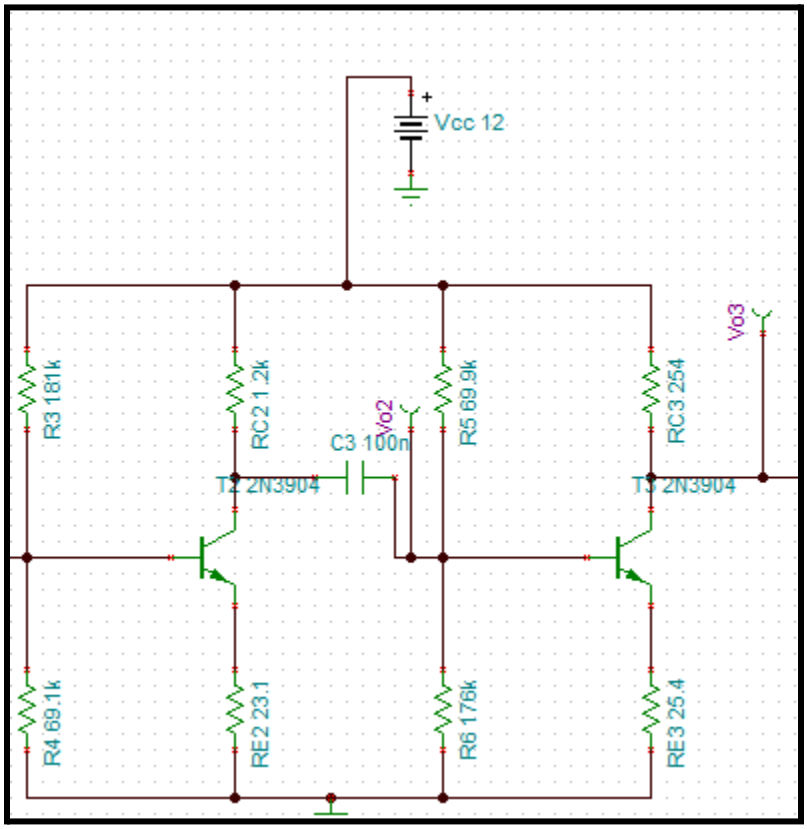

Figure 14: 2 Stage Common Emitter

C. Stage 3: Buffer Output (Emitter Follower)

The output buffer stage uses a BJT TIP31, an emitter resistor Re4=20Ω, and a coupling capacitor of 0.1 µF connected at the top of Re4. The purpose of this stage is to provide the necessary output current and power to drive the 8Ω load speaker. The circuit is biased with a Vcc of 12 V, and the input voltage Vs is equal to Vo3 from the previous stage. The final output Vo4 is where the load speaker is connected. Refer to **Figure 15** for the schematic of the output buffer stage.

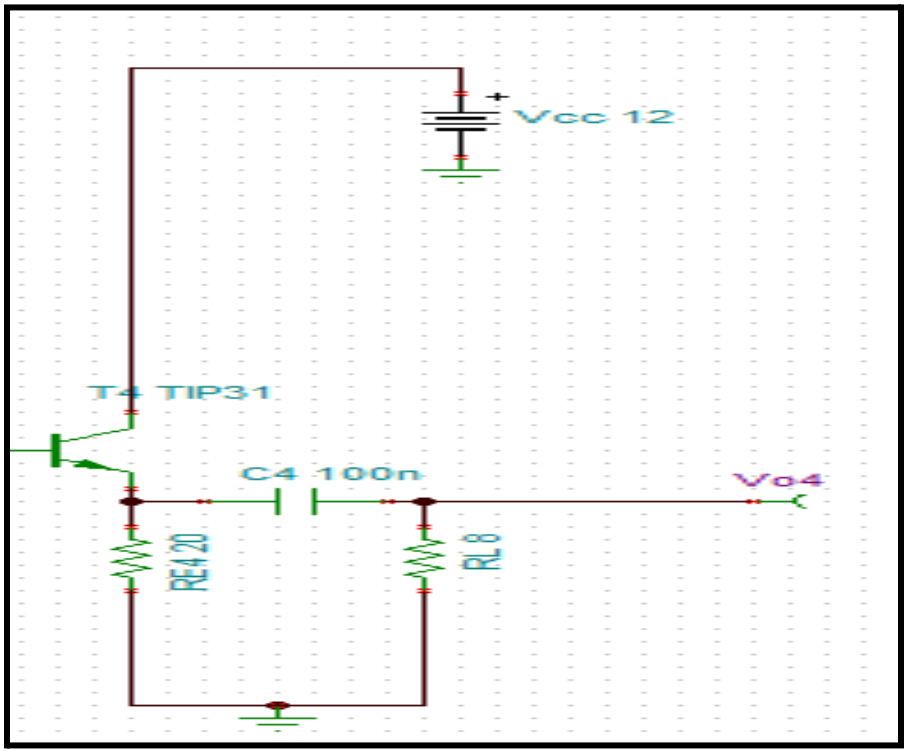

Figure 15: Output Buffer

D. Tina-TI Output

The complete audio amplifier circuit was constructed and simulated in TINA-TI software. The transient analysis output waveforms of all stages are shown in **Figure 17**. The input frequency was set to 7 kHz, which is reflected in the period of the output waveforms.

Refer to **Figure 16** for the complete amplifier construction in TINA-TI. Coupling capacitors: In a multi-stage amplifier, coupling capacitors are used to connect the output of one stage to the input of the next stage. They block any DC voltage from the previous stage, preventing it from affecting the biasing of the following stage. By doing so, they allow only the AC signal to pass through, ensuring that the next stage is biased correctly and can amplify the signal as intended. In the described audio amplifier circuit, coupling capacitors are used between the input buffer stage and the 2-stage common-emitter amplifier, as well as between the common-emitter amplifier and the output buffer stage.

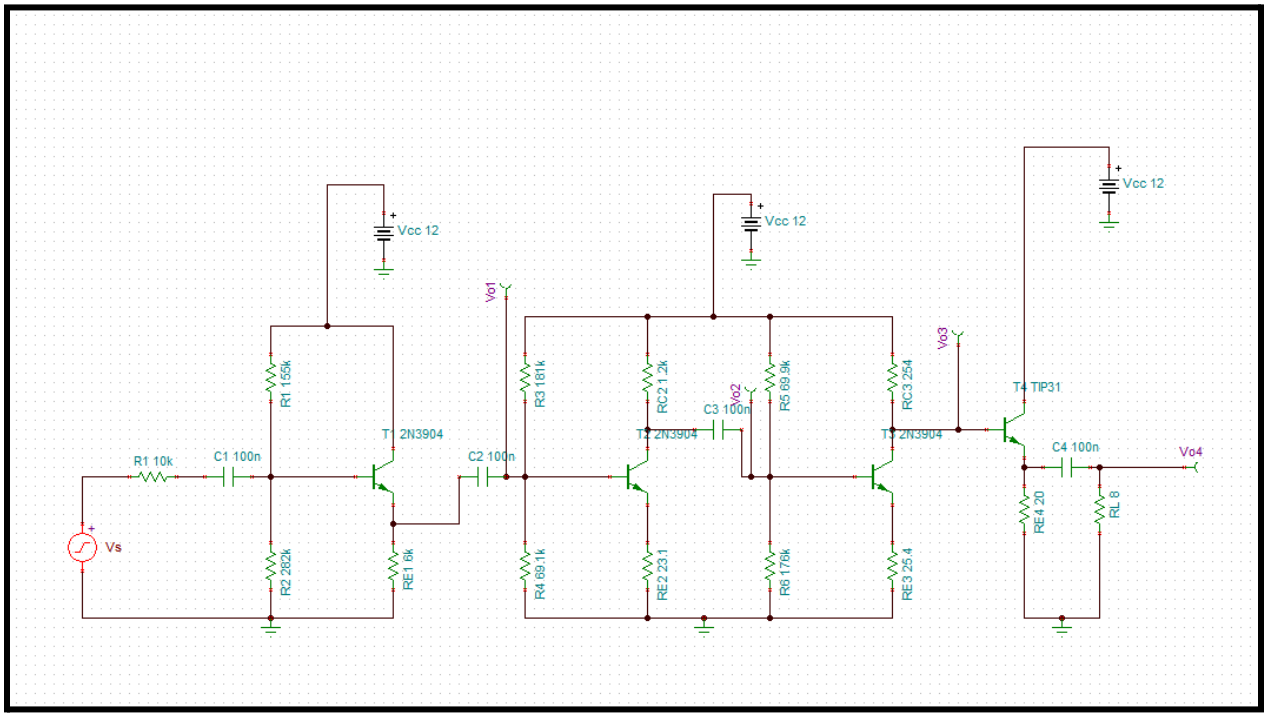

Figure 16: Total Circuit Construction

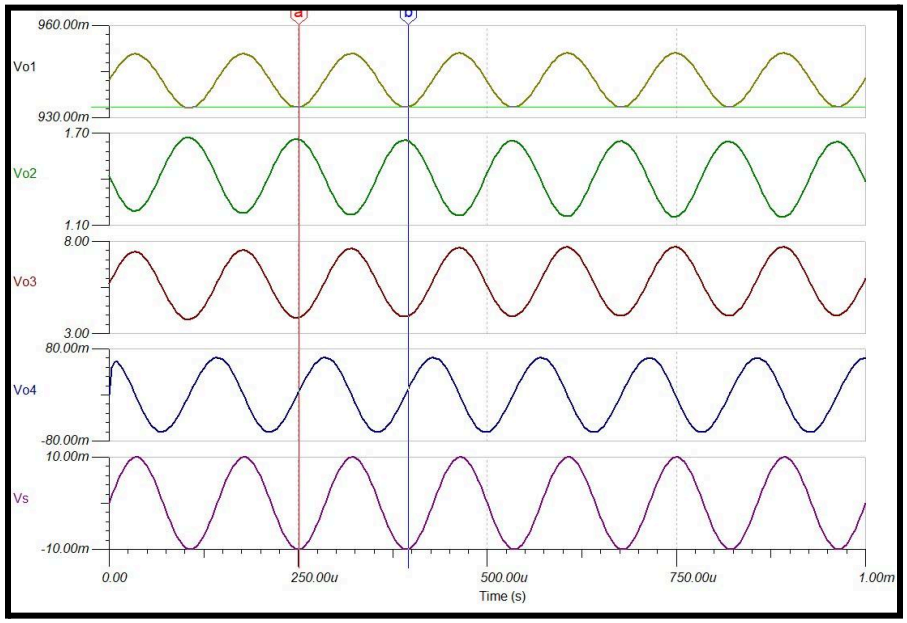

Figure 17: Transient Voltage Outputs

V. Progress Report 2

A. Circuit Construction and Initial Observations

In this phase of the project, we built the audio amplifier circuit on a breadboard based on the characteristics and design parameters obtained from the TINA-TI simulations. As we began to test the

physical circuit, we quickly realized that the breadboard and connecting wires introduced non-ideal conditions that differed from the simulations. These non-ideal conditions, such as parasitic capacitance and inductance, can cause discrepancies between the simulated and actual performance of the circuit.

Initially, we observed a maximum output voltage of 802 mV (**Figure 18**). To minimize the impact of the breadboard's non-ideal conditions and reduce the amount of noise, we reconstructed the circuit using fewer wires and aimed to keep the connections as short and direct as possible. Additionally, we added a large capacitor across the positive and negative terminals of the entire circuit to help filter out any noise, and we used a 0.1 µF capacitor on the output stage at this stage. Breadboards are not ideal for high-frequency circuits like this one, where the input is a 10 mV 7,000 Hz wave, because the parasitic capacitance, inductance, and resistance introduced by the breadboard and wires can negatively affect the circuit's performance and frequency response

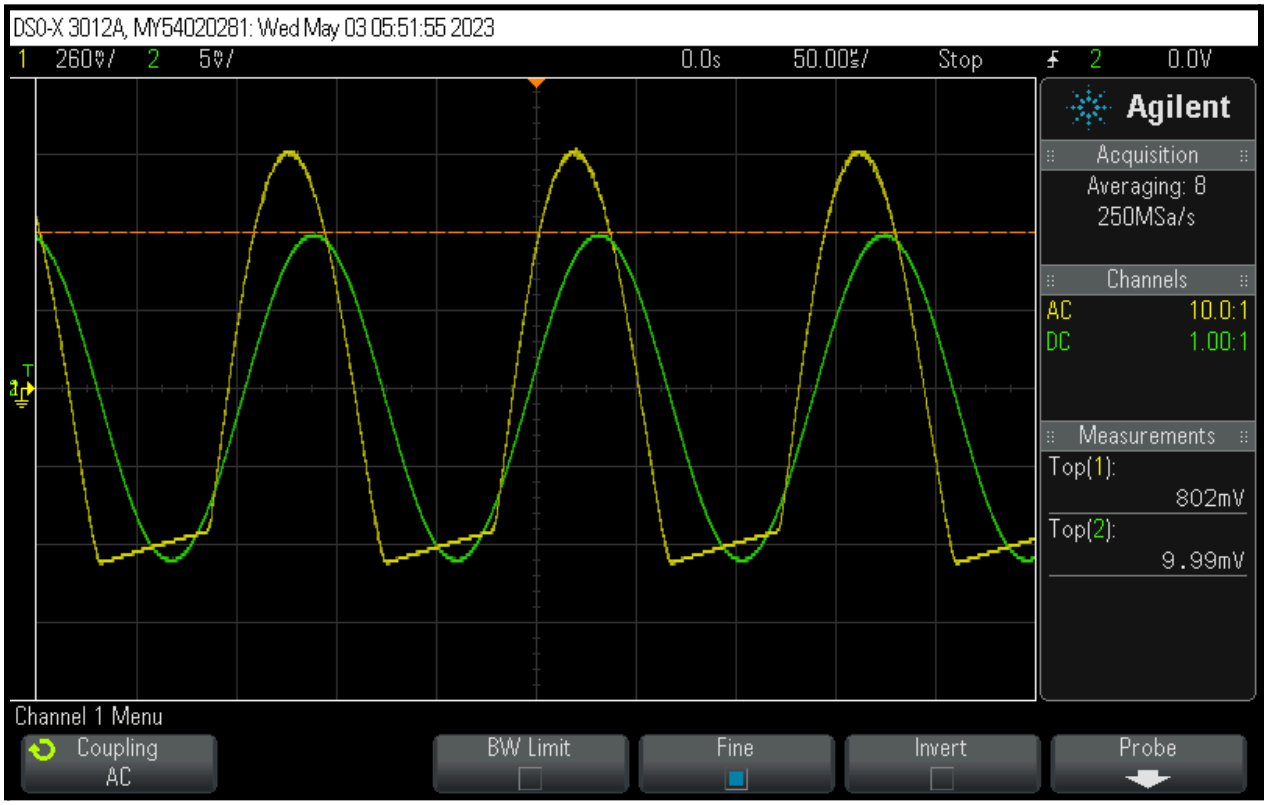

Figure 19: Initial Outputs

B. Adjustments to the Gain Stage

To further improve the performance of the audio amplifier, we made adjustments to the gain stage. We replaced the 0.1 µF capacitor at the output stage with a larger 0.33 µF capacitor and conducted more trials. We observed that the outputs Vo2 and Vo3 were influenced by the values of the Re and Rc resistors in the gain stage. To optimize the circuit's performance, we decided to lower the values of the Re resistors while slightly increasing the Rc resistors.

As a result of these modifications, we achieved an output voltage of 1.244 V, as shown in **Figure 20**. However, the output waveform exhibited significant noise on the rising edge. This noise could be caused by several factors, including parasitic inductance and capacitance in the breadboard and connecting wires, as well as electromagnetic interference from external sources. Another possible cause is the switching transients and non-linear behavior of the transistors, which can introduce high-frequency components into the output waveform.

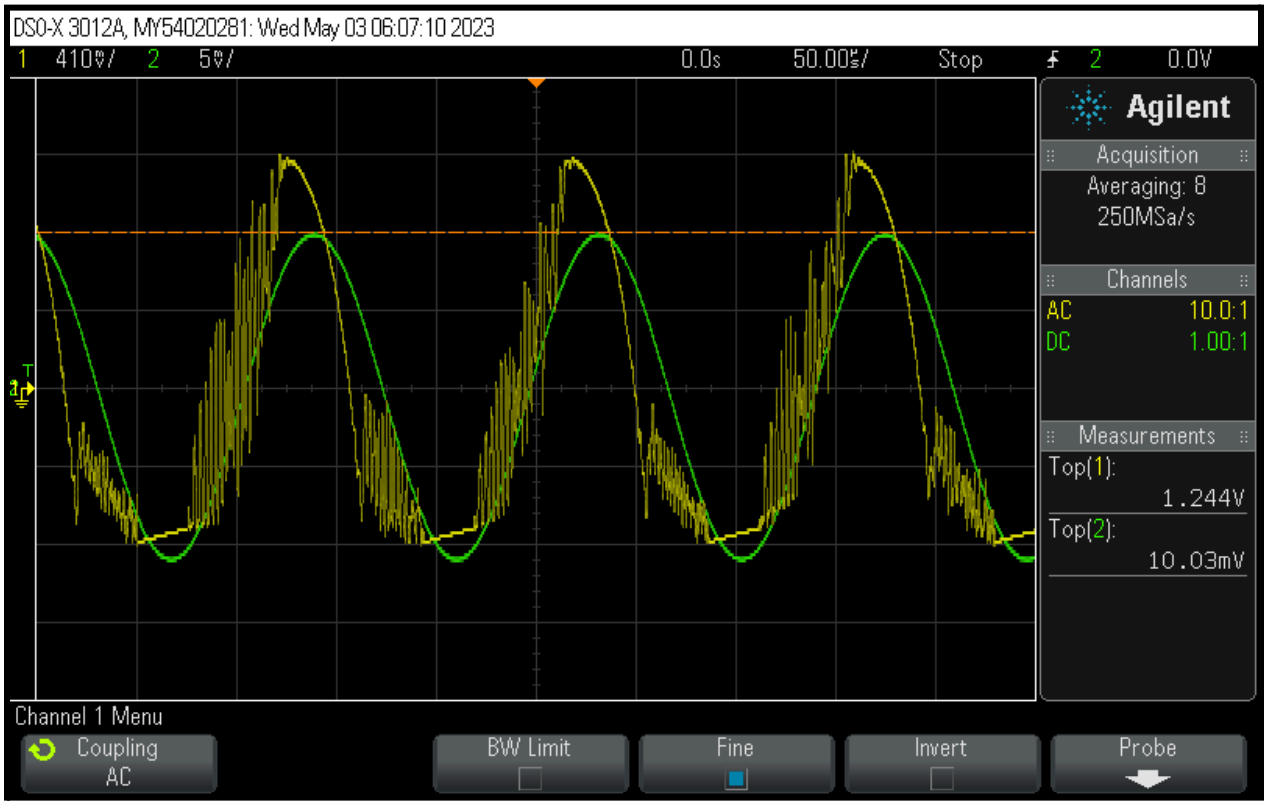

Figure 20: Gain Stage Adjustments

C. Fine-tuning and Results

After the adjustments to the gain stage, we performed further fine-tuning of the audio amplifier circuit. At an input frequency of 7000 Hz, we achieved an output voltage of 1.25 V, which is very close to the desired output of 1.26 V (**Figure 21**).

Next, we lowered the input frequency to 1000 Hz, resulting in a highly noisy, non-sinusoidal output voltage of 934 mV (**Figure 22**). The increased noise at this lower frequency could be attributed to the circuit's frequency response and the characteristics of the transistors used. The amplifier might exhibit higher gain or sensitivity at lower frequencies, causing it to pick up more noise and distort the output waveform.

We then increased the input frequency to the upper end of the audio range, 12 kHz. The output signal appeared to be less noisy, with a maximum output voltage of 1.212 V (**Figure 23**). The decreased noise at higher frequencies could be due to the amplifier's frequency response, which might have lower gain or sensitivity at these higher frequencies. This results in less noise being picked up and a cleaner output waveform.

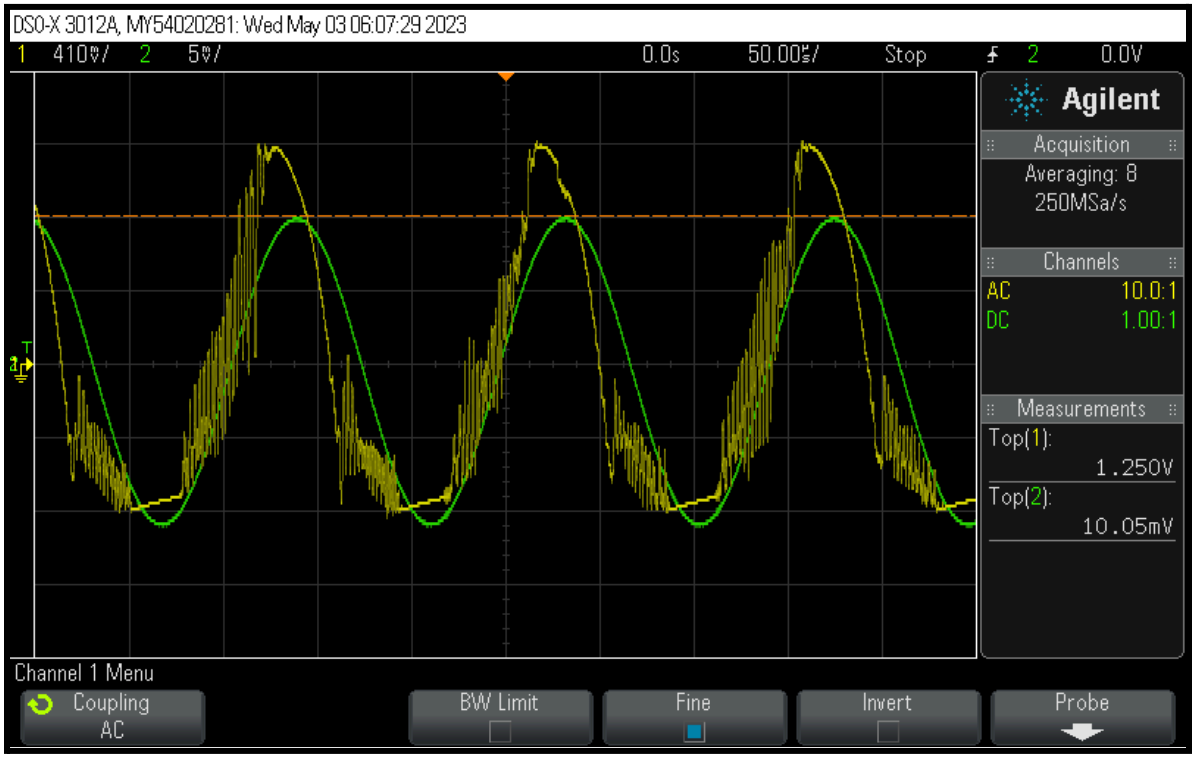

Figure 21: Fine Tune 7000 Hz

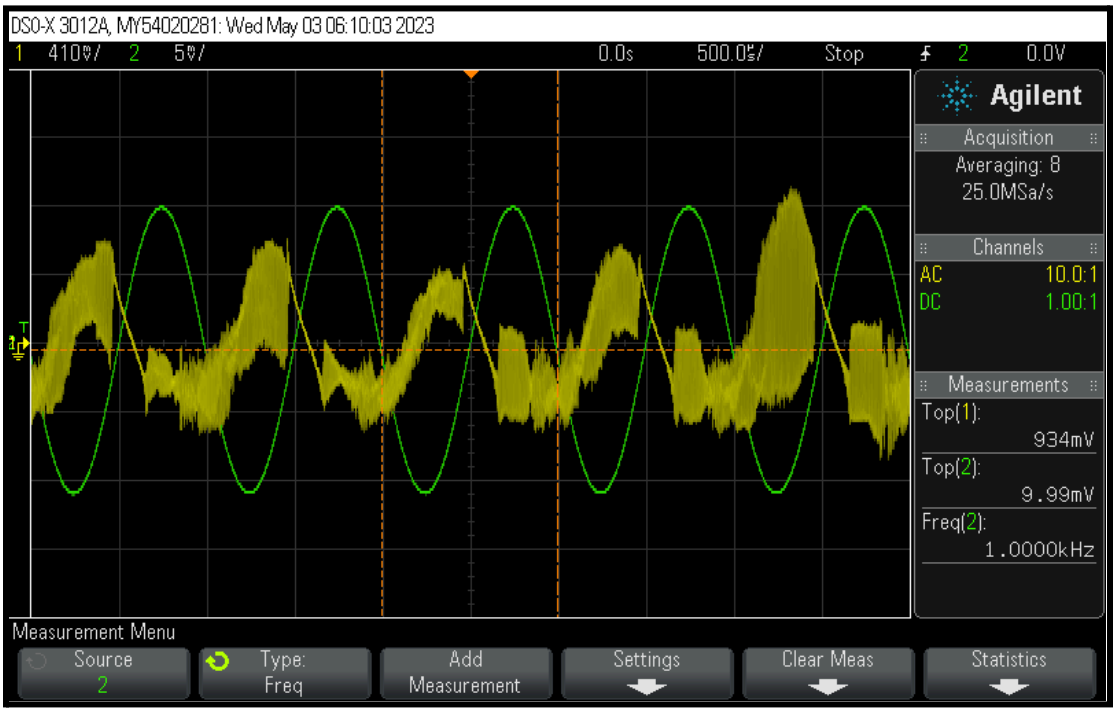

Figure 22: Fine Tune 1000 Hz

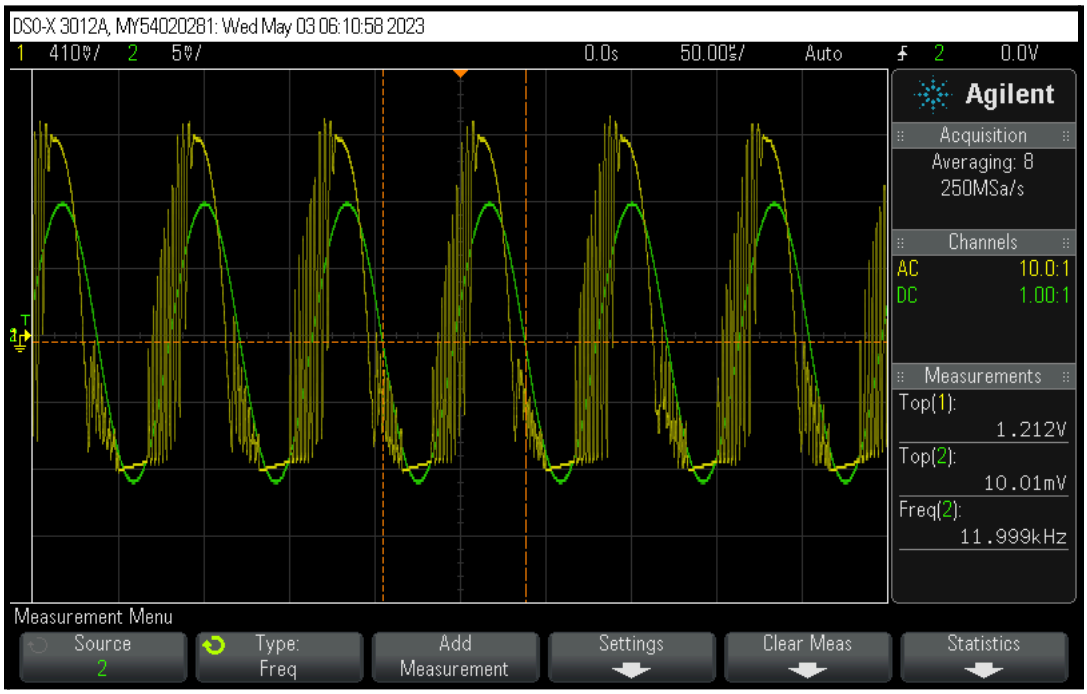

Figure 23: Fine Tune 12,000 Hz

VI. Circuit Values and Q Point Analysis

A. Input Stage

The Q point (quiescent point) is the DC operating point and is crucial as it affects the amplification properties of the transistor. For the input stage of our amplifier, an NPN BJT 2N3904 is used. This stage is biased with a Vcc of 12 V, and the input source has a resistance Rs of 10 kΩ and a voltage Vs of 10 mV. The Q point is determined by the biasing resistors R1 and R2, and the emitter resistor Re1. The voltage divider network created by R1 and R2 sets the base voltage, which is crucial to ensure that the transistor operates in the active region for signal amplification. The emitter resistor Re1 is used to stabilize the Q point against variations in transistor parameters.

The Q point for the input stage is depicted in **Figure 24** in the Appendix, which is a plot of the collector current (IC) versus the collector-emitter voltage (VCE). The Q point is where the load line intersects the characteristic curve of the transistor.

B. Gain Stage

The gain stage of the amplifier is made up of two common-emitter amplifier stages, each with its own Q point. The Q point for each stage is determined by the biasing resistors and the emitter resistor, similarly to the input stage. This biasing ensures that the transistor operates in the active region, where it acts as an amplifier.

The Q point is crucial in the gain stage because it affects the voltage gain of the amplifier. If the transistor is not biased at the correct Q point, the output signal may be distorted due to non-linear amplification.
The Q point for the gain stage is represented in **Figure 25** in the Appendix. It is again a plot of the collector current (IC) versus the collector-emitter voltage (VCE). The Q point is where the load line intersects the characteristic curve of the transistor.

C. Output Stage

The output stage uses a BJT TIP31 and is designed to provide the necessary output current and power to drive the load, in this case, an 8Ω speaker. As with the previous stages, the Q point is determined by the biasing resistors and the emitter resistor.

In the output stage, the Q point is especially important because it affects the power output of the amplifier. If the transistor is not biased at the correct Q point, the power output may be lower than expected, or the transistor may not operate in the correct region, leading to distortion of the output signal.
The Q point for the output stage is shown in **Figure 26** in the Appendix. Like the previous stages, it is a plot of the collector current (IC) versus the collector-emitter voltage (VCE). The Q point is where the load line intersects the characteristic curve of the transistor.

VII. Final Conclusions and Observations

The exploration of this three-stage audio amplifier circuit has been an enriching and enlightening journey, underscoring the intricate balance that governs the performance of audio amplifiers. It has offered us comprehensive insights into the meticulous nature of amplifier design and the pivotal role that each stage plays in the overall performance and efficiency of the amplifier. As with any complex engineering endeavor, this experiment showcased the delicate interplay between theory and practice, further reinforcing the importance of understanding fundamental principles, while also appreciating the potential variations and discrepancies that arise when theory is applied to real-world scenarios.

Our initial design achieved a commendable approximation of the target output, delivering an output of 1.25V for a 7000 Hz wave input. Although this was marginally lower than the desired 1.26V output, it is important to appreciate the inherent complexities and limitations that come into play with real-world components and simulation software. Such slight variations are not uncommon and can be attributed to a multitude of factors such as component tolerances, parasitic elements, and limitations of the simulation environment. Despite these challenges, it was noteworthy that our circuit design was able to approximate the desired output with a high degree of accuracy.

During the course of this experiment, the critical role of the gain stage resistors, Re and Rc, came to light. Alterations in these resistors led to the most significant changes in the output. Given that these resistors directly control the voltage gain of the amplifier, this observation was not surprising. Adjustments in these resistors provide a means to finely tune the amplifier's response to the input signal. This vital revelation underscores the significance of component selection in amplifier design. In an ideal world, we could achieve even greater control over the output through a more refined selection of these resistors, potentially utilizing an automated optimization process or adopting a more iterative design approach.

The introduction of a large capacitor across the entire positive and negative terminals of the circuit, otherwise known as a bypass or decoupling capacitor, played a significant role in the circuit's performance. This capacitor served as a power supply filter, smoothing out any noise or fluctuations, and providing a stable DC voltage source for the circuit. The stability offered by this capacitor is crucial for the consistent performance of the amplifier and likely contributed significantly to achieving an output close to the desired value. This aspect of the design emphasized the importance of power supply design and filtering in audio amplifier circuits, a lesson that will undoubtedly inform future design endeavors.

Looking ahead, transferring this circuit onto a printed circuit board (PCB) would likely enhance its performance even further. PCBs offer several advantages such as lower parasitic capacitance and inductance, better control over component placement, improved signal integrity, and better heat dissipation. Such improvements could lead to lower signal distortion and interference, and more reliable and consistent operation of the amplifier. This transition would be a logical next step in the development and improvement of this audio amplifier design and would provide an excellent platform for further experimental investigations.

Moreover, during this experiment, we had the opportunity to delve deeper into the nuances of audio amplifier circuits. The understanding we developed about the impact of component selection, circuit configuration, and biasing on the performance of the amplifier circuit was invaluable. This experiment was a testament to the fact that a theoretical understanding, while essential, needs to be complemented by practical implementation to truly appreciate and navigate the complexities of audio amplifier design.

In conclusion, this journey of designing and simulating a three-stage audio amplifier has been incredibly rewarding, offering countless lessons and insights. This experiment served as a clear demonstration of the fundamental principles underlying audio amplifier design and emphasized the significance of careful component selection and precise circuit design for achieving optimal amplifier performance. The insights gained from this work have not only provided a robust foundation for future

VIII. Appendix

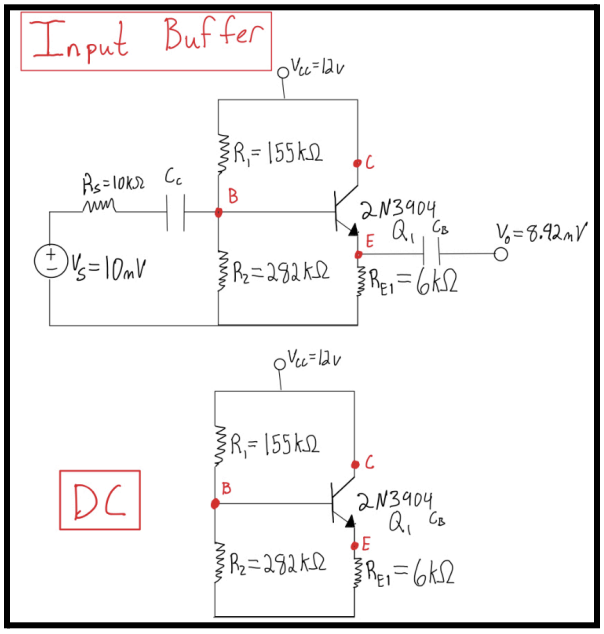

Figure 2: DC Design Input Buffer

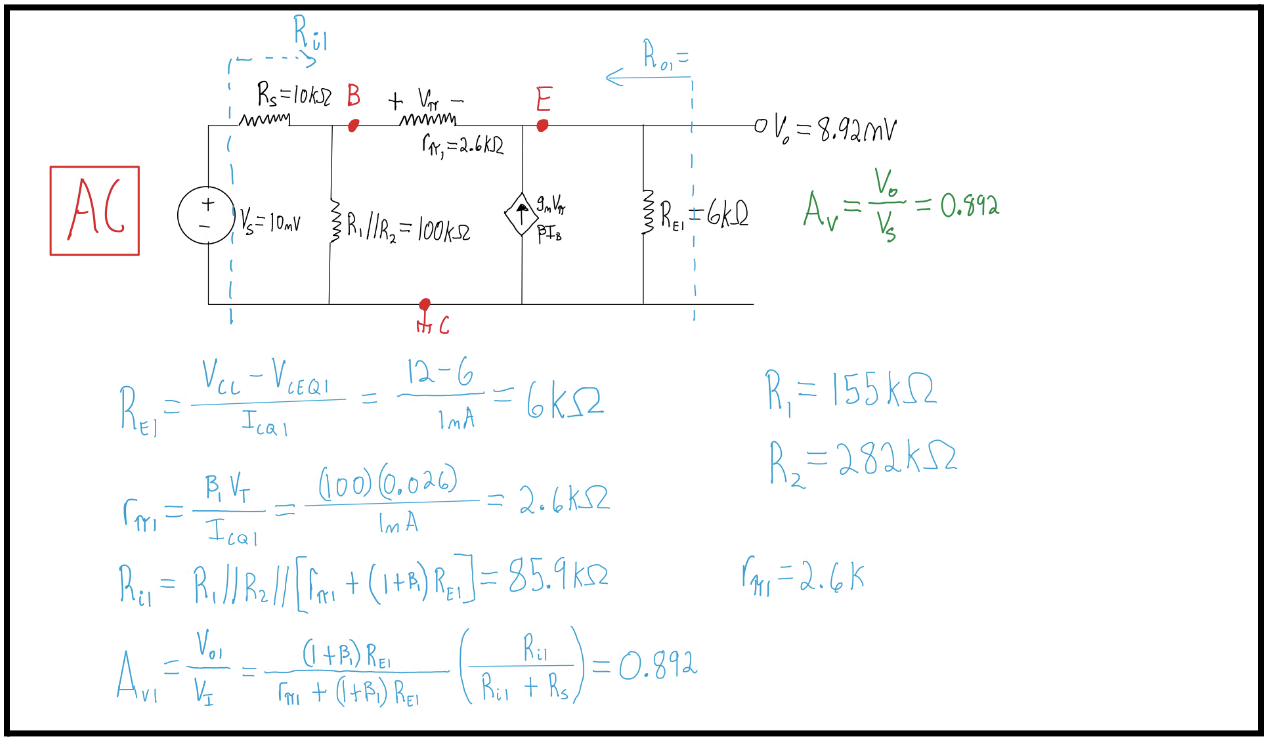

Figure 3: AC Design Input Buffer

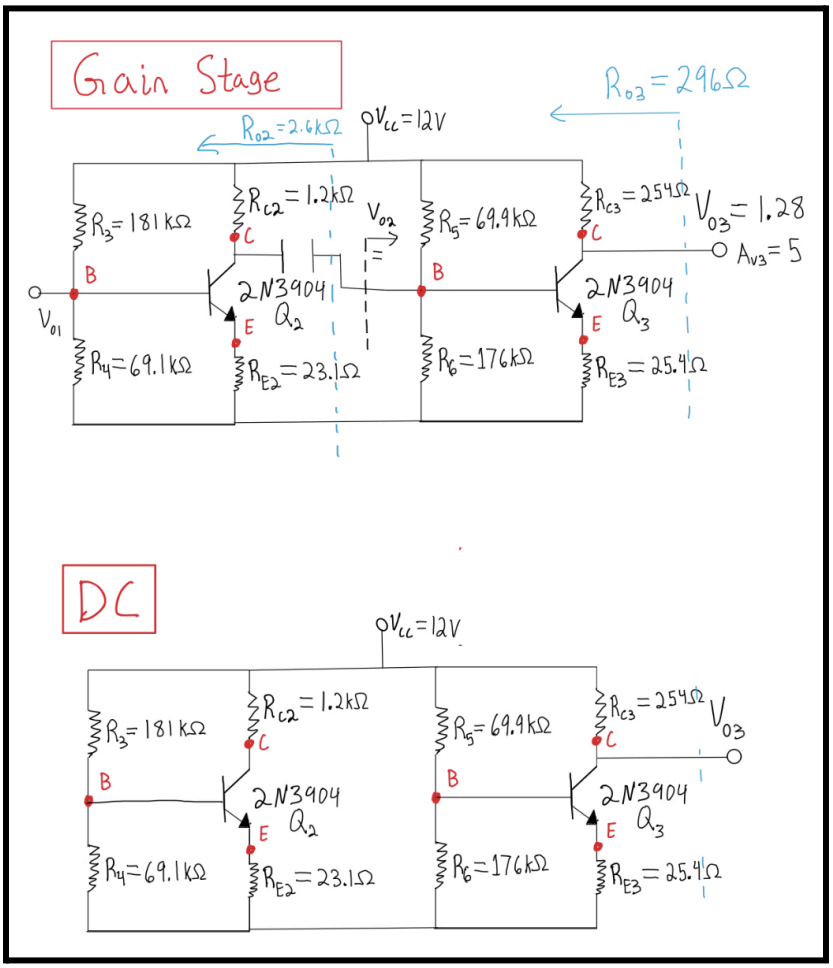

Figure 4: DC Design Gain Stage

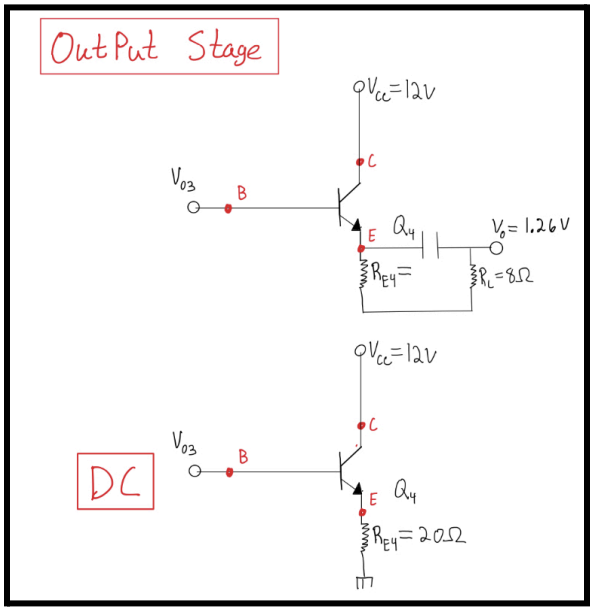

Figure 6: DC Design Output Buffer

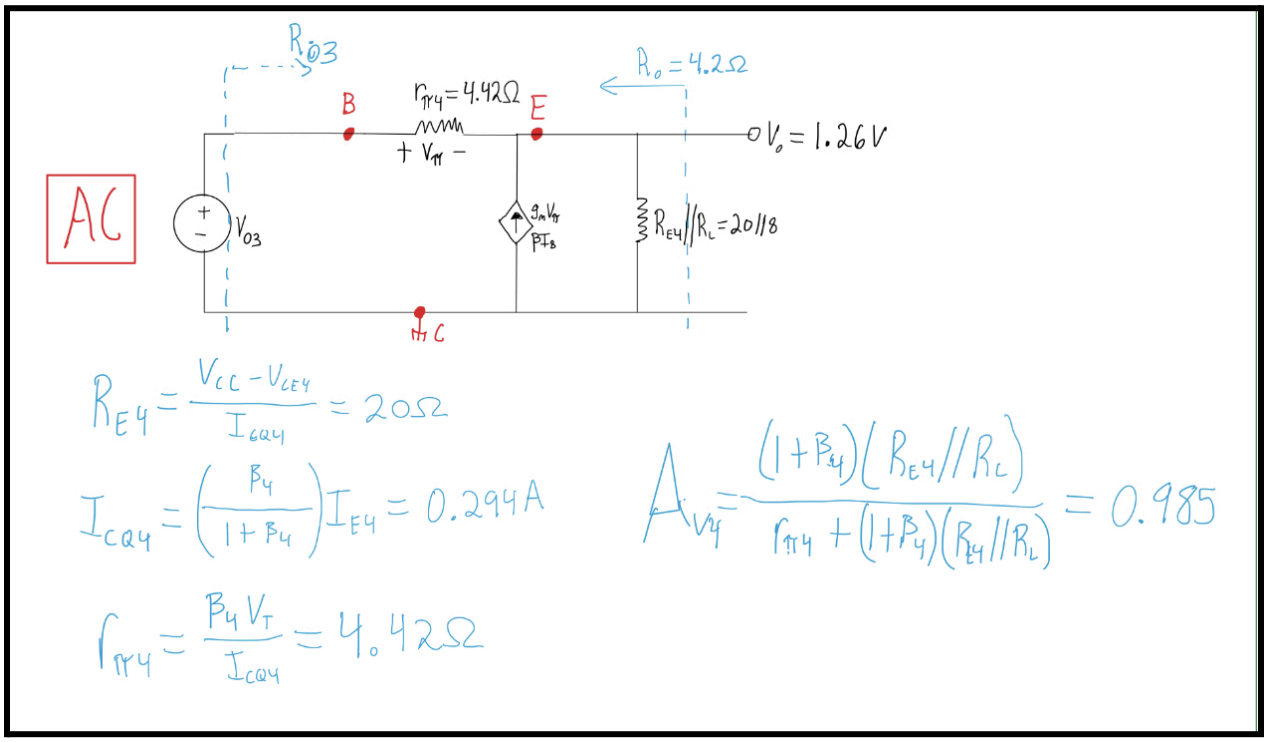

Figure 7: AC Design Output Buffer

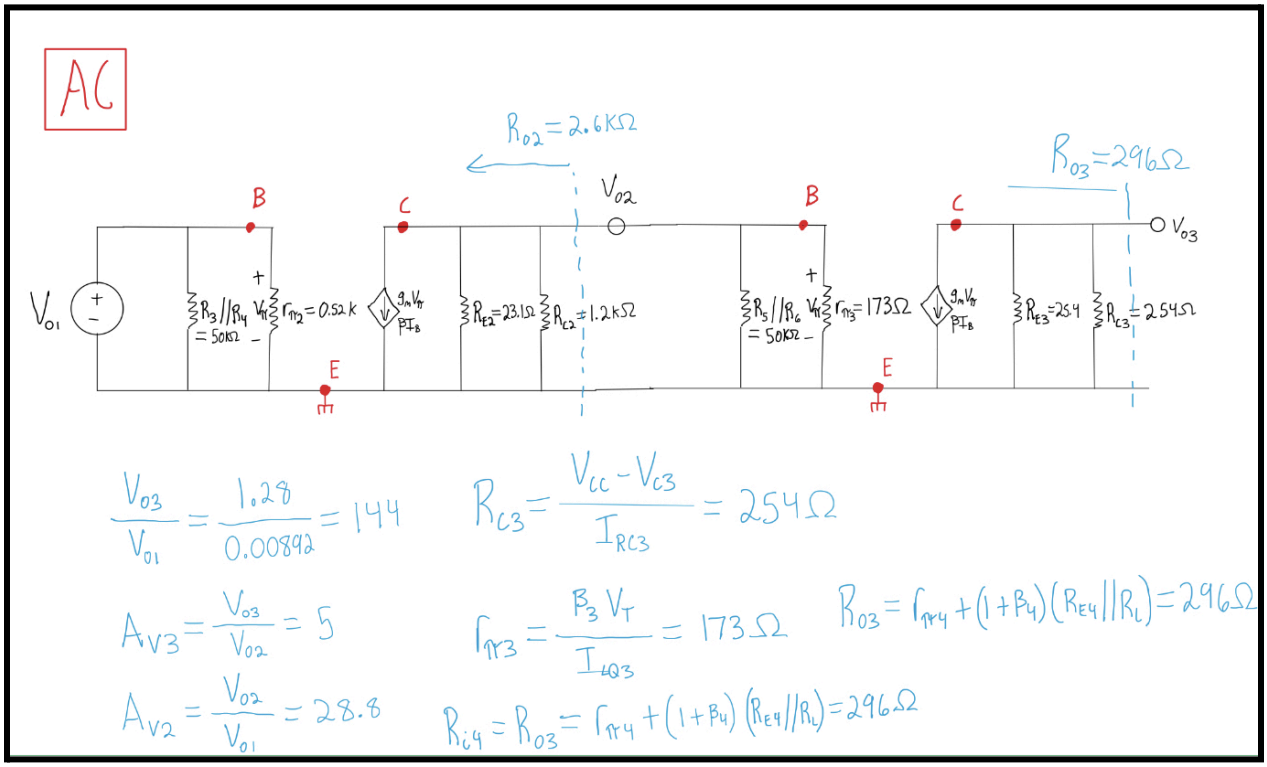

Figure 5: AC Design Gain Stage

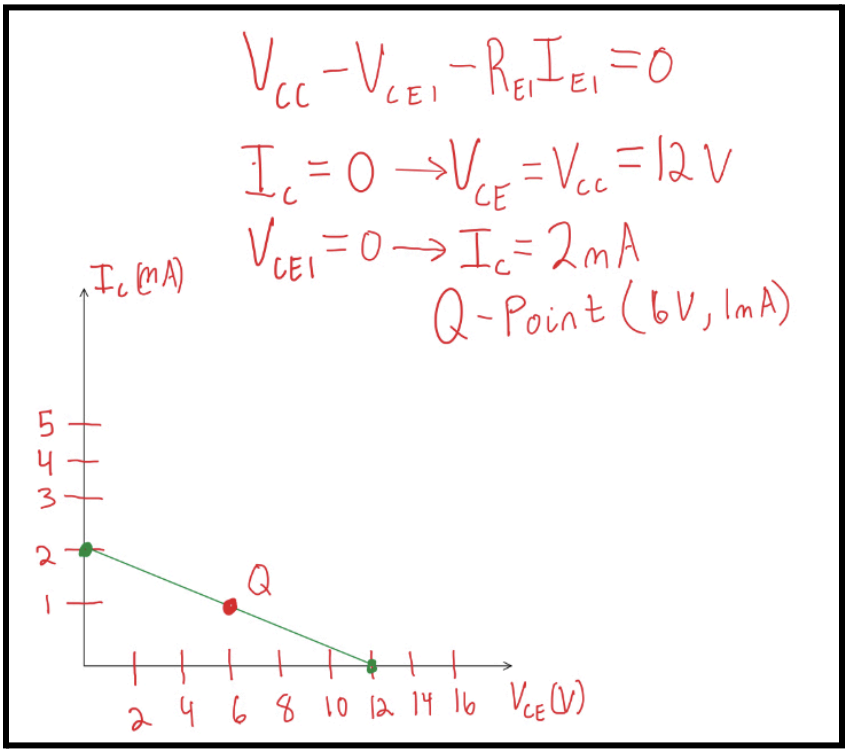

Figure 24: Input Q-Point

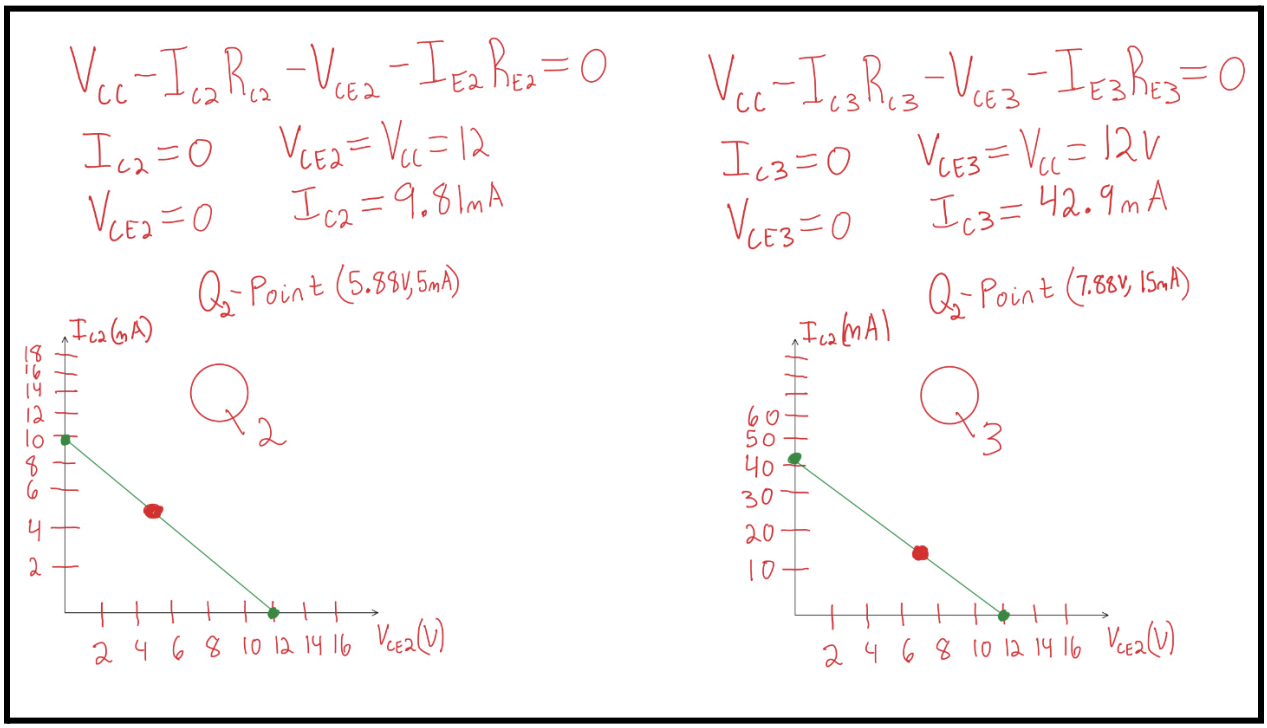

Figure 25: Gain Q-Point

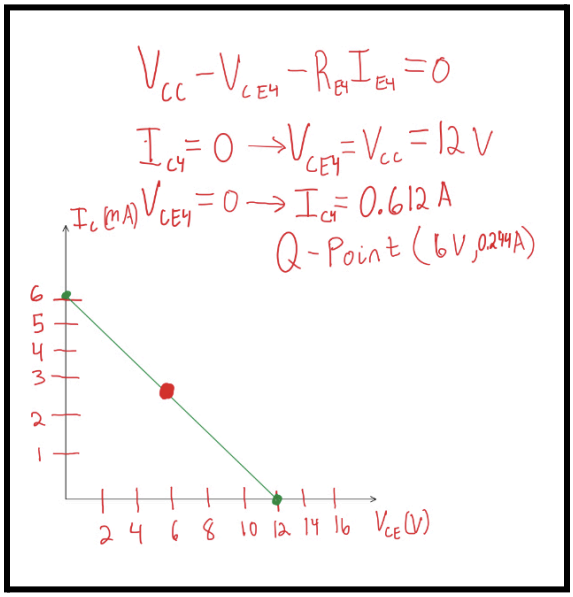

Figure 26: Output Q-Point