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Review

A nonlinear macromodel for current backward transconductance amplifier

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ABSTRACT

A SPICE-compatible macromodel for emulating the nonlinear behavior of the current backward transconductance amplifier (CBTA) at low-frequency is developed. The novelty of the proposed macromodel is that real physical active device performance parameters together with parasitic elements of the input–output terminals of the CBTA are taken into account. In a first step, the CBTA is designed with ±2.5 V by using standard CMOS technology of 0.35 μm AMS and the main performance parameters, such as: DC gain, bandwidth, slew-rate, dynamic range, along with parasitic elements are obtained. In a second step, the behavioral model of the CBTA is deduced and the SPICE-compatible macromodel is built. In a third step and to validate the deduced behavioral model, two topologies of saturated nonlinear function series (SNFS) based on CBTA are designed. At this point, a generated experimentally chaotic signal was applied as excitation signal to each SNFS built with the CBTA at the transistor level and to the proposed SPICE-compatible macromodel. As a consequence, the derived macromodel can effectively be used for forecasting the behavior of nonlinear circuits in the time-domain with good accuracy, decreasing the CPU-time compared with the model at the transistor level of abstraction.

Contents

1. Introduction

During the last few years, various multiport functional active devices have emerged in the literature to be used in the analog signal processing [1–3]. The main reason is due to the limitations on the constant gain-bandwidth (*GB*) product, low power consumption, low voltage operation and high slew-rate (*SR*) of the operational amplifier. In this sense, all disadvantages mentioned before have been diminished gradually by using hybrid active devices, which can handle current and voltage signals at their input–output ports. Among all multiport hybrid-mode active devices reported in the literature, the Current Backward Transconductance Amplifier (CBTA) handles both voltage and current signals at its input–output ports, which depends on how the ports will be used [4]. In this

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manner, its behavior can ideally be modeled with two current-controlled current sources: one between the *p*- and *w*-terminal and other between *n*- and *w*-terminal. Further, a voltage-controlled current source is between *z*- and the voltage difference of *p*- and *n*-terminals. Furthermore, a voltage-controlled voltage source is used between *w*- and *z*-terminal. Note that if *p*- and *n*-terminals are used as input, then voltage signals will be applied. Otherwise, if both terminals are used as output, then current signals will be got. For the *z*-terminal, if it is used as input, then a voltage signal will be applied, whereas if a current signal is obtained, then *z*-terminal is used as output. For the *w*-terminal, if it is used as input, then a current signal will be applied, whereas if a voltage signal is acquired, then the terminal is used as output. Due to these characteristics, the CBTA has been used in several linear voltage- and current-mode analog signal processing applications [5–9]. However, although the ideal macromodel described above has been used for researching the behavior of CBTA-based analog circuits, some performance parameters are not taken into account, like the *SR* and the dynamic range (*DR*), together with parasitic elements associated to the input–output terminals of the hybrid amplifier. On the one hand, the performance of CBTA-based analog circuits can be researched by using complex models, e.g., at the transistor level of abstraction. However, these models are not only complex and slow when they are used in CAD tools, but the CPU consumption along with the use of memory also increases. On the other hand, the accuracy diminishes whether simple models are used and as consequence, the predicted performance of CBTA-based circuits differs substantially from reality. In this sense, simple and accurate macromodels are required for decreasing the CPU-time and memory use, but without put down the accuracy [10,11]. Moreover, a macromodel not only helps to gain insight on the nonlinear behavior of complex analog circuits, a task that becomes cumbersome when models at the transistor level are used, but they are also useful in the development of electronic design automation methodologies and hence, to analyze and study the trade-off related with complex circuits like chaotic circuits, oscillators, comparators and so on.

The purpose of this paper is introduce a simple and accurate nonlinear macromodel to model the real behavior of CBTAs at low frequency. The derived macromodel includes the most influential performance parameters of CBTA, such as: DC gain (A_{dc}), *GB*, *SR* and *DR*. The rest of the paper is organized as follows: A CMOS design of the CBTA using technology of 0.35 μm AMS is described in Section 2 and HSPICE simulations on the nonlinear behavior of the hybrid amplifier are also illustrated. It is worth to stress that the main target of this paper is not the robust CMOS design of the hybrid amplifier, but the deduction of its nonlinear macromodel. Nevertheless, if sub-nanometer technologies are used, then short channel effects, voltage and temperature variations, inter- and intra-die process variations and corner effects like typical-typical (TT), fast–fast (FF), slow-slow (SS), fast-slow (FS) and slow-fast (SF) are obtained, which are very difficult to model and include them within a macromodel based on transactors and passive elements, since all these effects are probabilistic and statistical results [12]. Section 3 deals with the deduction of the behavioral macromodel for CBTA and its SPICE-compatible macromodel is also built. To validate the deduced SPICE-compatible macromodel, in Section 4 a chaotic waveform is applied to two saturated nonlinear function series (SNFS) based on CBTAs at the transistor level of abstraction and by using the proposed macromodel. It is worth mentioning that this nonlinear function not only is the main core of a chaotic dynamical system in order to generate chaotic waveforms at 1-direction, 2-directions, 3-directions and 4-directions, but also is the responsible on the behavior of some common metrics used for evaluating the complexity of nonlinear systems, such as Lyapunov exponents and so on [13]. Numerical simulations on the behavior of both topologies in the time-domain and by using each macromodel are compared. Finally, conclusions are drawn in Section 5.

2. CMOS design of CBTA

The CBTA is a hybrid amplifier which can process both voltage–current signals at its input–output ports. Its symbolic representation is shown in Fig. 1a) and its ideal behavior equation is described as

$$\begin{bmatrix} i_z \\ v_w \\ i_p \\ i_n \end{bmatrix} = \begin{bmatrix} g_m & -g_m & 0 & 0 \\ 0 & 0 & A_w & 0 \\ 0 & 0 & 0 & A_{ip} \\ 0 & 0 & 0 & -A_{in} \end{bmatrix} \begin{bmatrix} v_p \\ v_n \\ v_z \\ i_w \end{bmatrix} \tag{1}$$

where g_m is the transconductance gain, A_w is the voltage gain between the *w*- and *z*-terminal, A_{ip} and A_{in} are the current gains between the *w*- and *p*-terminal and *w*- and *n*-terminal, respectively. Ideally, A_w, A_{ip} and A_{in} are unitary, the input impedances at *p*- and *n*-terminal are infinities, the output impedance at *z*-terminal is infinite and the output impedance at *w*-terminal is zero. The CMOS implementation of the CBTA is shown in Fig. 1(b) [4], with $V_{DD} = -V_{SS} = 2.5$ V, $I_{b1} = I_{b2} = 200$ μA. The sizing of each CMOS transistor is given in Table 1 and all CMOS devices operate in the saturation region. To validate the behavior of Fig. 1(b), HSPICE simulations were carried out using AMS 0.35 μm CMOS process model parameters. The DC transconductance transfer characteristics from *p*- and *n*-terminal to *z*-terminal when $g_m = 1.161$ mS is shown in Fig. 2(a) and i_z (blue line) was obtained through $R_z = 1\ \Omega$ connected in the *z*-terminal and the *w*-terminal as open-circuit. According to Fig. 2(a), the CBTA linearly operates between $-100\ \mu A \leqslant i_z \leqslant 100\ \mu A$ for $-100\ mV \leqslant v_p - v_n \leqslant 100$ mV with an error less than 1%. However this error increases due to the nonlinear behavior of the CBTA. The frequency responses of the transconductance gain is illustrated in Fig. 2(b) (blue line) and as a result, the bandwidth of −3 dB is $BW_{-3dB} \approx 275.4$ MHz.

On the one hand, the DC current transfers of i_w (black line) vs. i_p (blue line) and i_w (brown line) vs. i_n (green line) are shown in Fig. 3 (a), respectively. Both output currents were obtained through $R_p = R_n = 1\Omega$ connected to *p*- and *n*-terminal, respectively, while *z*-terminal was grounded. From Fig. 3(a) one can observe that the CBTA linearly operates between $-0.6\ mA \leqslant i_p \leqslant 0.75$ mA and $-0.75\ mA \leqslant i_n \leqslant 0.6$ mA with an error less than 1%. However, the accuracy is lost due to the nonlinear behavior of the CBTA. On the other hand, the frequency responses of current gains are illustrated in Fig. 3(b) and hence, the bandwidth for both current gains are approximated as $BW_{-3dB} \approx 87.1$ MHz.

Moreover, the DC voltage transfer of v_z (black line) against v_w (blue line) is depicted in Fig. 4(a). The output voltage was acquired with a load capacitor $C_w = 1.5$ pF connected to *w*-terminal, whereas the *p*- and *n*-terminals were grounded. As a result, the CBTA linearly works in the range $-1.5\ V \leqslant v_w \leqslant 1.2$ V with an error less than 1%. However, this error also increases due to the nonlinear behavior of the CBTA. The frequency response of the voltage gain is illustrated in Fig. 4(b) and the $BW_{-3dB} \approx 371.5$ MHz. Finally the parasitic resistances and capacitances of the CBTA were computed and given in Table 2. Furthermore, from Figs. 2–4, the performance parameters of the CBTA were obtained and are summarized in Table 3, where $I_{zs,ps,ns}$ are the saturation currents and $DR^{i}_{z,p,n}$ is the *DR* in current at the *z*-, *p*- and *n*-terminal, respectively; $V_{sp,sn}$ are the positive–negative saturation voltages and DR^{v}_{w} is the *DR* in voltage at the *w*-terminal.

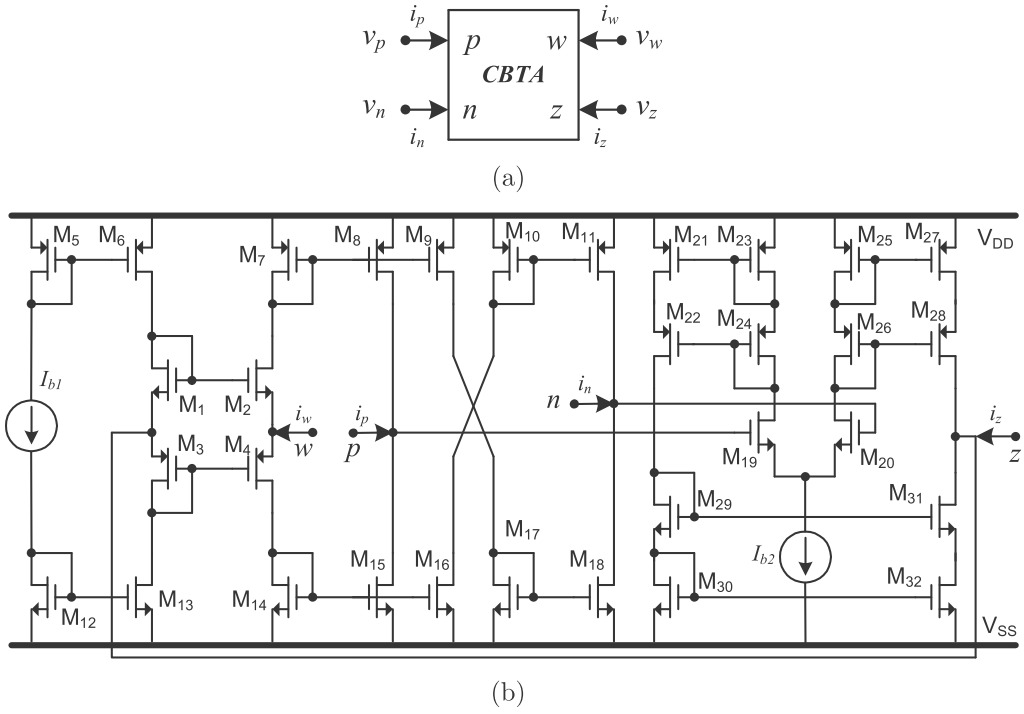

Fig. 1. (a) CBTA symbol and (b) CMOS design of CBTA.

Table 1
Sizing at μm of the CMOS transistors of Fig. 1(b).

PMOS	$M_{3,4}$	$M_{5,6}$	$M_{7,8,9}$	$M_{10,11}$	M_{21-26}	$M_{27,28}$
W/L	200/0.35	15/0.35	5.8/1.35	22/1.35	32/0.35	31/0.35
NMOS	$M_{1,2}$	$M_{12,13}$	$M_{14,15,16}$	$M_{17,18}$	$M_{19,20}$	M_{29-32}
W/L	200/0.35	10/0.35	2.3/1.35	8/1.35	20/0.35	10/0.35

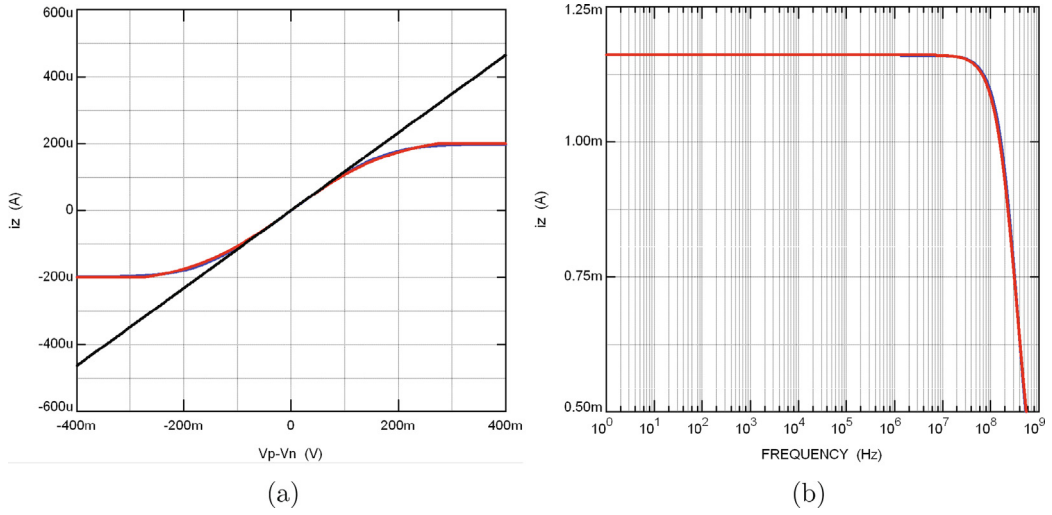

Fig. 2. Variation of $g_m = \frac{i_z}{v_p - v_n}$, blue line for CMOS CBTA, red line for nonlinear macromodel and black line is $v_p - v_n$: (a) DC response and (b) Frequency response. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

3. Behavioral model generation for CBTA

A macromodel is a compact circuit that emulates the real behavior of an active device or circuit without modeling each of its elements. The proposed nonlinear macromodel for CBTA is shown in Fig. 5, where the most influential performance parameters are included. From Fig. 5, $R_p, R_n, R_w, R_z, C_p, C_n, C_w$ and C_z are the parasitic resistances and capacitances on the p-, n-, w- and z-terminals, respectively, and the numerical value of each of them is given in Table 2. Here, V_x is a voltage source that is used not only to measure i_w, but can also be useful for modeling the offset. In each p-, n- and z-terminal, a pair of diodes together with

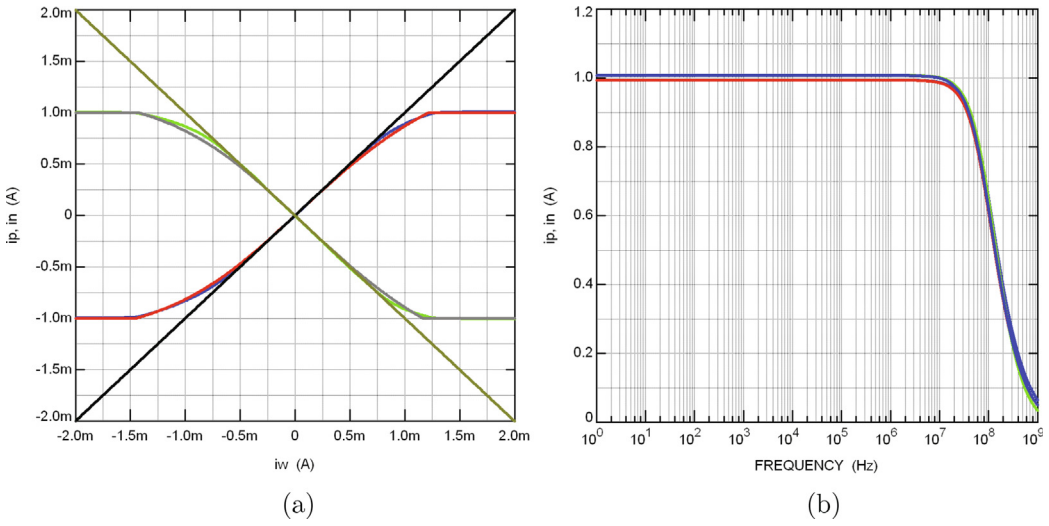

Fig. 3. Variation of: $i_p = A_{ip} i_w$, blue line for CMOS CBTA, red line for nonlinear macromodel and black line for i_w: $i_n = -A_{in} i_w$, green line for CMOS CBTA, gray line for nonlinear macromodel and brown line for $-i_w$: (a) DC response and (b) Frequency response. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

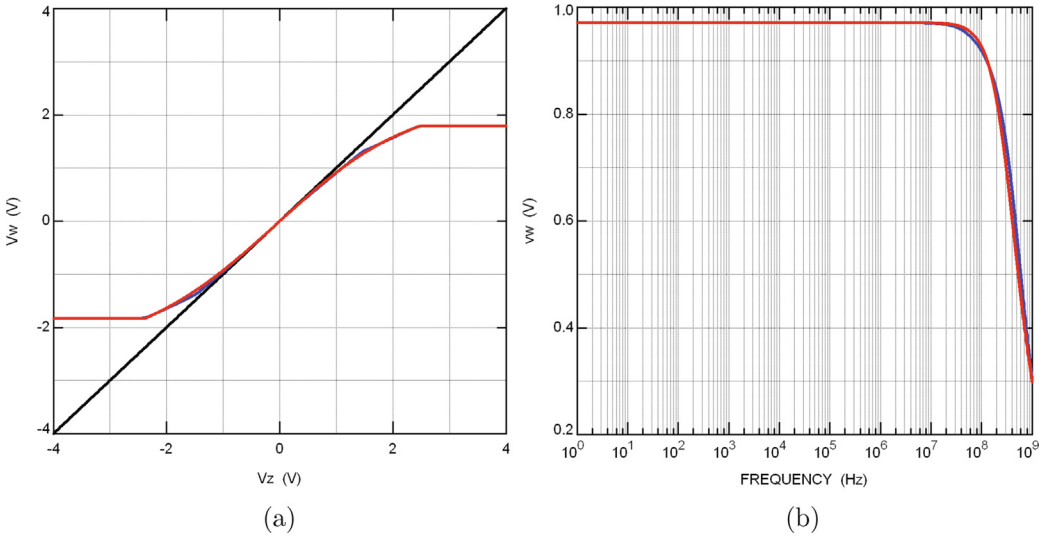

Fig. 4. Variation of $v_w = A_w v_z$, blue line for CMOS CBTA, red line for nonlinear macromodel and black line for v_z: (a) DC response and (b) Frequency response. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

Table 2
Parasitic elements associated to the input–output terminals of Fig. 1(b).

Element	R_p	R_n	R_w	R_z	C_p	C_n	C_w	C_z
Value	39.43 kΩ	39.91 kΩ	197Ω	20.55 kΩ	55pF	53pF	1pF	1.5pF

voltage sources are used to limit the output voltage. Since the CBTA is a transconductance amplifier with z-terminal as output, its linear behavior is governed by

$$\begin{aligned} \frac{dv_z(t)}{dt} &= GB_z(v_p(t) - v_n(t)) - \frac{GB_z}{A_{DCz}} v_z(t) + R_z \frac{GB_z}{A_{DCz}} i_z(t), \\ -\frac{SR_z}{GB_z} &\leqslant v_p(t) - v_n(t) \leqslant \frac{SR_z}{GB_z} \end{aligned} \tag{2}$$

where $A_{DCz} = g_m R_z$, $\omega_{dp} = \frac{1}{R_z C_z}$ is the dominant-pole corner frequency of the open-loop CBTA and $GB_z = \frac{g_m}{C_z}$. Otherwise, when the CBTA enters in the positive or negative saturation current zone, $v_z(t)$ evolves according to

$$\begin{aligned} \frac{dv_z(t)}{dt} &= +SR_z - \frac{GB_z}{A_{DCz}} v_z(t) + R_z \frac{GB_z}{A_{DCz}} i_z(t), \quad +\frac{SR_z}{GB_z} < v_p(t) - v_n(t) \\ \frac{dv_z(t)}{dt} &= -SR_z - \frac{GB_z}{A_{DCz}} v_z(t) + R_z \frac{GB_z}{A_{DCz}} i_z(t), \quad -\frac{SR_z}{GB_z} > v_p(t) - v_n(t) \end{aligned} \tag{3}$$

where $I_{zs} = C_z SR_z$ is the slew-rate current source. Grouping (2) and (3), the full nonlinear macromodel is deduced as

$$\begin{aligned} \frac{dv_z(t)}{dt} &= p_n - \frac{GB_z}{A_{DCz}} v_z(t) + R_z \frac{GB_z}{A_{DCz}} i_z(t), \\ p_n &= \begin{cases} +SR_z, & v_p(t) - v_n(t) > +\frac{SR_z}{GB_z} \\ GB_z(v_p(t) - v_n(t)), & -\frac{SR_z}{GB_z} \leqslant v_p(t) - v_n(t) \leqslant +\frac{SR_z}{GB_z} \\ -SR_z, & v_p(t) - v_n(t) < -\frac{SR_z}{GB_z} \end{cases} \end{aligned} \tag{4}$$

Table 3
Performance parameters of CMOS CBTA.

			z-terminal			
Parameter	g_m		I_{zs}	DR_z^i	BW_{-3dB}	GB_z
Value	1.161 mS		±200 μA	400 μA	275.4 MHz	319.739 kHz
			p-terminal			
Parameter	A_{ip}		I_{ps}	DR_p^i	BW_{-3dB}	GB_p
Value	0.9932		±1 mA	2 mA	87.1 MHz	86.5 MHz
			n-terminal			
Parameter	A_{in}		I_{ns}	DR_n^i	BW_{-3dB}	GB_n
Value	1.007		±1 mA	2 mA	87.1 MHz	87.7 MHz
			w-terminal			
Parameter	A_w	V_{sp}	V_{sn}	DR_w^v	BW_{-3dB}	GB_w
Value	0.9708	1.789 V	1.831 V	3.62 V	371.5 MHz	360.6 MHz

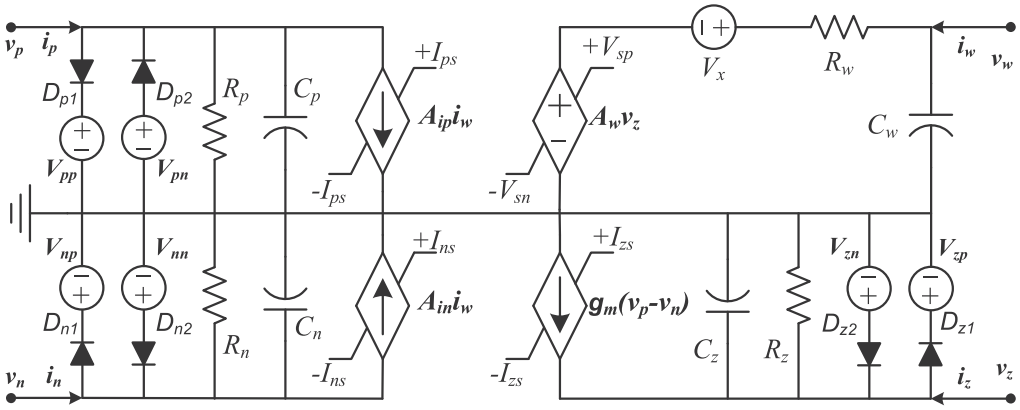

Fig. 5. Proposed nonlinear macromodel of CBTA.

and $v_z(t)$ is limited by the positive and negative saturation voltages given by $V_{zn} \leqslant v_z(t) \leqslant V_{zp}$ and the difference of them is the DR_z^v.

On the other hand, if *w*-terminal is taken as output, then the CBTA is configured as transconductance amplifier plus a voltage follower and its linear behavior is governed by

$$\begin{aligned}\frac{dv_w(t)}{dt} &= GB_w(v_p(t)-v_n(t)) - \frac{GB_w}{A_{DCw}}v_w(t) + R_w\frac{GB_w}{A_{DCw}}i_w(t)\\ &\quad + R_w\frac{di_w(t)}{dt} + \frac{GB_w}{A_{DC_w}}V_x + R_zA_w\frac{GB_w}{A_{DCw}}i_z(t),\\ &\quad -\frac{A_wSR_w}{GB_w} \leqslant v_p(t)-v_n(t) \leqslant \frac{A_wSR_w}{GB_w}\end{aligned} \tag{5}$$

similarly as before, in the positive and negative saturation zones, $v_w(t)$ evolves as

$$\begin{aligned}\frac{dv_w(t)}{dt} &= +A_wSR_w - \frac{GB_w}{A_{DCw}}v_w(t) + R_w\frac{GB_w}{A_{DCw}}i_w(t)\\ &\quad +R_w\frac{di_w(t)}{dt} + \frac{GB_w}{A_{DCw}}V_x + R_zA_w\frac{GB_w}{A_{DCw}}i_z(t), \quad +A_w\frac{SR_w}{GB_w} < v_p(t)-v_n(t)\\ \frac{dv_w(t)}{dt} &= -A_wSR_w - \frac{GB_w}{A_{DCw}}v_w(t) + R_w\frac{GB_w}{A_{DCw}}i_w(t)\\ &\quad +R_w\frac{di_w(t)}{dt} + \frac{GB_w}{A_{DCw}}V_x + R_zA_w\frac{GB_w}{A_{DCw}}i_z(t), \quad -A_w\frac{SR_w}{GB_w} > v_p(t)-v_n(t)\end{aligned} \tag{6}$$

It is important to mention that for this case, $A_{DCw} = A_wg_mR_z$, $GB_w = \frac{A_wg_m}{C_z}$ and $SR_w = SR_z$. Merging (5) and (6), the full nonlinear macromodel for $v_w(t)$ is deduced as

$$\begin{aligned}\frac{dv_w(t)}{dt} &= p_n - \frac{GB_w}{A_{DCw}}v_w(t) + R_w\frac{GB_w}{A_{DCw}}i_w(t) + R_w\frac{di_w(t)}{dt} + \frac{GB_w}{A_{DCw}}V_x\\ &\quad +R_zA_w\frac{GB_w}{A_{DCw}}i_z(t),\\ p_n &= \begin{cases} +A_wSR_w, & v_p(t)-v_n(t) > +\frac{A_wSR_w}{GB_w}\\ GB_w(v_p(t)-v_n(t)), & -\frac{A_wSR_w}{GB_w} \leqslant v_p(t)-v_n(t) \leqslant +\frac{A_wSR_w}{GB_w}\\ -A_wSR_w, & v_p(t)-v_n(t) < -\frac{A_wSR_w}{GB_w}\end{cases}\end{aligned} \tag{7}$$

and $v_w(t)$ is limited by the positive and negative saturation voltages given by $-V_{sn}+V_x \leqslant v_w(t) \leqslant V_{sp}+V_x$ and its difference is the DR_w^v.

Moreover, when the CBTA is used in backward sense, i.e. the *p*- and *n*-terminal configured as output, the linear behavior is derived as

$$\begin{aligned}\frac{dv_p(t)}{dt} &= GB_p(A_wv_z(t)+V_x-v_w(t)) - \frac{GB_p}{A_{DCp}}v_p(t) + R_p\frac{GB_p}{A_{DCp}}i_p(t),\\ &\quad -\frac{SR_p}{GB_p} \leqslant A_wv_z(t)+V_x-v_w(t) \leqslant \frac{SR_p}{GB_p},\end{aligned} \tag{8}$$

$$\begin{aligned}\frac{dv_n(t)}{dt} &= GB_n(A_wv_z(t)+V_x-v_w(t)) - \frac{GB_n}{A_{DCn}}v_n(t) + R_n\frac{GB_n}{A_{DCn}}i_n(t),\\ &\quad -\frac{SR_n}{GB_n} \leqslant A_wv_z(t)+V_x-v_w(t) \leqslant \frac{SR_n}{GB_n}\end{aligned} \tag{9}$$

and into the negative and positive saturation zones, $v_p(t)$ and $v_n(t)$ evolve as

$$\begin{aligned}
&\frac{dv_p(t)}{dt} = -SR_p - \frac{GB_p}{A_{DCp}}v_p(t) + R_p\frac{GB_p}{A_{DCp}}i_p(t),\\
&-\frac{SR_p}{GB_p} > A_w v_z(t) + V_x - v_w(t),\\
&\frac{dv_p(t)}{dt} = +SR_p - \frac{GB_p}{A_{DCp}}v_p(t) + R_p\frac{GB_p}{A_{DCp}}i_p(t),\\
&\frac{SR_p}{GB_p} < A_w v_z(t) + V_x - v_w(t)
\end{aligned} \tag{10}$$

$$\begin{aligned}
\frac{dv_n(t)}{dt} &= -SR_n - \frac{GB_n}{A_{DCn}}v_n(t) + R_n\frac{GB_n}{A_{DCn}}i_n(t),\\
&-\frac{SR_n}{GB_n} > A_w v_z(t) + V_x - v_w(t),\\
\frac{dv_n(t)}{dt} &= +SR_n - \frac{GB_n}{A_{DCn}}v_n(t) + R_n\frac{GB_n}{A_{DCn}}i_n(t),\\
&\frac{SR_n}{GB_n} < A_w v_z(t) + V_x - v_w(t)
\end{aligned} \tag{11}$$

Combining (8) with (10), the full nonlinear macromodel for $v_p(t)$ is got as

$$\frac{dv_p(t)}{dt} = p_n - \frac{GB_p}{A_{DCp}}v_p(t) + R_p\frac{GB_p}{A_{DCp}}i_p(t),$$

$$p_n = \begin{cases} +SR_p, & A_w v_z(t) + V_x - v_w(t) > +\frac{SR_p}{GB_p}\\ GB_p(A_w v_z(t) + V_x - v_w(t)), & -\frac{SR_p}{GB_p} \leqslant A_w v_z(t) + V_x - v_w(t) \leqslant +\frac{SR_p}{GB_p},\\ -SR_p, & A_w v_z(t) + V_x - v_w(t) < -\frac{SR_p}{GB_p} \end{cases}$$

$$i_w(t)R_w + V_x + V_{sn} \leqslant v_w(t) \leqslant i_w(t)R_w + V_x + V_{sp} \tag{12}$$

where $A_{DCp} = \frac{A_{ip}R_p}{R_w}$, $GB_p = \frac{A_{ip}}{R_w C_p}$, $I_{ps} = C_p SR_p$ and $v_p(t)$ is limited by the positive and negative saturation voltages given by $-V_{pn} \leqslant v_p(t) \leqslant V_{pp}$ and its difference is the DR_p^v. Similarly as before, the full nonlinear macromodel for $v_n(t)$ is obtained by merging (9) with (11) and given by

$$\frac{dv_n(t)}{dt} = p_n - \frac{GB_n}{A_{DCn}}v_n(t) + R_n\frac{GB_n}{A_{DCn}}i_n(t),$$

$$p_n = \begin{cases} +SR_n, & A_w v_z(t) + V_x - v_w(t) > +\frac{SR_n}{GB_n}\\ GB_n(A_w v_z(t) + V_x - v_w(t)), & -\frac{SR_n}{GB_n} \leqslant A_w v_z(t) + V_x - v_w(t) \leqslant +\frac{SR_n}{GB_n},\\ -SR_n, & A_w v_z(t) + V_x - v_w(t) < -\frac{SR_n}{GB_n} \end{cases}$$

$$i_w(t)R_w + V_x + V_{sn} \leqslant v_w(t) \leqslant i_w(t)R_w + V_x + V_{sp} \tag{13}$$

where $A_{DCn} = \frac{A_{in}R_n}{R_w}$, $GB_n = \frac{A_{in}}{R_w C_n}$, $I_{ns} = C_n SR_n$ and $v_n(t)$ is also limited by the positive and negative saturation voltages given by $-V_{nn} \leqslant v_n(t) \leqslant V_{np}$ and its difference is the DR_n^v. Note that (4), (7), (12) and (13) are taking into account performance parameters along with parasitic elements of CBTA and although they can be used to numerically analyze CBTA-based analog or digital circuits, the solution of the state-variables system of equations should be solved using customized software, which could becomes a tedious task for complex and large circuits. In this sense and for analysis flexibil-

Table 4
SPICE-type CBTA sub-circuit.

```
.subckt CBTA p n w z
*** p-terminal
.param Aip = 0.9932 Ips = 1 m kpp={0.5 m + Ips} knp={0.2 m + Ips} Vpp = 1.8 Vpn = 1.8
Rp p 0 39.43 k
Cp p 0 55p
Gp p 0 VALUE = {IF(0< = kpp*tanh(Aip/kpp*I(Vx)),
+IF(kpp*tanh(Aip/kpp*I(Vx))< = Ips,kpp*tanh(Aip/kpp*I(Vx)),Ips),
+IF(knp*tanh(Aip/knp*I(Vx))> = −Ips,knp*tanh(Aip/knp*I(Vx)),-Ips))}
Vpp Vpp 0 {Vpp}
Dp1 p Vpp DX
Vpn Vpn 0 {-Vpn}
Dp2 Vpn p DX
*** n-terminal
.param Ain=-1.007 Ins = 1 m knp = {0.3 m + Ins} knn = {0.6 m + Ins} Vnp = 1.8 Vnn = 1.8
Rn n 0 39.91 k
Cn n 0 53p
Gn n 0 VALUE={IF(0< = knp*tanh(Ain/knp*I(Vx)),
+IF(knp*tanh(Ain/knp*I(Vx))< = Ins,knp*tanh(Ain/knp*I(Vx)),Ins),
+IF(knn*tanh(Ain/knn*I(Vx))> = −Ins,knn*tanh(Ain/knn*I(Vx)),-Ins))}
Vnp Vnp 0 {Vnp}
Dn1 n Vnp DX
Vnn Vnn 0 {-Vnn}
Dn2 Vnn n DX
*** w-terminal
.param Aw = 0.9708 Vsp = 1.789 kp={0.5 + Vsp} Vsn = 1.831 kn={0.7 + Vsn}
Rw w a 197
Cw w 0 1p
Vx a b −2 m
Ew b 0 VALUE={IF(0< = kp*tanh(Aw/kp*V(z)),
+IF(kp*tanh(Aw/kp*V(z))< = Vsp,kp*tanh(Aw/kp*V(z)),Vsp),
+IF(kn*tanh(Aw/kn*V(z))> = −Vsn,kn*tanh(Aw/kn*V(z)),-Vsn))}
*** z-terminal
.param gm = 1.161 m Izs = 200u kz = {25u + Izs} Vzp = 0.9 Vzn = 1.05
Rz z 0 20.55 k
Cz z 0 1.5p
Gz z 0 VALUE={IF(0< = kz*tanh(gm/kz*V(p,n)),
+IF(kz*tanh(gm/kz*V(p,n))< = Izs,kz*tanh(gm/kz*V(p,n)),Izs),
+IF(kz*tanh(gm/kz*V(p,n))> = −Izs,kz*tanh(gm/kz*V(p,n)),-Izs))}
Vzp Vzp 0 {Vzp}
Dz1 z Vzp DX
Vzn Vzn 0 {-Vzn}
Dz2 Vzn z DX
.MODEL DX D(IS = 1E−15)
.ends
```

ity, the inclusion of the nonlinear macromodel of Fig. 5 into commercially available circuit analysis tools is very important, since different kind of analysis can easily be executed.

Table 4 shows the SPICE-type subcircuit of Fig. 5 and as a consequence, the nonlinear behavior of electronic circuits based on CBTA, such as oscillators, nonlinear resistors, multipliers, memristor emulators, square and triangular waveform generators, modulators and so on can be better forecasted. To validate the proposed nonlinear macromodel described in Table 4, HSPICE simulations were done and compared with numerical simulations obtained by the CMOS design under the same conditions. In this manner, the DC transconductance transfer function of *p*- and *n*-terminal to *z*-terminal is depicted in Fig. 2(a) (red line). From this figure, the CBTA linearly operates in the same range and error mentioned above. Outside the linear range, the proposed macromodel follow the behavior of the CMOS design and maintaining an error less than 1%. Fig. 2(b) (red line) illustrates the frequency response of the macromodel, obtaining the same bandwidth mentioned above. Similarly, the transfer functions of i_w (black line) vs. i_p (red line) and i_w (brown line) vs. i_n (gray line) are illustrated in Fig. 3(a). For this case, the CBTA linearly operates in the same range and error mentioned above. However, this error slightly increased to 3.42% for the nonlinear region and for both output currents. The frequency response for both output currents is shown in Fig. 3(b) and they are in good agreement with the numerical results obtained by the CMOS design. Finally, the transfer function of v_z vs. v_w under the same measurement conditions mentioned before is shown in Fig. 4(a) (red line). In the linear region, the linearity is similar to the CMOS design, whereas at the nonlinear zones, the proposed macromodel follow the behavior of the CMOS design and maintaining an error less than 2.85%. Fig. 4(b) (red line) shows the frequency response of the macromodel, obtaining a similar bandwidth with respect to the CMOS design. Note that into SPICE-type macromodel, the behavior of the four transactors was modeled with *tanh()* function. This trigonometric function was used in order to achieve a better modeling of the nonlinearities associated with the CMOS design, present at the boundary between the linear region and saturation zones. As a consequence, the macromodel described in Table 4 has slightly better accuracy compared with (4), (7), (12) and (13). Nevertheless, these equations are still very useful in order to gain insight on the behavior of any digital or analog electronic circuit.

4. Numerical results

To validate the derived macromodels, two topologies of SNFS based on CBTAs were designed. All simulations were executed on a 1.6 GHz Intel Core i5 processor with 4 GB RAM and a chaotic waveform experimentally generated and stored as text file was used as excitation signal [10,11]. It is worth mentioning that in the following numerical simulations and for analysis flexibility, only the SPICE-type macromodel together with the CMOS design were used. However, if the behavior models provided by (4), (7), (12) and (13) are used, then similar behaviors to those generated by the SPICE-type macromodel and CMOS design are obtained.

4.1. First topology

In this case, the CBTA was configured as transconductance amplifier plus voltage follower and the SFNS topology is shown in Fig. 6(a), where $R_{an} = 20\ \text{k}\Omega, R_{bn} = 1\ \text{k}\Omega$ for $n = 1,2,3$, $R_s = 10\Omega, \pm B_{pj} = \pm 1.5V$ is the j-th breakpoint with $j = 1$. Here, we assume that $v_s(x(t)) \approx 0$. Since Fig. 6(a) is built by stacked basic *n*-blocks, we will only analyze one of them. Substituting Fig. 5 in the *n*-block of Fig. 6(a), we get

$$\begin{aligned} &v_n(t) = \pm B_{pj}, \quad v_p(t) = x(t), \quad i_{zn}(t) = -\tfrac{v_{zn}(t)}{R_{bn}} \\ &i_{wn}(t) = -\tfrac{v_{wn}(x(t))}{R_{an}}, \quad \tfrac{di_{wn}(t)}{dt} = -\tfrac{1}{R_{an}}\tfrac{dv_{wn}(x(t))}{dt} \end{aligned} \tag{14}$$

and as a consequence (7) becomes

$$\tfrac{dv_{wn}(x(t))}{dt} = p_n - \tfrac{GB_w}{A_{DCw}} v_{wn}(x(t)) + \tfrac{GB_w R_{an}}{A_{DCw}(R_{an}+R_w)} V_x$$

$$p_n = \begin{cases} +\frac{R_{an}A_w SR_w}{R_{an}+R_w}, & x(t) - \pm B_{pj} > +\frac{R_{an}A_w SR_w}{(R_{an}+R_w)GB_w} \\ GB_w(x(t) - \pm B_{pj}), & -\frac{R_{an}A_w SR_w}{GB_w(R_{an}+R_w)} \leqslant x(t) - \pm B_{pj} \leqslant +\frac{R_{an}A_w SR_w}{GB_w(R_{an}+R_w)} \\ -\frac{R_{an}A_w SR_w}{R_{an}+R_w}, & x(t) - \pm B_{pj} < -\frac{R_{an}A_w SR_w}{(R_{an}+R_w)GB_w} \end{cases} \tag{15}$$

where $v_{wn}(x(t))$ is limited by $(-V_{sn} + V_x)\frac{R_{an}}{R_{an}+R_w} \leqslant v_{wn}(x(t)) \leqslant (V_{sp} + V_x)\frac{R_{an}}{R_{an}+R_w}$ and its difference is the DR_w^v. It is important to mention that for this particular case, $A_{DCw} = \frac{R_{an}R_{bn}R_z g_m A_w}{(R_{an}+R_w)(R_{bn}+R_z)}$ and $GB_w = \frac{R_{an}A_w g_m}{(R_{an}+R_w)C_z}$. From Fig. 6(a), the SNFS dynamic behavior is modeled by a set of *n*-differential equations and each $v_{wn}(x(t))$ must be computed numerically for finally obtain the total output current given by

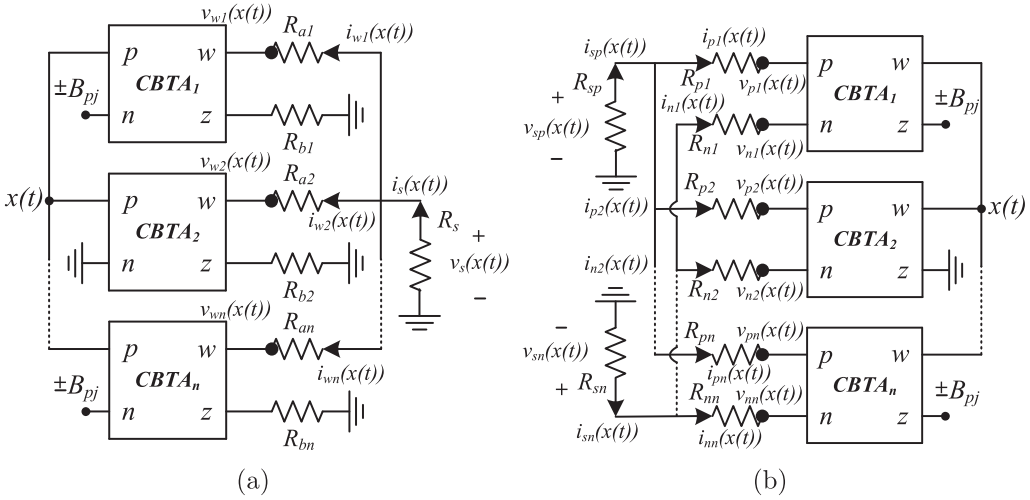

Fig. 6. SNFS based on CBTA configured in: (a) direct sense and (b) backward sense.

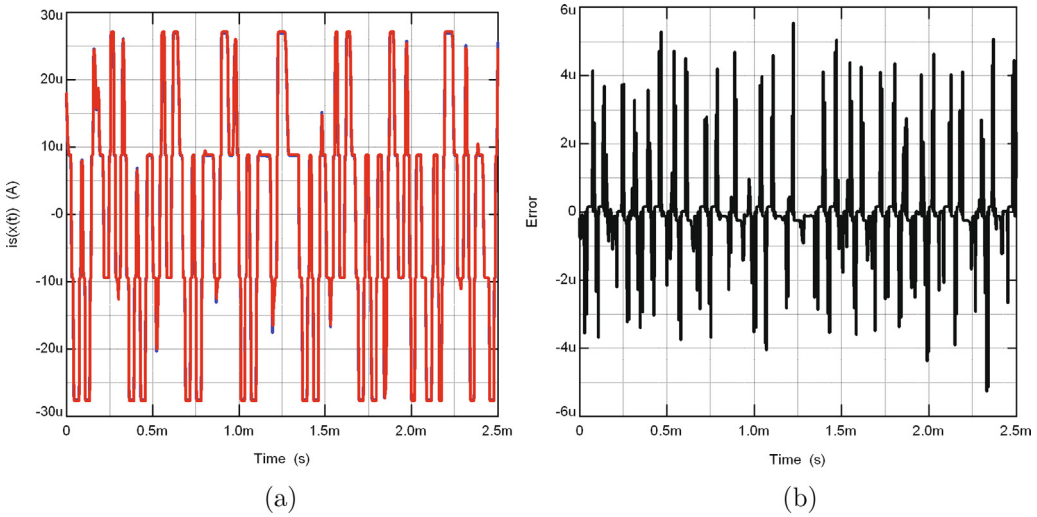

Fig. 7. (a) Time-domain comparisons among CMOS design (blue line) and SPICE-type macromodel (red line) of Fig. 6(a), (b) Error for each interval time. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

Table 5
CPU times and memory usage computations.

	CMOS design		SPICE subcircuit	
	Fig. 6(a)	Fig. 6(b)	Fig. 6(a)	Fig. 6(b)
CPU time (s)	30.75	58.65	12.42	17.87
Memory use (kB)	205.591	387.723	12.342	16.054

$$i_s(x(t)) \approx \frac{v_{w1}(x(t))}{R_{a1}} + \frac{v_{w2}(x(t))}{R_{a2}} + \ldots \frac{v_{wn}(x(t))}{R_{an}} \tag{16}$$

According to [10,11], a chaotic waveform $x(t)$ was applied to the SNFS designed at the transistor level of abstraction and to the proposed macromodel given in Table 4. Numerical simulations in the time-domain for $i_s(x(t))$ of both designs were computed, as illustrated in Fig. 7(a). To very the accuracy of the derived nonlinear macromodel, the error on each integration step was computed, as illustrated in Fig. 7(b). According to this figure, the error is into the $\pm 5\mu$A range. Table 5 gives the CPU time and memory consumption used during the numerical simulations and as a can observe, the differences are significant.

4.2. Second topology

For this case, the CBTA was configured in backward sense and the SFNS topology is shown in Fig. 6(b), where $R_{pn} = R_{nn} = 40$ kΩ, $R_{sp} = R_{sn} = 10\Omega$, the numeric value of the breakpoints are the same as was described above and for this topology, we have two output currents, $i_{sp}(x(t))$ and $i_{sn}(x(t))$. Similarly as above, by substituting Fig. 5 in the n-block we get

$$v_z(t) = \pm B_{pj}, \quad v_w(t) = x(t), \quad i_{pn,nn}(x(t)) = -\frac{v_{pn,nn}(x(t))}{R_{pn,nn}} \tag{17}$$

therefore (12) becomes

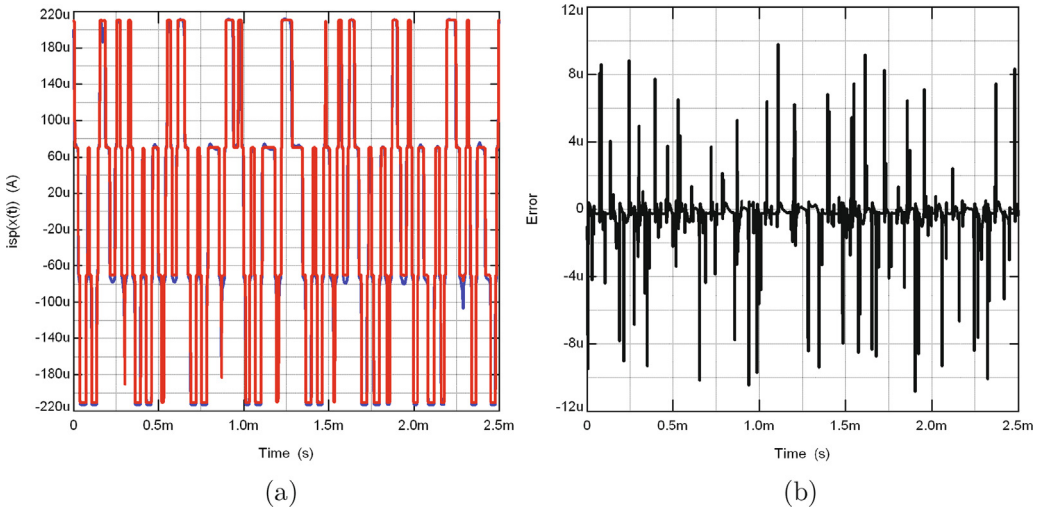

Fig. 8. (a) Time-domain comparisons among CMOS design (blue line) and SPICE-type macromodel (red line) of Fig. 6(b) and for $i_{sp}(x(t))$, (b) Error for each interval time. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

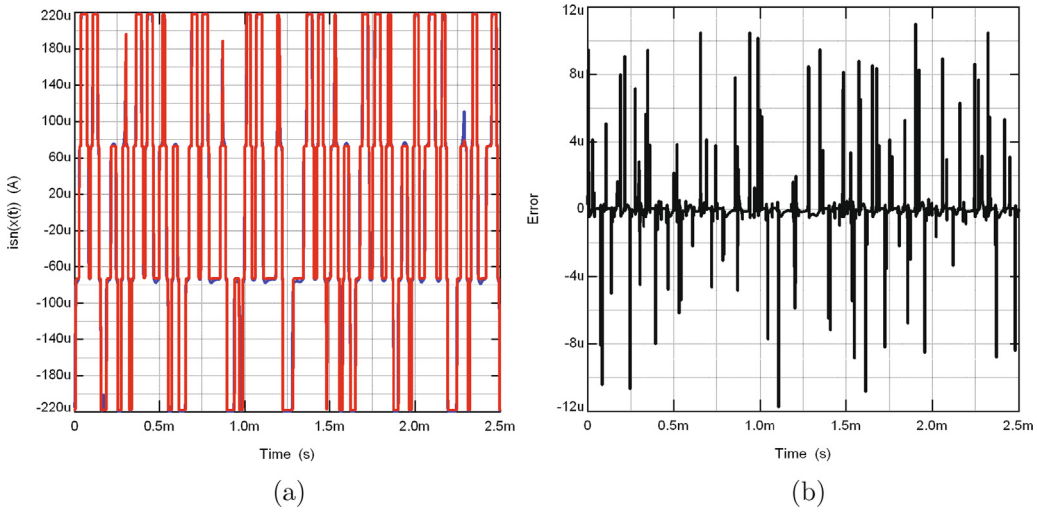

Fig. 9. (a) Time-domain comparisons among CMOS design (blue line) and SPICE-type macromodel (red line) of Fig. 6(b) and for $i_{sn}(x(t))$, (b) Error for each interval time. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

$$\frac{dv_{pn}(x(t))}{dt} = p_n - \frac{GB_p}{A_{DCp}} v_{pn}(x(t)),$$

$$p_n = \begin{cases} +SR_p, & \pm A_w B_{pj} + V_x - x(t) > +\frac{SR_p}{GB_p} \\ GB_p(\pm A_w B_{pj} + V_x - x(t)), & -\frac{SR_p}{GB_p} \leqslant \pm A_w B_{pj} + V_x - x(t) \leqslant +\frac{SR_p}{GB_p}, \\ -SR_p, & \pm A_w B_{pj} + V_x - x(t) < -\frac{SR_p}{GB_p} \end{cases}$$

$$i_w(t)R_w + V_x + V_{sn} \leqslant x(t) \leqslant i_w(t)R_w + V_x + V_{sp} \tag{18}$$

where $A_{DCp} = \frac{A_{ip}R_pR_{pn}}{R_w(R_p+R_{pn})}$. Furthermore, again using (17), (13) becomes

$$\frac{dv_{nn}(x(t))}{dt} = p_n - \frac{GB_n}{A_{DCn}} v_{nn}(x(t)),$$

$$p_n = \begin{cases} +SR_n, & \pm A_w B_{pj} + V_x - x(t) > +\frac{SR_n}{GB_n} \\ GB_n(\pm A_w B_{pj} + V_x - x(t)), & -\frac{SR_n}{GB_n} \leqslant \pm A_w B_{pj} + V_x - x(t) \leqslant +\frac{SR_n}{GB_n}, \\ -SR_n, & \pm A_w B_{pj} + V_x - x(t) < -\frac{SR_n}{GB_n} \end{cases}$$

$$i_w(t)R_w + V_x + V_{sn} \leqslant x(t) \leqslant i_w(t)R_w + V_x + V_{sp} \tag{19}$$

where $A_{DCn} = \frac{A_{in}R_nR_{nn}}{R_w(R_n+R_{nn})}$. The expression for both output currents are approximated as

$$i_{sp}(x(t)) \approx \frac{v_{p1}(x(t))}{R_{p1}} + \frac{v_{p2}(x(t))}{R_{p2}} + \ldots \frac{v_{pn}(x(t))}{R_{pn}} \tag{20}$$

and

$$i_{sn}(x(t)) \approx \frac{v_{n1}(x(t))}{R_{n1}} + \frac{v_{n2}(x(t))}{R_{n2}} + \ldots \frac{v_{wnn}(x(t))}{R_{nn}} \tag{21}$$

Similarly as in Section 4.1, a chaotic waveform was applied to both macromodels and for each topology. Numerical simulations in the time-domain for $i_{sp}(x(t))$ are illustrated in Fig. 8(a) and for $i_{sn}(x(t))$ are depicted in Fig. 9(a). As one can observe, both numerical results are in good agreement and the waveform of $i_{sn}(x(t))$ is the inverted version of $i_{sp}(x(t)$. Table 5 gives also the CPU-time and memory consumption. Moreover, the error for each topology was computed, as illustrated in Fig. 8(b) and Fig. 9(b), respectively. In both figures, the maximum error range is approximately ±10 μA. All in all, the use of accurate and simple models that considering performance parameters of CMOS CBTAs are very useful for improving the behavior of nonlinear functions, e.g., the SNFS based on CBTAs, saving CPU resources when complex and nonlinear circuits are designed and analyzed. We remark that to the best knowledge of the authors, all the behavioral models described above, the proposed SPICE-type nonlinear macromodel for this hybrid amplifier along with the topologies for the SNFS based on CBTAs have not been reported in the literature, until today.

5. Conclusions

A simple and accurate nonlinear macromodel for emulating the behavior of the CBTA at low-frequency has been deduced. The novelty of the derived macromodel is that parasitic elements, nonlinear terms along with the most influential performance parameters were taken into account. Numerical simulations on the performance of the SPICE-type macromodel were researched and compared with the CMOS design, showing an error less than 3.42% in all cases. Leveraging the nonlinear SPICE-type macromodel, the nonlinear behavior for two proposed topologies of SNFS with 4-plateaus based on CBTAs have also been researched, showing a maximum error of ±10 μA for both numerical simulations in the time-domain. The results show that the new macromodel can be used for forecasting the linear or nonlinear behavior of analog circuits based on CBTA, reducing the CPU time and memory consumption and without worsening the accuracy. All in all, the SPICE-type sub-circuit given in Table 4 is more useful for the reasons mentioned above.

Declaration of Competing Interest

None.

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Appendix A. Supplementary material

Supplementary data associated with this article can be found, in the online version, at https://doi.org/10.1016/j.aeue.2020.153286.

References

[1] Sánchez-López C, Fernández FV, Tlelo-Cuautle E, Tan SX-D. Pathological element-based active device models and their application to symbolic analysis. IEEE Trans Circ Syst I: Reg Papers 2011;58:1382–95. https://doi.org/10.1109/TCSI.2010.2097696.

[2] Sánchez-López C. Pathological equivalents of fully-differential active devices for symbolic nodal analysis. IEEE Trans Circ Syst I: Reg Papers 2013;60:603–15. https://doi.org/10.1109/TCSI.2013.2244271.

[3] Sánchez-López C, Ruiz-Pastor A, Ochoa-Montiel R, Carrasco-Aguilar MA. Symbolic nodal analysis of analog circuits with modern multiport functional blocks. Radioengineering 2013;22:518–25.

[4] Ayten UE, Sagbas M, Sedef H. Current mode leapfrog ladder filters using a new active block. AEU-Int J Electron Commun 2010;64:503–11. https://doi.org/10.1016/j.aeue.2009.03.012.

[5] Ayten UE, Sagbas M, Herencsar N, Koton J. Novel floating FDNR, inductor and capacitor simulator using CBTA. Proc Int Conf Telecom Signal Process 2011;1:312–6. https://doi.org/10.1109/TSP.2011.6043719.

[6] Ayten UE, Sagbas M, Herencsar N, Koton J. Novel floating general element simulators using CBTA. Radioengineering 2012;21:11–9.

[7] Ayten UE, Sagbas M, Sedef H. Electronically tunable sinusoidal oscillator circuit with current and voltage outputs. Int J Electron 2012;99:1133–44. https://doi.org/10.1080/00207217.2011.653951.

[8] Koksal M, Ayten UE, Sagbas M. Realization of new mutually coupled circuit using CC-CBTAs. Circ Syst Signal Process 2012;31:435–46. https://doi.org/10.1007/s00034-011-9322-9.

[9] Koksal M. Realization of a general all-pole current transfer function by using CBTA. Int J Circ Theory Appl 2013;41:319–29. https://doi.org/10.1002/cta.806.

[10] Ortega-Torres E, Ruíz-Hernández S, Sánchez-López C. A nonlinear macromodel for current feedback operational amplifier. Microelectron. J. 2015;46:941–9. https://doi.org/10.1016/j.mejo.2015.07.007.

[11] Sánchez-López C, Carrasco-Aguilar MA, Morales-López FE. A SPICE-compatible Nonlinear CCII Macromodel. J Circ Syst Comp 2017;26:1750144-1–44-8. https://doi.org/10.1142/S0218126617501444.

[12] Akbari M, Hashemipour O, Moaiyeri MH, Aghajani A. An efficient approach to enhance bulk-driven amplifiers. Analog Integr Circ Sig Process 2017;92:489–99. https://doi.org/10.1007/s10470-017-1010-7.

[13] Carbajal-Gómez VH, Sánchez-López C. Determining accurate Lyapunov exponents of a multiscroll chaotic attractor based on SNFS. Nonlinear Dyn 2019;98:2389–402. https://doi.org/10.1007/s11071-019-05288-9.