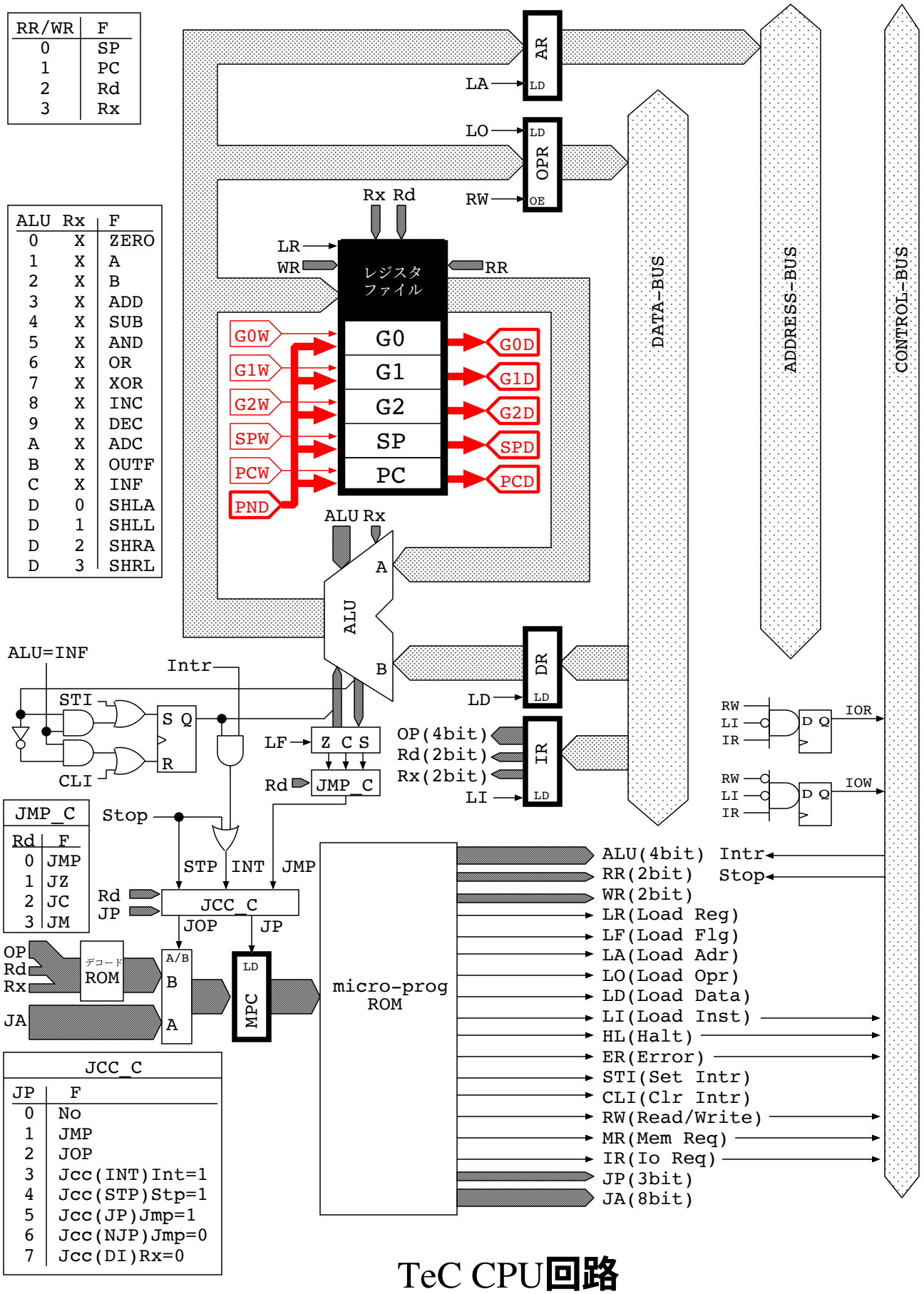
RR/WR | F
0 SP
1 PC
2 Rd
3 Rx
ALU Rx F
0 X ZERO
1 X A
2 X B
3 X ADD
4 X SUB
5 X AND
6 X OR
7 X XOR
8 X INC
9 X DEC
A X ADC
B X OUTF
C X INF
D 0 SHLA
D 1 SHLL
D 2 SHRA
D 3 SHRL
AR
LA
LD
LO
OPR
RW
OE
Rx Rd
LR
WR
RR
レジスタ
ファイル
G0
G1
G2
SP
PC
G0W
G1W
G2W
SPW
PCW
PND
G0D
G1D
G2D
SPD
PCD
DATA-BUS
ADDRESS-BUS
CONTROL-BUS
ALU Rx
ALU
A
B
DR
IR
LF
Z C S
Rd
JMP_C
OP(4bit)
Rd(2bit)
Rx(2bit)
LI
ALU=INF
Intr
STI
CLI
S Q
R
RW
LI
IR
D Q
IOR
IOW
JMP_C
Rd F
0 JMP
1 JZ
2 JC
3 JM
Stop
STP INT JMP
Rd
JP
JCC_C
JOP
JP
OP
Rd
Rx
デコード
ROM
A/B
B
A
JA
LD
MPC
micro-prog
ROM
ALU(4bit) Intr
RR(2bit) Stop
WR(2bit)
LR(Load Reg)
LF(Load Flg)
LA(Load Adr)
LO(Load Opr)
LD(Load Data)
LI(Load Inst)
HL(Halt)
ER(Error)
STI(Set Intr)
CLI(Clr Intr)
RW(Read/Write)
MR(Mem Req)
IR(Io Req)
JP(3bit)
JA(8bit)
JCC_C
JP F
0 No
1 JMP
2 JOP
3 Jcc(INT)Int=1
4 Jcc(STP)Stp=1
5 Jcc(JP)Jmp=1
6 Jcc(NJP)Jmp=0
7 Jcc(DI)Rx=0

TeC CPU回路