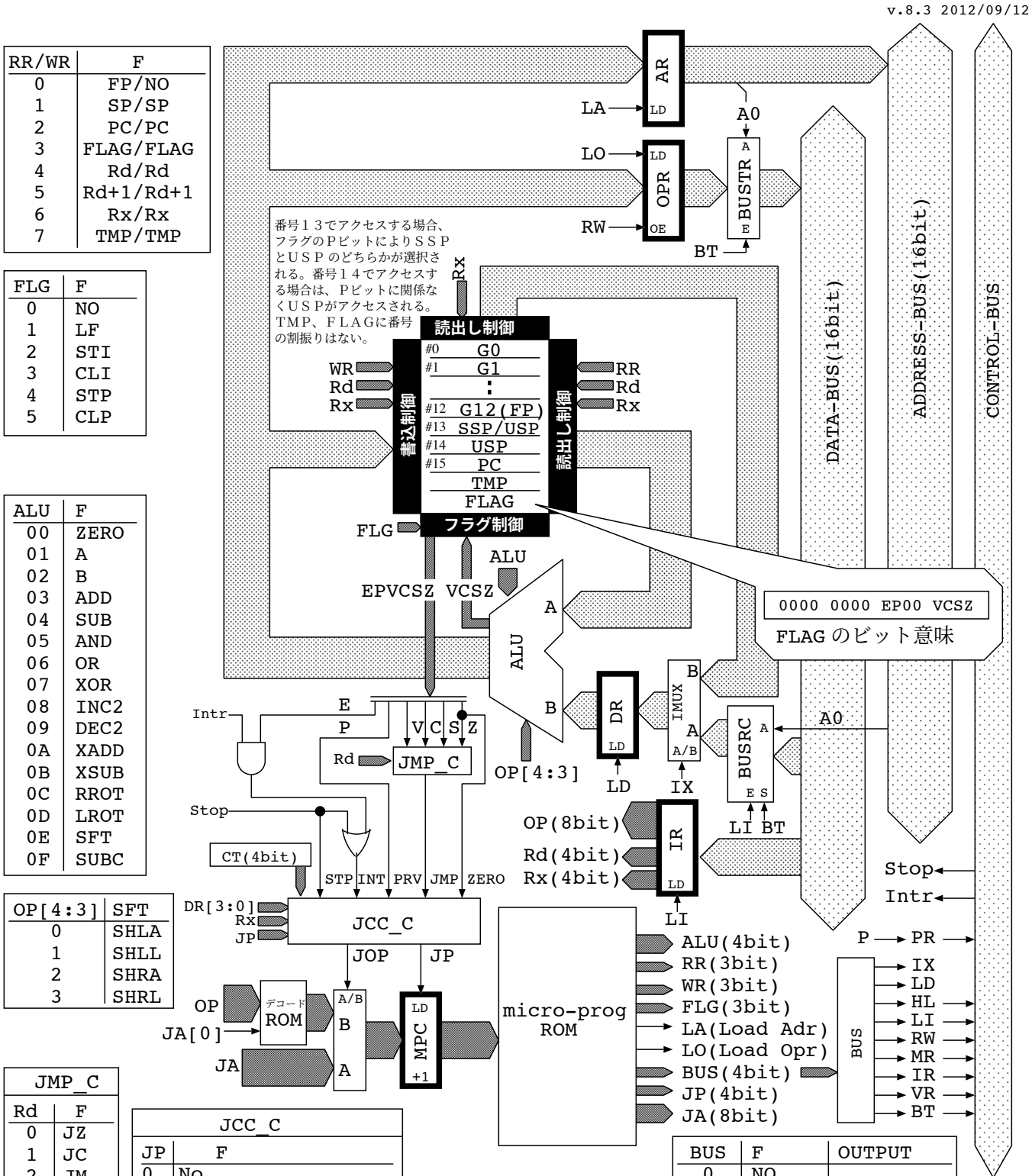

RR/WR	F
0	FP/NO
1	SP/SP
2	PC/PC
3	FLAG/FLAG
4	Rd/Rd
5	Rd+1/Rd+1
6	Rx/Rx
7	TMP/TMP

FLG	F
0	NO
1	LF
2	STI
3	CLI
4	STP
5	CLP

ALU	F
00	ZERO
01	A
02	B
03	ADD
04	SUB
05	AND
06	OR
07	XOR
08	INC2
09	DEC2
0A	XADD
0B	XSUB
0C	RROT
0D	LROT
0E	SFT
0F	SUBC

OP[4:3]	SFT
0	SHLA
1	SHLL
2	SHRA
3	SHRL

JMP_C	
Rd	F
0	JZ
1	JC
2	JM
3	JO
4	JGT
5	JGE
6	JLE
7	JLT
8	JNZ
9	JNC
A	JNM
B	JNO
C	JHI
D	
E	JLS
F	JMP

JCC_C	
JP	F
0	No
1	JMP
2	JOP
3	Jcc(INT) INT=1
4	Jcc(CTDR)CT++<>DR
5	Jcc(NJMP)JMP=0
6	Jcc(CT16)CT++<>FH
7	Jcc(STP) STP=1
8	Jcc(DI) Rx=0H
9	Jcc(SPR) Rx=DH
A	Jcc(PCR) Rx=EH
B	Jcc(IM) Rx=FH
C	Jcc(NPRV)PRV=0
D	Jcc(ZERO)ZERO=1

BUSTR	
	F
E&!A	SHLL 8bit

BUSRC	
	F
E	Signed Nibble
	To Word(16bit)
S	Select Byte

BUS	F	OUTPUT
0	NO	
1	MEMR	LD,MR
2	MEMW	RW,MR
3	IOR	LD,IR
4	IOW	RW,IR
5	FETCH	LI,LD,MR
6	VECT	LD,VR
7	IOF	LI,IR
8	LDRX	IX,LD
9	HALT	HL
A	MEMRB	LD,MR,BT
B	MEMWB	RW,MR,BT
C	IORB	LD,IR,BT
D	IOWB	RW,IR,BT

TaC CPU回路