Design and implement a 3–bit Up/Down Counter

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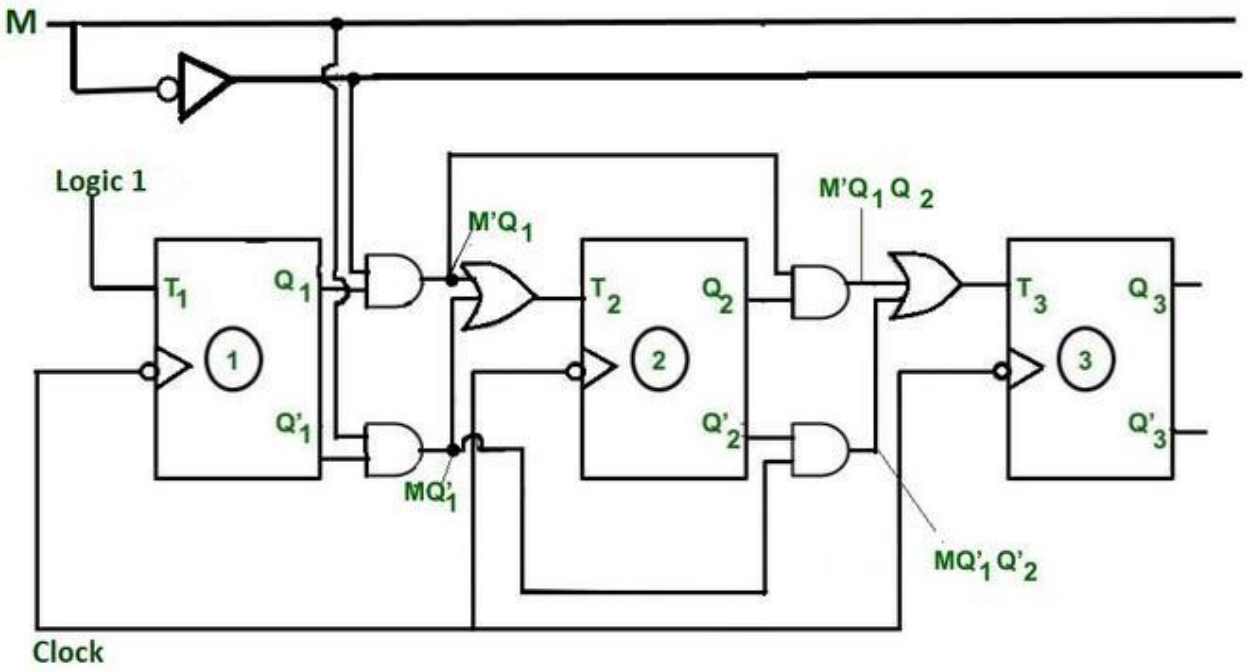
- Abstract

A 3-bit Up/Down Counter is a digital circuit designed to count in both ascending (up) and descending (down) directions based on a control signal. This counter utilizes three flip-flops to represent binary values from 0 to 7. When the control signal is set for counting up, the counter increments its value with each clock pulse, transitioning through the states in binary form. Conversely, when the control signal is activated for counting down, the counter decrements its value. The design includes asynchronous reset functionality, allowing the counter to be reset to a predetermined state (usually zero). The implementation of the Up/Down Counter is essential in various applications, including digital clocks, frequency dividers, and event counters, providing versatility in digital systems. The counter's behavior can be visualized using state diagrams and truth tables, making it a fundamental concept in digital electronics and computer architecture.

- Circuit diagram



- Truth table

M	Q3	Q2	Q1	Q3*	Q2*	Q1*
Up counter						
0	0	0	0	0	0	1
0	0	0	1	0	1	0
0	0	1	0	0	1	1
0	0	1	1	1	0	0
0	1	0	0	1	0	1
0	1	0	1	1	1	0
0	1	1	0	1	1	1
0	1	1	1	0	0	0
Down counter						
1	0	0	0	1	1	1
1	0	0	1	0	0	0
1	0	1	0	0	0	1
1	0	1	1	0	1	0
1	1	0	0	0	1	1
1	1	0	1	1	0	0
1	1	1	0	1	0	1
1	1	1	1	0	1	0