Date of Examination: 10.11.2021

AHSANULLAH UNIVERSITY OF SCIENCE AND TECHNOLOGY

Department: Computer Science and Engineering
Program: B.Sc. in Computer Science and Engineering
Semester Final Examination: Fall 2020
Year: 2nd Semester: 2nd
Course Number: CSE 2213
Course Name: Computer Architecture

Time: 02(Two) Hours **Full Marks: 50**

Use single answer script

Instructions:	i)	Answer script should be hand written and should be written in A4 white paper. You must submit the hard copy of this answer script to the Department when the university reopens.
	ii)	You must write the following information at the top page of each answer script: **Department:** **Program:** **Course no:** **Course Title:** **Examination:** **Semester (Session):** **Student ID:** **Signature and Date:**
	iii)	Write down Student ID, Course number and put your signature on top of every single page of the answer script.
	iv)	Write down page number at the bottom of every page of the answer script.
	v)	Upload the scan copy of your answer script in PDF format through provided **google form** at the respective course site (i.e., **google classroom)** using institutional email within the allocated time. Uploading clear and readable scan copy (uncorrupted) is your responsibility and must cover the full page of your answer script. However, for clear and readable scan copy of the answer script student should use only one side of a page for answering the questions.
	vi)	You must avoid **plagiarism,** maintain **academic integrity, and ethics**. You are not allowed to take any help from another individual and if taken so can result in stern disciplinary actions from the university authority.
	vii)	Marks allotted are indicated in the **right margin.**
	viii)	Necessary **charts/tables** are attached at the end of the question paper. You may use graph papers where necessary.
	ix)	Assume any reasonable data if needed.
	x)	Symbols and characters have their usual meaning.
	xi)	Before uploading rename the PDF file as **CourseNo_StudentID.pdf** For example, CE 451_180103001.pdf
	xii	The answer script **(one single pdf file)** must be uploaded at designated location in the provided **google form link** available in the google classroom.

There are 6 (Six) Questions. Answer any 4 (Four).

Question 1. [Marks: 12.5]		
a)	What do you understand by Multiprocessors and Multi-computer systems?	**[2]**
b)	Write necessary machine instructions to evaluate the following statement: A= (A+2)*B – C*(D+200) using one address instruction format.	**[4]**
c)	What are the different techniques to handle simultaneous interrupt requests? Explain each one of them.	**[6.5]**
Question 2. [Marks: 12.5]		
a)	What is double buffering?	**[2]**
b)	Design a sequential circuit for division of two integer numbers. Explain its various components and operations.	**[5]**
c)	Describe the distributed Bus arbitration procedure using an example.	**[5.5]**
Question 3. [Marks: 12.5]		
a)	What do you understand by "big-endian" and "little-endian" assignments of memory addresses?	**[2]**
b)	Briefly explain the three factors that affect the performance of a computer.	**[5]**
c)	Draw and briefly describe the internal organization of the memory chips with Memory Cells.	**[5.5]**
Question 4. [Marks: 12.5]		
a)	What is the role of the cache memory in pipelining?	**[2]**
b)	What is DMA? How does it work?	**[5]**
c)	Write down the micro-routine (including control sequences) for the fetch and execution stages of the following instruction, assuming single bus architecture of the processor data path: DIV (R1)+, R2	**[5.5]**
Question 5. [Marks: 12.5]		
a)	In a system with a single interrupt request line, how the CPU can identify which device has generated an interrupt?	**[2]**
b)	Write down the Control Sequences for **ADD (R1)+, -(R2), (R3)** for the Three bus CPU Data-Path Architecture.	**[5]**
c)	What is addressing mode? Explain each of the following addressing modes with examples: Base with index and offset, Relative, Auto increment.	**[5.5]**
Question 6. [Marks: 12.5]		
a)	Identify the differences between single-bus and three-bus architecture.	**[2]**
b)	Describe what happens when read and write miss occur?	**[4]**
c)	Describe the two different design paradigms for the CPU control unit.	**[6.5]**