LPC2478 EMC
External Memory Controller

Goal	Activity	Note
Understanding the LPC2478 static memory controler	Overview Definition Configuration Usage Example Exercise Summary	
Practice / Excercises:	*Exercise2*	
Teaching Material:	LPC2478 User Manual Ch. 5 LPC2478 Electrical datasheet	

Overview

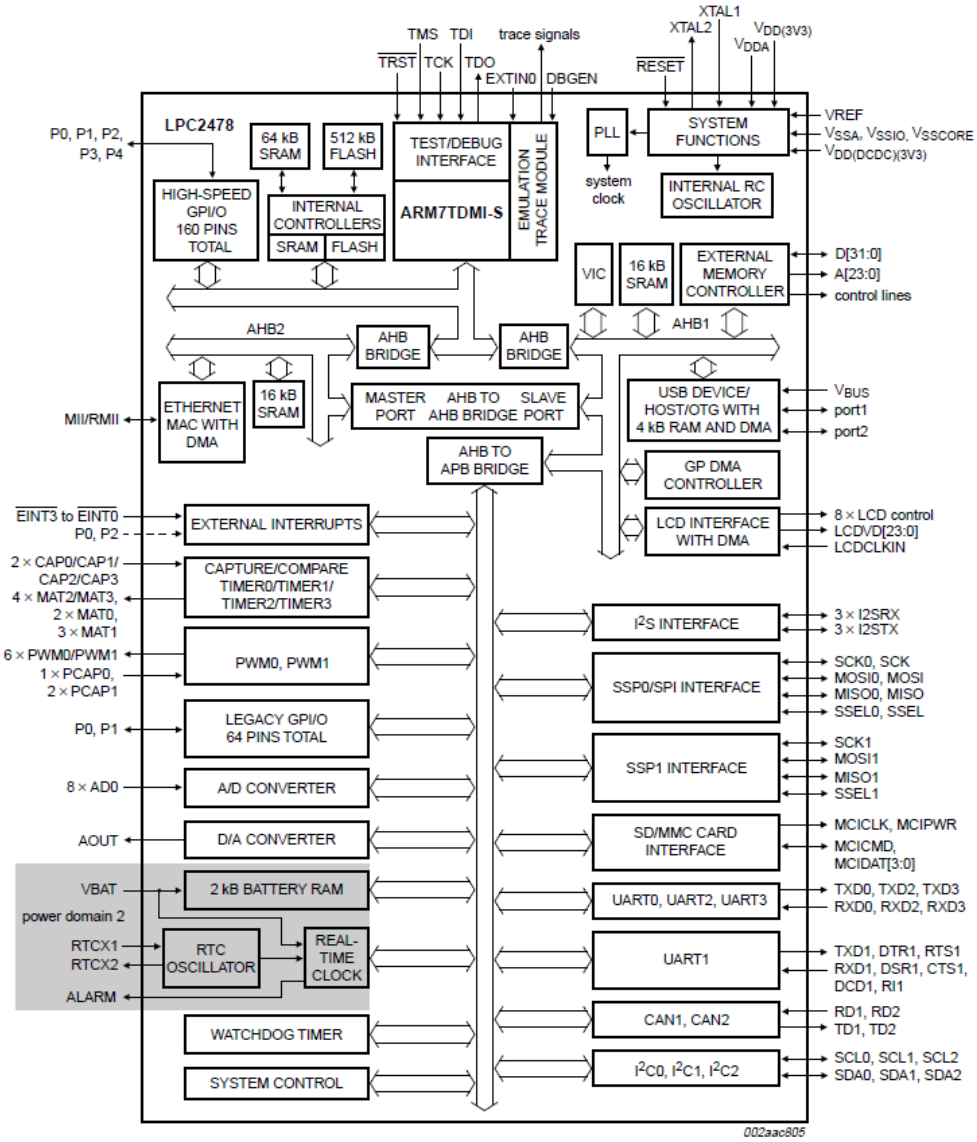
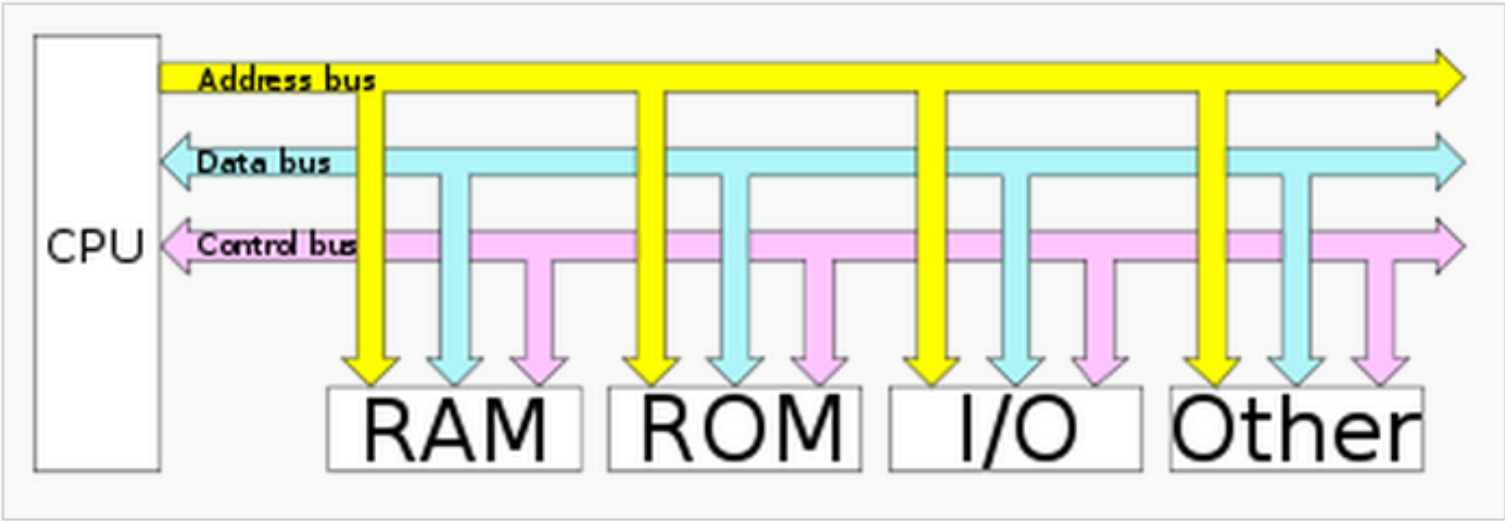


Fig 5. LPC2478 block diagram

What is a bus ?

Address/Data bus



EMC Block diagram

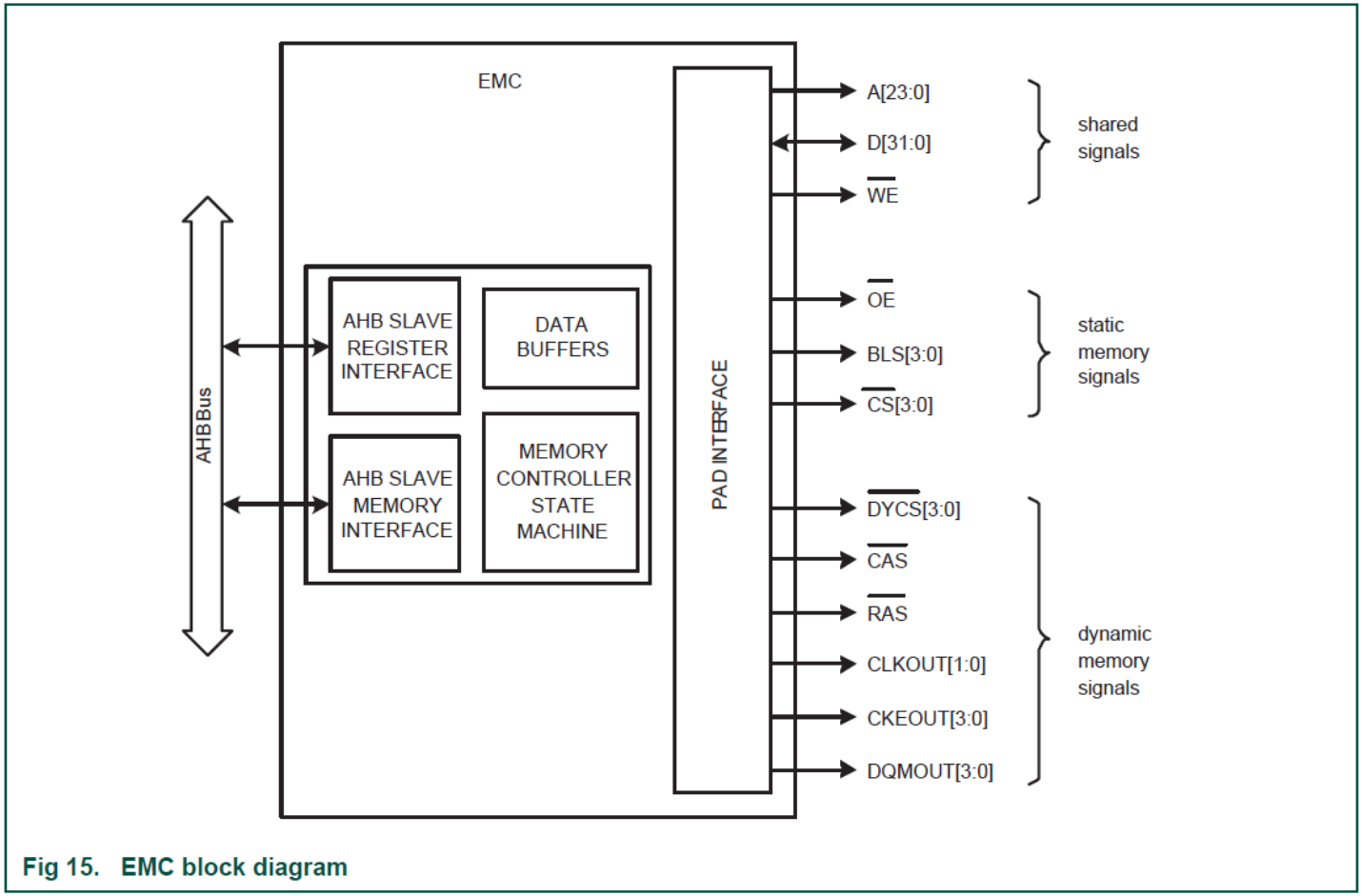


Fig 15. EMC block diagram

EMC Pins

Table 64. EMC configuration

	Data bus width/ memory transaction size	Pins	SDRAM configuration registers	Static memory configuration registers	External memory connection
LPC2458	8-bit, 16-bit	A[19:0] D[15:0] OE, WE BLS[1:0] CS[1:0] DYCS[1:0] CAS, RAS CLKOUT[1:0] CKEOUT[1:0] DQMOUT[1:0]	EMCDynamic Config1/0 EMCDynamic RasCas1/0	EMCStatic Config1/0 EMCStatic WaitWen1/0 EMCStatic WaitOen1/0 EMCStatic WaitRd1/0 EMCStatic WaitPage1/0 EMCStatic WaitWr1/0 EMCStatic WaitTurn1/0	Section 5–11.2, Section 5–11.3
LPC2420, LPC2460, LPC2468, LPC2470, LPC2478	8-bit, 16-bit, 32-bit	A[23:0] D[31:0] OE, WE BLS[3:0] CS[3:0] DYCS[3:0] CAS, RAS CLKOUT[1:0] CKEOUT[3:0] DQMOUT[3:0]	EMCDynamic Config3/2/1/0 EMCDynamic RasCas3/2/1/0	EMCStatic Config3/2/1/0 EMCStatic WaitWen3/2/1/0 EMCStatic WaitOen3/2/1/0 EMCStatic WaitRd3/2/1/0 EMCStatic WaitPage3/2/1/0 EMCStatic WaitWr3/2/1/0 EMCStatic WaitTurn3/2/1/0	Section 5–11.1, Section 5–11.2, Section 5–11.3

Static EMC

Dynamic EMC

Table 66. Pad interface and control signal descriptions

Name	Type	Value on POR reset	Value during self-refresh	Description
A[23:0]	Output	0x0000 0000	Depends on static memory accesses	External memory address output. Used for both static and SDRAM devices. SDRAM memories use only bits [14:0].
D[31:0]	Input/ Output	Data outputs = 0x0000 0000	Depends on static memory accesses	External memory data lines. These are inputs when data is read from external memory and outputs when data is written to external memory.
$\overline{OE}$	Output	1	Depends on static memory accesses	Low active output enable for static memory devices.
BLS[3:0]	Output	0xF	Depends on static memory accesses	Low active byte lane selects. Used for static memory devices.
$\overline{WE}$	Output	1	Depends on static memory accesses	Low active write enable. Used for SDRAM and static memories.
$\overline{CS}$[3:0]	Output	0xF	Depends on static memory accesses	Static memory chip selects. Default active LOW. Used for static memory devices.

- The EMC is an IP, by ARM ltd., see PL172 doc for details:

  http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0215e/index.html

Memory Bank Select

Eight independently-configurable memory chip selects are supported:

- Pins CSn3 to CSn0 are used to select static memory devices.
- Pins DYCSn3 to DYCSn0 are used to select dynamic memory devices.

Static memory chip select ranges are each 16 megabytes in size, while dynamic memory chip selects cover a range of 256 megabytes each. Table 5–65 shows the address ranges of the chip selects.

Table 65. Memory bank selection[1]

Chip select pin	Address range	Memory type	Size of range
$\overline{CS0}$	0x8000 0000 - 0x80FF FFFF	Static	16 MB
$\overline{CS1}$	0x8100 0000 - 0x81FF FFFF	Static	16 MB
$\overline{CS2}$	0x8200 0000 - 0x82FF FFFF	Static	16 MB
$\overline{CS3}$	0x8300 0000 - 0x83FF FFFF	Static	16 MB
$\overline{DYCS0}$	0xA000 0000 - 0xAFFF FFFF	Dynamic	256 MB
$\overline{DYCS1}$	0xB000 0000 - 0xBFFF FFFF	Dynamic	256 MB
$\overline{DYCS2}$	0xC000 0000 - 0xCFFF FFFF	Dynamic	256 MB
$\overline{DYCS3}$	0xD000 0000 - 0xDFFF FFFF	Dynamic	256 MB

Memory map

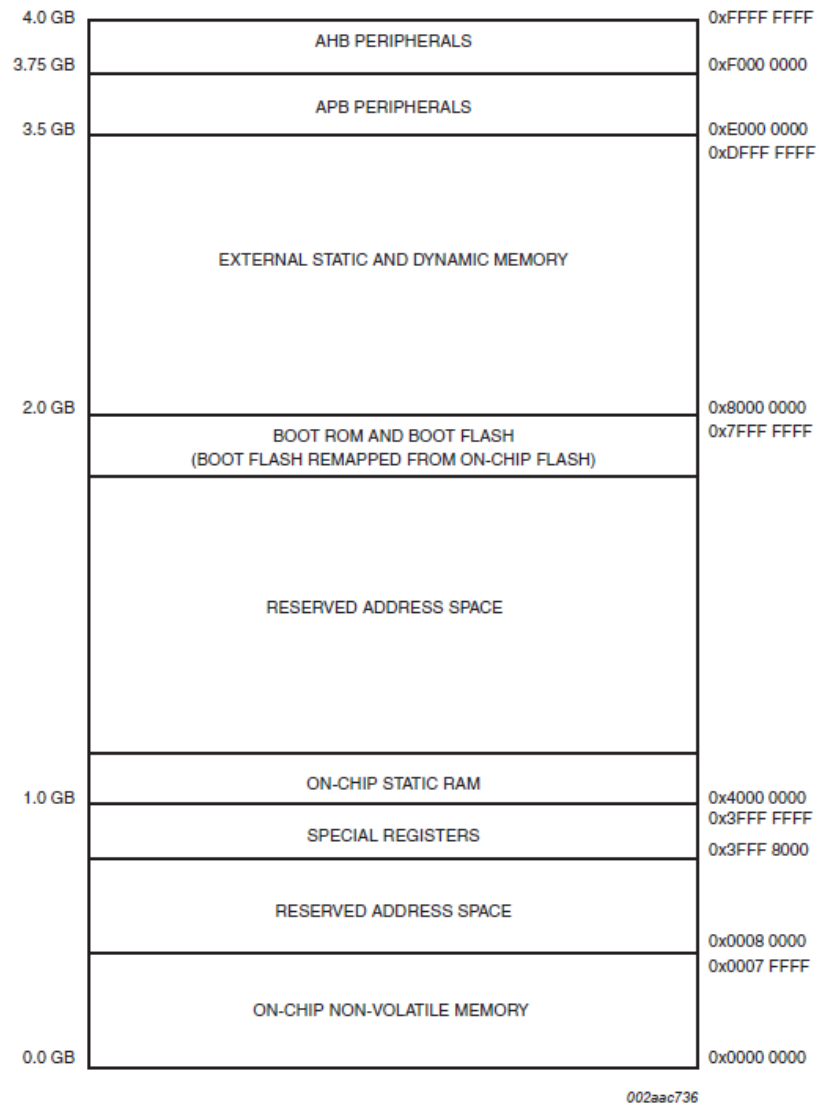


Fig 4. LPC2478 memory map

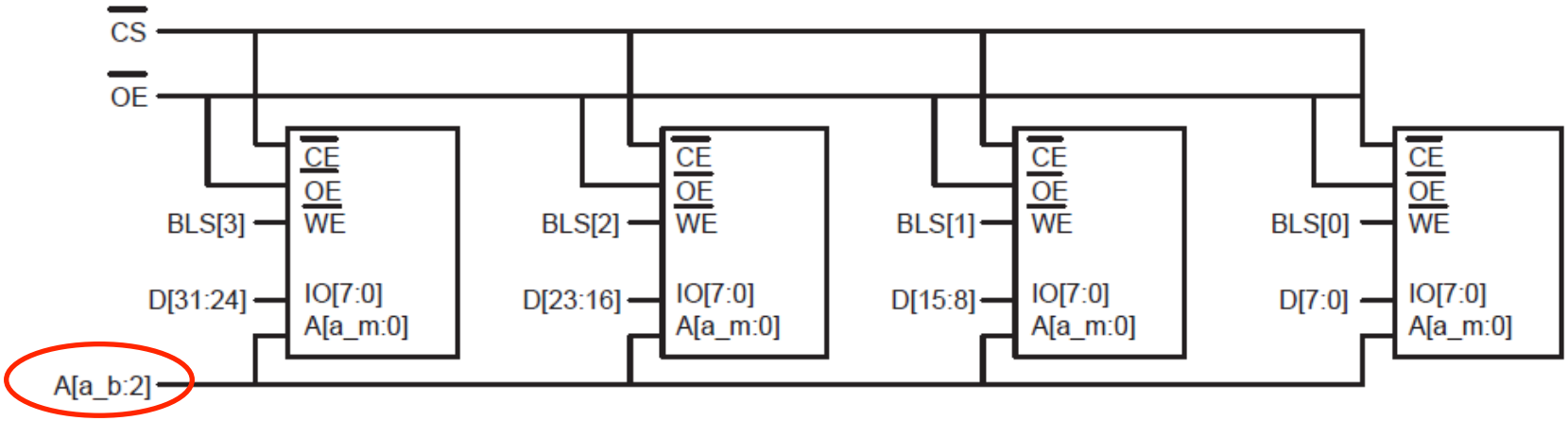
Example

```
#define FPGA_MODE_REG      (*(volatile short *)0x83000010)


/*set bits 0 & 3*/
FPGA_MODE_REG = 0x09;

/*Read register*/
Val = FPGA_MODE_REG;
```

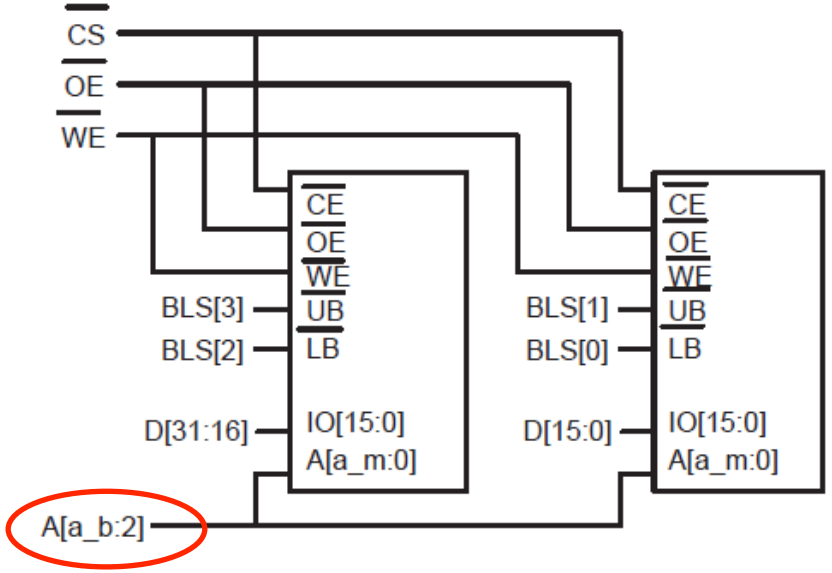
Interfacing off chip peripherals

External memory interfacing depends on the bank width (32, 16 or 8 bit selected via MW bits in corresponding EMCStaticConfig register).

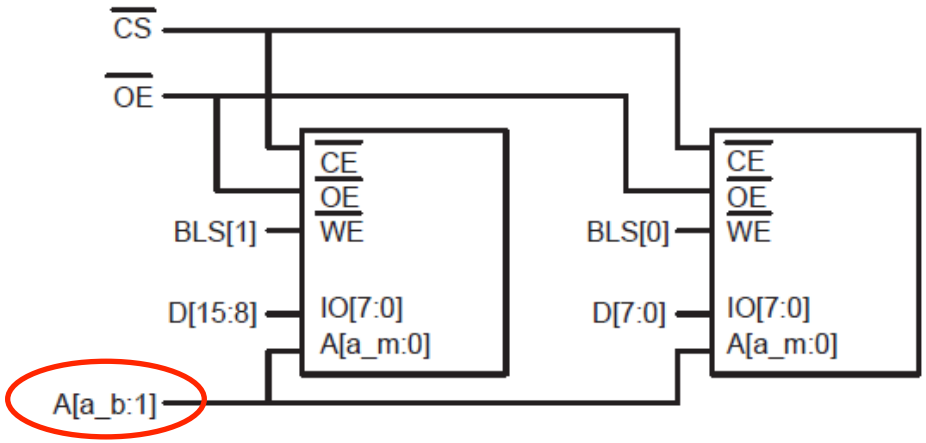
If a memory bank is configured to be 32 bits wide, address lines A0 and A1 can be used as non-address lines. If a memory bank is configured to 16 bits wide, A0 is not required. However, 8 bit wide memory banks do require all address lines down to A0. Configuring A1 and/or A0 line(s) to provide address or non-address function is accomplished using the Pin Function Select Register (see Section 9–3).



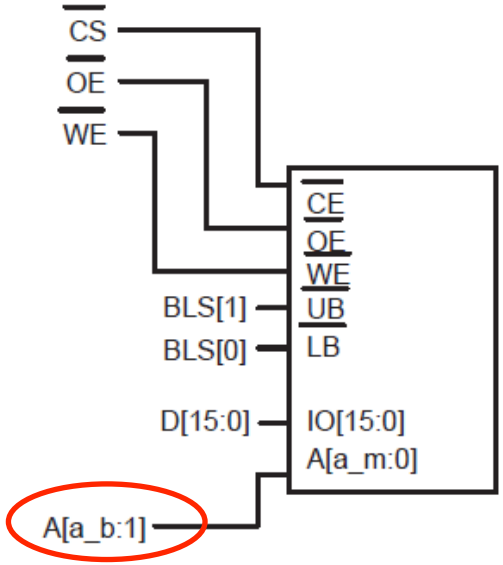
a. 32 bit wide memory bank interfaced to four 8 bit memory chips



b. 32 bit wide memory bank interfaced to two 16 bit memory chips



a. 16 bit wide memory bank interfaced to two 8 bit memory chips



b. 16 bit wide memory bank interfaced to a 16 bit memory chip

Fig 17. 16 bit bank external memory interfaces (bits MW = 01)

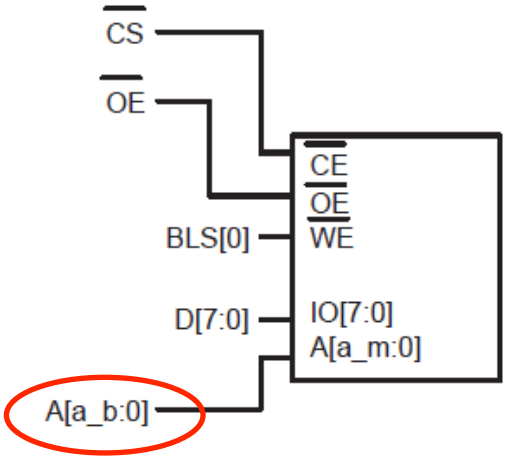
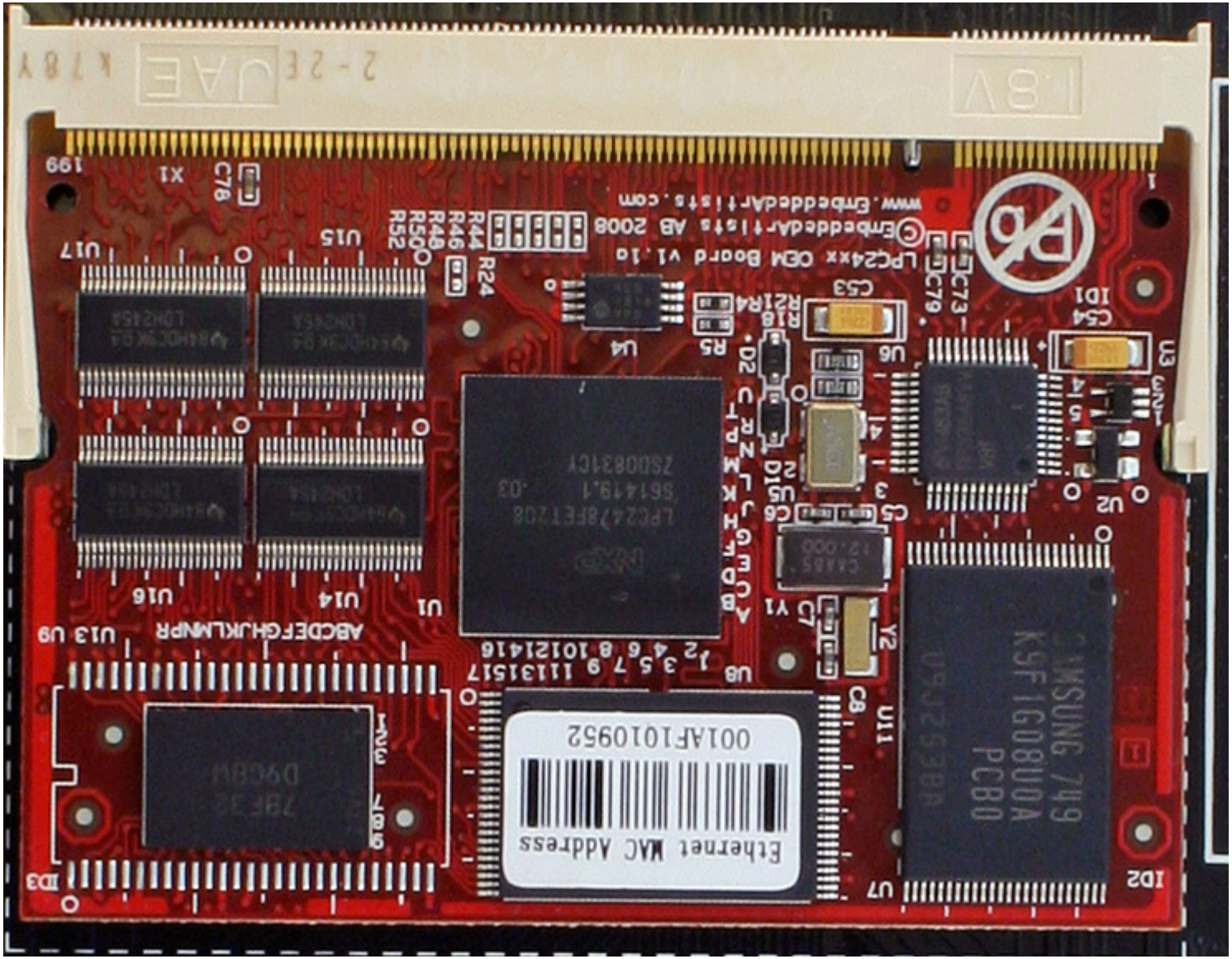


Fig 18. 8 bit bank external memory interface (bits MW = 00)

User manual

- Usermanual chapter 5
  ..\doc\user.manual.lpc24xx.pdf#page=68

Usage


LPC24xx OEM Board v1.1a
SAMSUNG 749
K9F1G08U0A
PCB0
Ethernet MAC Address
00IAF10109S2

- We only focus on using the STATIC memory controller !

Usage #1

The EMC is configured using the following registers:

1. Power: In the PCONP register (Table 4–63), set bit PCEMC.

   Remark: The EMC is enabled on reset (PCEMC = 1). On POR and warm reset, the EMC is enabled as well, see Table 5–68 and Table 5–71.

2. Clock: see Table 4–53.

3. Pins: Select data, address, and control pins and their modes in PINSEL6/8/9 and PINMODE6/8/9 (see Section 9–5).

4. Configuration: see Table 5–68 to Table 5–71.

Usage #2

- Setup memory bank acess:
  - memory width (8/16/32 bit)
  - read timing
  - write timing
  - byte acess

Registers, static EMC

0xFFE0 8200	EMCStatic Config0	Selects the memory configuration for static chip select 0.	-	0x0	R/W
0xFFE0 8204	EMCStatic WaitWen0	Selects the delay from chip select 0 to write enable.	-	0x0	R/W
0xFFE0 8208	EMCStatic WaitOen0	Selects the delay from chip select 0 or address change, whichever is later, to output enable.	-	0x0	R/W
0xFFE0 820C	EMCStatic WaitRd0	Selects the delay from chip select 0 to a read access.	-	0x1F	R/W
0xFFE0 8210	EMCStatic WaitPage0	Selects the delay for asynchronous page mode sequential accesses for chip select 0.	-	0x1F	R/W
0xFFE0 8214	EMCStatic WaitWr0	Selects the delay from chip select 0 to a write access.	-	0x1F	R/W
0xFFE0 8218	EMCStatic WaitTurn0	Selects the number of bus turnaround cycles for chip select 0.	-	0xF	R/W
0xFFE0 8220	EMCStatic Config1	Selects the memory configuration for static chip select 1.	-	0x0	R/W
0xFFE0 8224	EMCStatic WaitWen1	Selects the delay from chip select 1 to write enable.	-	0x0	R/W
0xFFE0 8228	EMCStatic WaitOen1	Selects the delay from chip select 1 or address change, whichever is later, to output enable.	-	0x0	R/W
0xFFE0 822C	EMCStatic WaitRd1	Selects the delay from chip select 1 to a read access.	-	0x1F	R/W
0xFFE0 8230	EMCStatic WaitPage1	Selects the delay for asynchronous page mode sequential accesses for chip select 1.	-	0x1F	R/W
0xFFE0 8234	EMCStatic WaitWr1	Selects the delay from chip select 1 to a write access.	-	0x1F	R/W
0xFFE0 8238	EMCStatic WaitTurn1	Selects the number of bus turnaround cycles for chip select 1.	-	0xF	R/W
0xFFE0 8240	EMCStatic Config2	Selects the memory configuration for static chip select 2.	-	0x0	R/W
0xFFE0 8244	EMCStatic WaitWen2	Selects the delay from chip select 2 to write enable.	-	0x0	R/W
0xFFE0 8248	EMCStatic WaitOen2	Selects the delay from chip select 2 or address change, whichever is later, to output enable.	-	0x0	R/W
0xFFE0 824C	EMCStatic WaitRd2	Selects the delay from chip select 2 to a read access.	-	0x1F	R/W
0xFFE0 8250	EMCStatic WaitPage2	Selects the delay for asynchronous page mode sequential accesses for chip select 2.	-	0x1F	R/W
0xFFE0 8254	EMCStatic WaitWr2	Selects the delay from chip select 2 to a write access.	-	0x1F	R/W
0xFFE0 8258	EMCStatic WaitTurn2	Selects the number of bus turnaround cycles for chip select 2.	-	0xF	R/W
0xFFE0 8260	EMCStatic Config3	Selects the memory configuration for static chip select 3.	-	0x0	R/W
0xFFE0 8264	EMCStatic WaitWen3	Selects the delay from chip select 3 to write enable.	-	0x0	R/W
0xFFE0 8268	EMCStatic WaitOen3	Selects the delay from chip select 3 or address change, whichever is later, to output enable.	-	0x0	R/W
0xFFE0 826C	EMCStatic WaitRd3	Selects the delay from chip select 3 to a read access.	-	0x1F	R/W
0xFFE0 8270	EMCStatic WaitPage3	Selects the delay for asynchronous page mode sequential accesses for chip select 3.	-	0x1F	R/W
0xFFE0 8274	EMCStatic WaitWr3	Selects the delay from chip select 3 to a write access.	-	0x1F	R/W
0xFFE0 8278	EMCStatic WaitTurn3	Selects the number of bus turnaround cycles for chip select 3.	-	0xF	R/W

Register layout

0xFFE0 8204	EMCStatic WaitWen0	Selects the delay from chip select 0 to write enable.	-	0x0	R/W
0xFFE0 8208	EMCStatic WaitOen0	Selects the delay from chip select 0 or address change, whichever is later, to output enable.	-	0x0	R/W
0xFFE0 820C	EMCStatic WaitRd0	Selects the delay from chip select 0 to a read access.	-	0x1F	R/W
0xFFE0 8210	EMCStatic WaitPage0	Selects the delay for asynchronous page mode sequential accesses for chip select 0.	-	0x1F	R/W
0xFFE0 8214	EMCStatic WaitWr0	Selects the delay from chip select 0 to a write access.	-	0x1F	R/W
0xFFE0 8218	EMCStatic WaitTurn0	Selects the number of bus turnaround cycles for chip select 0.	-	0xF	R/W

Common for all 4 banks

Timing, electrical datasheet

11.5 Static external memory interface

Table 14. Dynamic characteristics: Static external memory interface

C_L = 30 pF, T_{amb} = −40 °C to 85 °C, $V_{DD(DCDC)(3V3)}$ = $V_{DD(3V3)}$ = 3.0 V to 3.6 V, AHB clock = 1 MHz

Symbol	Parameter	Conditions	Min	Typ	Max
Common to read and write cycles[1]					
t_{CSLAV}	$\overline{CS}$ LOW to address valid time		−0.29	0.20	2.54
Read cycle parameters[1][2]					
t_{OELAV}	$\overline{OE}$ LOW to address valid time		−0.29	0.20	2.54
t_{CSLOEL}	$\overline{CS}$ LOW to $\overline{OE}$ LOW time		$-0.78 + T_{cy(CCLK)} \times$ WAITOEN	$0 + T_{cy(CCLK)} \times$ WAITOEN	$0.49 + T_{cy(CCLK)} \times$ WAITC
t_{am}	memory access time	[3][4]	(WAITRD − WAITOEN + 1) × $T_{cy(CCLK)}$ − 8.11	(WAITRD − WAITOEN + 1) × $T_{cy(CCLK)}$ − 9.57	(WAITRD − WAITOEN + $T_{cy(CCLK)}$ − 12.70
$t_{h(D)}$	data input hold time	[5]	0	-	-
t_{CSHOEH}	$\overline{CS}$ HIGH to $\overline{OE}$ HIGH time		−0.49	0	0.20
t_{OEHANV}	$\overline{OE}$ HIGH to address invalid time		−0.20	0.20	2.44
t_{OELOEH}	$\overline{OE}$ LOW to $\overline{OE}$ HIGH time		−0.59 + (WAITRD − WAITOEN + 1) × $T_{cy(CCLK)}$	0 + (WAITRD − WAITOEN + 1) × $T_{cy(CCLK)}$	0.10 + (WAITRD − WAITOEN + 1) × $T_{cy(CCL}$
t_{BLSLAV}	$\overline{BLS}$ LOW to address valid time		−0.39	0	2.54
$t_{CSHBLSH}$	$\overline{CS}$ HIGH to $\overline{BLS}$ HIGH time		−0.88	0.49	0.68
Write cycle parameters[1][6]					
t_{CSLWEL}	$\overline{CS}$ LOW to $\overline{WE}$ LOW time		$-0.88 + T_{cy(CCLK)} \times$ (1 + WAITWEN)	$0.10 + T_{cy(CCLK)} \times$ (1 + WAITWEN)	$0.20 + T_{cy(CCLK)} \times$ (1 + WAITWEN)
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time		−0.88	0.49	0.98
t_{WELDV}	$\overline{WE}$ LOW to data valid time		0.68	2.54	5.86
t_{CSLDV}	$\overline{CS}$ LOW to data valid time		0	2.64	4.79
t_{WELWEH}	$\overline{WE}$ LOW to $\overline{WE}$ HIGH time	[3]	$-0.78 + T_{cy(CCLK)} \times$ (WAITWR − WAITWEN + 1)	$0 + T_{cy(CCLK)} \times$ (WAITWR − WAITWEN + 1)	$0.10 + T_{cy(CCLK)} \times$ (WAITWR − WAITWEN -
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	[3]	$-0.88 + T_{cy(CCLK)} \times$ (WAITWR − WAITWEN + 3)	$0 + T_{cy(CCLK)} \times$ (WAITWR − WAITWEN + 3)	$0.59 + T_{cy(CCLK)} \times$ (WAITWR − WAITWEN -
t_{WEHANV}	$\overline{WE}$ HIGH to address invalid	[3]	0 + $T_{cy(CCLK)}$	0.20 + $T_{cy(CCLK)}$	2.74 + $T_{cy(CCLK)}$

Table 14. Dynamic characteristics: Static external memory interface *...continued*

C_L = 30 pF; T_{amb} = −40 °C to 85 °C, $V_{DD(DCDC)(3V3)}$ = $V_{DD(3V3)}$ = 3.0 V to 3.6 V, AHB clock = 1 MHz

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{WEHDNV}	$\overline{WE}$ HIGH to data invalid time		[3]	0.78	2.54	5.96	ns
$t_{BLSHANV}$	$\overline{BLS}$ HIGH to address invalid time		[3]	−0.29	0.20	2.54	ns
$t_{BLSHDNV}$	$\overline{BLS}$ HIGH to data invalid time		[3]	0	2.54	5.37	ns

[1] V_{OH} = 2.5 V, V_{OL} = 0.2 V.

[2] V_{IH} = 2.5 V, V_{IL} = 0.5 V.

[3] $T_{cy(CCLK)} = 1/CCLK$.

[4] Latest of address valid, $\overline{CS}$ LOW, $\overline{OE}$ LOW to data valid.

[5] Earliest of $\overline{CS}$ HIGH, $\overline{OE}$ HIGH, address change to data invalid.

[6] Byte lane state bit (PB) = 1.

Bus cycles R/W

Read

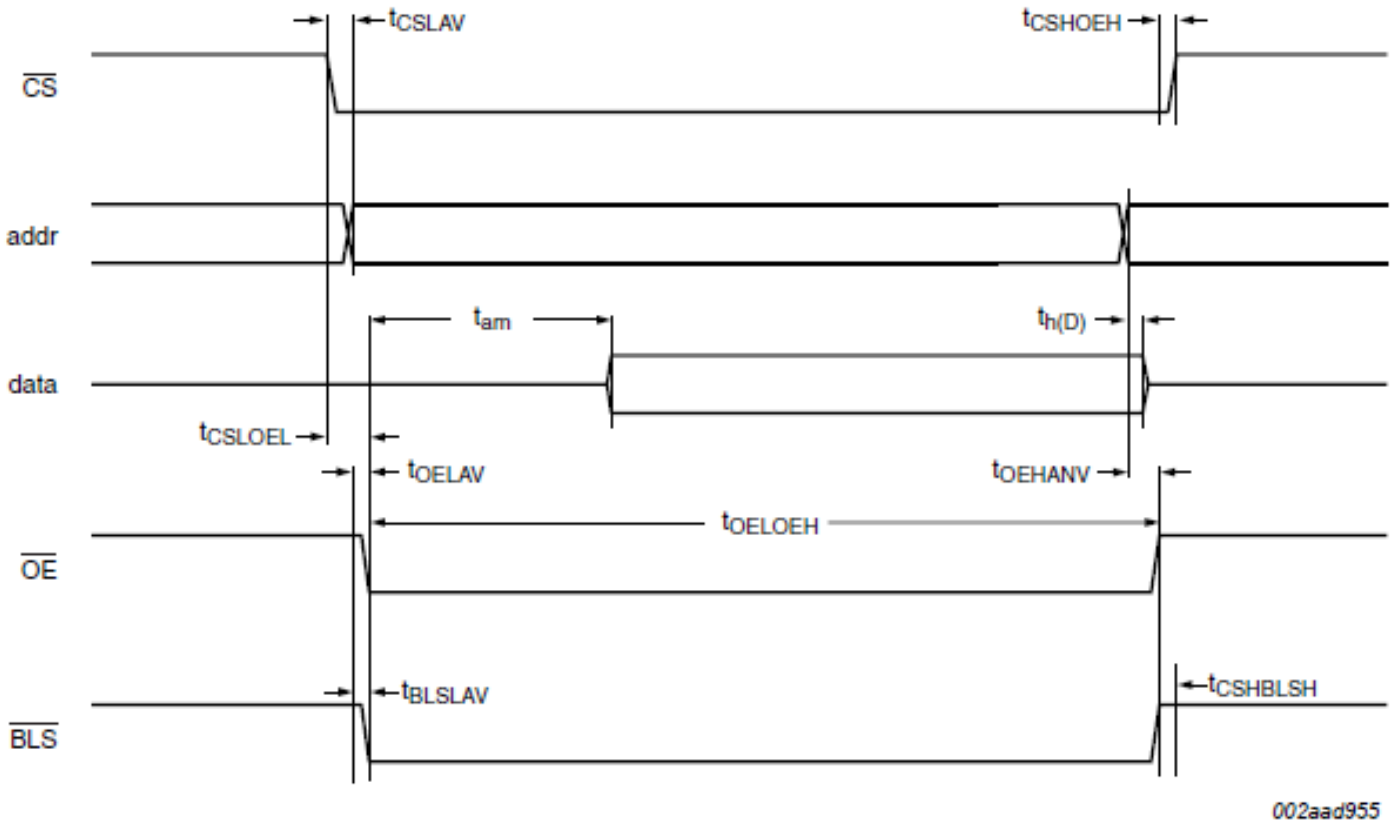


Fig 14. External memory read access

Read timing #1

t_{CSLOEL}	$\overline{CS}$ LOW to $\overline{OE}$ LOW time	$-0.78 + T_{cy(CCLK)} \times WAITOEN$	$0 + T_{cy(CCLK)} \times WAITOEN$	$0.49 + T_{cy(CCLK)} \times WAITOEN$	ns

10.23 Static Memory Output Enable Delay registers (EMCStaticWaitOen0-3 - 0xFFE0 8208, 228, 248, 268)

The EMCStaticWaitOen0-3 registers enable you to program the delay from the chip select or address change, whichever is later, to the output enable. It is recommended that these registers are modified during system initialization, or when there are no current or outstanding transactions. This can be ensured by waiting until the EMC is idle, and then entering low-power, or disabled mode. These registers are accessed with one wait state.

Table 5–91 shows the bit assignments for the EMCStaticWaitOen0-3 registers.

Table 91. Static Memory Output Enable delay registers (EMCStaticWaitOen03 - address 0xFFE0 8208, 0xFFE0 8228, 0xFFE0 8248, 0xFFE0 8268) bit description

Bit	Symbol	Value	Description	Reset Value
3:0	Wait output enable (WAITOEN)		Delay from chip select assertion to output enable.	0x0
		0x0	No delay (POR reset value).	
		0x1 - 0xF	n cycle delay. The delay is WAITOEN x tCCLK.	
31:4	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

Read timing #2

t_{OELOEH}	$\overline{OE}$ LOW to $\overline{OE}$ HIGH time	–0.59 + (WAITRD – WAITOEN + 1) × $T_{cy(CCLK)}$	0 + (WAITRD – WAITOEN + 1) × $T_{cy(CCLK)}$	0.10 + (WAITRD – WAITOEN + 1) × $T_{cy(CCLK)}$

10.24 Static Memory Read Delay registers (EMCStaticWaitRd0-3 - 0xFFE0 820C, 22C, 24C, 26C)

The EMCStaticWaitRd0-3 registers enable you to program the delay from the chip select to the read access. It is recommended that these registers are modified during system initialization, or when there are no current or outstanding transactions. This can be ensured by waiting until the EMC is idle, and then entering low-power, or disabled mode. It is not used if the extended wait bit is enabled in the EMCStaticConfig0-3 registers. These registers are accessed with one wait state.

Table 5–92 shows the bit assignments for the EMCStaticWaitRd0-3 registers.

Table 92. Static Memory Read Delay registers (EMCStaticWaitRd0-3 - address 0xFFE0 820C, 0xFFE0 822C, 0xFFE0 824C, 0xFFE0 826C) bit description

Bit	Symbol	Value	Description	Reset Value
4:0	Non-page mode read wait states or asynchronous page mode readfirst access wait state (WAITRD)		Non-page mode read or asynchronous page mode read, first read only:	0x1F
		0x0 - 0x1E	(n + 1) CCLK cycles for read accesses. For non-sequential reads, the wait state time is (WAITRD + 1) x tCCLK.	
		0x1F	32 CCLK cycles for read accesses (POR reset value).	
31:5	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

Read

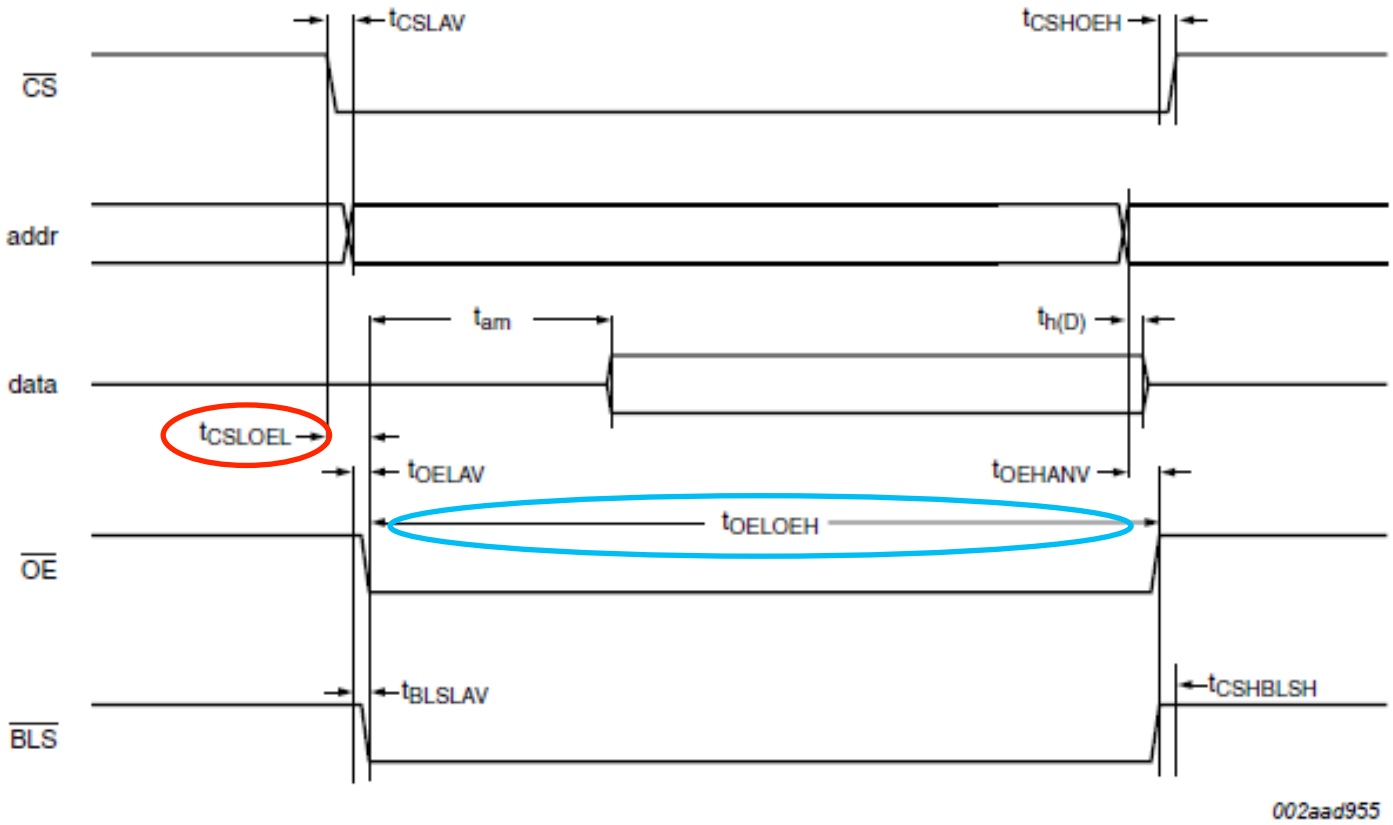


Fig 14. External memory read access

Write

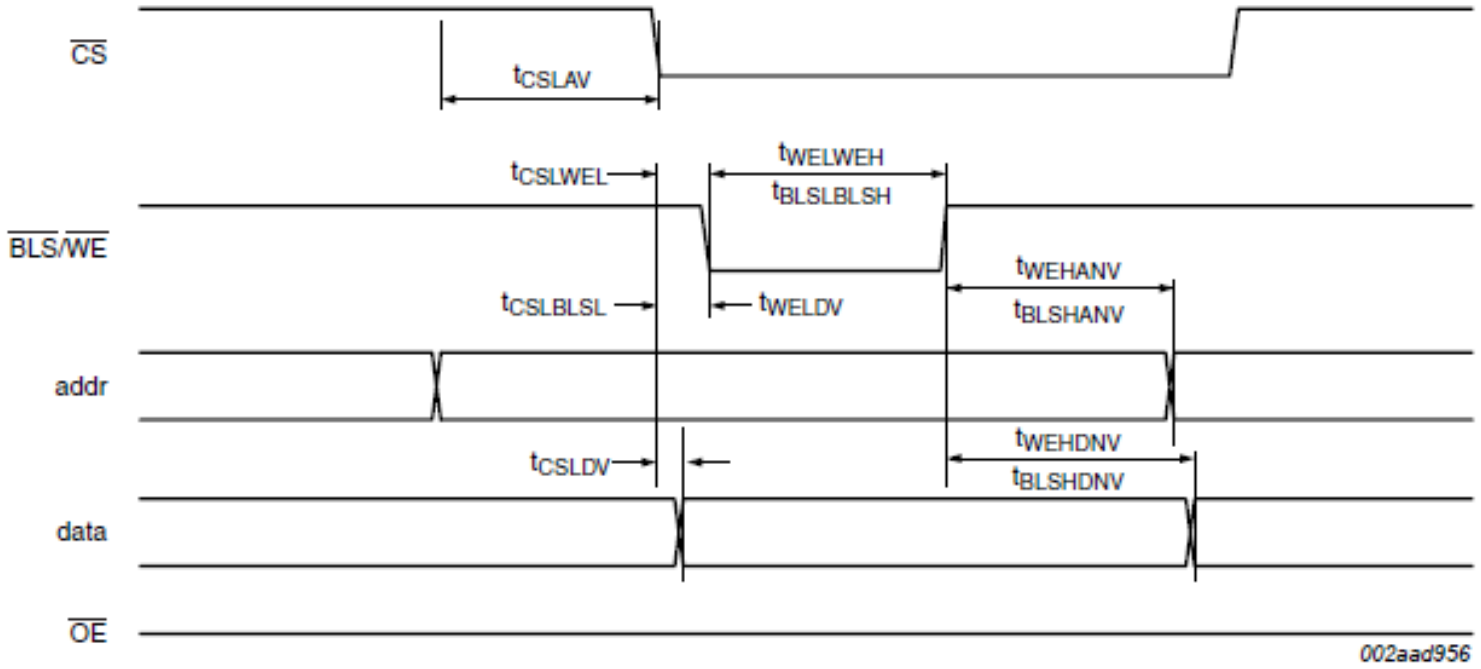


Fig 15. External memory write access

Write timing #1

t_{CSLWEL}	$\overline{CS}$ LOW to $\overline{WE}$ LOW time	$-0.88 + T_{cy(CCLK)} \times (1 +$ WAITWEN)	$0.10 + T_{cy(CCLK)} \times (1 +$ WAITWEN)	$0.20 + T_{cy(CCLK)} \times (1 +$ WAITWEN)	ns

10.22 Static Memory Write Enable Delay registers (EMCStaticWaitWen0-3 - 0xFFE0 8204, 224, 244 ,264)

The EMCStaticWaitWen0-3 registers enable you to program the delay from the chip select to the write enable. It is recommended that these registers are modified during system initialization, or when there are no current or outstanding transactions. This can be ensured by waiting until the EMC is idle, and then entering low-power, or disabled mode. These registers are accessed with one wait state.

Table 90. Static Memory Write Enable Delay registers (EMCStaticWaitWen0-3 - address 0xFFE0 8204,0xFFE0 8224, 0xFFE0 8244, 0xFFE0 8264) bit description

Bit	Symbol	Value	Description	Reset Value
3:0	Wait write enable (WAITWEN)		Delay from chip select assertion to write enable.	0x0
		0x0	One CCLK cycle delay between assertion of chip select and write enable (POR reset value).	
		0x1 - 0xF	(n + 1) CCLK cycle delay. The delay is (WAITWEN +1) x tCCLK.	
31:4	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

Write timing #2

t_{WELWEH}	$\overline{WE}$ LOW to $\overline{WE}$ HIGH time	[3]	$-0.78 + T_{cy(CCLK)} \times (WAITWR - WAITWEN + 1)$	$0 + T_{cy(CCLK)} \times (WAITWR - WAITWEN + 1)$	$0.10 + T_{cy(CCLK)} \times (WAITWR - WAITWEN + 1)$	ns

10.26 Static Memory Write Delay registers (EMCStaticWaitwr0-3 - 0xFFE0 8214, 234, 254, 274)

The EMCStaticWaitWr0-3 registers enable you to program the delay from the chip select to the write access. It is recommended that these registers are modified during system initialization, or when there are no current or outstanding transactions. This can be ensured by waiting until the EMC is idle, and then entering low-power, or disabled mode.These registers are not used if the extended wait (EW) bit is enabled in the EMCStaticConfig register. These registers are accessed with one wait state.

Table 5–94 shows the bit assignments for the EMCStaticWaitWr0-3 registers.

Table 94. Static Memory Write Delay registers0-3 (EMCStaticWaitWr - address 0xFFE0 8214, 0xFFE0 8234, 0xFFE0 8254, 0xFFE0 8274) bit description

Bit	Symbol	Value	Description	Reset Value
4:0	Write wait states (WAITWR)		SRAM wait state time for write accesses after the first read:	0x1F
		0x0 - 0x1E	(n + 2) CCLK cycle write access time. The wait state time for write accesses after the first read is WAITWR (n + 2) x tCCLK.	
		0x1F	33 CCLK cycle write access time (POR reset value).	
31:5	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

Write

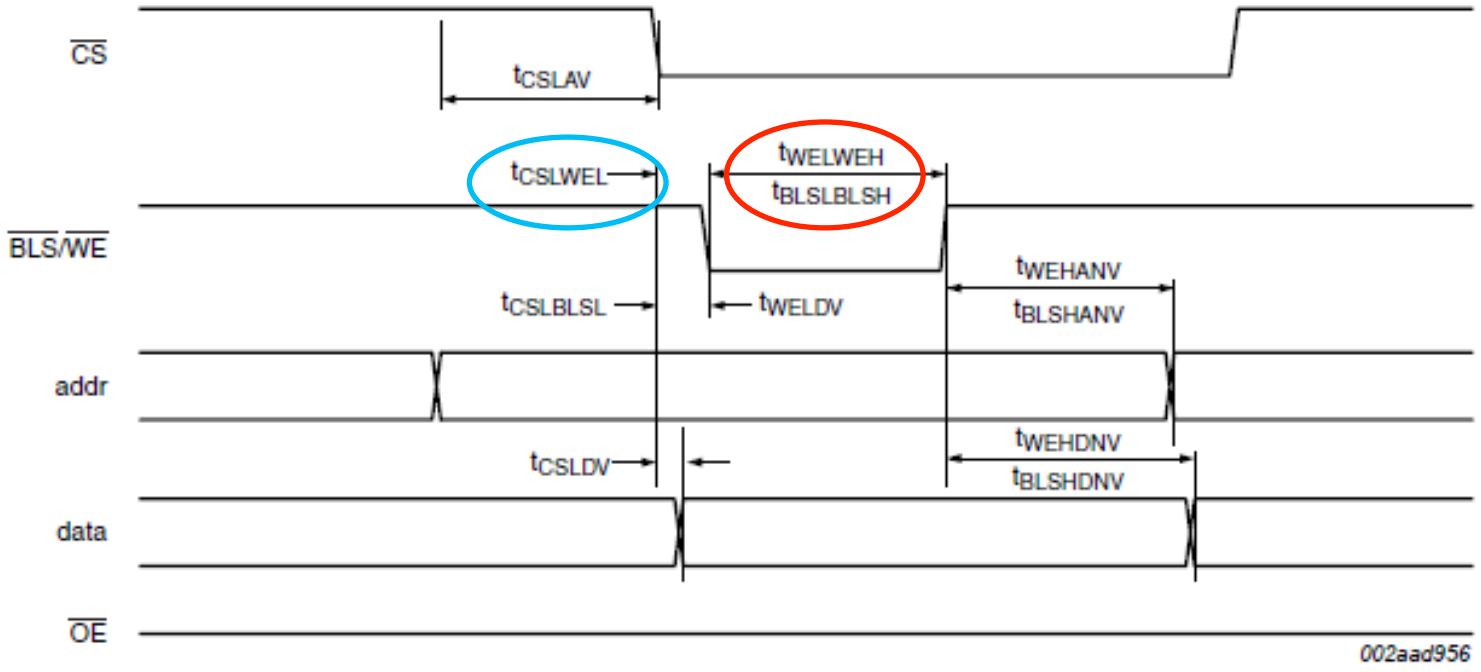


Fig 15. External memory write access

Quiz :

My Board runs 57.6MHz:

- The joystick has 4 positions, each position initializes the EMC on CS2 with different values.
- Find the values for **EMCStaticWaitOen2 and EMCStaticWaitRd2** in position UP and RIGHT
- Find the values for **EMCStaticWaitOen2 and EMCStaticWaitWr2** in position DOWN and LEFT

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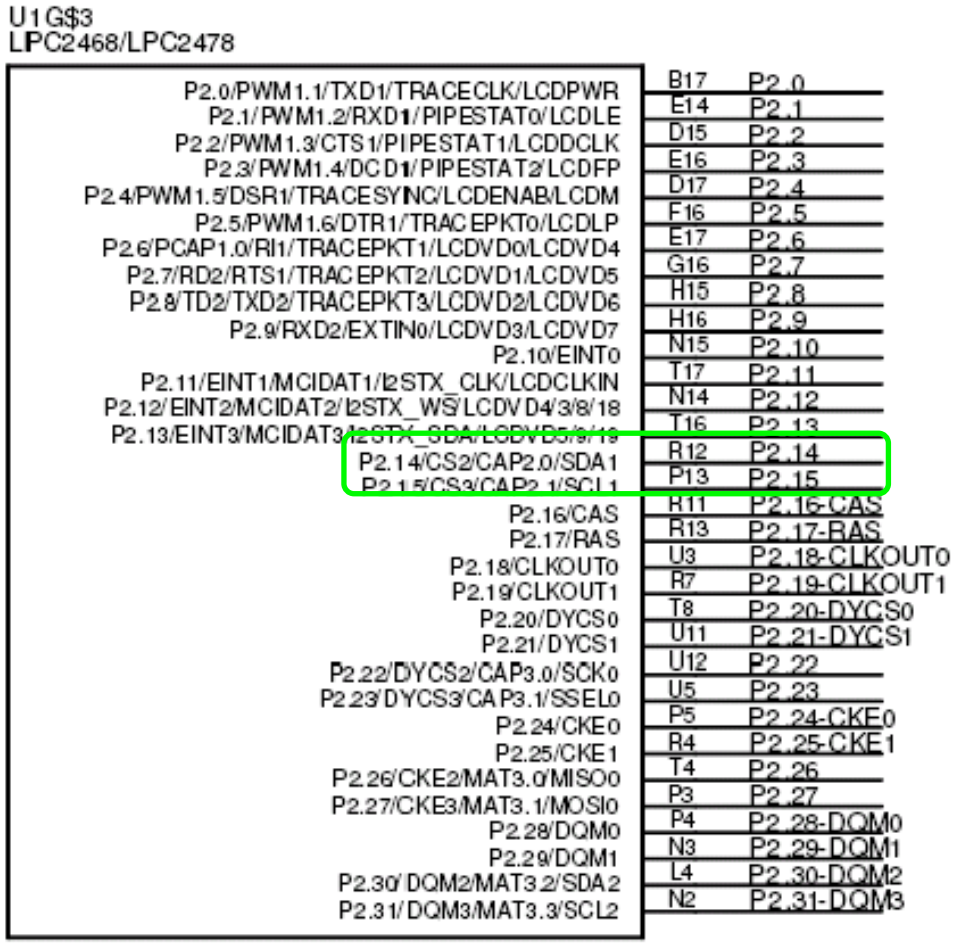
2.2 Memory Layout

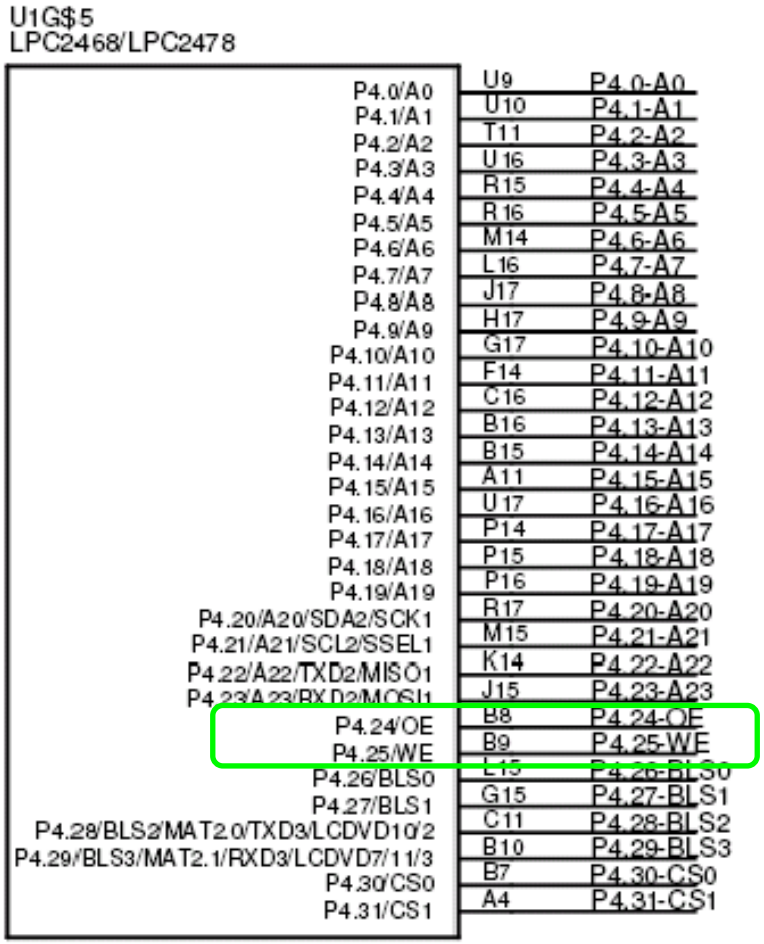
The external memory controller on the LPC2478 defines eight memory regions, named: CS0, CS1, CS2, CS3, DYCS0, DYCS1, DYCS2, and DYCS3. Of these eight, three memory areas are used by the *LPC2478 OEM Board*. These are:

- CS0 (address range: 0x8000 0000 – 0x80FF FFFF)
  An external NOR FLASH (32 MBit = 4 MByte in size) is addressed.
- CS1 (address range: 0x8100 0000 – 0x81FF FFFF)
  An external NAND FLASH (1 GBit = 128 MByte in size) is addressed.
- DYCS0 (address range: 0xA000 0000 – 0xAFFF FFFF)
  An external SDRAM (256 MBit = 32 MByte in size) is addressed.

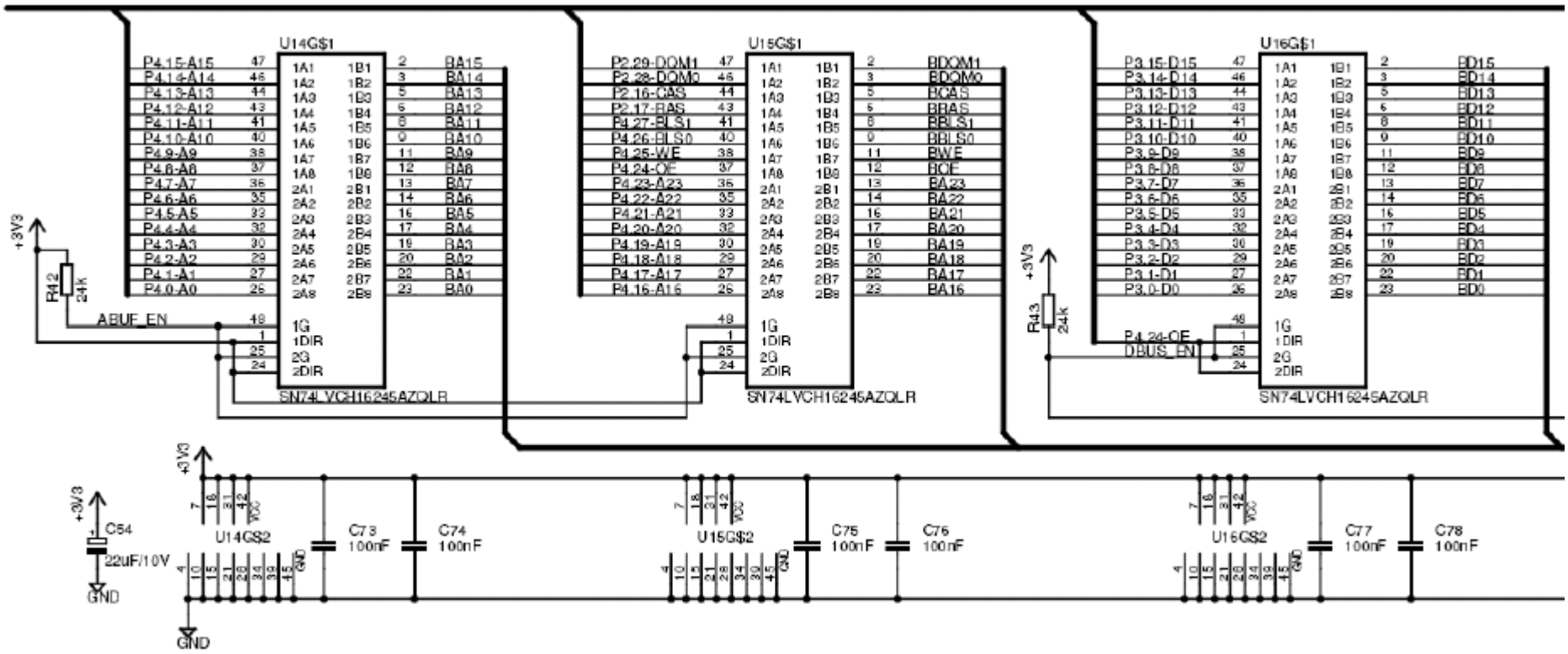
These three memory regions cannot be used by external devices. CS2 and DYCS1 are however free for external use via the buffered memory interface. Both address and data busses are buffered.

LPC2478 Board

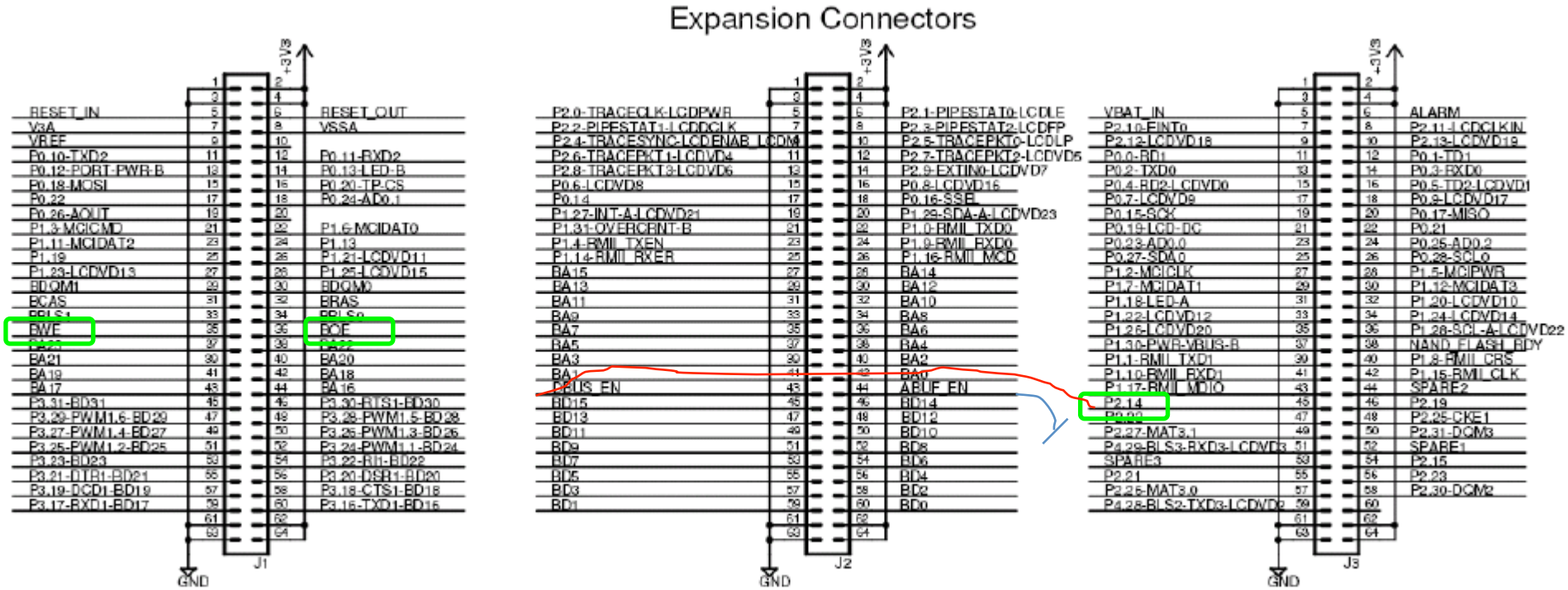




Address/data buffers



Extension connectors



Interfacing outside the PCB

2.1.6 External Memory Interface

The LPC2478 memory interface is available on the expansion connector. The data bus width is either 16- or 32-bits on the external interface (depending on board version). All signals are buffered. The buffers are disabled unless enabled by external signals.

By pulling signal ABUF_EN low, the two buffers for address and control signals are enabled and act as outputs (from the *LPC2478 OEM Board*).

The data bus buffer is controlled by the signal DBUS_EN. By pulling this signal low, the data bus buffer is enabled. The LPC2478 signal OE controls the direction of the data bus buffer. During read operations the buffer acts as an input and during write operations it acts as an output.

Note that DBUS_EN must not be pulled low constantly. In that case the buffer will collide with the board's internal data bus. DBUS_EN must only be pulled low when an external memory/IO device is accessed. If, for example, CS2 is used to decode and access an external device, connect the signal CS2 directly to DBUS_EN.

If more than one chip select signal is used, (logically) AND all chip select signal together before driving the DBUS_EN signal.

If the external memory interface is not used, leave ABUS_EN and DBUS_EN unconnected.

Find out more :

LPC2478 User manual

LPC2478 electrical datasheet:

http://www.nxp.com/documents/data_sheet/LPC2478.pdf

Arm prime cell memory controller

http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0215e/index.html