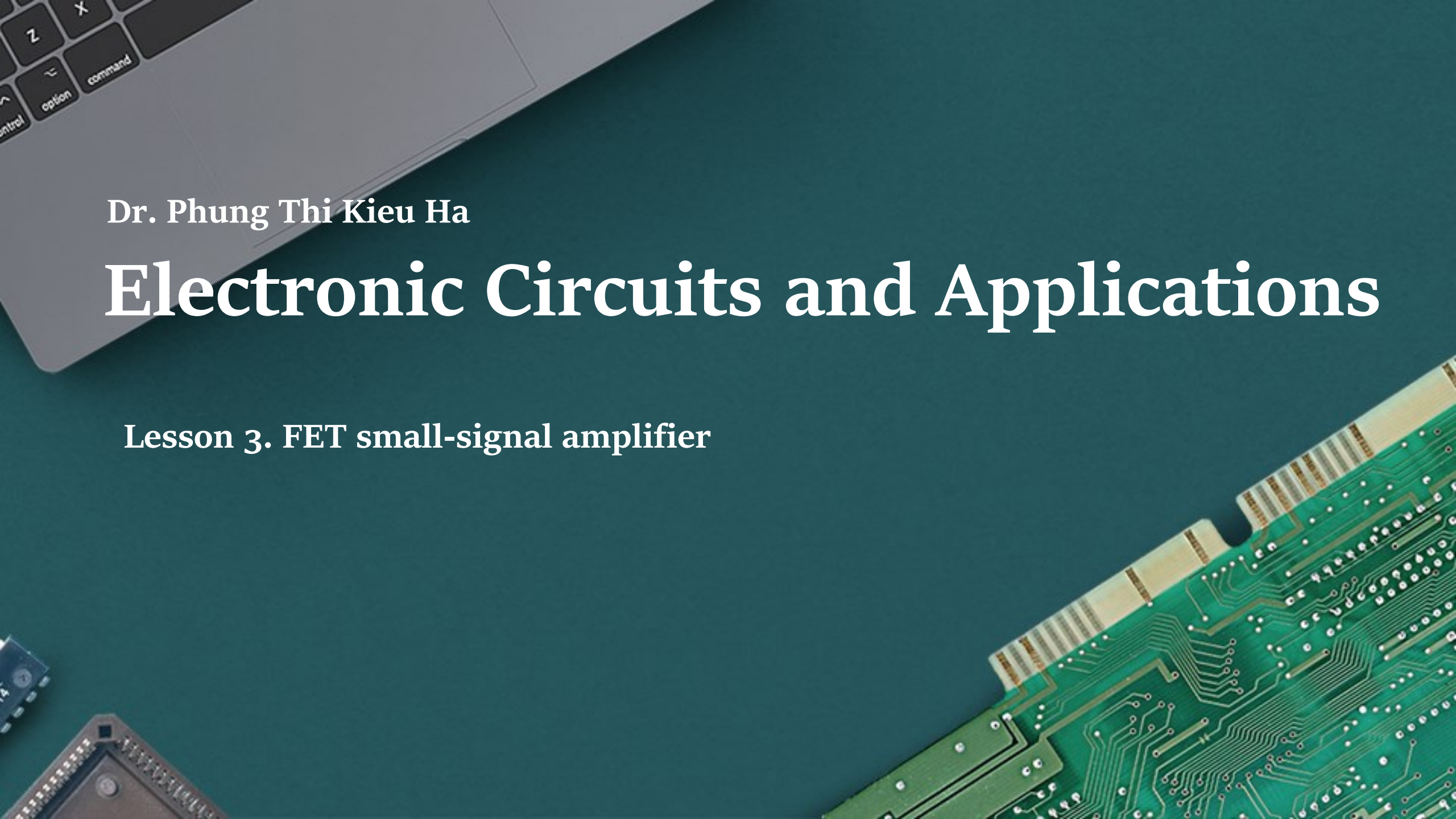
Dr. Phung Thi Kieu Ha

Electronic Circuits and Applications

Lesson 3. FET small-signal amplifier



Learning Contents

1. Introduction of FET devices
2. FET biasing
3. FET small-signal amplifier
4. Comparison

Learning Goals

1. Be able to perform a dc analysis of JFET and MOSFET networks.
2. Become acquainted with the small-signal ac model for a JFET and MOSFET.
3. Be able to perform a small-signal ac analysis of a variety of JFET and MOSFET configurations.
4. Be able to analyze cascaded configurations with FETs and/or BJT amplifiers.

1. Introduction

1.1. FET characteristics & classifications

1.2. JFET

1.3. DMOS

1.4. EMOS

1. Introduction

1.1. FET characteristics & classification

- Very large input impedance, nMΩ-n100MΩ
- To control by voltage
- Low power consumption
- Low noise suitable for small signal source
- Less impact by temperature
- Small size, production technology allow to integrate very large number of devices
- Good as a switch

1. Introduction

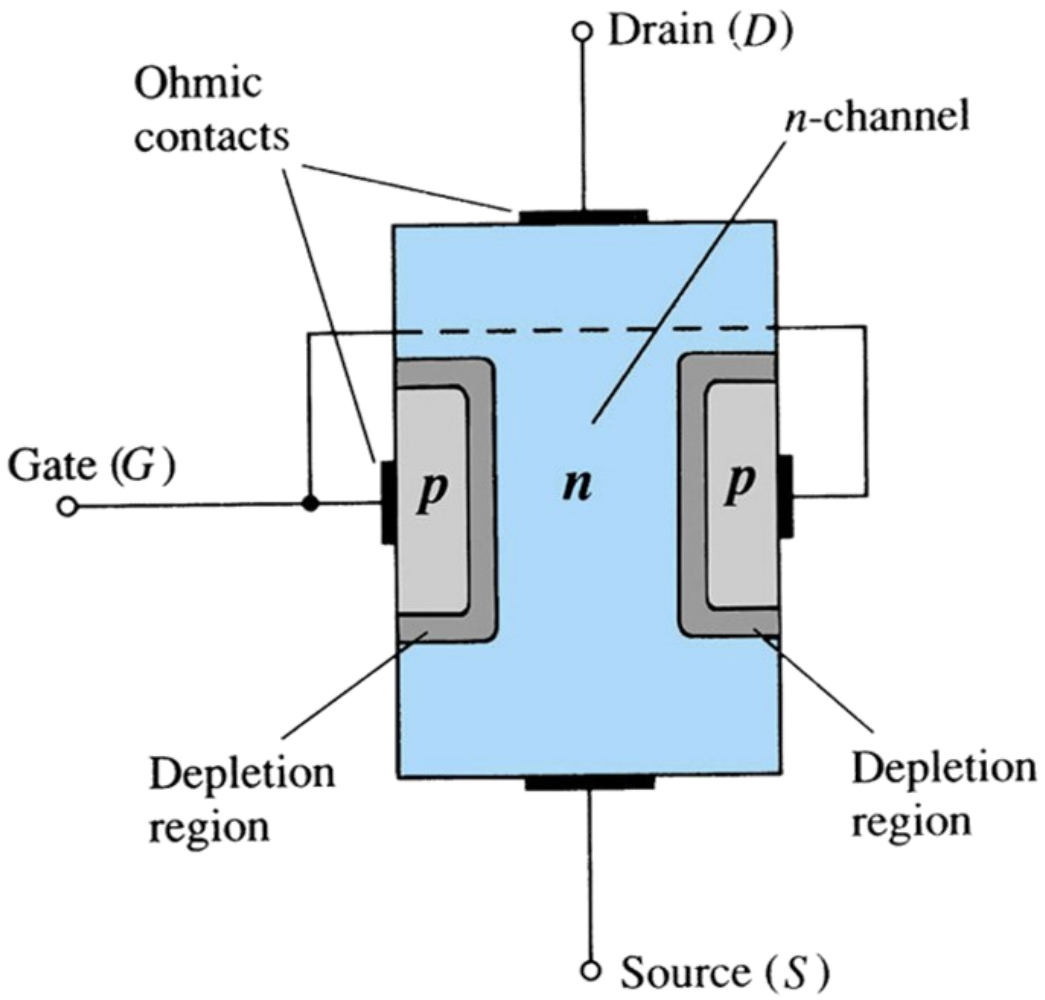
1.1. FET characteristics & classification

Classification

- JFET-Junction Field Effect Transistor
  - ✓N-channel
  - ✓P-channel
- MOSFET-Metal Oxide Semiconductor FET
  - ✓Depletion-type - DMOS
    - N and P channel
  - ✓Enhancement-type - EMOS
    - N and P channel

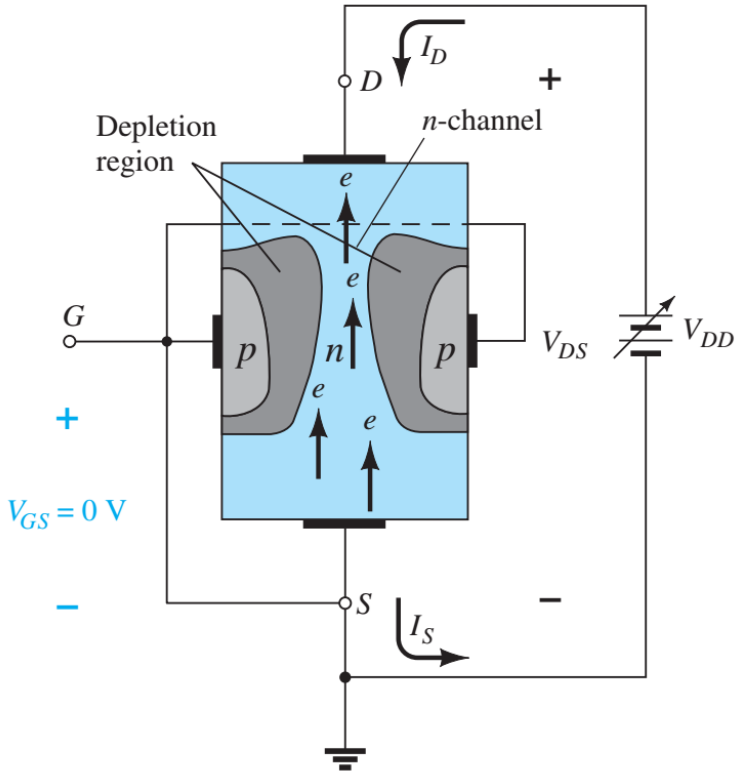
1. Introduction

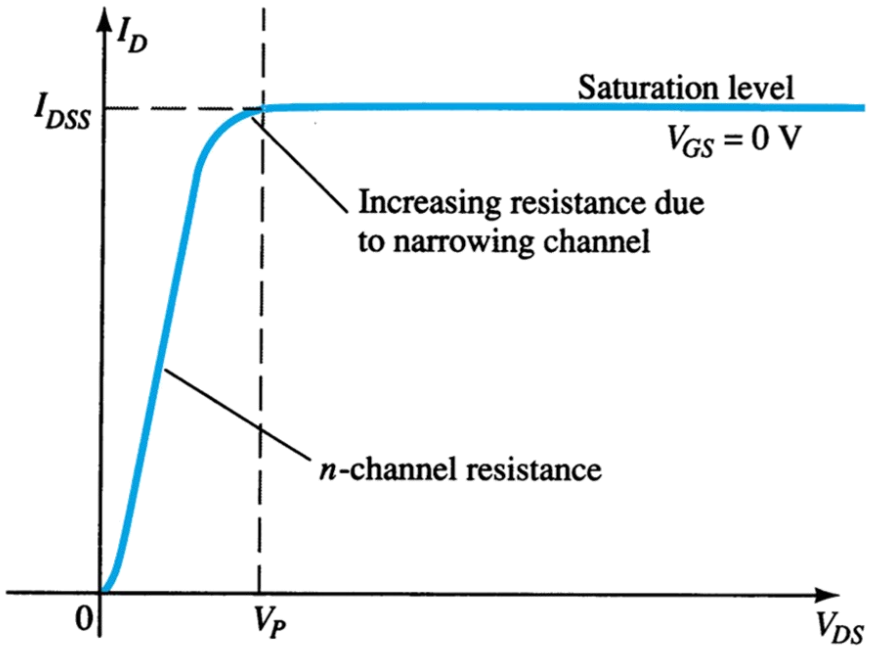
1.2. JFET structure & operation



1. Introduction

1.2. JFET structure & operation

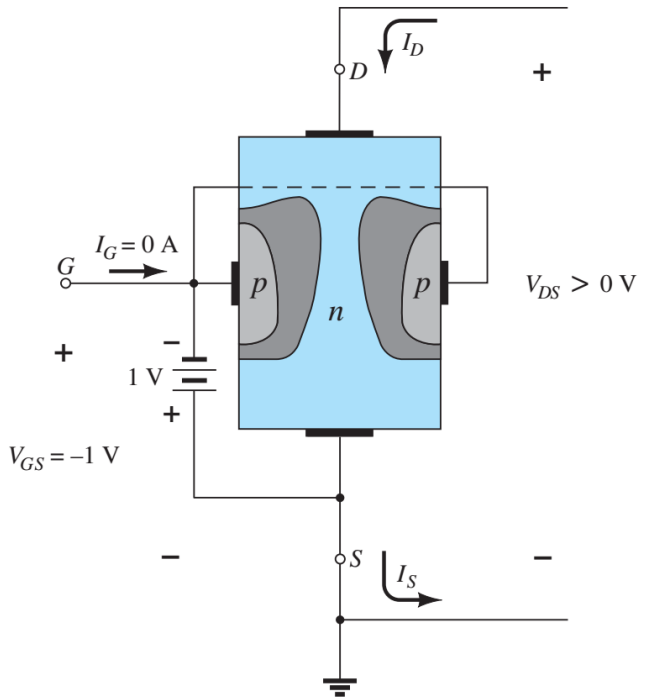


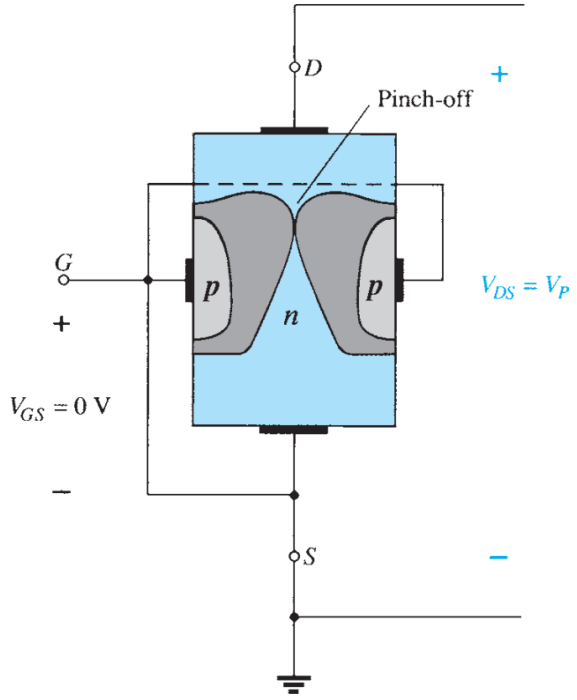


$V_{GS} = 0$, V_{DS} increases, I_D increases

1. Introduction

1.2. JFET structure & operation



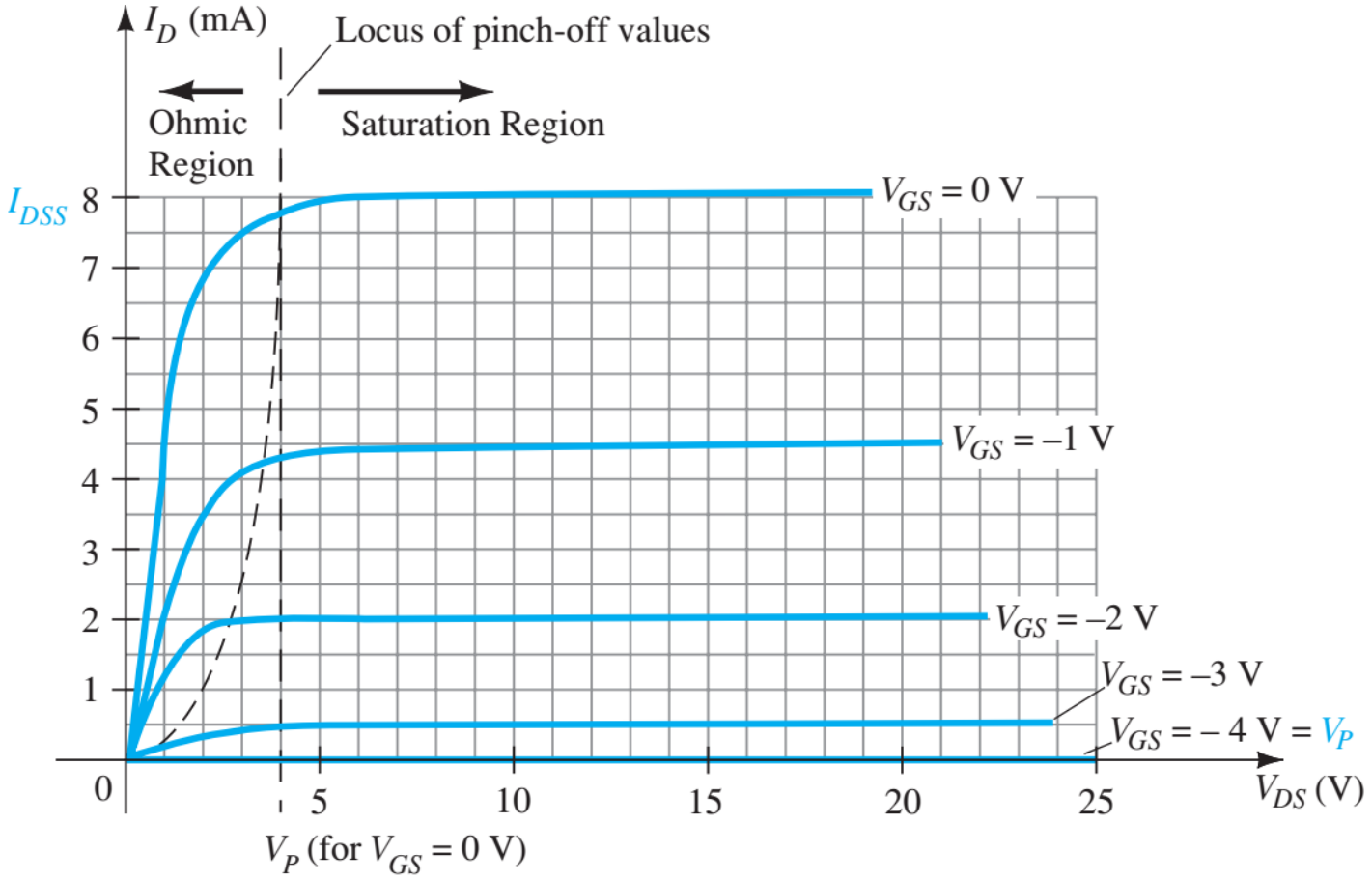


$V_{GS} < 0$, $V_{DS} > 0$,
the saturation level of
I_D decrease

$V_{GS}=V_P$ (pinch-off voltage),
$I_D=0$

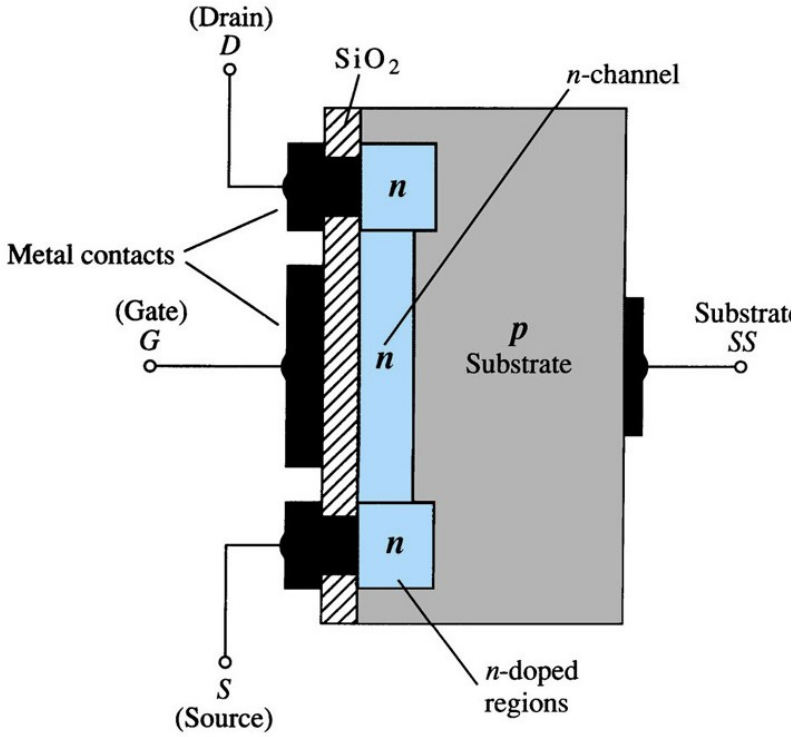
1. Introduction

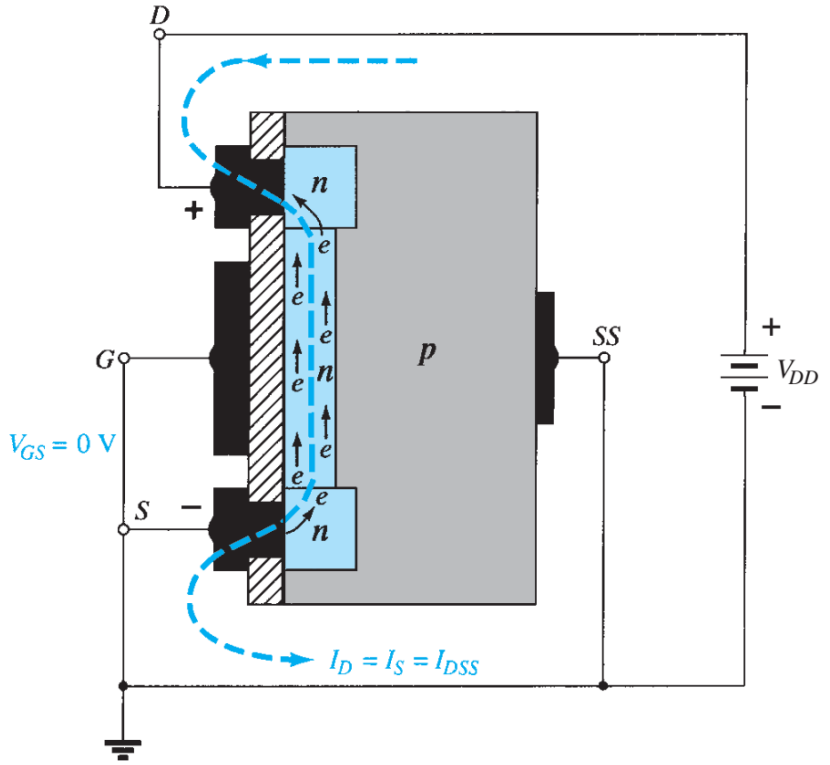
1.2. JFET structure & operation



1. Introduction

1.3. D-MOSFET structure & operation

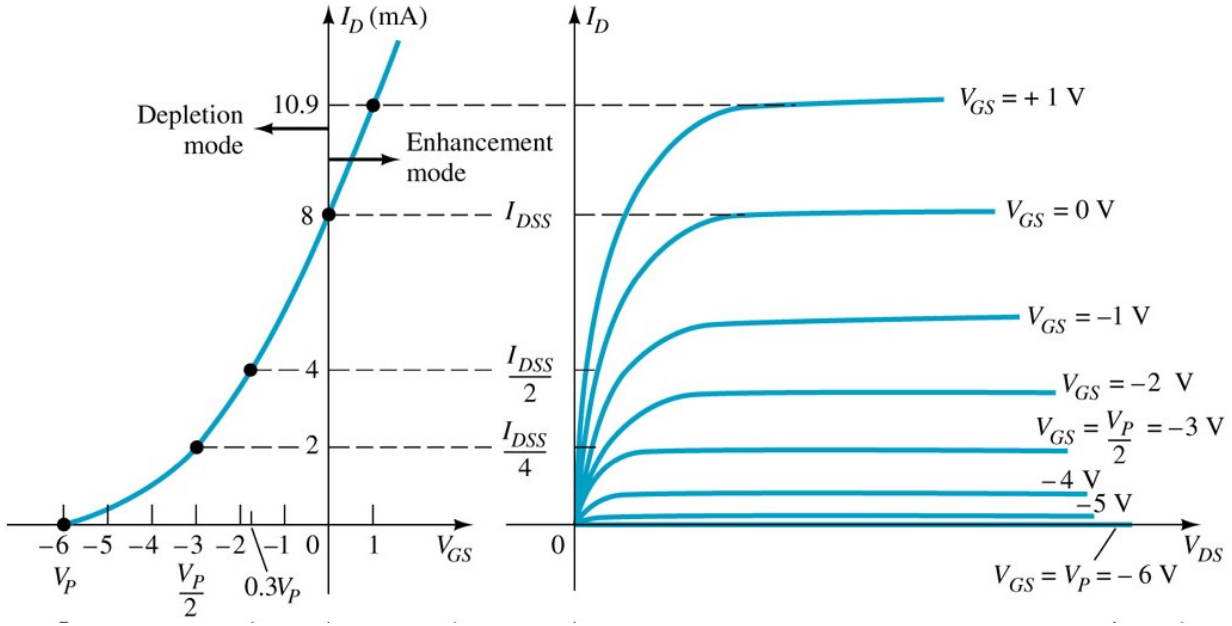




N-channel depletion DMOS

1. Introduction

1.3. D-MOSFET structure & operation



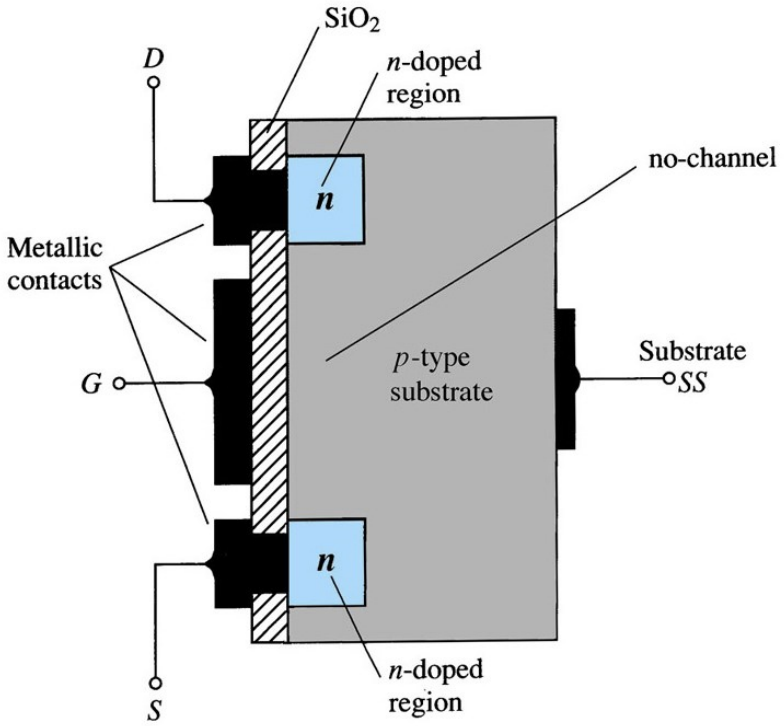
Transfer characteristic follows Shockley equation:

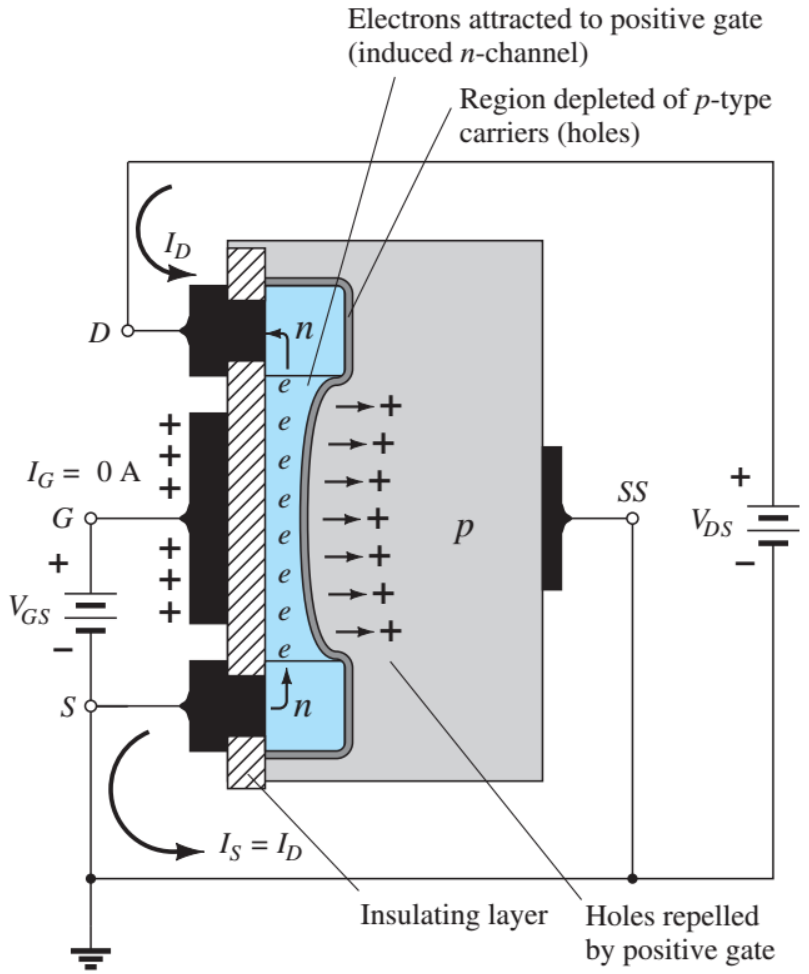
$$I_D = I_{DSS}(1 - V_{GS}/V_P)^2$$

Note: DMOS can operate at $V_{GS} > 0$, $I_D > I_{DSS}$, enhancement mode

1. Introduction

1.4. E-MOSFET structure & operation



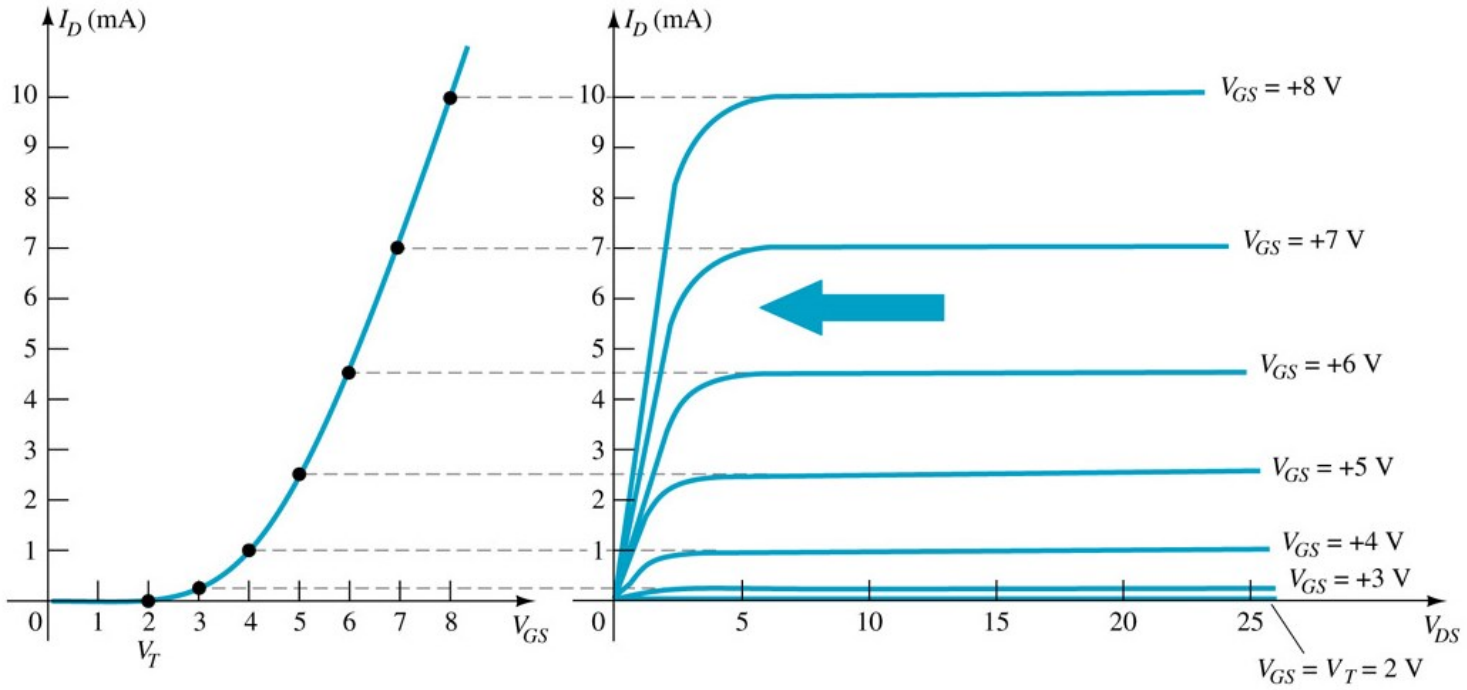


N-channel EMOS

$V_{GS} > 0$, $V_{DS} > 0$

1. Introduction

1.4. E-MOSFET structure & operation



Different transfer characteristics

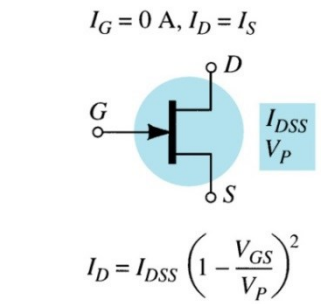
$I_D = k(V_{GS} – V_T)^2$ in which $V_T > 0$ (N channel)

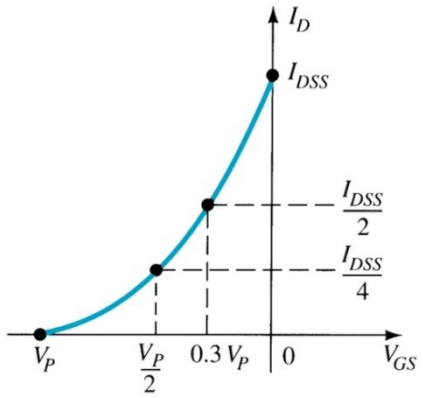
Note: $V_{GS} < V_T$, $I_D = 0$

1. Introduction

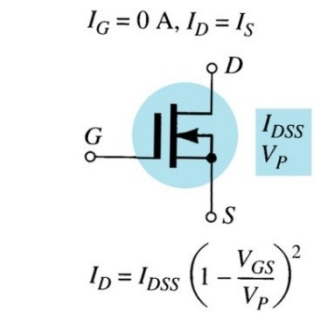
Summary

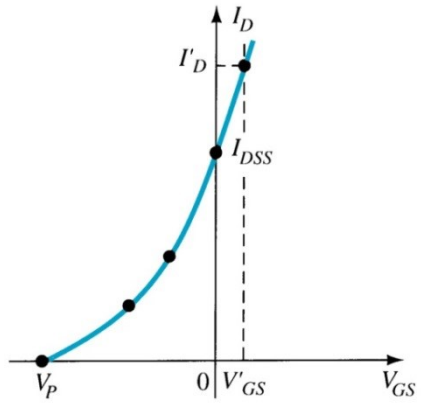
JFET



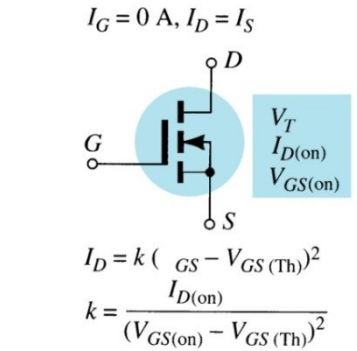


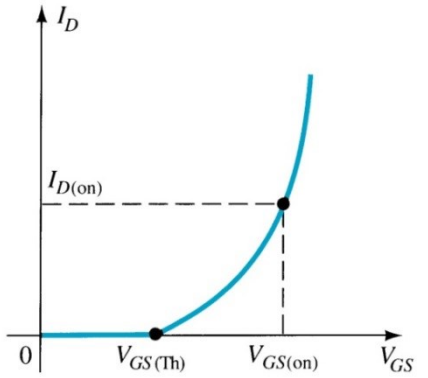
DMOS





EMOS





2. FET biasing

2.1. Fix bias configuration

2.2. Self-bias conf.

2.3. Voltage-divider conf.

2.4. Voltage-feedback conf.

2. FET biasing

The relationship of current & voltage when FET is in "amplifier" mode

For all type of FET:

$$I_G = 0A$$

$$I_D = I_S$$

JFET & DMOS:

$$I_D = I_{DSS}(1 - V_{GS}/V_P)^2$$

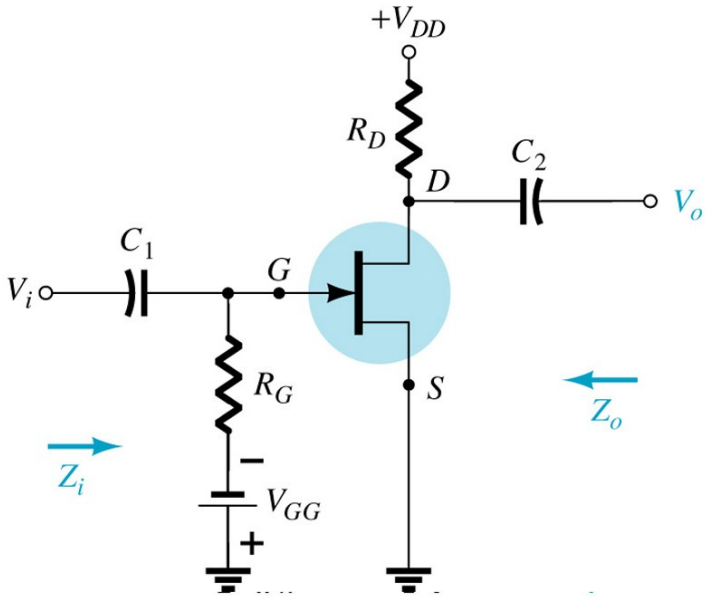
EMOS:

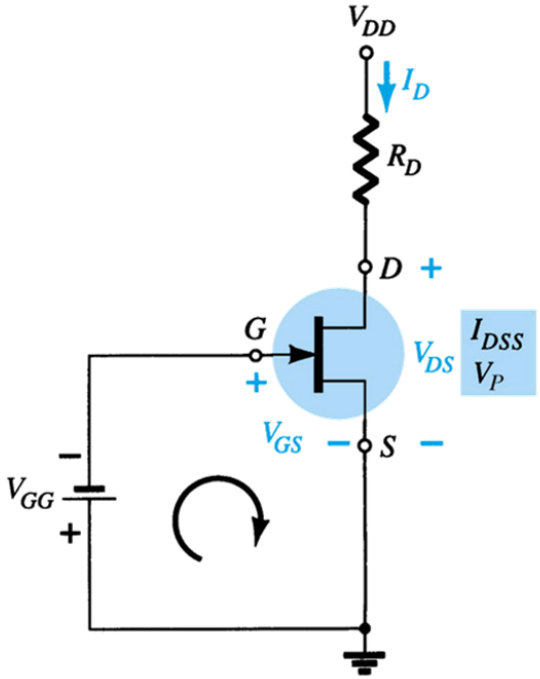
$$I_D = k(V_{GS} - V_T)^2$$

Non-linear relationship of V_{GS} and I_D

2. FET biasing

2.1. Fix bias circuit





$I_G = 0, V_S = 0$

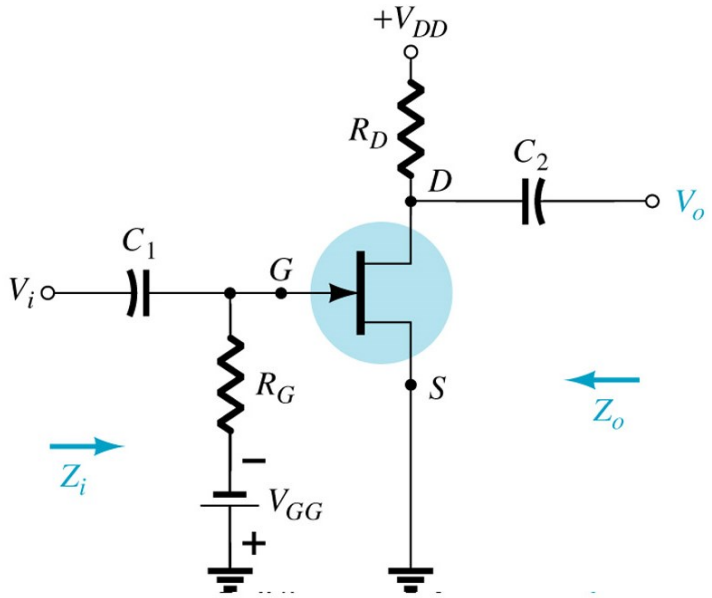
$V_{GS} = V_G = - V_{GG},$

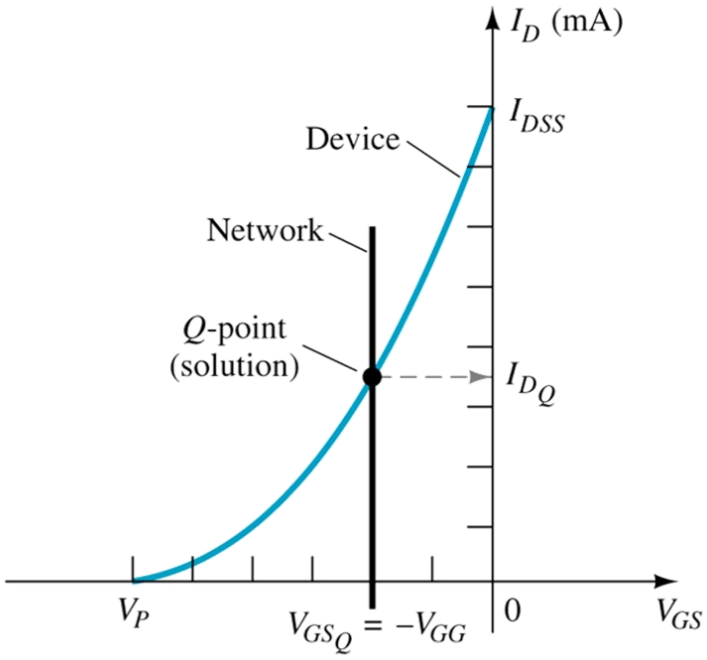
V_{GS} is fixed by a DC voltage source V_{GG}

$I_D = I_{DSS}(1-V_{GS}/V_p)^2$

2. FET biasing

2.1. Fix bias circuit





Load line equation

$V_{GS} = - V_{GG}$

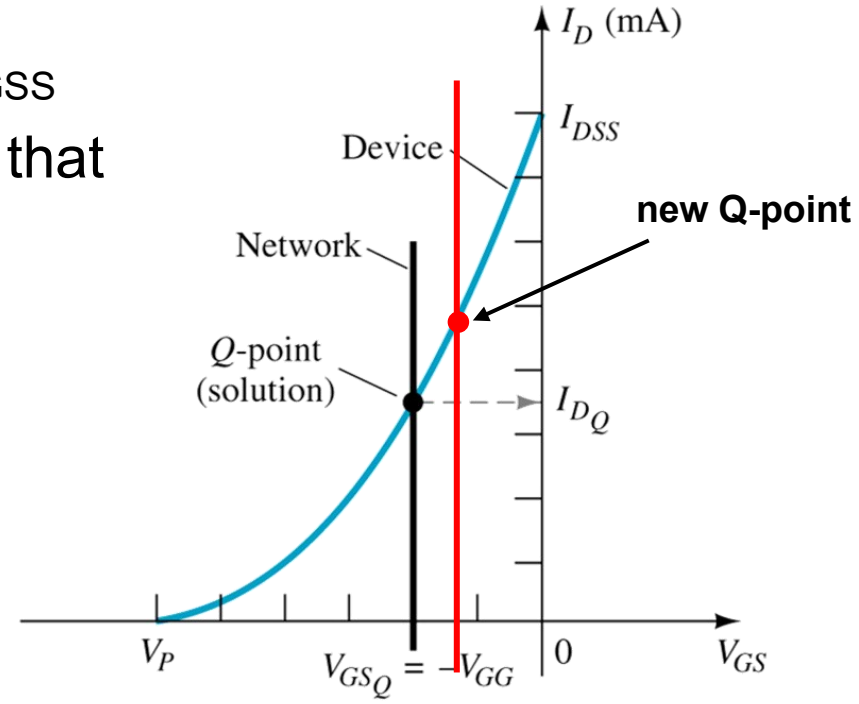
2. FET biasing

2.1. Fix bias circuit

In reality, leakage current I_{GSS} increases with temperature that it can not be neglected

Operating point movement

$$V_{GS} = V_{GG} + I_{GSS}*R_G$$



2. FET biasing

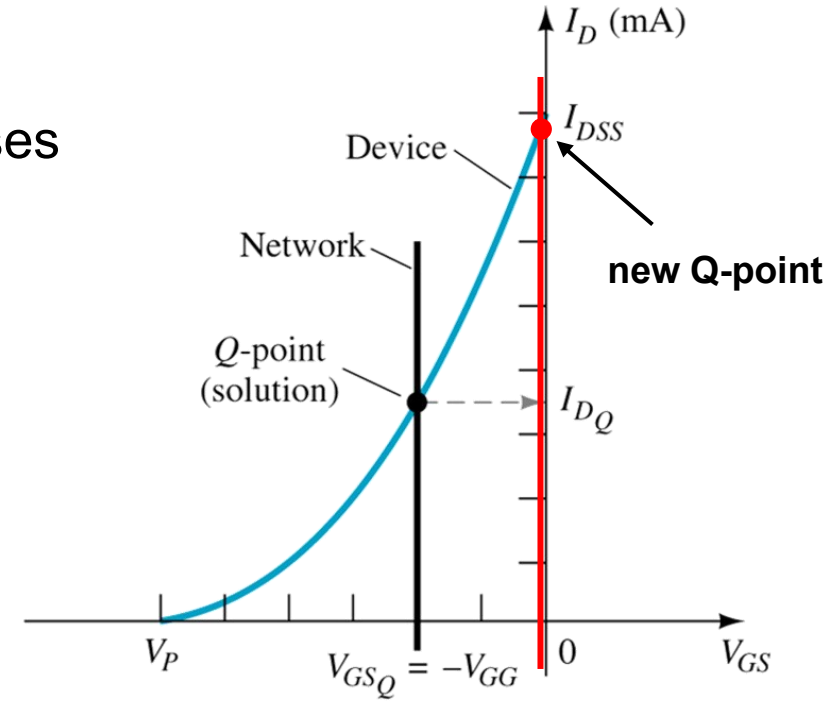
2.2. Fix bias circuit

V_{GG}=-1V and R_G=1 MΩ.
I_{GSS}=10nA at room temperature 25°C and double when temperature increases 10°C.
V_{GS} at temp of 125°C?

Solution

At 25°C, $I_{GSS} \times R_G = 10^{-9} \times 10^6$ = 1mV, neglected since V_{GG}= -1V.

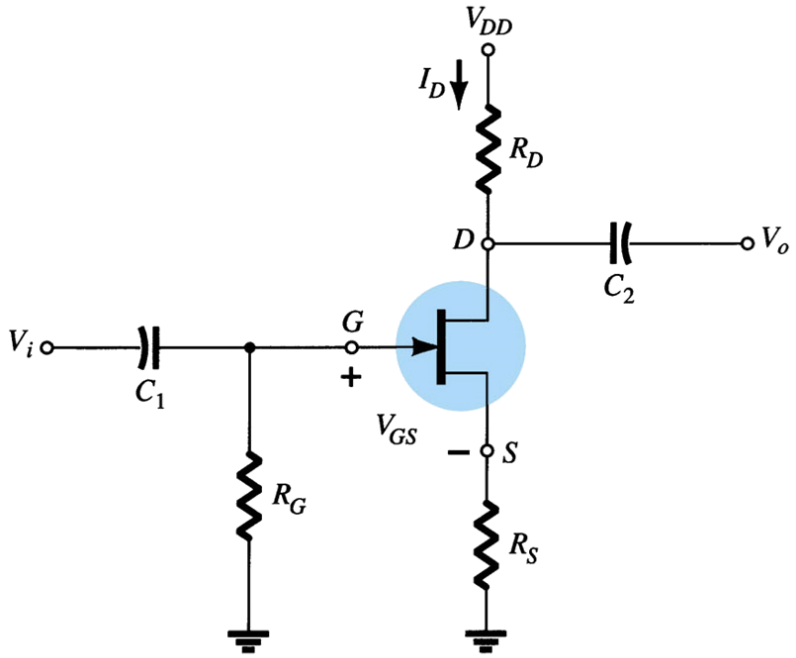
At 125°C, I_{GSS} increase 2^{10} (≈10^3), then
I_{GSS} = 10^3 ×1nA =1μA
I_{GSS}*R_G= 1V
V_{GS} = 0V and I_D = I_{DSS}

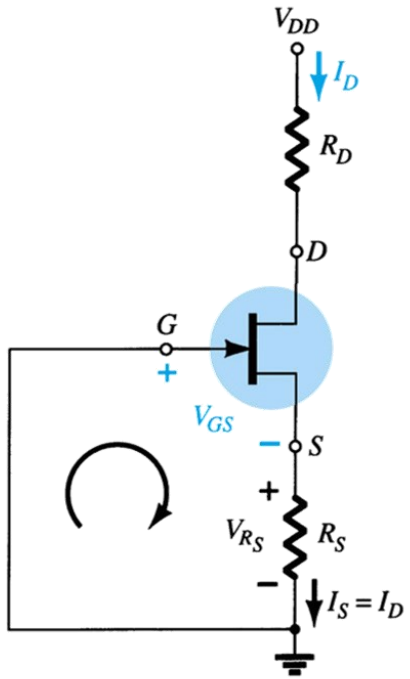


Moved Q is far from the pre-designed configuration at room temperature

2. FET biasing

2.2. Self-bias circuit





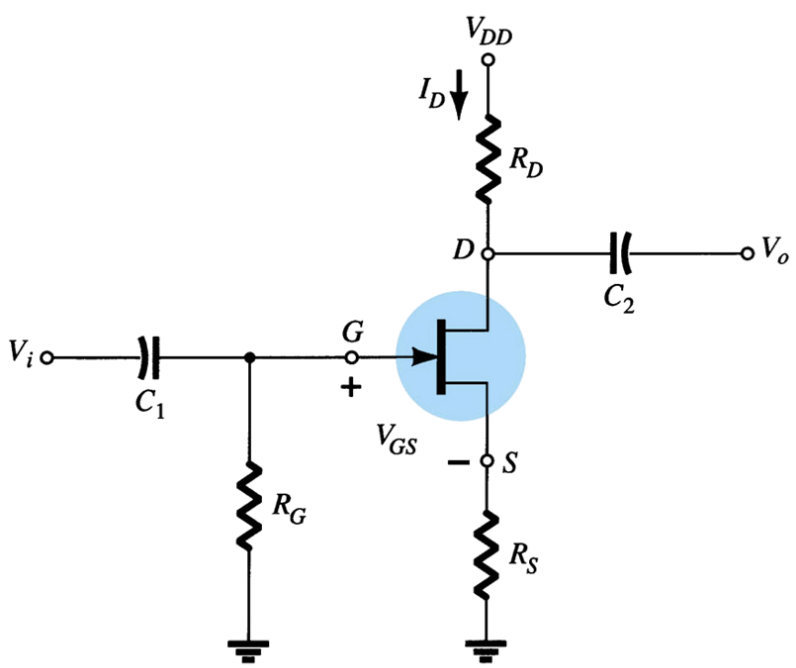
$I_G = 0 \Rightarrow V_G = 0V \Rightarrow$

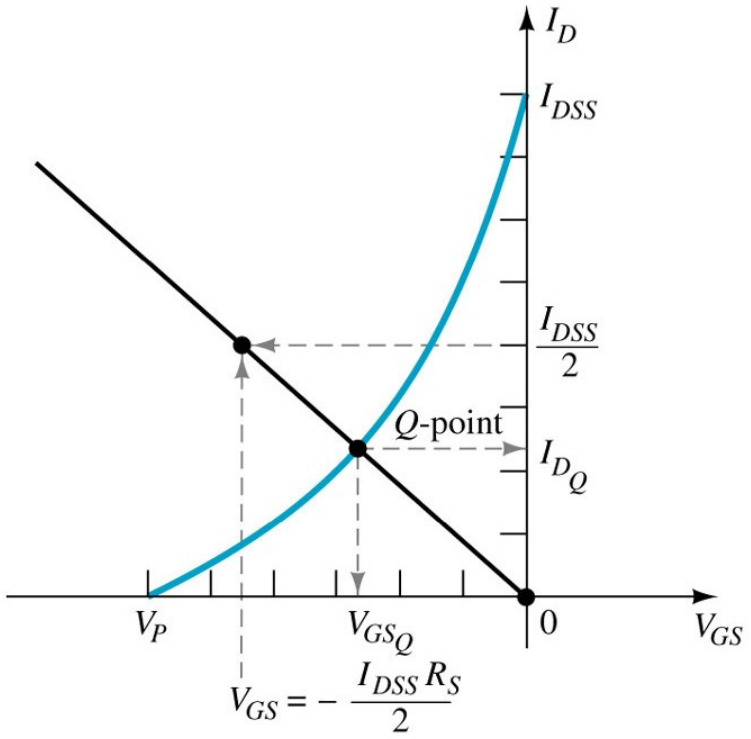
$V_{GS} = - I_S R_S$

$I_D = I_{DSS}(1-V_{GS}/V_p)^2$

2. FET biasing

2.2. Self-bias circuit



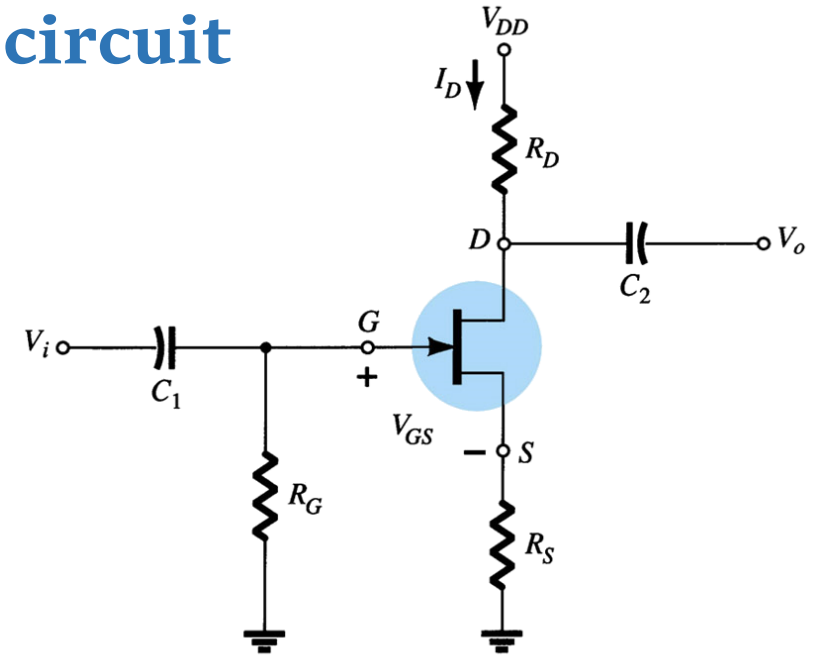


Load line equation

$V_{GS} = - I_S * R_S$

2. FET biasing

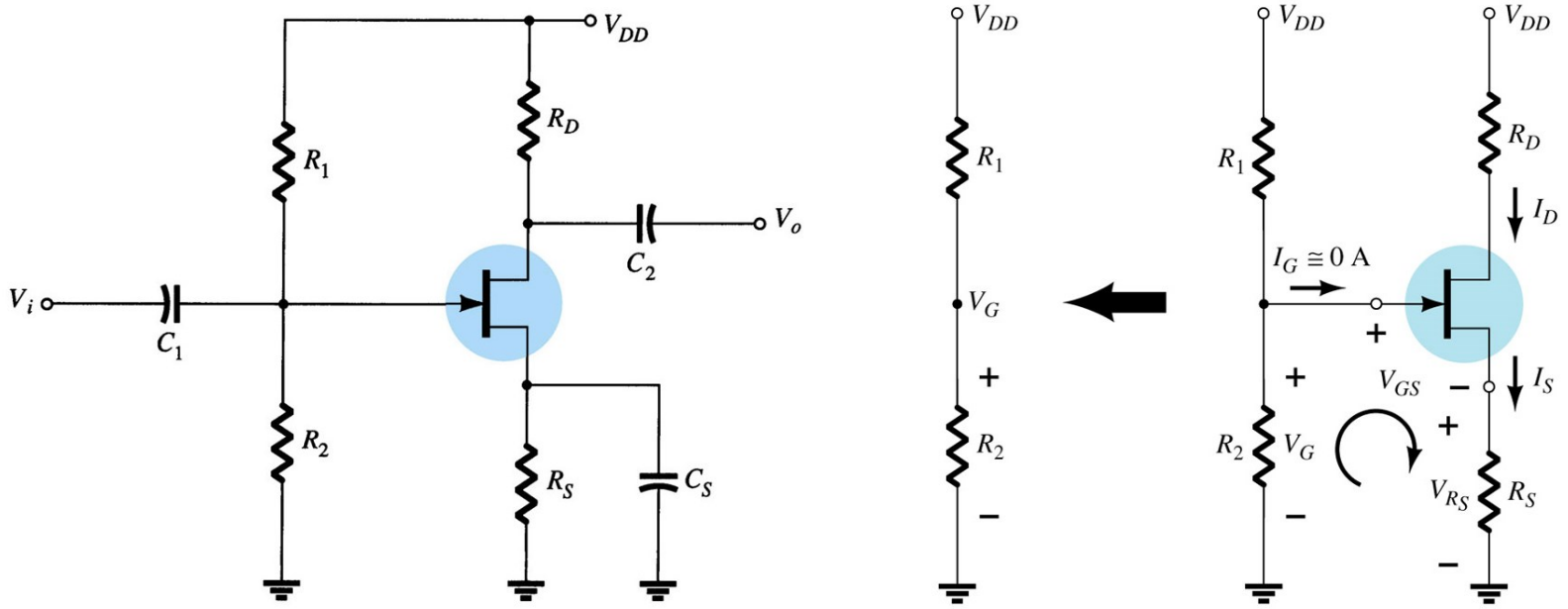
2.2. Self-bias circuit



- What is the difference from Fix-base?
- Why is it called “self-bias?
- What is the role of R_S?
- Can we neglect R_G?
- How is the temperature stability?

2. FET biasing

2.3. Voltage-divider bias for JFET



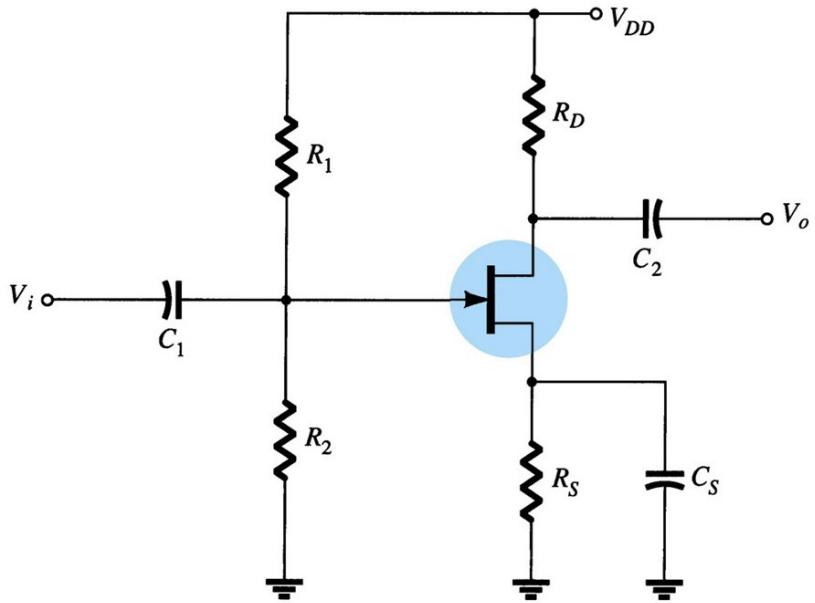
$I_G = 0$, then $V_G = V_{DD}R_2/(R_1+R_2)$

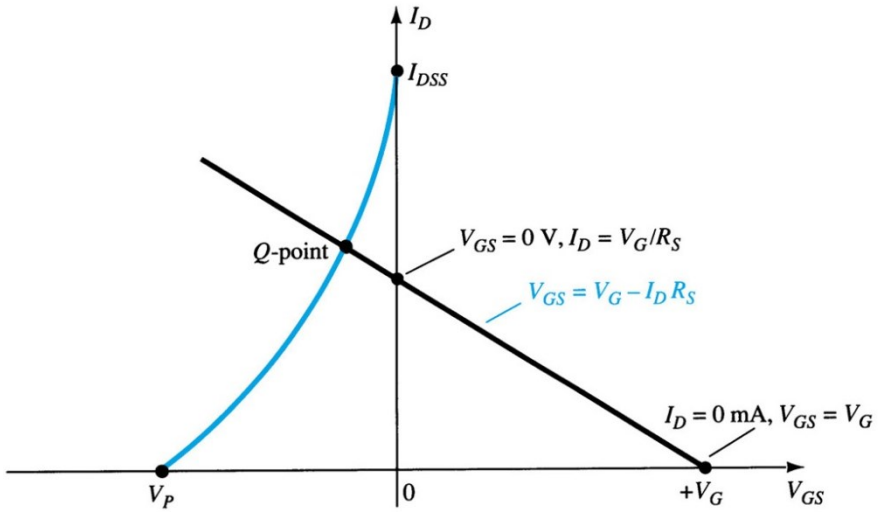
$V_{GS} = V_G - I_D R_S$

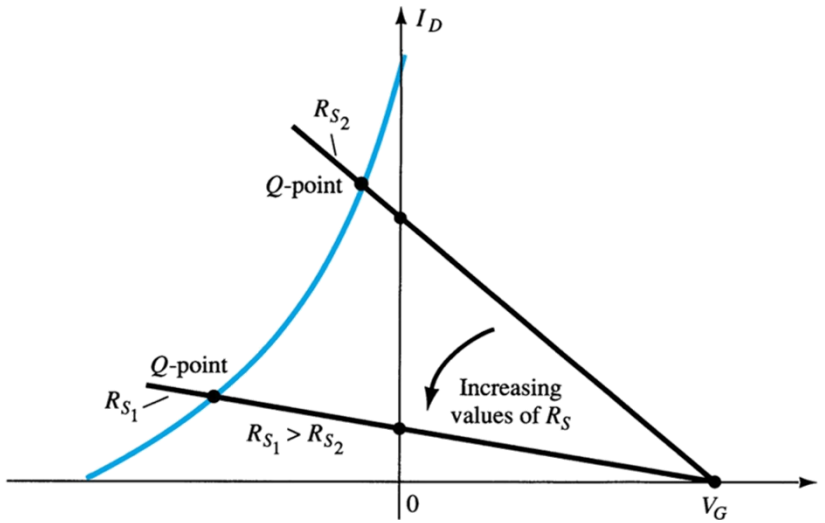
$I_D = I_{DSS}(1-V_{GS}/V_P)^2$

2. FET biasing

2.3. Voltage-divider bias for JFET

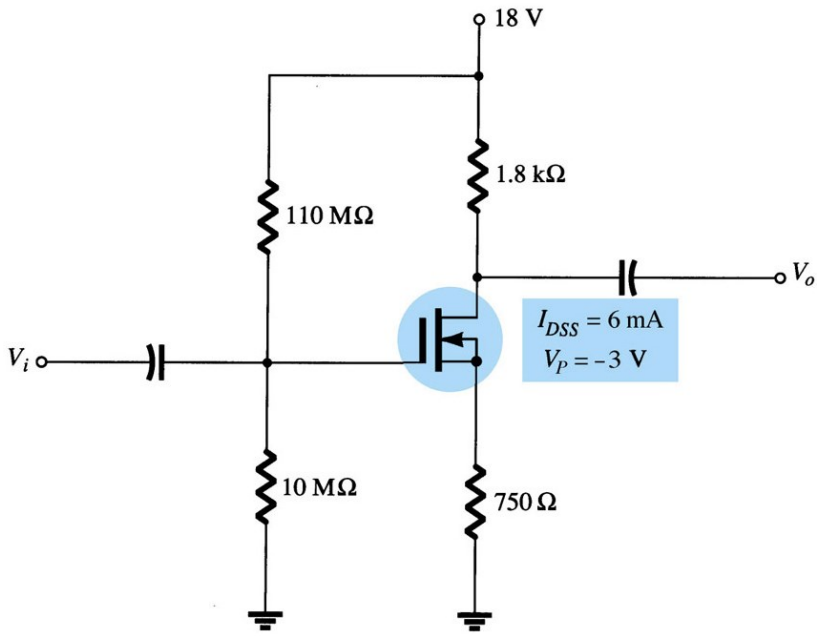






2. FET biasing

2.3. Voltage-divider bias for DMOS



$V_G = V_{DD} * 10M\Omega/(110M\Omega+10M\Omega)$

Load line equation

$V_{GS} = V_G - I_S * 0.75K\Omega$ (1)

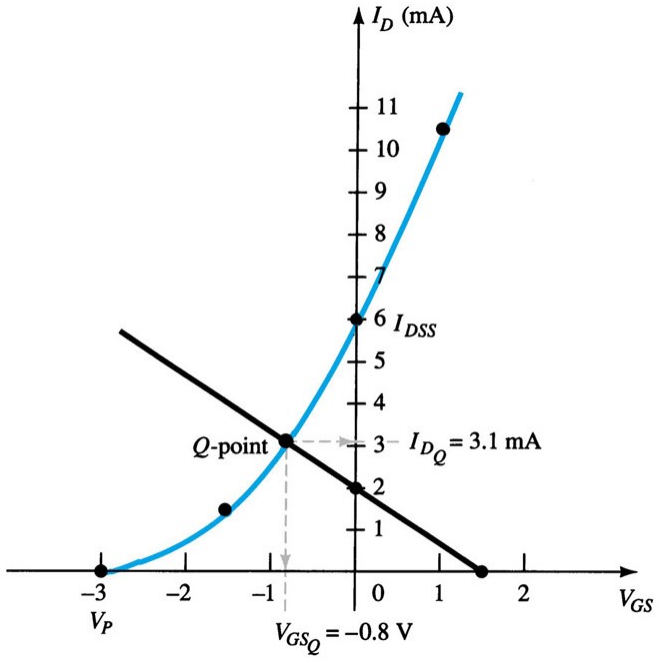
DMOS characteristic:

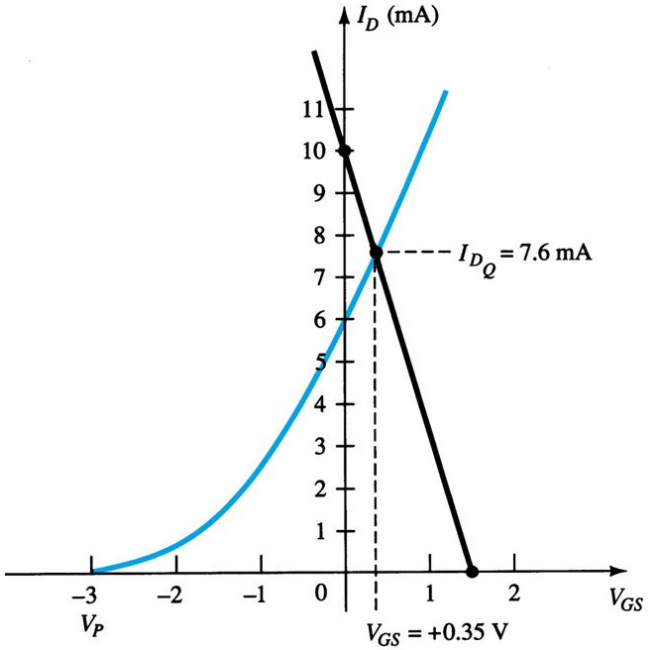
$I_D = I_{DSS}(1-V_{GS}/V_P)^2$ (2)

Note: V_{GS} can be positive

2. FET biasing

2.3. Voltage-divider bias for DMOS

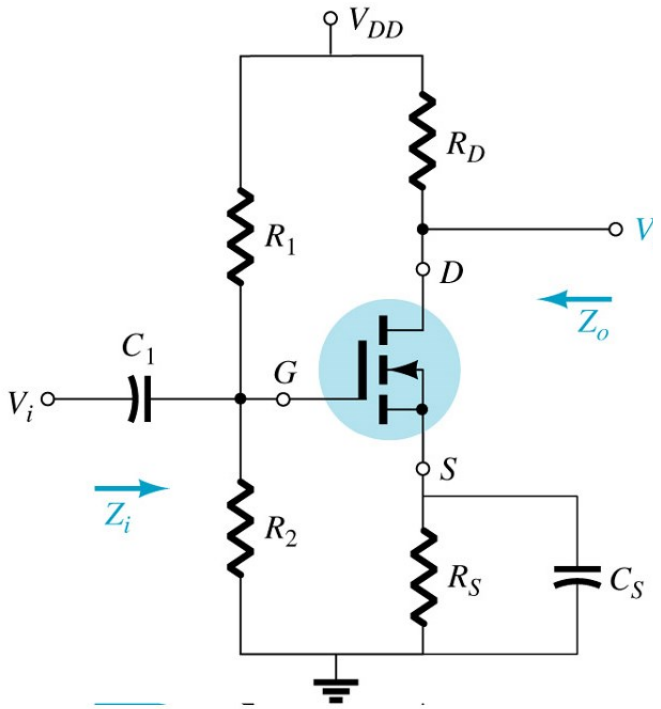


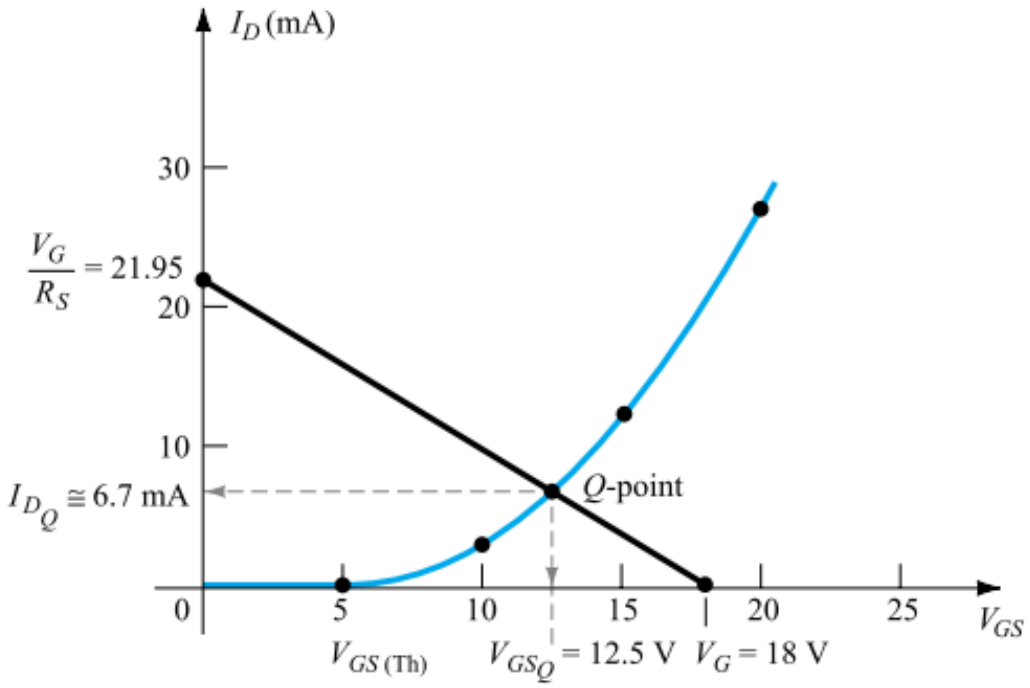


DMOS: $I_D = I_{DSS}(1-V_{GS}/V_P)^2$ V_{GS} can be positive

2. FET biasing

2.3. Voltage-divider bias for EMOS





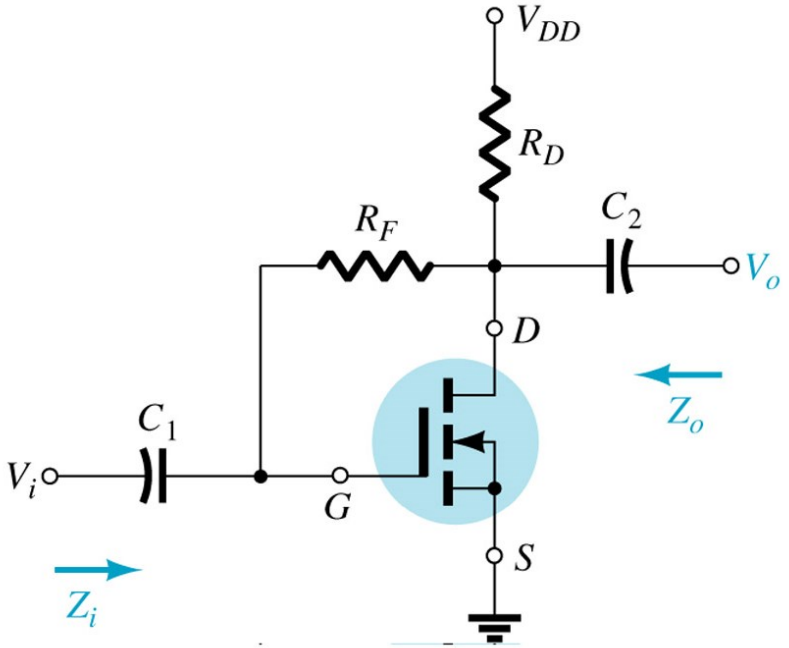
EMOS characteristics:

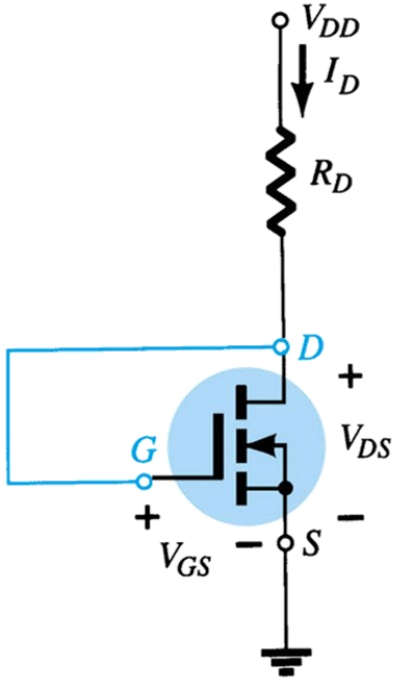
$I_D = k(V_{GS}-V_T)^2$

$k=I_{Don}/(V_{GSon}-V_T)_2$

2. FET biasing

2.4. Voltage-feedback bias for EMOS





$I_G = 0 \Rightarrow V_G = V_D$

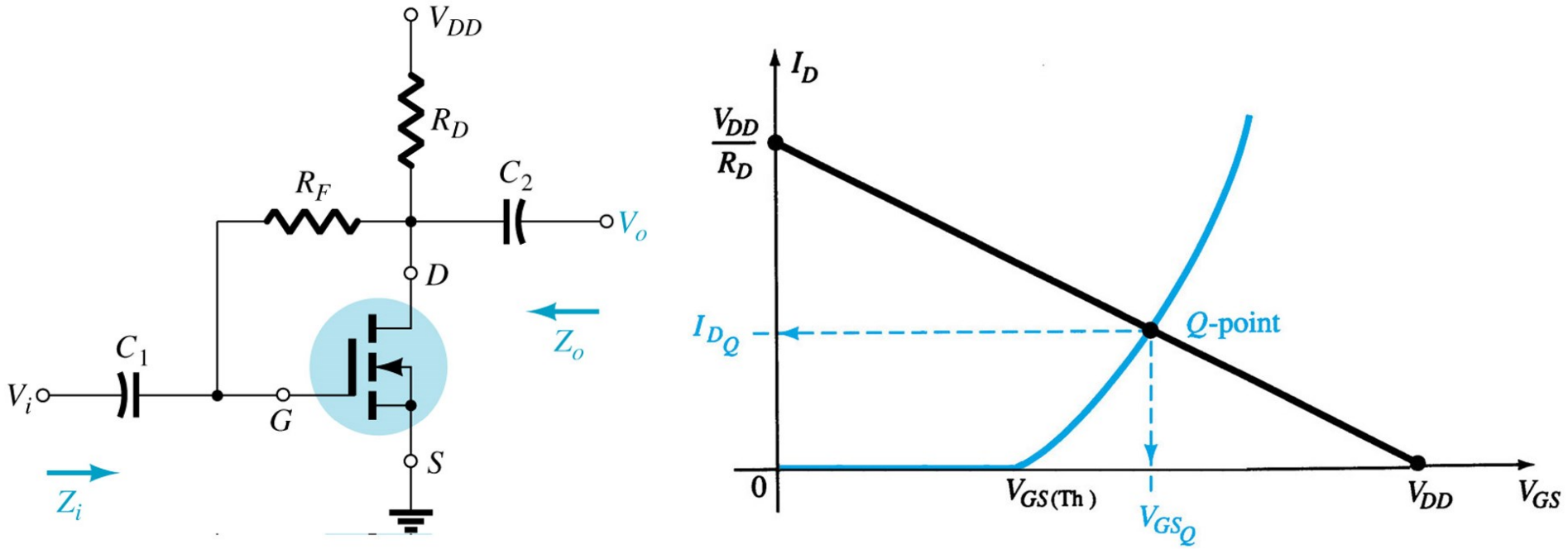
$V_{GS} = V_{DS} = V_{DD} - R_D I_D$

$I_D = k(V_{GS} - V_T)^2$

$k = I_{Don}/(V_{GSon} - V_T)^2$

2. FET biasing

2.4. Voltage-feedback bias for EMOS



Can this configuration be used to bias JFET?

3. FET small-signal amplifier

3.1. Equivalent circuit model

3.2. Common-Gate circuit

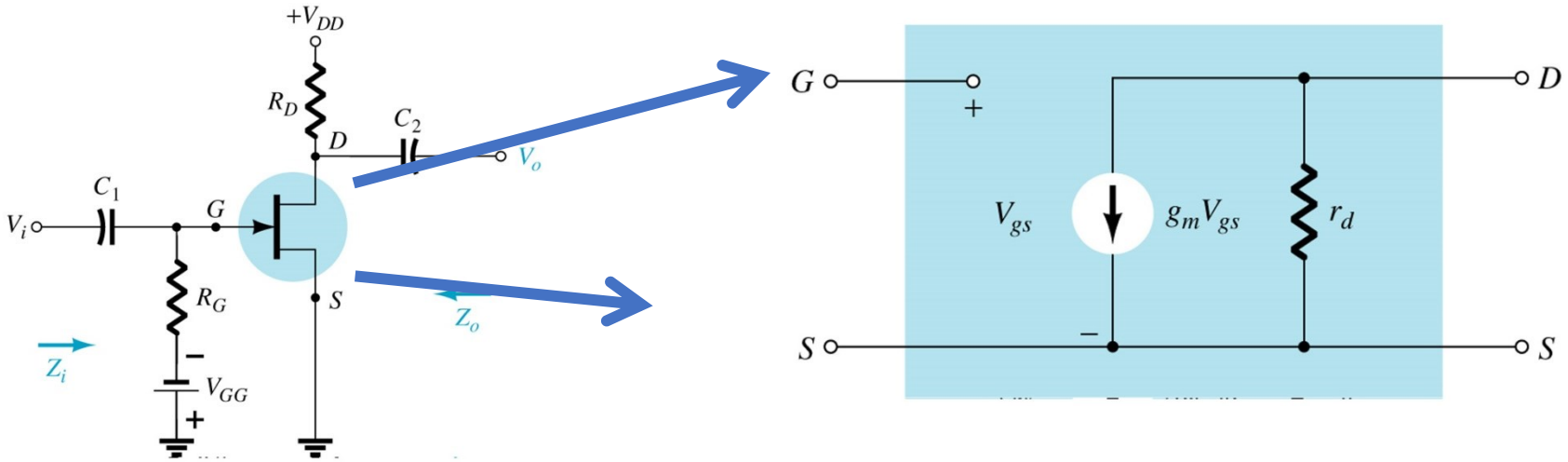
3.3. Common-Source circuit

3.4. Common-Drain circuit

3.5. Common-Source configuration with EMOS

3. FET Small-signal amplifier

3.1. FET equivalent model



An open-circuit between G and S as very large input impedance (n100-n1000 MΩ)

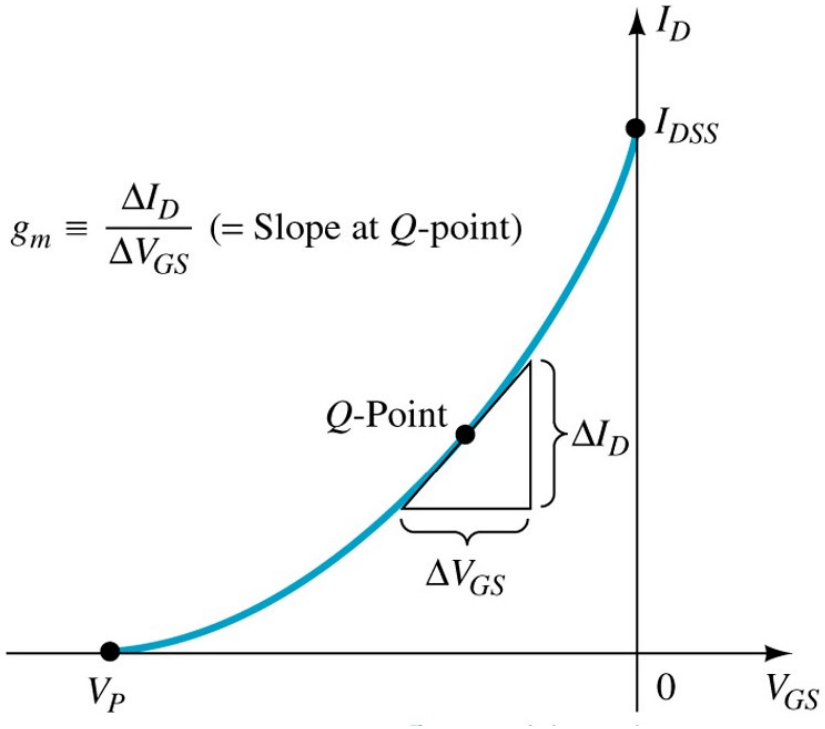
A voltage-controlled current source

A trans-conductance factor g_m –

An output impedance r_d

3. FET small-signal amplifier

3.1. FET equivalent model

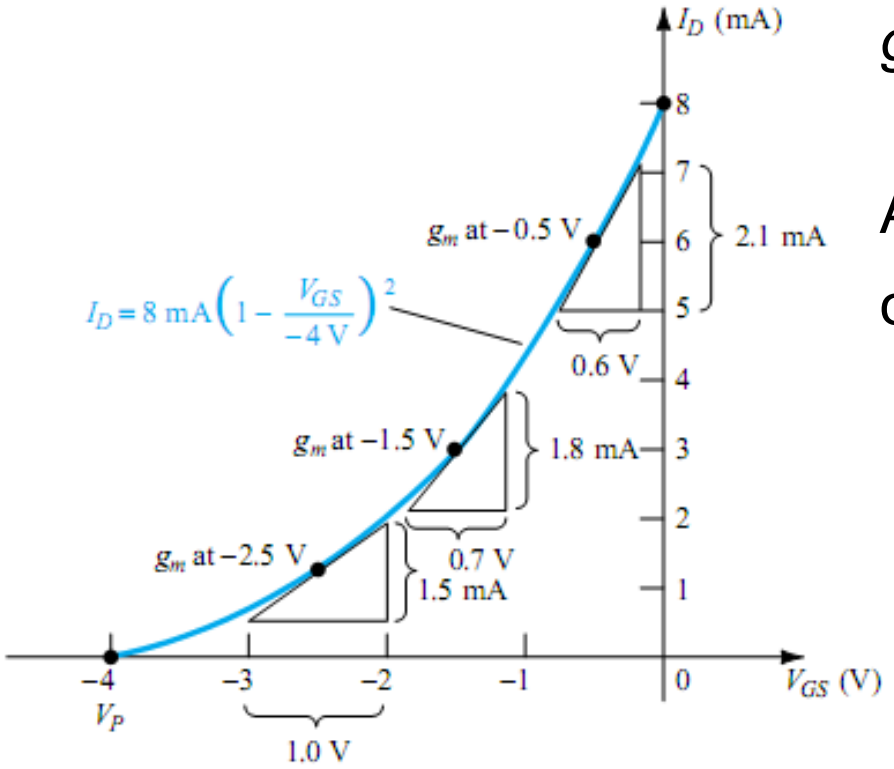


$g_m = \Delta I_D / \Delta V_{GS} = d(I_D(V_{GS}))$

Show the speed of the
variation of I_D in the variation of V_{GS}

3. FET small-signal amplifier

3.1. FET equivalent model



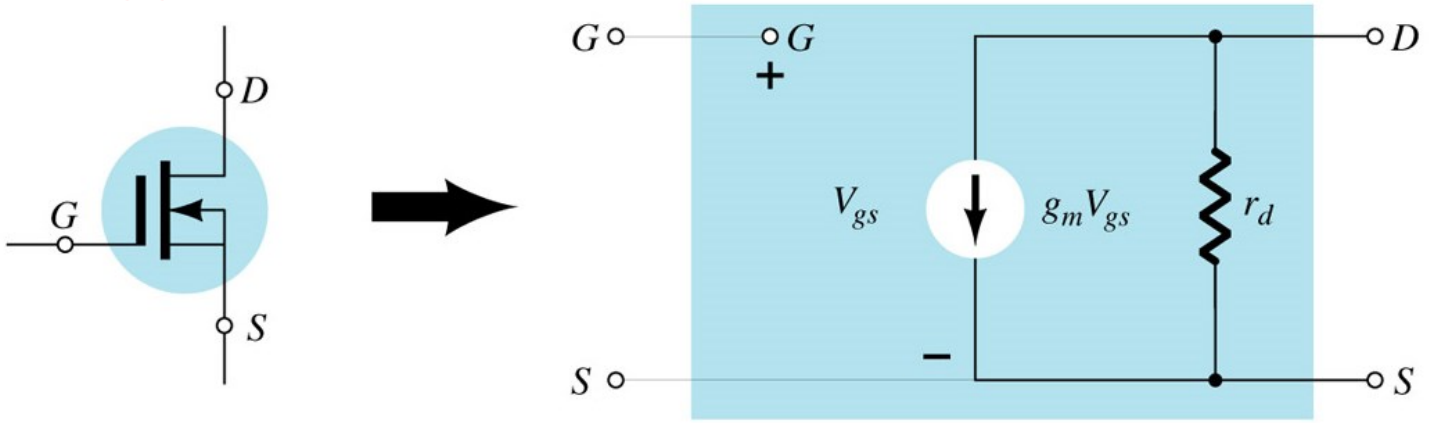
g_m depends on the operating point

Approximately determine the g_m at the operating point

3. FET small-signal amplifier

3.1. FET equivalent model

DMOSFET



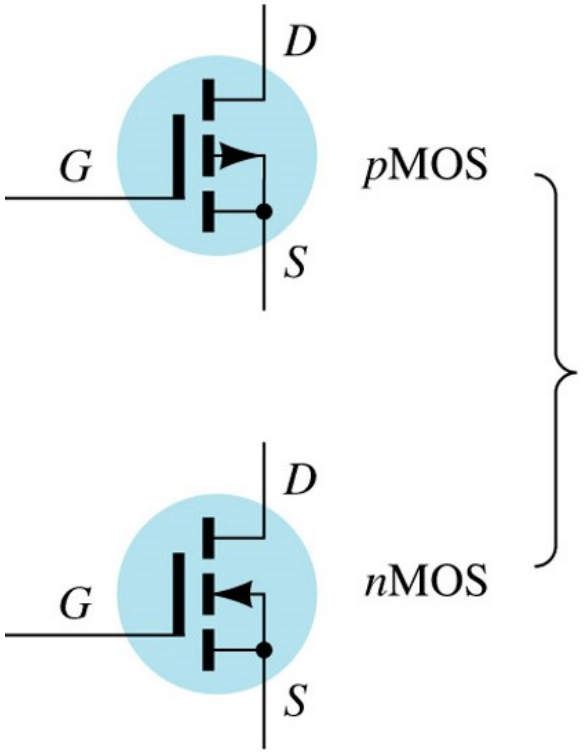
Similar to the model of JFET

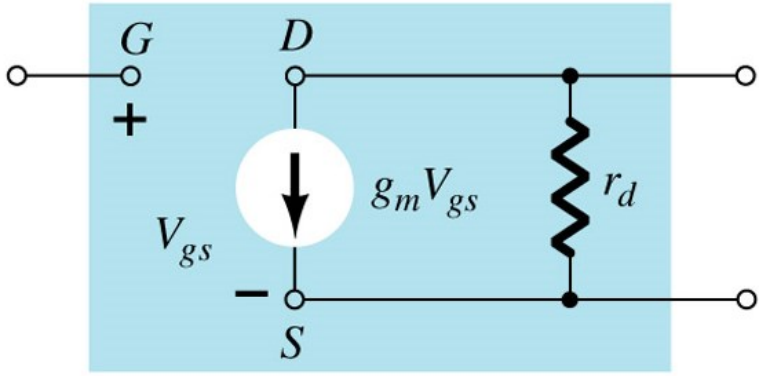
Note on the possible value of g_m

3. FET small-signal amplifier

3.1. FET equivalent model

EMOSFET





$$g_m = |y_{fs}| \ , \ r_d = \frac{1}{|y_{os}|}$$

3. FET small-signal amplifier

3.1. FET equivalent model

Trans-conductance factor of JFET/DMOS

Shockley equation for transfer characteristics

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

=> trans-conductance

$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{V_{GS}}{V_P}\right]$$

3. FET small-signal amplifier

3.1. FET equivalent model

Transfer characteristics equation

$$I_D = k(V_{GS} - V_{GS(\mathrm{Th})})^2$$

Trans-conductance factor of EMOS

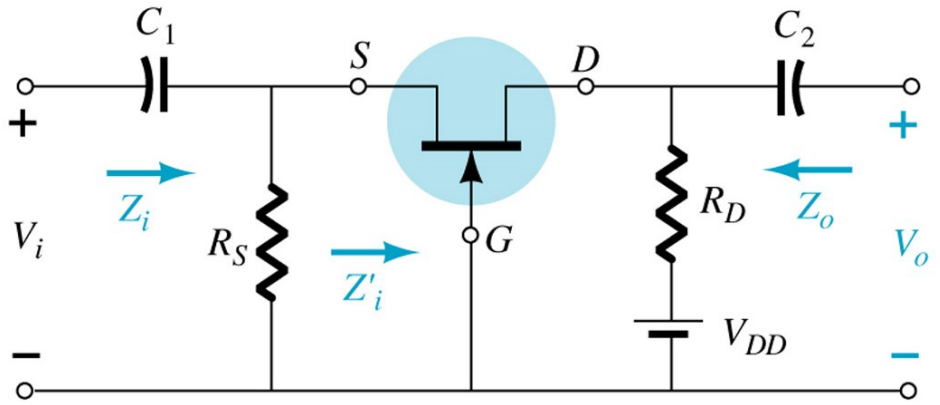
$$g_m = 2k(V_{GS_Q} - V_{GS(\mathrm{Th})})$$

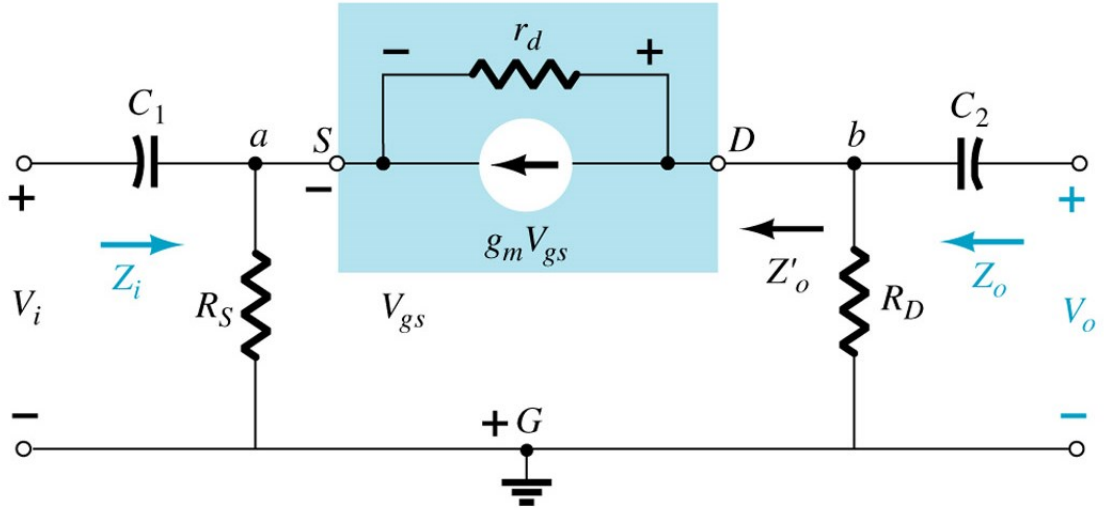
in which k is determined

$$k = \frac{I_{D(\mathrm{on})}}{(V_{GS(\mathrm{on})} - V_{GS(\mathrm{Th})})^2}$$

3. FET small-signal amplifier

3.2. Common-Gate configuration





3. FET small-signal amplifier

3.2. Common-Gate configuration

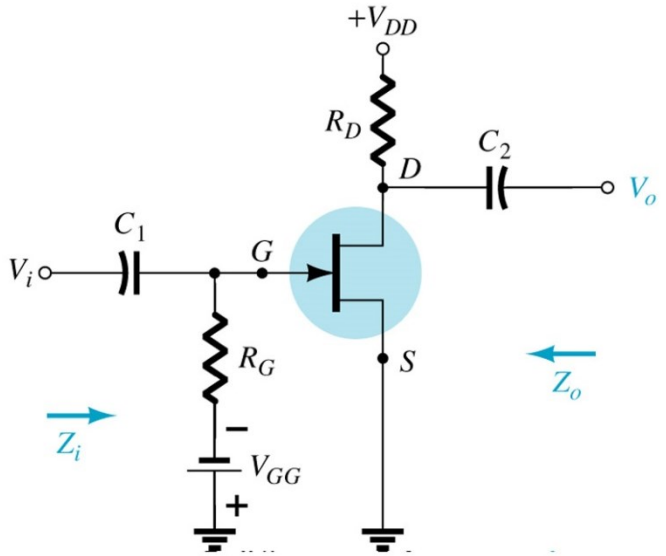
$Z_i = R_s//[(r_d+R_D)/(1+g_m r_d)] \quad \approx R_S//(1/g_m)$ when $r_d > 10R_D$

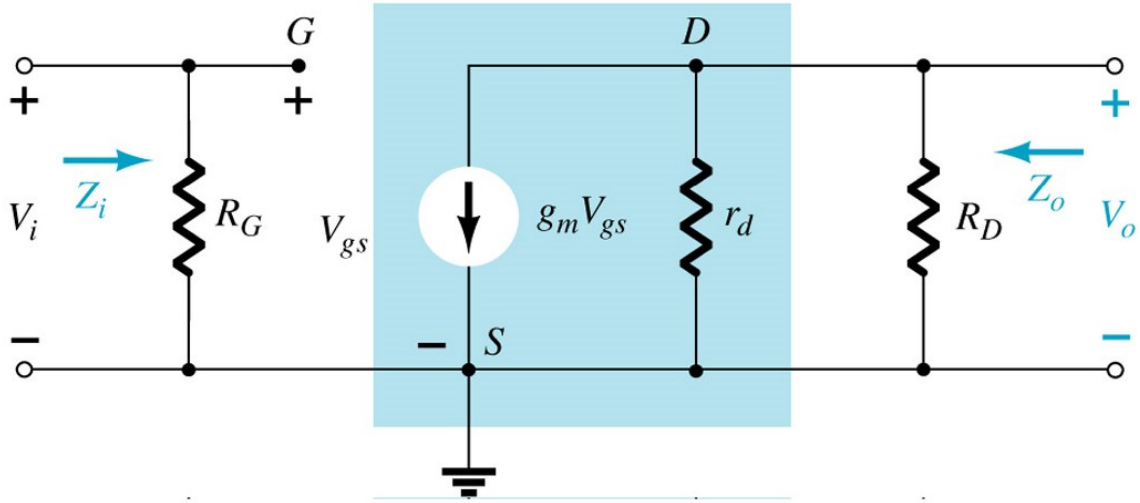
$Z_o = r_d//R_D \quad \approx R_D$ when $r_d > 10R_D$

$A_V = [g_m R_D + (R_D/r_d)]/[1+ R_D/r_d] \quad \approx g_m R_D$ when $r_d > 10R_D$

3. FET small-signal amplifier

3.3. Common-Source configuration





3. FET small-signal amplifier

3.3. Common-Source configuration

$Z_i = R_G$

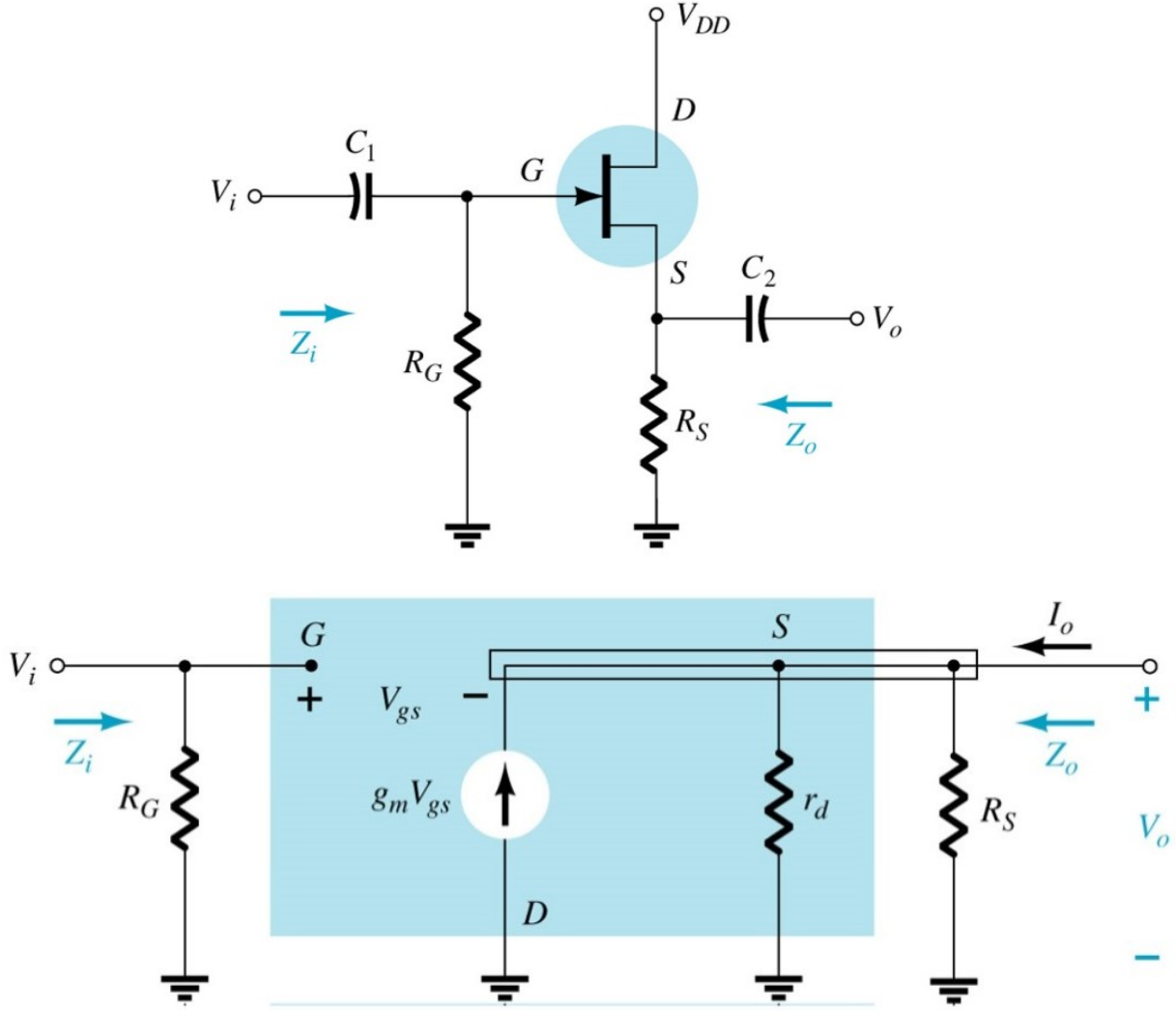
$Z_o = r_d // R_D \approx R_D$ when $r_d > 10R_D$

$A_V = - g_m(r_D // R_D) \approx - g_m R_D$ when $r_d > 10R_D$

V_i & V_o are in reversed phase

3. FET small-signal amplifier

3.4. Common-Drain configuration



3. FET small-signal amplifier

3.4. Common-Drain configuration

$Z_i = R_G$

$Z_o = r_d // R_S // (1/g_m) \approx R_S // (1/g_m)$ when $r_d > 10R_S$

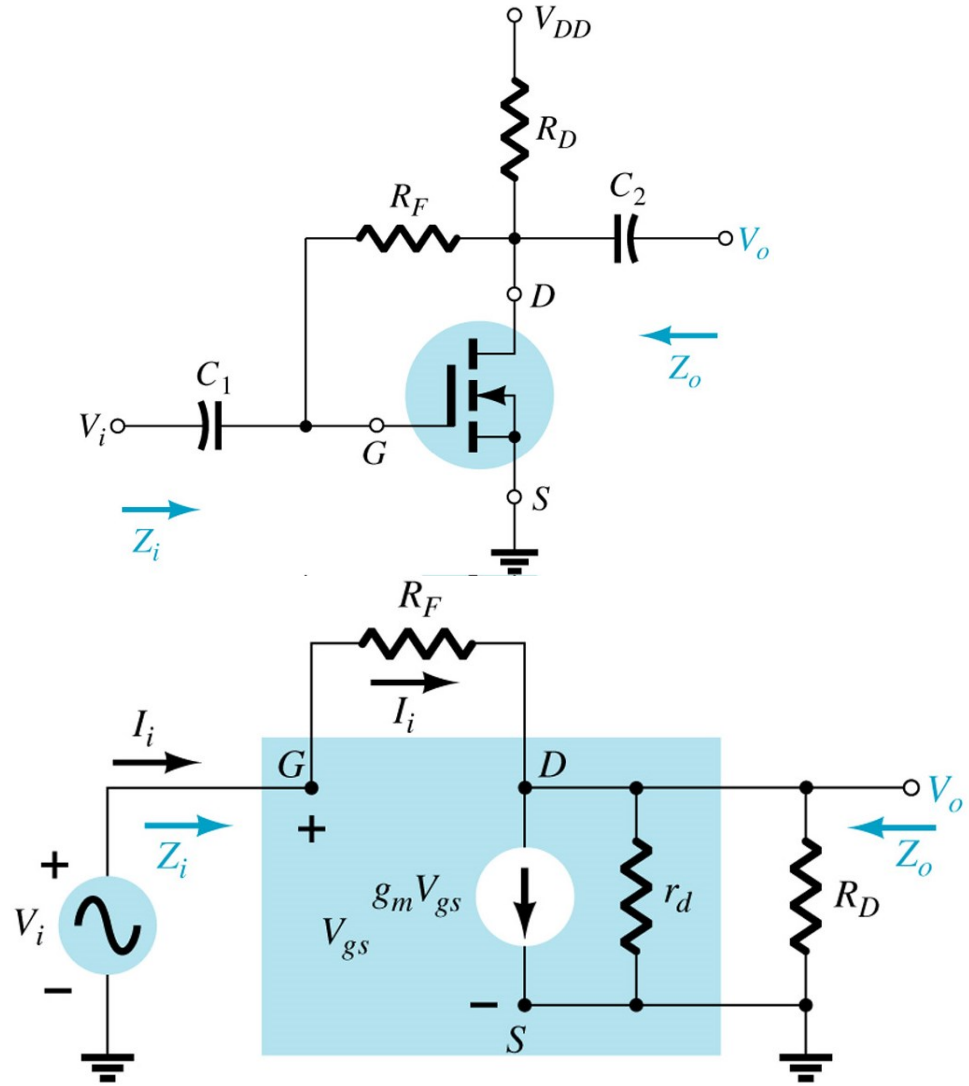
$A_V = -g_m(r_d // R_S)/[1+g_m(r_d // R_S)]$

$\approx g_m R_S/[1+g_m R_S)]$ when $r_d > 10R_S$

≈ 1 when $g_m R_S >> 1$

3. FET small-signal amplifier

3.5. Common-Source configuration with EMOS



3. FET small-signal amplifier

3.5. Common-Source configuration with EMOS

$$Z_i = (R_F + r_d // R_D)/[1+g_m(r_d // R_D)]$$
$$\approx R_F/(1+g_m R_D) \qquad \text{when } r_d > 10R_D,\ R_F >> r_d // R_D$$

$$Z_o = R_F // r_d // R_D$$
$$\approx R_D \qquad \text{when } r_d > 10R_D,\ R_F >> r_d // R_D$$

$$A_V = g_m R_F // r_d // R_D$$
$$\approx g_m R_D \qquad \text{when } r_d > 10R_D,\ R_F >> r_d // R_D$$

Summary

1. **Transfer characteristic** equation shows a **nonlinear** relationship between the gate-to-source voltage and the drain current of a FET device.
2. A **very large input impedance** between the gate and the source allows that the gate current is zero.
3. The **trans-conductance *gm*** is determined by the ratio of the change in drain current associated with a particular change in gate-to-source voltage in the region of interest.
4. The **magnitude of voltage gain** of FET networks, except the common-gate configuration, are typically between 2-20 times, normally lower that the BJT networks.
5. The **input impedance** for most FET configurations is quite high, except that it is quite low for the common-gate configuration.

Next lesson guide…

Lesson 4: Effect of Load & Source Resistance

Reference

Electronics devices and Circuits theory – Robert Boylestad, Louis Nashelsky, Prentice Hall, 11th edition

Electronic principles – Albert Paul Malvino