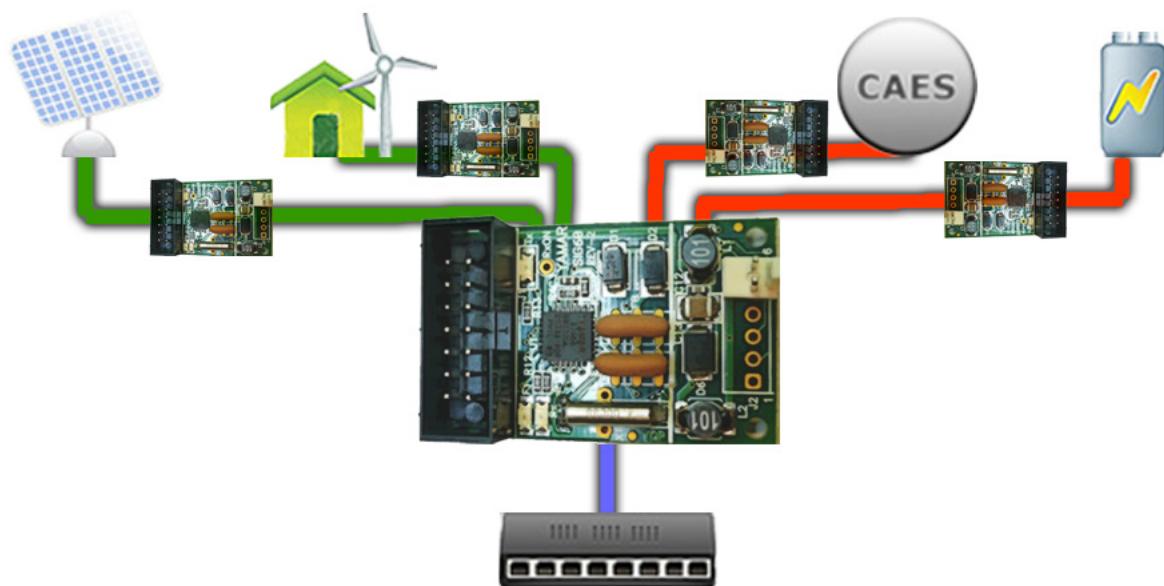


# EPRO 3 & 4

## PLC - Hardware Interface

### Renewable Energy System

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# Chapter 1

## Introduction

This document describes the process of making a common hardware interface for powerline communication (from here on referred to as PLC), the interface is going to be used by all teams. This includes selection of which chip to use, prototyping and development of the PCB.

### 1.1 History

14-12-2011: V0.1 Initial document copied from the wiki<sup>1</sup>

26-02-2012: V0.2 Added functional test of the prototype

27-02-2012: V0.3 Redesign section of the PCB added.

27-02-2012: V0.4 Redesign section 2 and 3 added. End test section begun and setup of the system documented.

29-03-2012: V0.5 Finished describtion of end test. Plus several minor corrections.

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<sup>1</sup>[http://e10.ede.hih.au.dk/index.php/HW\\_Interface\\_PLC#Device\\_Comparison](http://e10.ede.hih.au.dk/index.php/HW_Interface_PLC#Device_Comparison)

# Chapter 2

## Finding a Device

One of the first things to decide was which IC to use for the powerline communication. This chapter describes the thoughts and considerations which was taken into account when settling for an IC for the project.

### 2.1 ST

Suggestion from Ulrich: PLC device from ST interfacing through SPI or UART<sup>1</sup>

### 2.2 Yamar

Kristian has contacted Yamar about their PLC module with CAN interface which will be perfect for the system as CAN has a lot of build in features like: ID handling, checksum, variable data length etc. also we might be able to use some of the code from E09<sup>2</sup> as they used CAN between their modules. Unfortunately the devices is still only on a prototype state<sup>3</sup>

#### Mail correspondence with Yamar

Hey

We are considering using the DCAN250 in a product, but we need some additional data about it, besides the overview available on the website. So could you please send a datahseet about both the DCAN250 and the DCAN250 evaluation board. We would also like to get the prices of both the DCAN250 and the DCAN250 evaluation board.

Regards Kristian Rahbek

Hello Kristian

Thank you for the Email.

The DCAN250 is available only as FPGA board that is used by our customers for testing. ASIC will be late next year. Meanwhirl I would like you to consider to use of the SIG60 devices for UART/LIN communication at speeds up to 115Kbps.

Evaluation boards and devices areavaialble from stock.

For pricing, I need the full address.

Regards,

To not risk using an unstable device, the DCAN was scraped. After some more research and conversations with the other groups, it has been decided to run SPI or UART instead of CAN as interface to the PLC PHY. The devices mentioned by Yamar is fortunately the same as the ones used in the wind-turbine racer. Thomas Baltzer from E09 has been contacted and luckily he had 3 modules available, so a small test setup could be made <sup>4</sup>. the SIG60 can be setup to work both as a master or a slave. Another device from Yamar is working only as a slave in a network with a SIG60 as the master<sup>5</sup>

The SIG61 does however only work as a dummy device, where the communication to it is handled over the Power Line via. a SIG60. In practice this means that the SIG60 can set some output pins on the SIG61 high or low

<sup>1</sup>[http://www.st.com/internet/imag\\_video/product/130228.jsp](http://www.st.com/internet/imag_video/product/130228.jsp)

<sup>2</sup>The class one year above us, which have been working on the same project, but with slighlty different requirements.

<sup>3</sup><http://www.yamar.com/dcan250.php>

<sup>4</sup><http://www.yamar.com/sig60evel.php>

<sup>5</sup><http://www.yamar.com/sig61.php>

or read some input pins, the SIG61 do not have any UART port so it isn't really suited for communicating with any microprocessor board. The SIG60 and SIG61 datasheet is available on YAMAR's website<sup>6</sup>

Ulrich has contacted Yamar with regard to the SIG60 evaluation boards. These does however cost 1100 Euro for 4 devices. Now he is trying to get some prices on single devices. If they are much cheaper (which they hopefully are) Kristian and Dennis will make a PCB layout similar to the evaluation board from Yamar, and provide each team with this.

## 2.3 Device Comparison

To be able to select the best device for the system, a comparison between the different devices has been made. Only two devices have been found interesting: SIG60 & ST7540:

	Max Speed (BPS)	Band in use detection	Interface	Price	Duplex	Supply voltage	Dev board
Yamar SIG60	115200	Yes	UART / LIN	60dkr (plus 375dkr shipping from Yamar)	Half	3.0-3.6V	2000dkr (from Yamar)
ST7540	4800	Yes	UART / SPI	75dkr (plus shipping rom ST)	Half	7.5-13.5V	3000dkr (from Farnell)

Table 2.1: Comparison table

Another difference between the modules is the way they communicate on the power line and the way of writing to their registers. These informations are however subordinate.

### 2.3.1 Speed

There's a significant difference is the speed of the devices. A rough estimation have been done saying that 20 characters are transmitted between two modules to send a command and respond with a command. With 10 modules it gives approximately 200 characters sent. With a baud rate of 4800 the hub can send and receive 24 packages per second from each module.

### 2.3.2 Interface

On the team meetings it has been decided to use UART and implement our own protocol.

### 2.3.3 Supply Voltage

The EA board is supplied from a usb cable or a 9-15 volt supply. A regulator on the EA board feeds the ARM processor with a 3.3V supply. In other words, the ST device can be supplied form the same supply as the EA board and the Yamar device can be supplied from the same source as the ARM processor. So non of the two devices needs a seperate power supply circuit in order to work.

### 2.3.4 Development Boards

In order to get something up and running as fast as possible it could be a good idea to have a development board, to be sure how to configure the device before making a PCB. The ST dev board is more expensive, however 3 development boards for the SIG60 are left from the Wind-turbine racer project which we have been able to borrow.

<sup>6</sup><http://yamar.com/>

### 2.3.5 The device chosen

The Yamar SIG60 has been chosen. The difference between the two devices is insignificant, but as the Yamar devices could be found "on the shelf" it was chosen.

## 2.4 HW Setups

### 2.4.1 First setup with an MBED

The first small setup with PLC working is up and running. Two SIG60 evaluation boards have been used, two MBED's, a fan to make some noise on the powerline and a PC to send and receive data. The video is uploaded to youtube and can be found here<sup>7</sup>

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<sup>7</sup><http://www.youtube.com/watch?v=G120aoARFeI>

# Chapter 3

## Design

### 3.1 Power supply

We want to be capable of using two different FPGA boards, Spartan 3A and Atlys Spartan 6. Some groups may want to use the Beagle board. Below is a list which shows the power requirements for the different boards the groups might want to use.

Board	Voltage	Current	Notes
Spartan 3A	5V	50mA	
Spartan 6	5V	+4A	With everything enabled
Arm7 Board	5V or 12V	325mA @ 5V	With display enabled. Can be supplied from a 5V or 12V connection
Arm7 Board	5V or 12V	215mA @ 5V	With display disabled. Can be supplied from a 5V or 12V connection
Beagle Board	5V	750mA	
Sig 60 IC	3.3V	50mA	

Table 3.1: Power requirements of the boards which might be used

All the boards above can be supplied from a 5V supply, the sig 60 IC needs a 3.3V supply fortunately the Arm 7 board has an onboard 3.3V voltage regulator. The idea is to make a 5V power supply on the powerline board which is capable of supplying all the boards the teams might want to use. The powerline module is then powered from the 3.3V output of the Arm 7 Board, see figure 9.1. Based on the above requirements the powersupply should be capable of delivering a minimum of 5.2 A. To meet this requirement it has been chosen to use a A4403 IC. It's capable of delivering 3A in 5V, this will be enough power for most of the groups but a few might need more power in order to supply all their boards. In order to meet this demand there's made room for two A4403 based power supplies, these are connected in parallel. Each group then has to decided on there own if they want to solder both power supplies onto the PCB, giving them a maximum of 6A, or they can settle for one if 3A is enough.

#### 3.1.1 Thermal considerations

Figure 3.1 below a shows the efficiency of the A4403. The maximum efficiency is about 85 %. This means that when sourcing 3A from the IC approximately 2.25 W of power will be dissipated in the IC. Consequently a lot of heat will be generated when sourcing big currents.

$$(1.00 - 0.85) * 3A * 5V = 2.25W$$

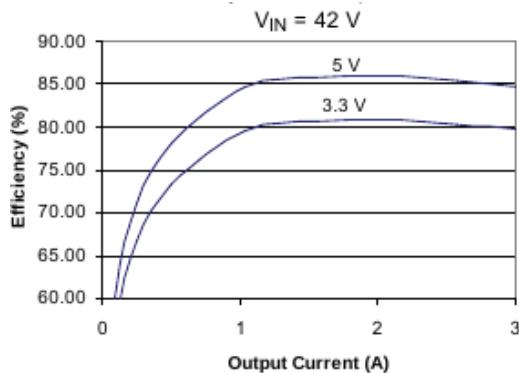


Figure 3.1: Efficiency versus output current

In the datasheet it's suggested to use a PCB with high thermal efficiency, and several vias (approx 4 to 8) should be used to connect the thermal pad of the IC to the internal ground plane. This should be done to stay within a safe operating temperature. The A4403 is a smd component unfortunately we don't really have the possibility of making vias beneath the smd. It has been attempted to meet this suggestion by drilling a small hole in the PCB where the A4403 is located and filling this with solder paste before the board was put in the solder oven.

The circuit is the typical application as found in the datasheet no changes have been applied. All components used in the circuits are from the series recommended in the datasheet.

## 3.2 PLC

The design of the powerline circuit has been taken directly from the application note. The only change is that the connector is changed. Some of the pins which were connected to the connector has been made as jumpers instead, since we don't need to access them from software. The pins in question is:

**Pin 16 -F1nF0** Channel select, high = F1, low = F0

**Pin 17 - HDC** Change between data and command mode, low to write to internal registers

## 3.3 Interface

Direction	Pin	Description
Input	1	Gnd
	2	3.3V supply
	3	nSleep, low to go to sleep mode
	4	nReset
	5	wake, edge-triggered wakeup device and send wakeup message
	6	HDI - uart rx
Output	7	HDO - uart tx

Table 3.2: Connector interface for PLC board

All input and outputs are compatible with 3.3V CMOS logic.

# Chapter 4

## Test and verification

### 4.1 Functional test

This section describes the initial functional test of the prototype. Based on the test results and observations some fixes were made and ported to the final version of the PLC module. The test of the prototype is divided into two tests, a test of the powerline-communication function and a test of the power supply.

#### 4.1.1 Communication

##### 4.1.1.1 Setup

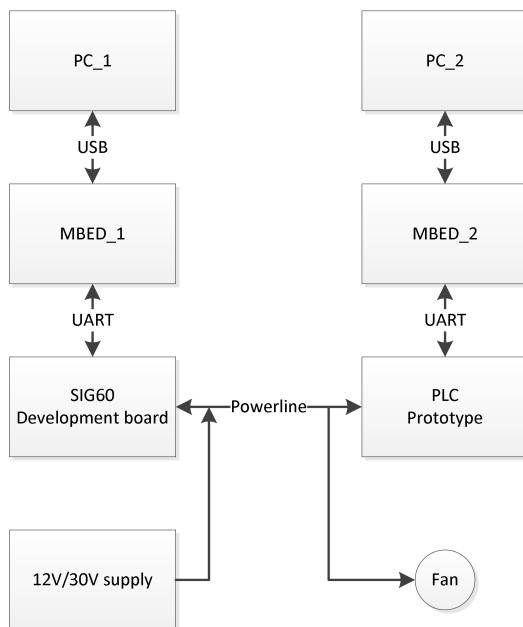


Figure 4.1: Setup for testing the communication

Figure 4.1 shows the setup which was made in order to test the communication between the two modules. The mbeds were setup as a gateway between the PCs and the PLC modules. Mbed\_2 were connected to the prototype and Mbed\_1 to a development board based on the SIG60. The test was carried out by sending some text from a terminal program on one of the PC's to the other PC, this test was made in both directions. The test was made two times. First with no power supply and no fan connected to the powerline, and afterwards with the power supply and fan connected, the fan was connected in order to introduce some noise on the line.

##### 4.1.1.2 Results and observations

As default the sig60 is setup to loopback data, so whenever it receives something it should loop the data back no matter if it successfully transmitted the data to the powerline or not. At the first attempt to send data over powerline the prototype didn't loopback the data as expected. It showed out that this was caused by a short of the oscillator.

After this fix the communication still didn't work so after taking a close look at the application note it showed out that we missed a  $18\Omega$  resistor in series with the 4 bas70 diodes and we missed a  $18\Omega$  resistor in series with the TxO pin.

After these fixes the prototype successfully transmitted and received data over the powerline. When the fan was connected to the powerline some errors did however occur, the prototype board received some random characters especially when touching the PCB track between the two filters. The noise was dramatically decreased by connecting a termination resistor of  $100k\Omega$  from this track to ground. From this point on only a few transmitting errors were seen and they only occurred when trying to send a lot of data in both directions simultaneously. This is however not optimal, therefore the filter circuit has to be redesigned with shortened tracks and components placed closer to the power line device.

Various Small fixes:

- Rearrangement of rtx/tx diode

#### 4.1.2 Power supply

##### 4.1.2.1 Setup

The power supply was tested by connecting it to a variable power resistor and measuring the current through it and the voltage over the output. The two focus areas under the test was to test if the supply is capable of delivering 3A as it is supposed to without overheating and to test that the voltage remains stable under different load conditions.

##### 4.1.2.2 Results and observations

With no load connected the output voltage was 5.3V the resistors used in the feedback loop isn't very accurate so it was expected that there would be some offset. As the load resistance was decreased the voltage rose, at an output of 2.2A the voltage had risen to 6.3V. At an output of 2.4A the supply did withstand for approximately a minute before the thermal protection built into the IC shutdown the power supply. A ripple voltage of 400mV was measured at 1.8 A.

It was expected that the supply would become hot to actually deliver 3A. Underneath the A4403 IC there's supposed to be between 4 and 8 vias connecting the thermal pad to ground in order to dissipate the heat. These vias does however not exist on the prototype.

The unstable voltage output is not very satisfying so a few fixes were made before another test was carried out. The distance between the parallel coupled resistor and capacitor in the feedback loop was shortened, and the feedback loop was shortened by soldering a wire directly from point to point. Finally the resistor connecting the feedback loop to ground was relocated in an attempt of making a better ground connection. After these fixes the voltage output when the supply isn't loaded is 4.5V and it dropped to 4.1V at 2.1A. Generally the IC also seemed to be cooler than before. The changes made the output voltage more stable although an explanation to why the openloop voltage changed from 5.3V to 4.5V wasn't found. Later on it came to our attention that we had been measuring the output voltage at the end of some rather long wires so the error is probably less because of the voltage drop over the wire.

# Chapter 5

## Redesign 1

### 5.1 Power Supply

As described the supply was unstable when loaded, however the shorter feedback track minimized the offset. In the new version the layout of the power supply have been rerouted to shorten especially the feedback track. In general all components have been moved closer to the switch mode device, to decrease the effect loss in long PCB tracks. Beside that several vias have been added to the ground plane around the device for better heat dissipation.

The prototype was built based upon the application note in the datasheet. This was revision 2, along with the sig60 ICs Yamar send a revision 3.1 of the application note. According to Yamars Rev3.1 document two new resistors have been added

An error from the first version was *Agnd* which was not connected to the ground plane, this have been fixed in the newest version.

### 5.2 PLC

On the second version of the PCB, the focus have been on placing the filters and the crystal as close to the SIG60 device as possible. In general all components have been placed closer to the device. The track to the output pin (power line) has been shortened very much, so all the noise from the communication is not routed by the power supply.

The way the *receive LED* was mounted, the diode was lighting up all the time, except for the few micro seconds it received something from the CPU. The LED has instead been connected to a separate LED pin on the device.

### 5.3 Component footprint

- The LED footprint was wrong, it have been changed to the right type.
- The area between the pads on the inductor footprint made the inductors short-circuit to ground, more pad have been added to the footprint.
- Bigger copper plane have been made for the through hole components (filters + pins).
- Ground plane is moved away from the devices footprints, as the plane was moving the components during soldering in the oven because of the surface tension. This fix ensures an equal drag from all sides.

## 5.4 Diagrams and Layout

In this chapter the state of the schematics and PCB layout after the fixes above can be seen.

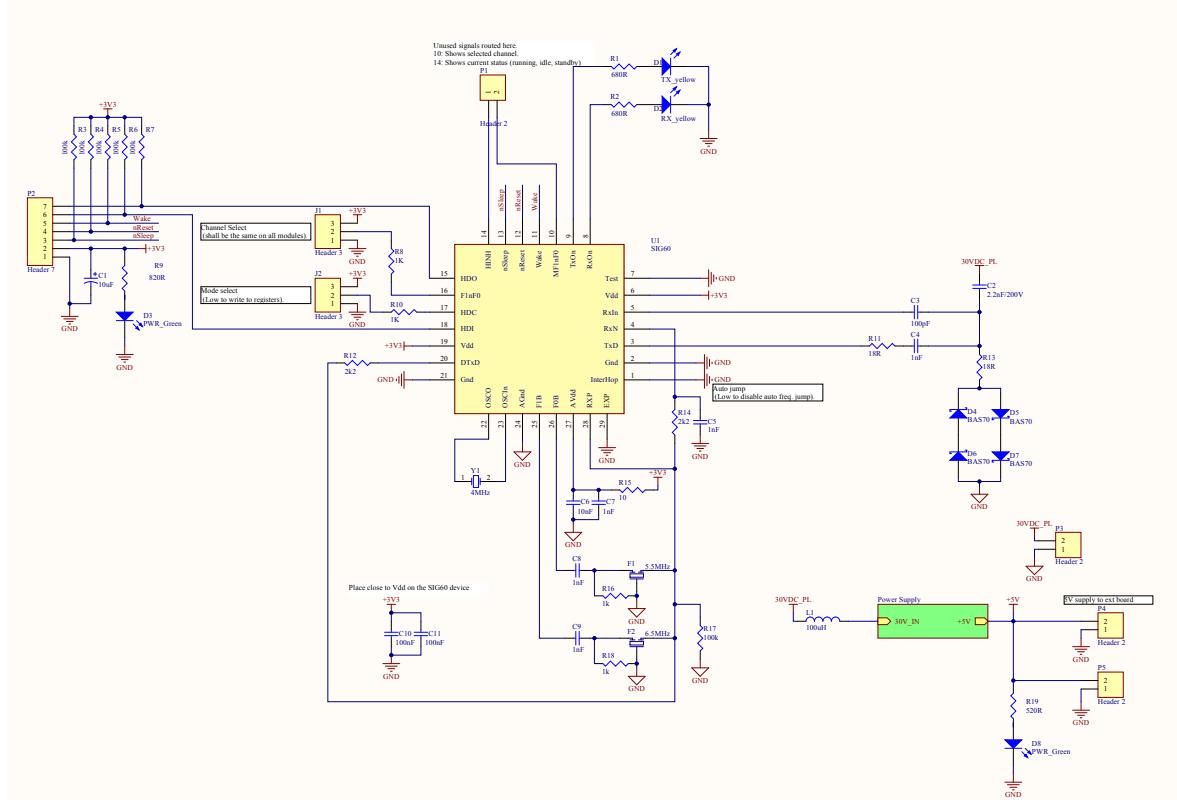


Figure 5.1: Power line circuit version 0.2

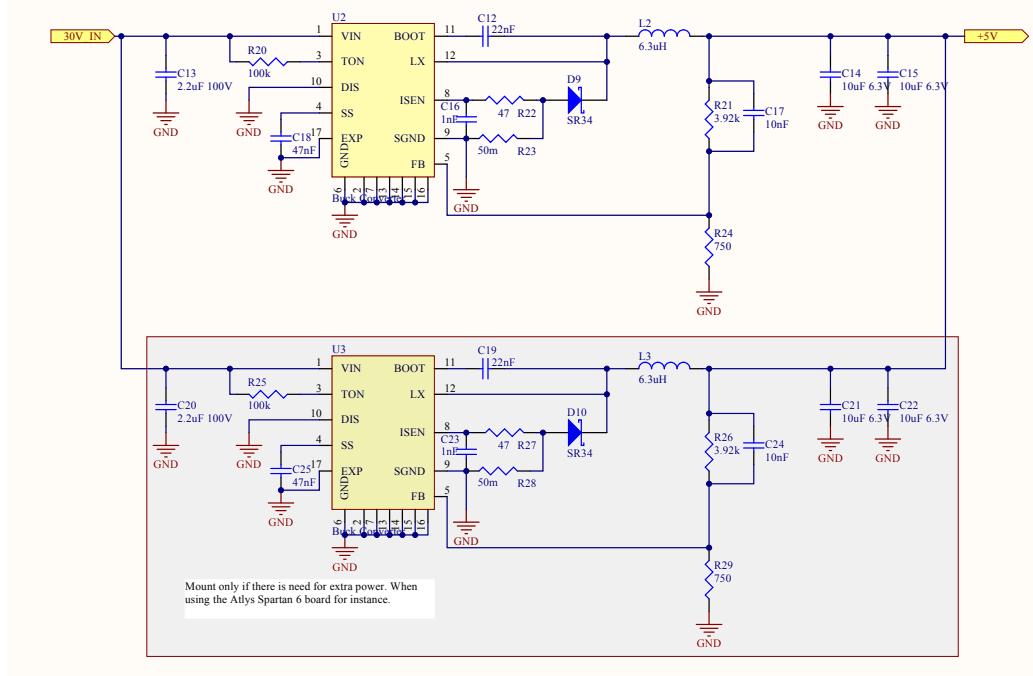


Figure 5.2: Power supply. 2 x 5 volt 3 ampere version 0.2.

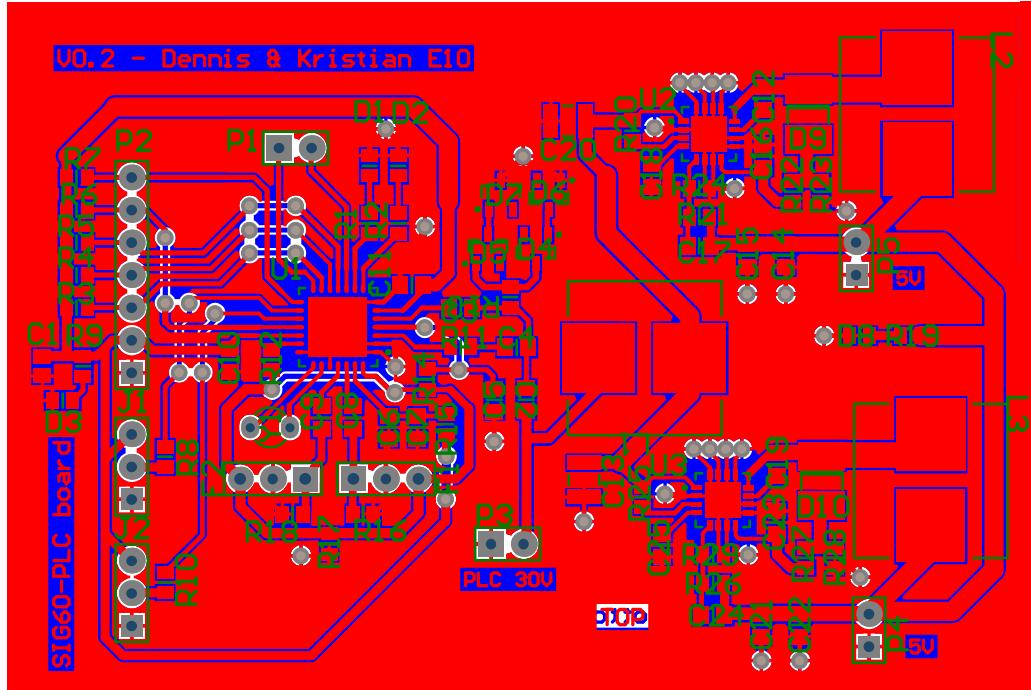


Figure 5.3: PCB layout of the power line circuit and the 5 volt power supply version 0.2.

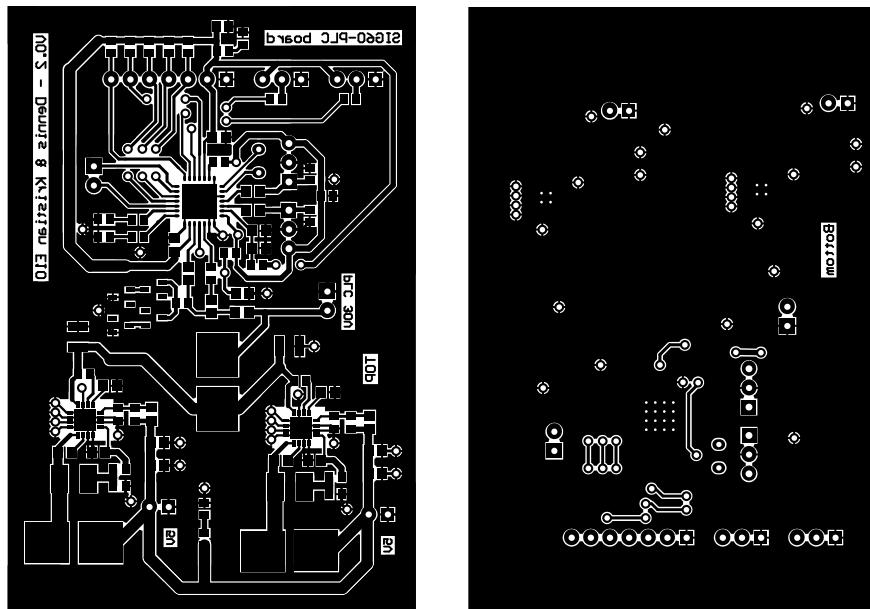


Figure 5.4: PCB layout, top and bottom

# Chapter 6

## Redesign 2

The changes from v0.2 to v0.3 is mostly that clearance between the tracks have been increased to 10 mil, as there was problems with short-circuits a lot of places.

### 6.1 Power Supply

No changes.

### 6.2 PLC

No changes.

### 6.3 Component footprint

No footprints changed.

### 6.4 Diagrams and Layout

Below is the state of the schematic and PCB layout after the second redesign.

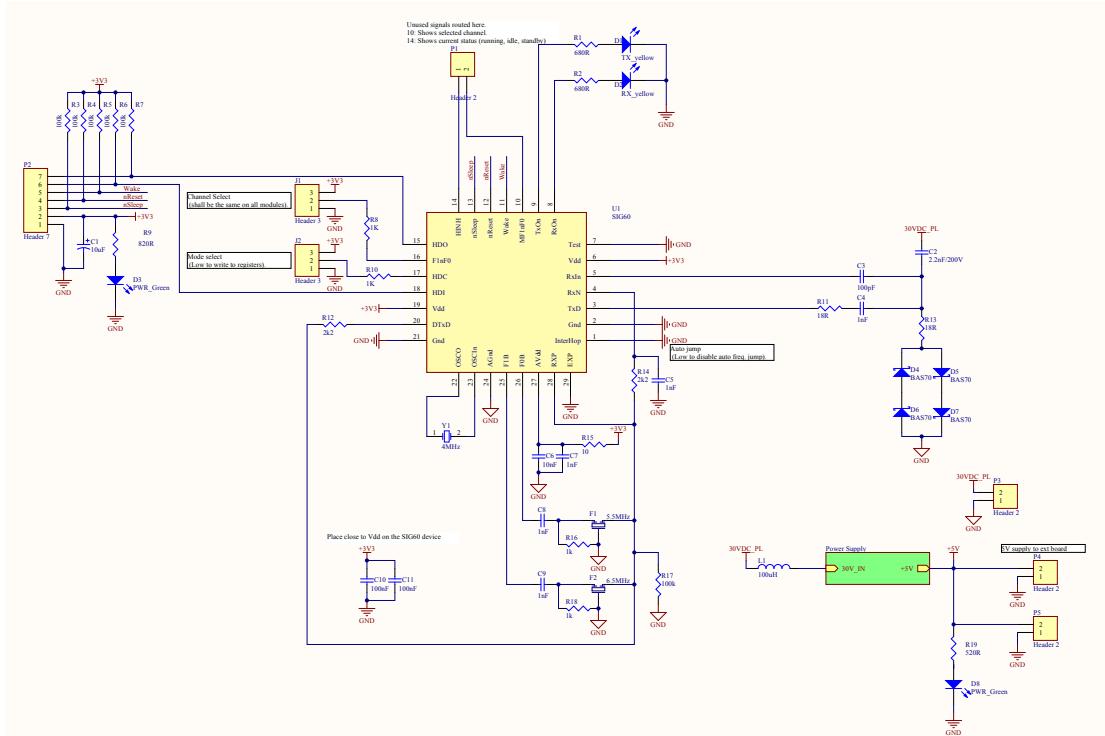


Figure 6.1: Power line circuit version 0.3

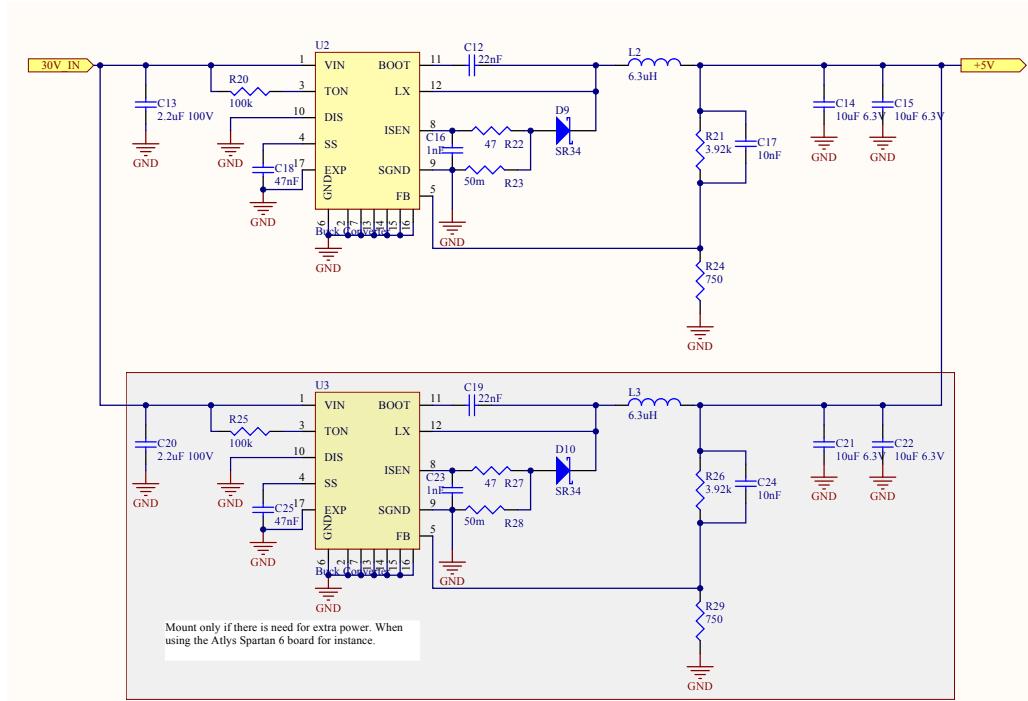


Figure 6.2: Power supply. 2 x 5 volt 3 ampere version 0.3.

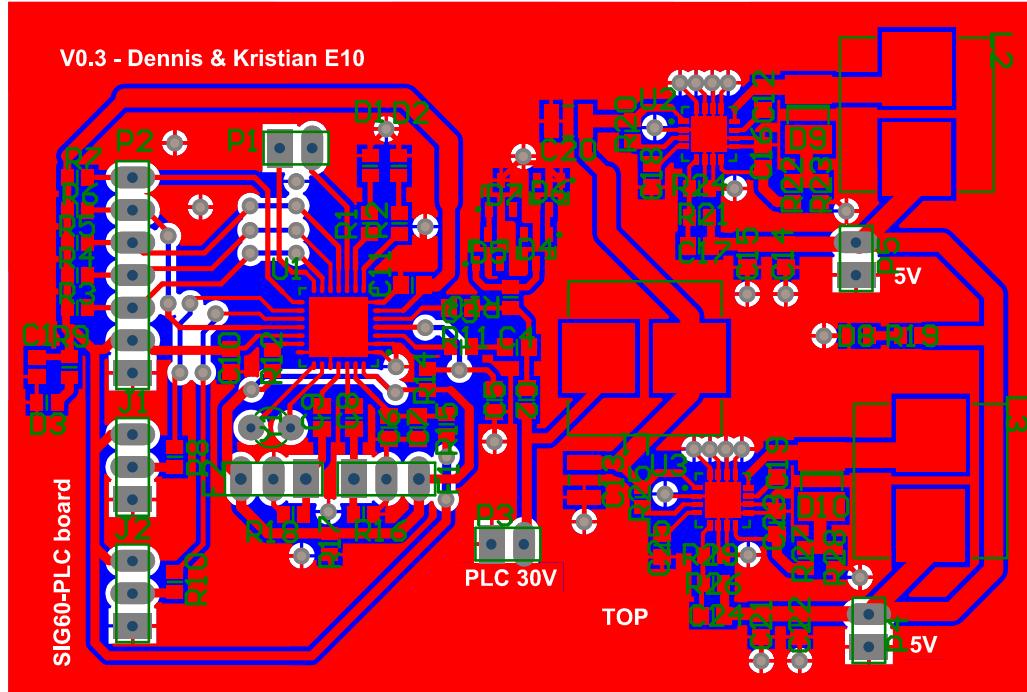


Figure 6.3: PCB layout of the power line circuit and the 5 volt power supply version 0.3.

# Chapter 7

## Redesign 3

There's only one small change in this redesign.

### 7.1 Power Supply

No changes.

### 7.2 PLC

The rx diode is turned and the anode is connected to 3.3 volt instead of ground.

### 7.3 Component footprint

No footprints changed.

### 7.4 Diagrams and Layout

Below is the final version of the schematic and PCB layout.

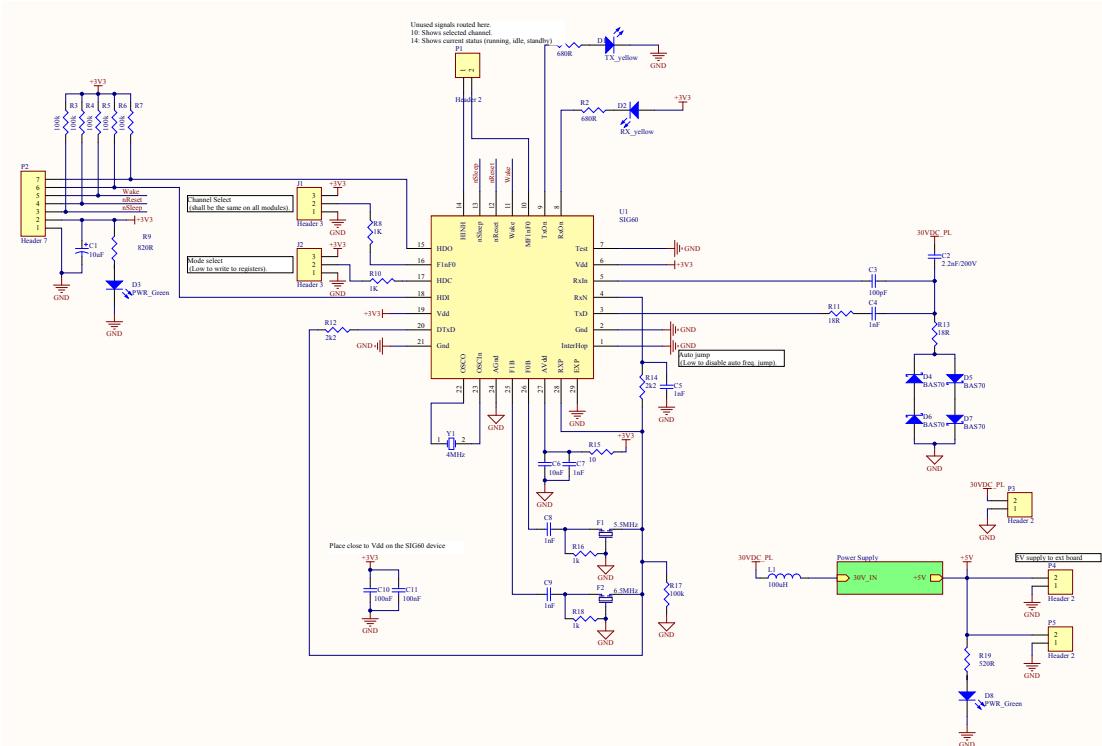


Figure 7.1: Power line circuit version 0.4

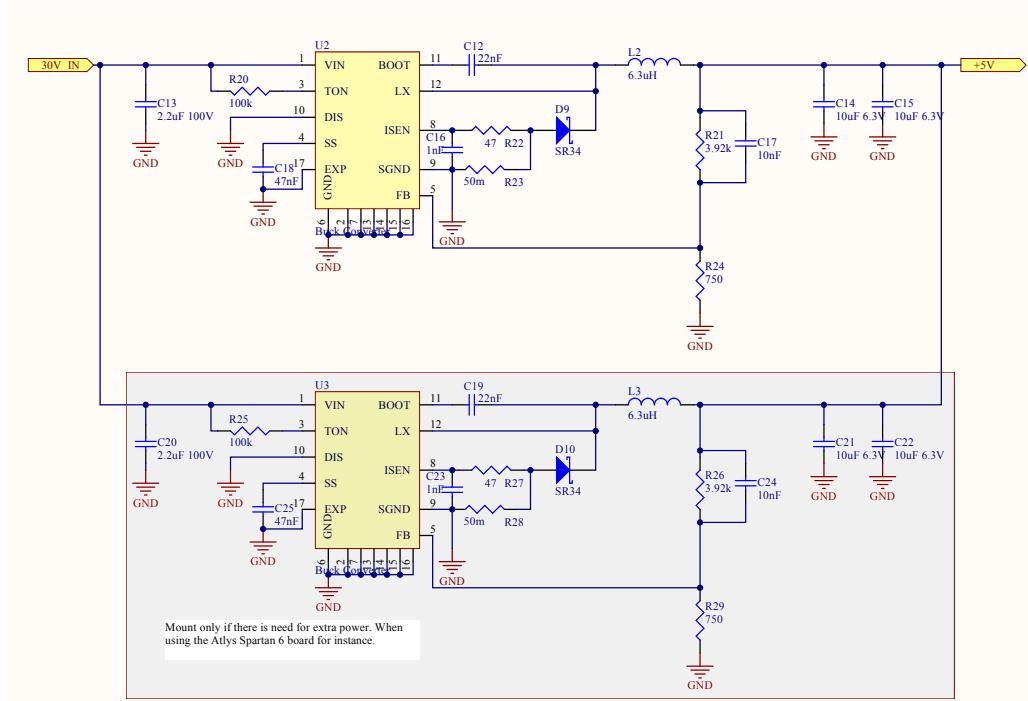


Figure 7.2: Power supply. 2 x 5 volt 3 ampere version 0.4.

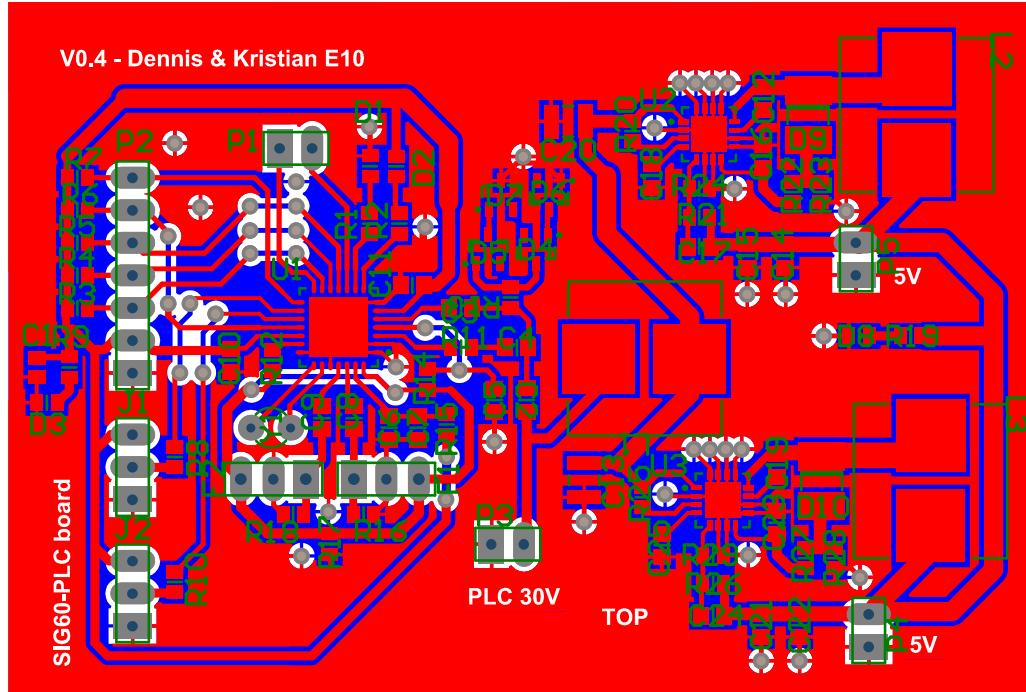


Figure 7.3: PCB layout of the power line circuit and the 5 volt power supply version 0.4.

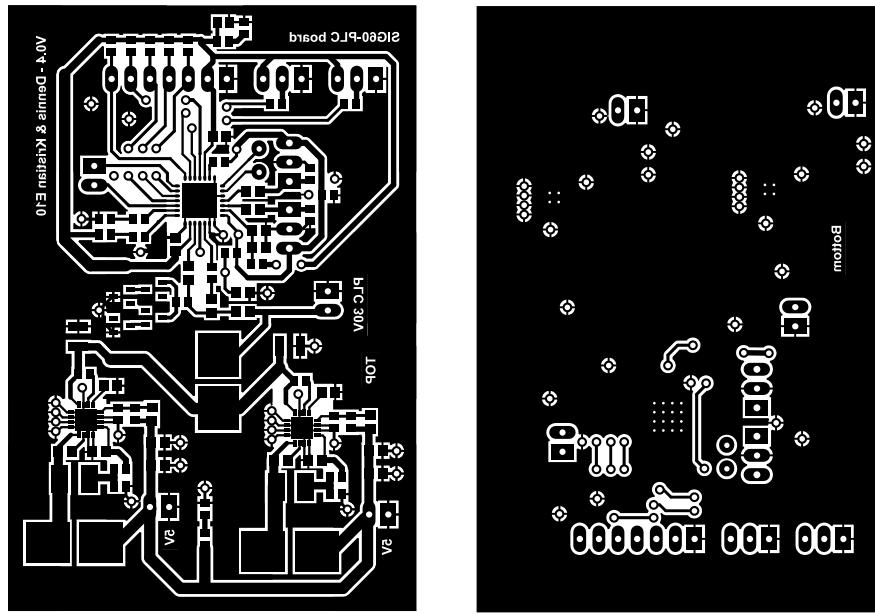


Figure 7.4: PCB layout, top and bottom

# Chapter 8

## End Test

After finishing the prototype phase of the development 6 PLC modules was made one for each team. All of these modules have been tested by the procedures described below, the final test of the modules was carried out in the same way as the initial test of the first prototype as described in chapter 4.

### 8.1 Power Supply

Once again the power supply was connected to a variable power resistor and the current and voltage output was measured. This time the voltage was measured directly at the output pins on the board to avoid any errors caused by a voltage drop over the long wires as opposed to the measurements of the first prototype. Below is a list of the results. The supply has been at each load level for a period of 2 minutes to verify whether it runs hot or not at that load.

0 Amp: 4.96

1 Amp: 4.93

2 Amp: 4.90

2.2 Amp: 4.895

2.3 Amp: 4.888

2.4 Amp: 4.888

When increasing the current further an audible noise was introduced from the coils so the test was stopped. These results clearly shows that the fixes which was made to stabilize the supply voltage have worked nicely. At 2.4 A the supply gets pretty hot but its not overheating.

### 8.2 Communication

The communication was tested in the exact same way as in the initial test of the first prototype. See figure 4.1 for the test setup. Data was sent in both direction between the two PCs for 15 minutes without encountering any errors. This was done while the fan was connected to the powerline in order to get some noise on the line.

# Chapter 9

## Setup

This chapter is a quick guide about how to setup the board.

### 9.1 Power Supply

The overall setup for routing of the supply wires is:

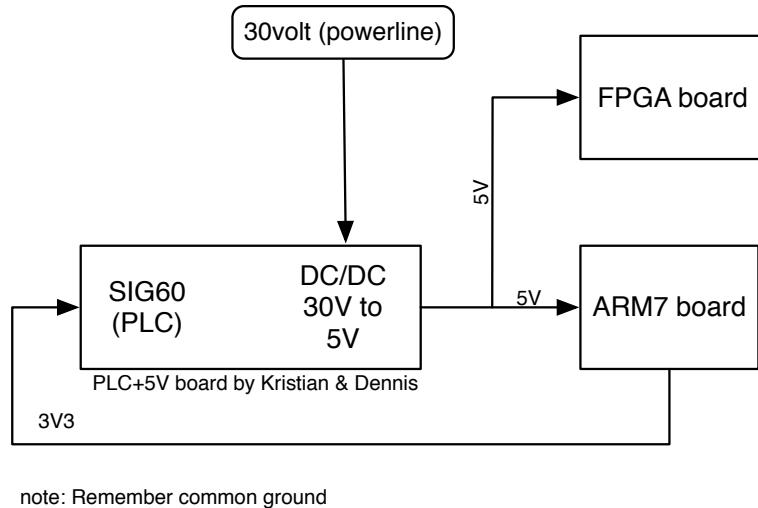


Figure 9.1: Power connection between the different circuit boards in each device.

This setup has been chosen to decrease the amount of DC/DC converters needed in the system.

### 9.2 PLC

The board have 2 jumpers, 5 signal wires to the ARM board and two pins that is not to be used (just mounted in case these signals should be used).

**Inputs to the board from the processor:** Rx, Wake, nReset, nSleep.

**Output from the board to the processor:** Tx.

The select channel jumper shall be placed equal on all boards that wants to communicate with each other (auto jump is turned off on all modules and cannot be turned on).

Mode shall be in normal all the time, except when a write to the internal registers is performed. It is only necessary to write to the internal registers when changing the setup of the SIG60.

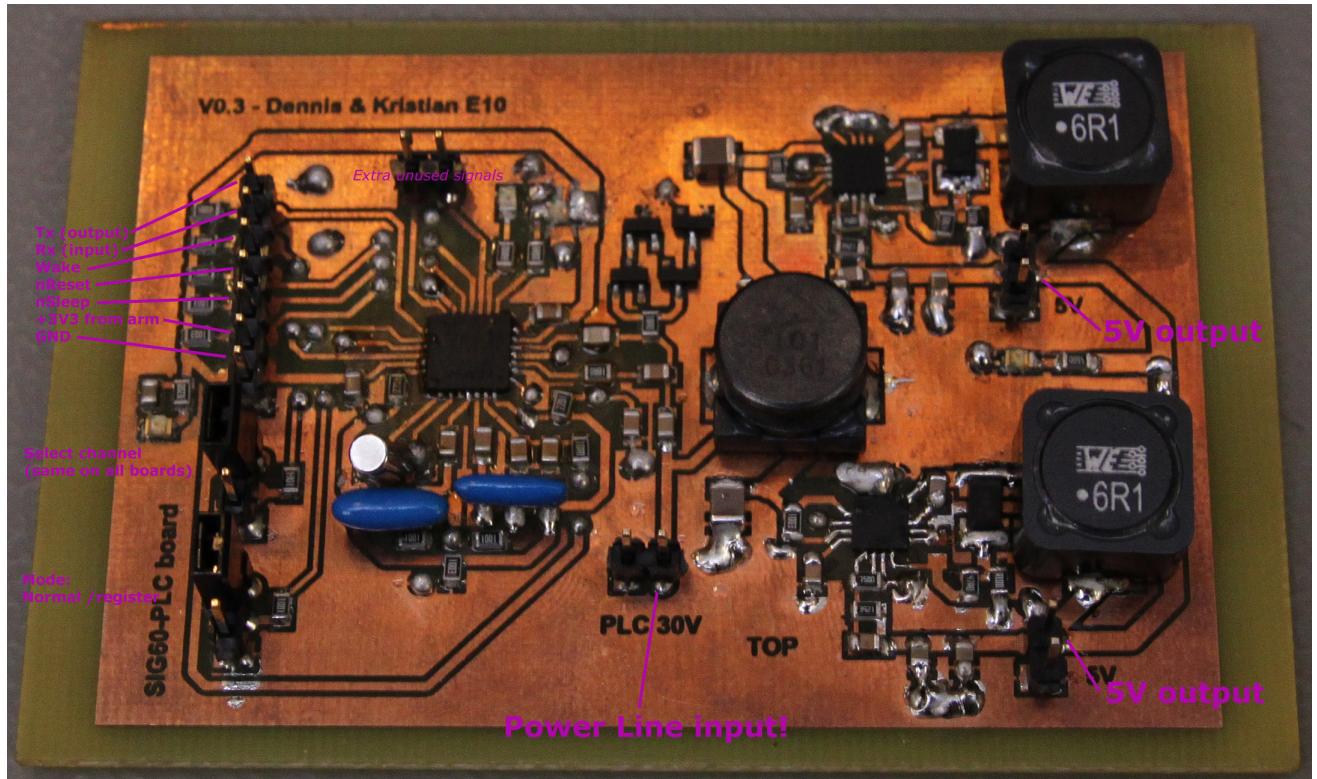


Figure 9.2: Picture of the final board with explanation text.

*Note: v0.3 and v0.4 is similar except a diode that has been turned.*

The interface between the ARM processor and the SIG60 PLC device is handled out through UART2 in the test code.

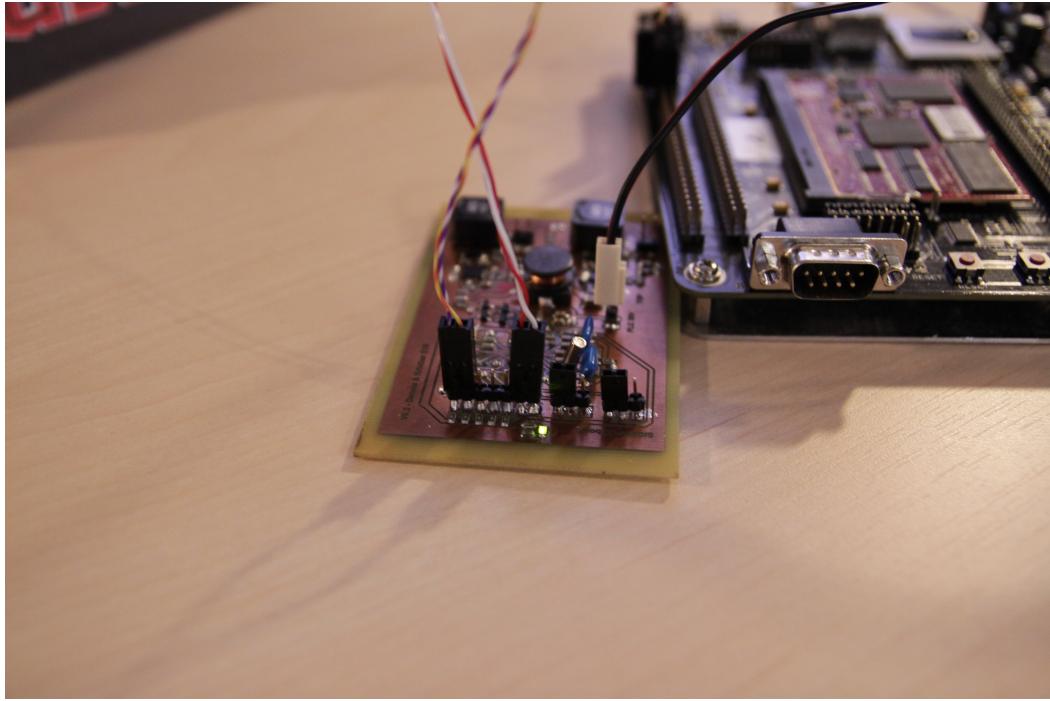


Figure 9.3: Communication between PLC and ARM.

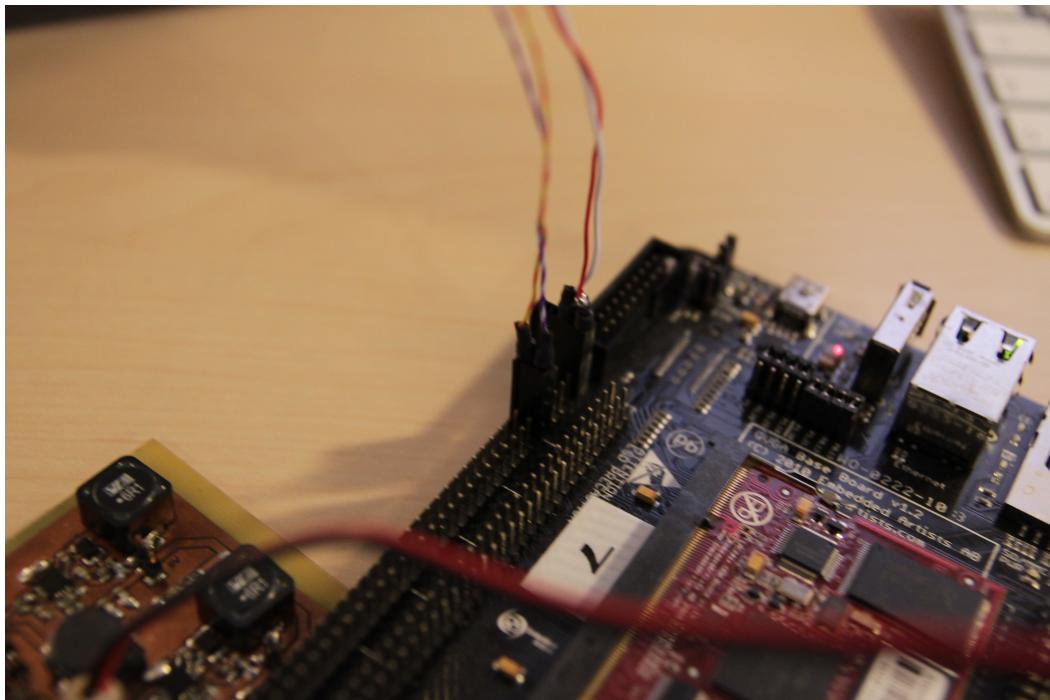


Figure 9.4: Communication between PLC and ARM. UART2 is used

Unfortunately it was not able to upload the test code used to the wiki page. If you need it, please email Dennis Madsen from E10. The code is basically the UART loop (exercise 2) from Mortens Opprud Jacobsens class last semester which has been slightly modified.

# Chapter 10

## Appendix

Yamar v2 datasheet

Yamar v3 diagram and pcb layout

Switch mode device datasheet with diode and inductor