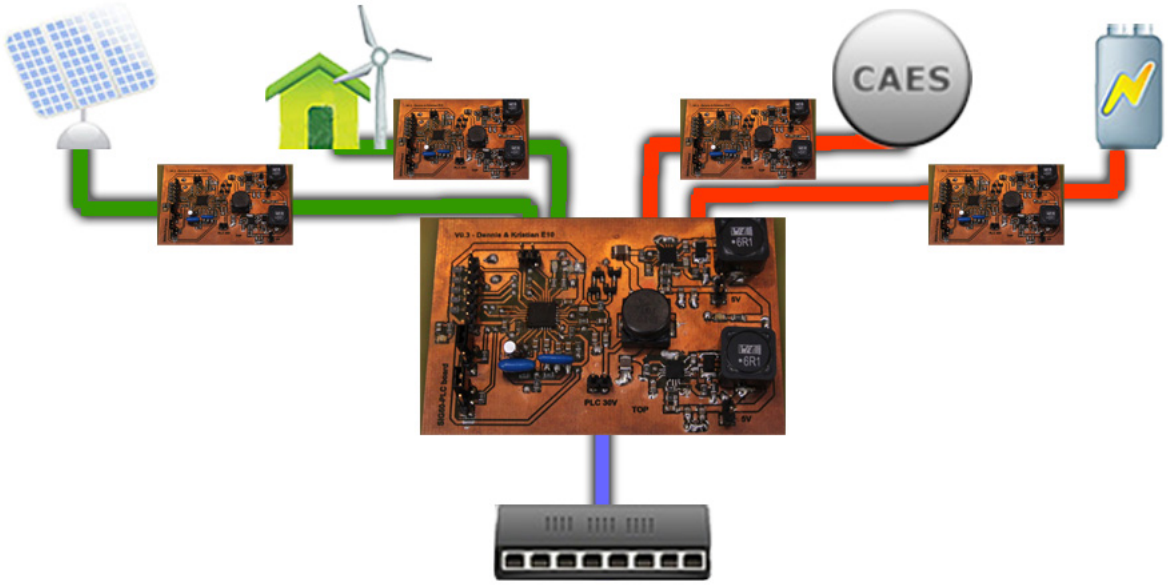
AU-Herning : EEMC1
Electromagnetic compatibility

Counselor: Per Lysgaard



BY E10 - Team3:

Theis Christensen (10691)

Dennis Madsen (90248)

Paulo Fontes (10484)

Due date : 25.05.2012

Table of Content

1 Introduction **4**

2 Design **5**
1 Standards . . . 5
1.1 Schematic and first PCB layout . . . 6
1.1.1 Schematic . . . 6
1.2 Review 1 . . . 8
1.3 Review 2 . . . 8
1.3.1 Testing the PCB . . . 9
1.4 Final design . . . 10

3 Test **12**
1 Radiation test . . . 12
2 Immunity test . . . 16
2.1 LF magnetic field immunity & HF irradiation . . . 16
2.2 Electrostatic discharge . . . 17
2.3 Burst and energy transients . . . 17
3 Design optimization . . . 17

4 Conclusion **18**

5 Appendix **19**

Chapter 1

Introduction

The EMC report is written as part of the EEMC1 (Electrostatic Compatibility) course attended in the start of 4th semester on the Electronic Design Engineering education at AU-Herning. The report contains information about designing a device in order to accomplish good EMC. The different parts which will be described and discussed concerns designing the PCB including review meetings, functional test, EMC test (radiation and immunity tests).

Chapter 2

Design

This chapter describes how the PCB has been designed in order to obtain EMC. The different laws used and reviews with supervisor *Per Lysgaard* are also described.

1 Standards

The different European standards according to Electromagnetic compatibility is found on the European Commission website [1]. The standard: *EN 50412-2-1:2005* deals with: *Power line communication apparatus and systems used in low-voltage installations in the frequency range 1.6 MHz to 30 MHz.* However, the power line is not to work on a low-voltage installation but in an isolated DC environment. Another reason why not to use this standard is its expire date: 01/04/2008. Instead of this standard, a generic standard is used.

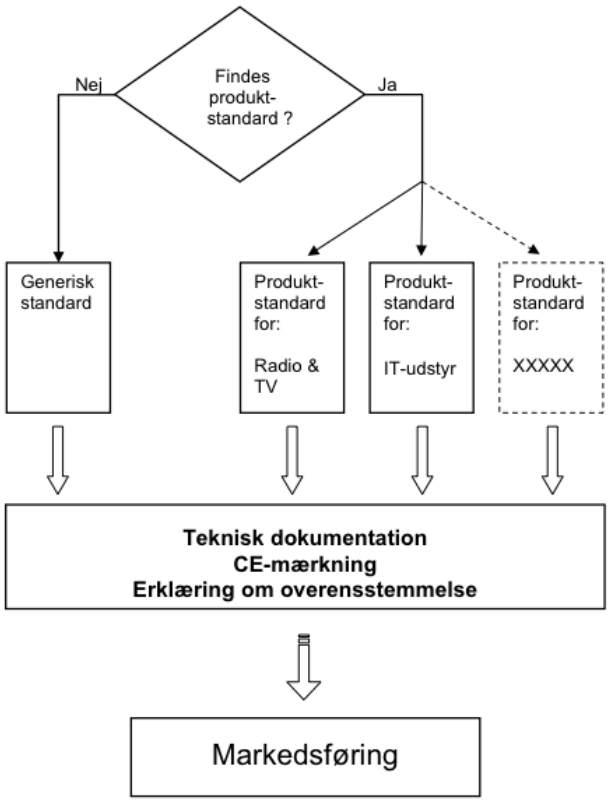


Figure 1.1: Choosing a relevant generic standard.

Basically there are two different generic standards both when talking immunity and emission. The standards are either residential or industrial. The definition of an industry is a place with its own transformer station. As the power line module can be used both places a mix is chosen, where the immunity test have to withstand the demands for industrial implementation and the emission have to withstand the demands for residential

[1] `http://ec.europa.eu/enterprise/policies/european-standards/harmonised-standards/electromagnetic-compatibility/index_en.htm#Note2.3`

implementation. In the industry there is a high requirement of immunity on the devices and low requirement for emission. This is vice versa for the residential requirements. The standards used is therefore:

- *61000-6-2* for immunity (industrial requirements)
- *61000-6-3* for emission (residential requirements)

The two standards describes what demands the equipment have to fulfill, how the tests should be done and how the measurements should be reported.

1.1 Schematic and first PCB layout

Full documentation of the schematic design can be found in the Appendix *EPRO_3_&_4_PLC - Hardware*. The design consists of two parts, a SMPS (switch mode power supply) and a PLC (power line communication) module. Both modules takes input from the power line (30VDC), where the Power Line part filters out the communication on top of the DC voltage and also sends commands to other modules on the net. The SMPS converts the 30VDC input to a 5VDC supply that can be used to power the Processor board and the FPGA board used in the project[2]. The PCB has been divided into two sections with the 30VDC connection in between the two modules to have as little interference as possible.

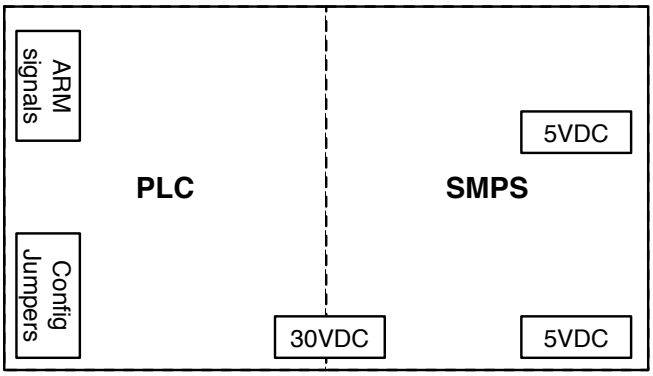


Figure 1.2: Overview of how the board is divided (Setup of the final board).

1.1.1 Schematic

The schematic has only changed slightly during the different versions of the circuit board. The newest version of the schematic is shown below (the PCB that fits to the schematic is shown in review 2).

[2]EPRO4

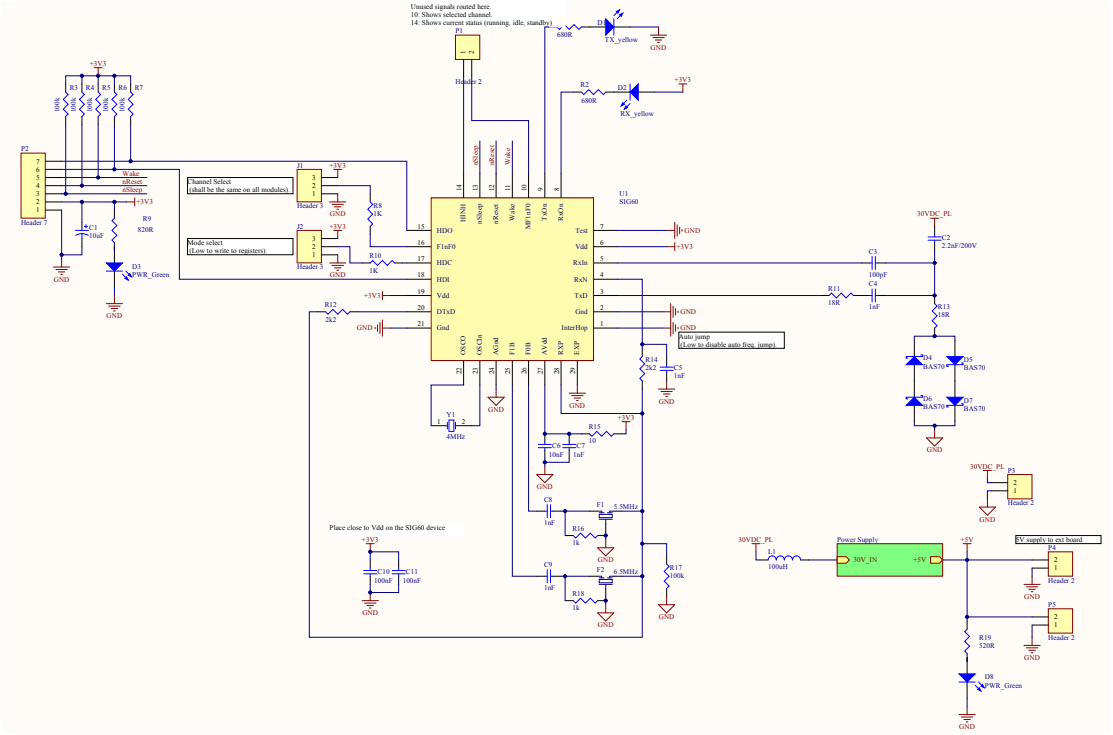


Figure 1.3: Communication part of the design.

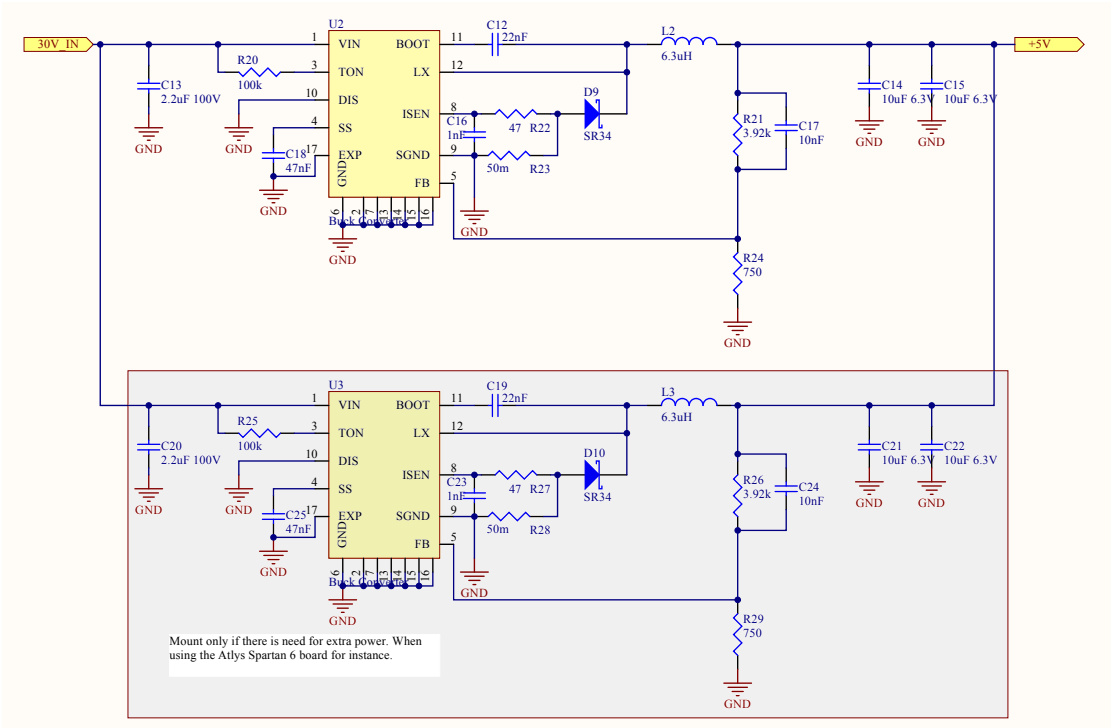


Figure 1.4: Power supply section of the design.

1.2 Review 1

The first PCB layout was made before attending the EMC course in the start of February 2012. In the end of the course feedback for the design was given. Two aspects should be changed:

- Shorten tracks on bottom side, so a clean ground plane is held.
- Enlarge track width (especially power tracks).

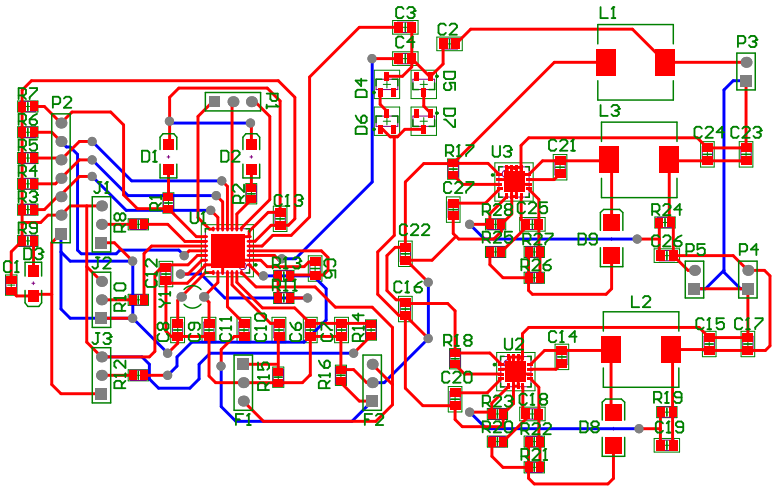


Figure 1.5: First routing of the circuit-board.

1.3 Review 2

In the second layout all track widths were adjusted, track length shortened and the amount of long tracks on the ground plane minimized. The only remark for this design was one of the tracks on the ground plane at twice the length of the other tracks. A PCB was made with this design as the remark was not critical and a redesign would require quiet some time.
Note: the free space on the PCB was connected to ground on both planes.

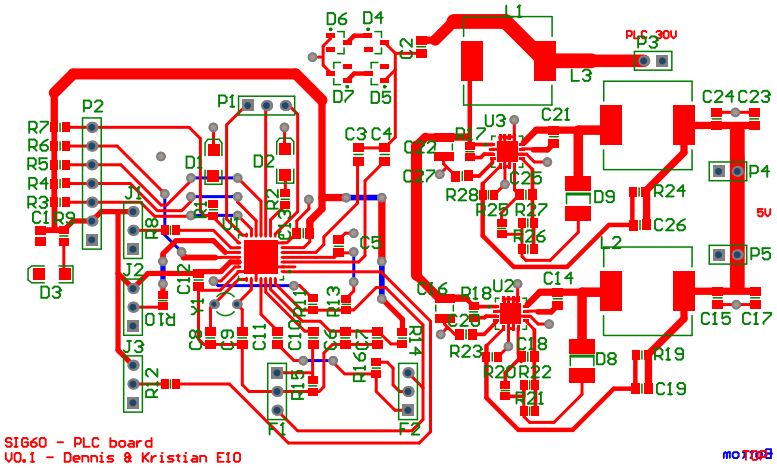


Figure 1.6: First redesign of the PCB layout.

1.3.1 Testing the PCB

Testing of the first PCB is documented in the Appendix *EPRO_3_&_4_PLC - Hardware*. A short resume:

- The output of the switch mode was unstable when loaded.
  - The feedback track shall be made shorter and the width of it enlarged.
  - Generally all components shall be placed closer to the switch mode device to shorten track lengths.
  - More vias for better connection to the ground plane, if it is possible, one or more should be placed underneath the switch mode device.
- When noise was added to the power line, random characters appeared in the communication.
  - A big resister has been added between the receive pin and ground.
  - Filters and crystal shall be placed as close as possible to the power line device to decrease the noise.

- The receive diode lightens up all the time.
  - The diode shall use the RxOn pin on the Power Line device instead of the receive pin to fix the problem.

1.4 Final design

In the final layout, all components have been placed even closer to the different IC's. The board size has decreased to approximately 65% of the last version.
To ease mounting, all vias and pads have been increased in size. As the pin-headers shall be soldered on both sides, the pads have also been shaped oblongly. Clearance between the tracks is defined to 15 mil as this distance can easily be made on homemade PCB's.
The 5 volt output tracks should be able to withstand 3 amperes maximum, according to the book *PCB Design Tutorial page 7* (see appendix), the track size shall be minimum 50mil. A width of 60 mil have been chosen.
As it can be seen on fig: 1.2 how the connectors on the board is placed. Usually it is preferable to have all connections in one side of a PCB (possible two). Although, to keep tracks as short as possible, and to place the shared item (30 Volt plug) a central place for both sides of the PCB, this rule has not been kept strict.

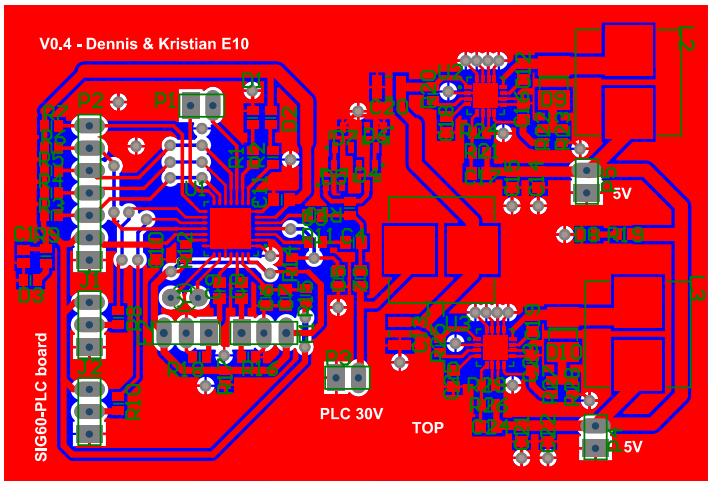


Figure 1.7: Final version of the PCB.

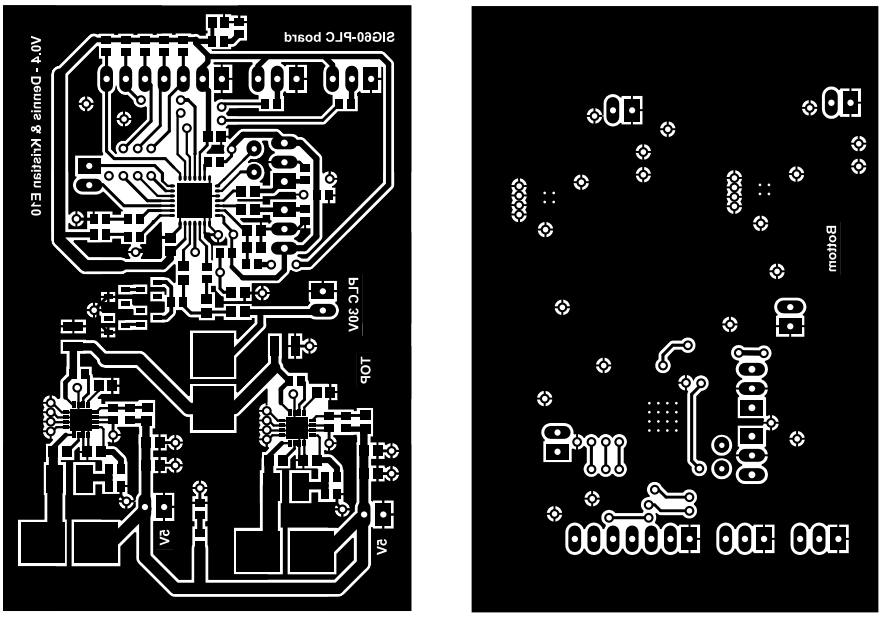


Figure 1.8: PCB layout, top and bottom

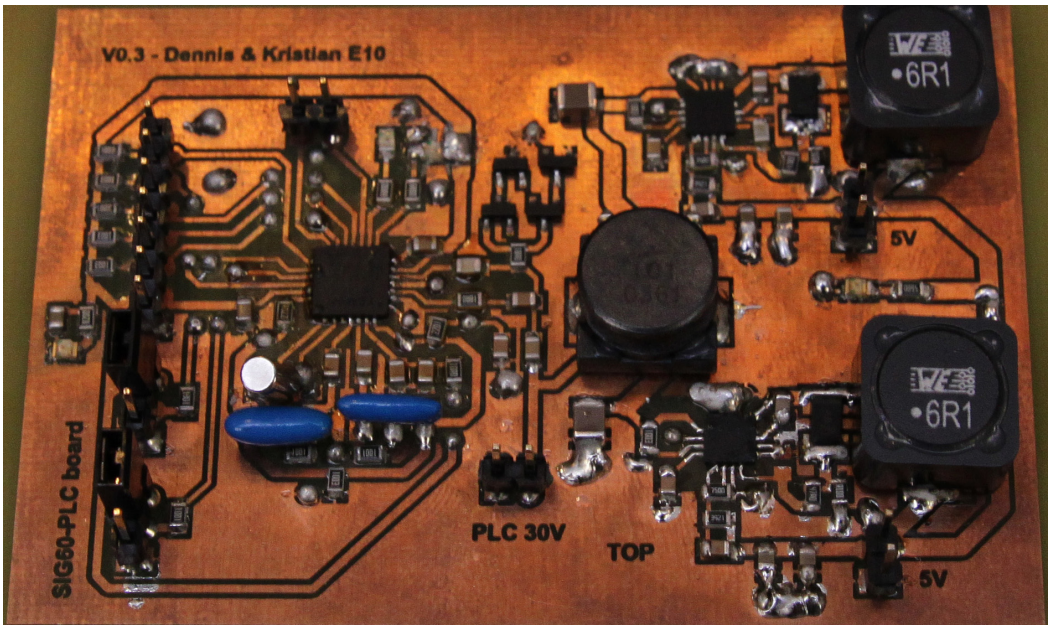


Figure 1.9: Final PCB mounted with both switch mode supplies

Chapter 3

Test

The order of the tests are defined from which tests that can harm the system. The most destructive tests are performed at last.

1 Radiation test

The test is performed in a TEM-cell (Transverse ElectroMagnetic field cell). The measurement in a TEM-cell can be compared to an open air measurement if the object is small and without inlets.

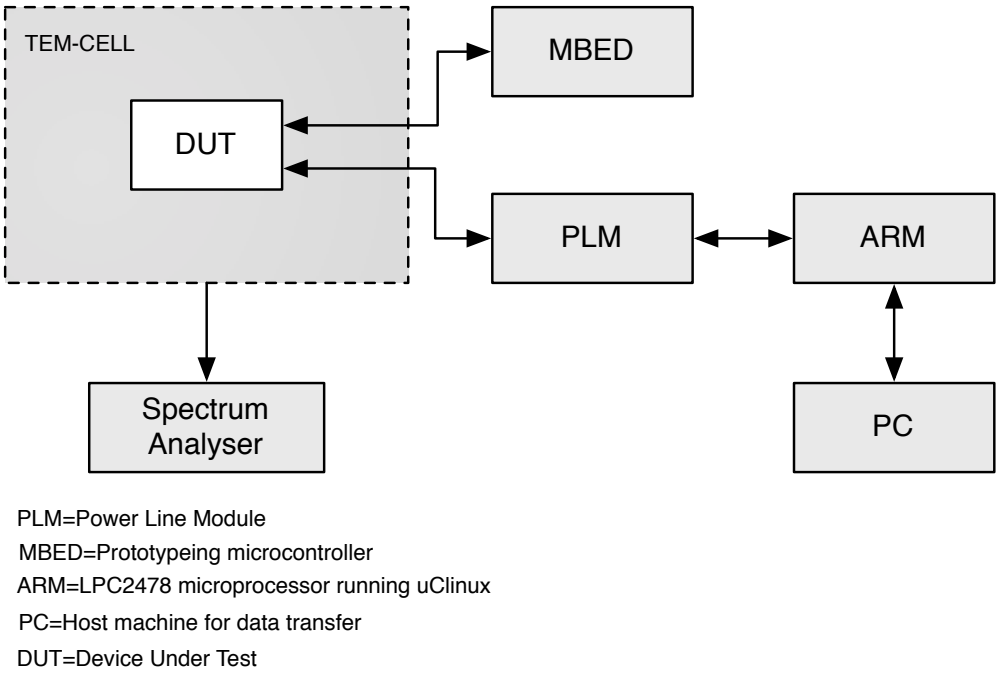


Figure 1.1: Emission test setup.

During the test, data was sent from the PC to the ARM board and the Power Supply on the device loaded in order to have the setup to emit the maximum amount of noise.

Figure 1.2: Emission test setup.

The board was rotated in order to find the position where it was emitting its maximum. In picture 1.3 the connected board is shown in its maximum emission position.

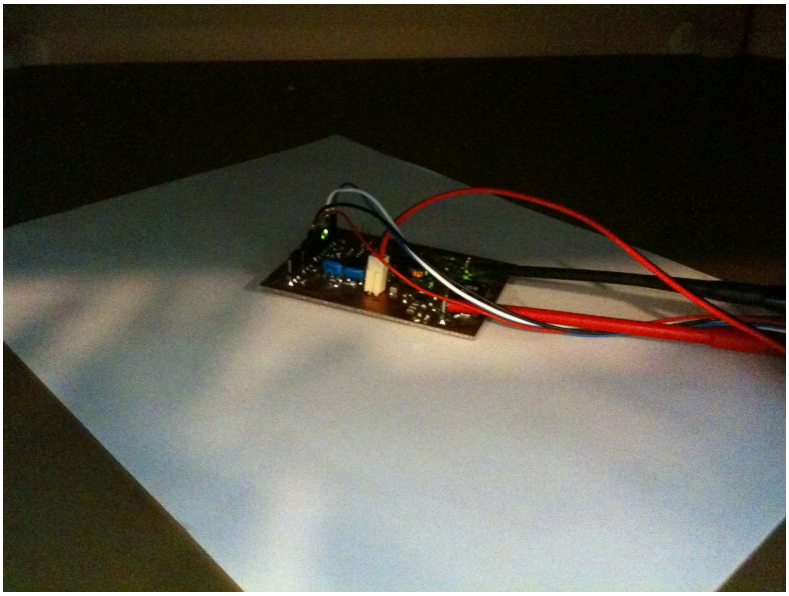


Figure 1.3: Board placement inside the TEM-cell.

Figure 1.4 shows the spectrum analyzer when the board is turned off. The big spike to the left is the DC level (0Hz).

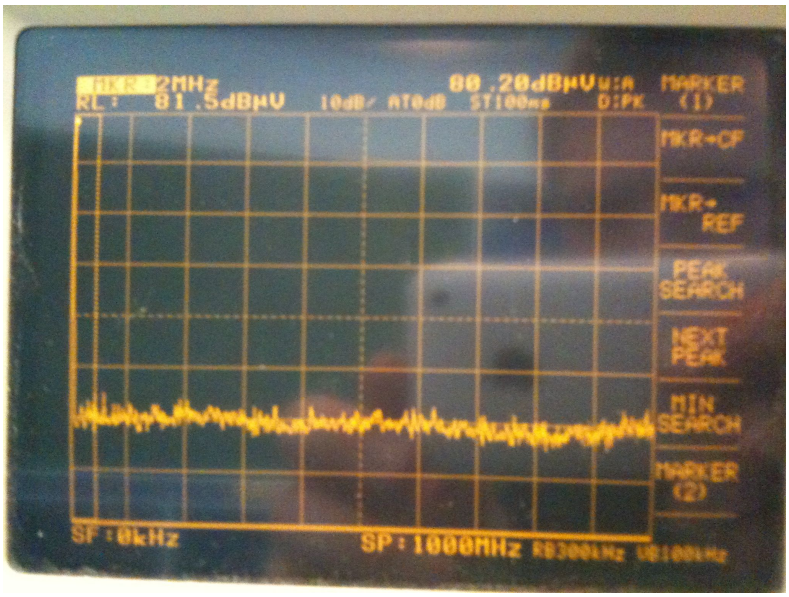


Figure 1.4: Spectrum analyzer when the device is turned off.

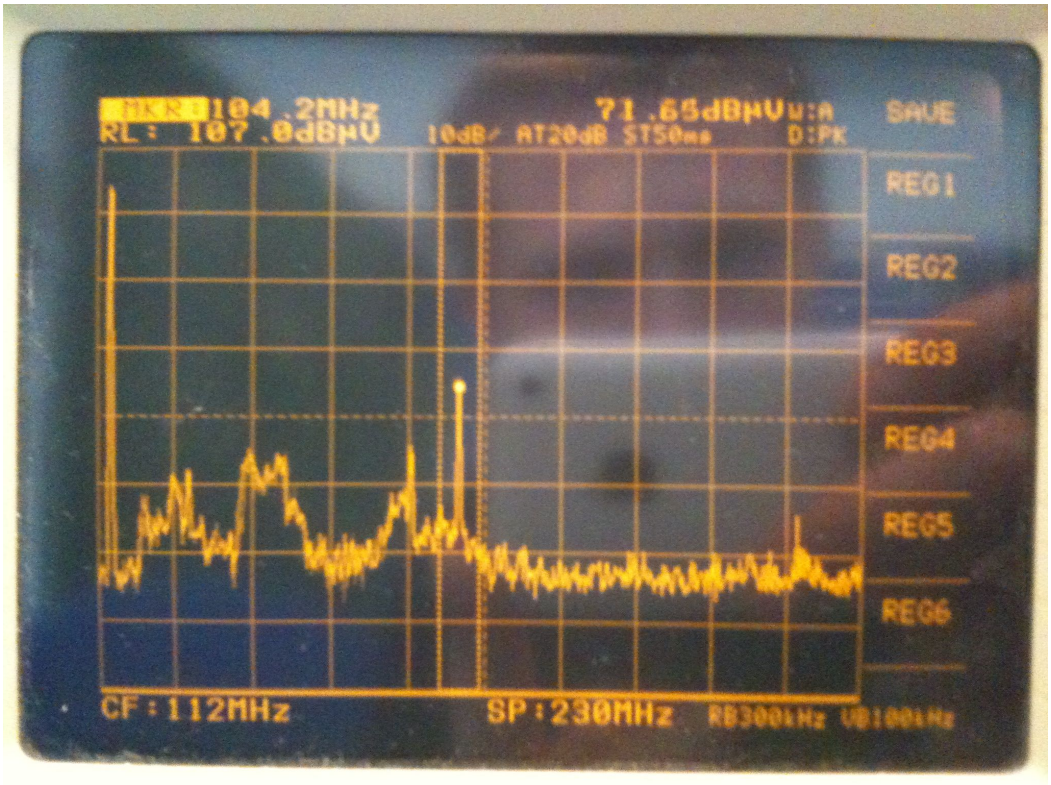


Figure 1.5: Emission spectrum of the unit. 0 to 230MHz.

Figure 1.5 shows the maximum level emitted from the device. Note the spike at approximately 100 MHz and the more broad noise at 20 to 50 MHz. Usually spikes comes from microprocessors or similar, in this case the Power Line circuit and the broad noise comes from Switching devices, in this case two switch mode circuits[1]. It is also measured that values above 230MHz are not emitted from the device.

The spike at 103MHz is the one emitting the most. As the test are performed in a TEM-Cell, the read value needs to be converted in order to be able to compare to the standards. The conversion is made in a small MathCAD document, fig: 1.6

$b := 0.3m$

$r := 10m$

$\lambda := 10$

$G := 1.6$

$V_{meas} := 72$ at 103Mhz

$$E_r = \frac{b \cdot 377}{\lambda \cdot r \cdot 50} \cdot \sqrt{\frac{2 \cdot G}{3}} \cdot V_{meas}$$

$$E_r := 20 \log\left(\frac{b \cdot 377}{\lambda \cdot r \cdot 50} \cdot \sqrt{\frac{2 \cdot G}{3}}\right) + V_{meas}$$ $E_r = 39.37$ dBµV / m

$E_{r\_max} := E_r + 7$ $E_{r\_max} = 46.37$ dBµV / m

Figure 1.6: MathCAD calculation of the emission.

The values read in a TEM-Cell can only be used as guidelines as the offset can be up to 7 dB. This gives a worst case value of $46.37 dB\mu V/m$.

According to table 1.1[2], the value measured is approximately $17 dB\mu V/m$ higher than the upper limit value. However, the values from table 1.1 is based on emission limits for cabinet ports. As the device is not mounted in a cabinet, table 1.2 & 1.3 might be used instead as these describes the emission from the signal and DC ports which is not shielded in this case.

[1] Grundlaeggende EMC2 - Page 29

[2] Table from *Grundleaggende EMC2 - page 73*

Fenomena	Frequency-span	Limit	Basis standard
	30 - 230 MHz 230 - 1000MHz	30dB(μV/m) in 10 m distance 37 dB(μV/m) in 10 m distance	CISPR 16-2-3
Radio Frequent electro magnetic fields	1 - 3 GHz 3 - 6 GHz	70 dB(μV/m) peak 50 dB(μV/m) average in 3 m distance 74 dB(μV/m) peak 54 dB(μV/m) average in 3 m distance	CISPR 16-1-1 CISPR 16-1-4 CISPR 16-2-3

Table 1.1: Emission limit values for cabinet-ports according to the EN 61000-6-3 standard.

Fenomena	Frequency-span	Limit	Basis standard
Noise	0.15 - 0.5 MHz	79dB(μV/m) quasi-peak 66dB(μV/m) average	CISPR 16-1-2 & 16-2-1
Noise	0.5 - 30 MHz	73dB(μV/m) quasi-peak 60dB(μV/m) average	CISPR 16-1-2 & 16-2-1

Table 1.2: Emission limit values for DC power ports.

Fenomena	Frequency-span	Limit	Basis standard
Noise	0.15 - 0.5 MHz	79-87dB(μV/m) quasi-peak 84-74dB(μV/m) average	CISPR 22
Noise	0.5 - 30 MHz	87dB(μV/m) quasi-peak 74dB(μV/m) average	CISPR 22

Table 1.3: Emission limit values for signal power ports.

In section 3 (Design Optimization) different suggestions to improving EMC are discussed.

2 Immunity test

Down below different test cases are described, which the product has to fulfill in order to be EMC proved and get the CE mark. None of the tests are however performed as the immunity test equipment for the LF magnetic field immunity test and the HF irradiation test is non functional at the time and as the device is a prototype board the ESD and burst / energy transients are not performed. The two last test are not performed as these are meant for a finish product in its housing where the different connectors are stressed in order to verify its immunity.

2.1 LF magnetic field immunity & HF irradiation

In this section it is shortly described how the immunity test for the device shall be performed.

The setup for immunity test is equal to the one for emission (see fig: 1.1). During the test the equipment have to fulfill criteria
A: The equipment have to operate normally during and after the test.

By this criteria is in this case meant that the communication have to continue during the test (transmit and receive) and the output voltage have to be kept stabile at its 5 volt level.

Fenomena	Test requirements	Basis standard	Fail criterium
Radiofrekvent	0.15 - 80 MHz		
CM coubling	10 V	EN 61000-4-6	A
AM modulated	80 % AM (1kHz)		

Table 2.1: Immunity: signal ports and DC power ports

Table 2.1 shows the field and irradiation values the device shall be able to withstand.

2.2 Electrostatic discharge

Not tested as the board is only in prototype state.

2.3 Burst and energy transients

Not tested as the board is only in prototype state.

3 Design optimization

As the radiation test did not fulfill the requirements given according to the standard EN 61000-6-2, some improvements have to be made. Different solutions to decrease the noise emitted by the device will be discussed here.

An easy fix is to mount the board inside a shielded housing to improve EMC. The board will most likely still have some emission because of the different connector holes.

Another more systematical approach will be to use a small antenna (probe ground connected to probe input) connected to an oscilloscope to find hotspots components and track on the board which emits the most. At the different hotspots some different approaches can be taken:

- Decoupling capacitors.
- Analog lowpass filters.
- Local shielding.
- Re-routing twisted tracs.
- Expand ground plane.

Chapter 4

Conclusion

During the EMC course, an overall knowledge about why products needs good EMC have been gained. The feedback sessions have helped in pointing out less good PCB routing when talking about good EMC. Also the hands on approach where a radiation and an immunity test should be performed after designing a device according to good EMC guidelines have been very good.

Generally good tools have been gained during the course which can be used in future projects to accomplish good EMC.

Chapter 5

Appendix

Report:
EPRO_3_&_4_PLC - Hardware

Tutorial:
PCB Design Tutorial by David L. Jones, link:
`www.alternatezone.com/electronics/files/PCBDesignTutorialRevA.pdf`