

# AFE7906 具有 3GSPS ADC 的 6 通道、5MHz 至 12GHz 射频采样接收器

## 1 特性

- [申请完整数据表](#)
- 六个射频采样 14 位、3 GSPS ADC
- 最大射频信号带宽：
  - 4 个 ADC：每个 ADC 为 1200 MHz
  - 6 个 ADC：每个 ADC 为 600 MHz
- 射频频率范围：5 MHz 至 12 GHz
- 数字步进衰减器 (DSA)：25 dB 范围，0.5 dB 步进
- 单频带 DDC ( 在 6 个通道上 ) 和双频带 DDC ( 在 4 个通道上 )
- 每个 DDC 通道 16 个 NCO
- 可选内部 PLL/VCO，提供 ADC 采样率下的 ADC 时钟或外部时钟
- Sysref 对齐检测器
- 串行器/解串器数据接口：
  - 可兼容 JESD204B 和 JESD204C
  - 8 个高达 29.5 Gbps 的串行器/解串器发送器
  - 子类 1 多器件同步
- 封装：17mm × 17mm FCBGA，间距 0.8 mm

## 2 应用

- 雷达
- 导引头前端
- 国防无线电
- 无线通信测试

## 3 说明

AFE7906 是一款高性能、高带宽、多通道接收器，集成了六个射频采样 ADC。此器件具有高达 12GHz 的工作频率，支持直接在 L、S、C 和 X 带频率范围内进行射频采样，无需额外的频率转换级。密度和灵活性提高后可支持高通道数、多任务系统。

每个接收器链均包含一个 25dB 范围的数字步进衰减器 (DSA)，后跟一个 3GSPS 模数转换器 (ADC)。四个接收器通道都有模拟峰值功耗检测器和各种数字功耗检测器，可辅助进行外部或内部自主自动增益控制器，另外还具有射频过载检测器，用于提供器件可靠性保护。灵活的抽取选项提供高达 1200MHz ( 对于四个 RX ) 或 600MHz 的数据带宽优化。

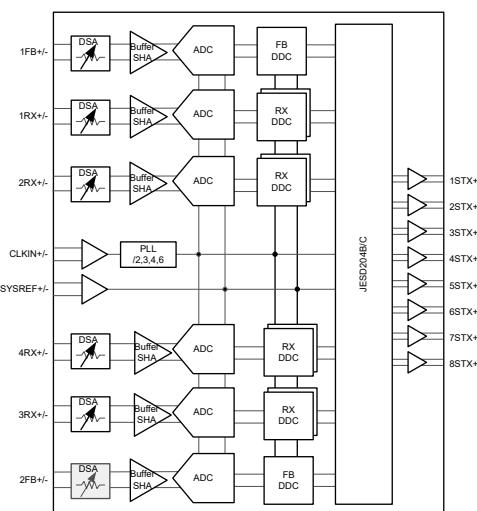
该器件包含一个 SYSREF 时序检测器，用于优化相对于器件时钟的 SYSREF 输入时序。

### 封装信息

| 器件型号    | 封装 <sup>(1)</sup> | 封装尺寸 <sup>(2)</sup> |
|---------|-------------------|---------------------|
| AFE7906 | FC-BGA            | 17.00mm × 17.00mm   |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

(2) 封装尺寸 ( 长 × 宽 ) 为标称值，并包括引脚 ( 如适用 )。



功能方框图



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 [www.ti.com](http://www.ti.com)，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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## 4 说明 (续)

每个接收器链均包含一个 25dB 范围的数字步进衰减器 (DSA)，后跟一个 3GSPS 模数转换器 (ADC)。每个接收器通道都有多个模拟峰值功耗检测器和各种数字功耗检测器，可辅助进行外部或内部自主自动增益控制器，另外还有一个射频过载检测器，用于提供器件可靠性保护。灵活的抽取选项可为数据带宽提供高达 1200MHz 的优化（对于四条不带 FB 路径的 RX），或为带两条 FB 路径（每条 1200MHz 带宽）提供 600MHz 的优化。

该器件包含一个 SYSREF 时序检测器，用于优化相对于器件时钟的 SYSREF 输入时序。

## 5 Revision History

注：以前版本的页码可能与当前版本的页码不同

### Changes from July 9, 2022 to May 30, 2023 (from Revision B (July 2022) to Revision C (May 2023))

|  | Page |
|--|------|
| • 将“器件信息”更改为封装信息表.....                                 | 1    |
| • Changed $I_{IH}$ and $I_{IL}$ units to $\mu A$ ..... | 14   |

### Changes from March 11, 2022 to July 8, 2022 (from Revision A (March 2022) to Revision B (July 2022))

|   | Page |
|---|------|
| • Deleted ABJ from the <a href="#">Thermal Information</a> table. The table applies to both ABJ and the ALK packages..... | 4    |
| • Changed 0RX - 3RX to 1RX - 4RX in several plots.....  | 42   |
| • Changed 0RX - 3RX to 1RX - 4RX in several plots.....  | 47   |

### Changes from Revision \* (January 2022) to Revision A (March 2022)

|  | Page |
|--|------|
| • 向“申请完整数据表”添加了特性 .....  | 1    |
| • Added the <a href="#">Specification</a> tables to the data sheet.....            | 4    |
| • Changed Power Mode 4 to $f_{RX} = 2.25$ GHz.....                                 | 15   |
| • Added the <a href="#">Typical Characteristics</a> section to the data sheet..... | 19   |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                      |  | MIN   | MAX              | UNIT |
|----------------------|--|-------|------------------|------|
| Supply Voltage Range | DVDD0P9, VDDT0P9   | - 0.3 | 1.2              | V    |
|                      | VDD1P2RX, VDD1P2TXCLK, VDD1P2TXENC, VDD1P2PLL, VDD1P2PLCLKREF, VDD1P2FB, VDD1P2FBCML, VDD1P2RXCML                              | - 0.3 | 1.4              | V    |
|                      | VDD1P8RX, VDD1P8RXCLK, VDD1P8TX, VDD1P8TXDAC, VDD1P8TXENC, VDD1P8PLL, VDD1P8PLLVCO, VDD1P8FB, VDD1P8FBCLK, VDD1P8GPIO, VDDA1P8 | - 0.5 | 2.1              | V    |
| Pin Volatge Range    | {1/2/3/4}RXIN+/-   | - 0.5 | VDDRX1P8+0.3     | V    |
|                      | 1FBIN+/-, 2FB+/-   | - 0.5 | VDDFB1P8+0.3     | V    |
|                      | REFCLK+/-, SYSREF+/-   | - 0.3 | 1.4              | V    |
|                      | {1:8}STX+/-  | - 0.3 | 1.4              | V    |
|                      | GPIO{B/C/D/E}x, SPICLK, SPISDIO, SPISDO, SPISEN, RESETZ, BISTB0, BISTB1  | - 0.5 | VDD1P8GPIO + 0.3 | V    |
|                      | IFORCE, VSENSE   | - 0.3 | VDDCLK1P8 + 0.3  | V    |
|                      | SRDAMUX1, SRDAMUX2   | - 0.3 | VDDA1P8+0.3      | V    |
| Peak Input Current   | any input  |       | 20               | mA   |
| T <sub>J</sub>       | Junction temperature   |       | 150              | °C   |
| T <sub>stg</sub>     | Storage temperature  | - 65  | 150              | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#). Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

|                    |                         | VALUE   | UNIT |
|--------------------|-------------------------|---|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>     | 1000 |
|                    |                         | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins <sup>(2)</sup> | 150  |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible if necessary precautions are taken.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|  |  | MIN  | NOM   | MAX                | UNIT |
|--|--|------|-------|--------------------|------|
| DVDD0P9, VDDT0P9   | Supply voltage 0.9V                    | 0.9  | 0.925 | 0.95               | V    |
| VDD1P2{RX/TXCLK/TXENC/FB/PLL/<br>PLLCLKREF/FBCML/RXCML}                  | Supply voltage 1.2V                    | 1.15 | 1.2   | 1.25               | V    |
| VDD1P8{RX/RXCLK/TX/TXDAC/<br>TXENC/PLL/PLLCO/FB/FBCLK/<br>GPIO}, VDDA1P8 | Supply voltage 1.8V                    | 1.75 | 1.8   | 1.85               | V    |
| T <sub>A</sub>   | Ambient temperature                    | - 40 |       | 85                 | °C   |
| T <sub>J</sub>   | Operating Junction Temperature         |      |       | 110 <sup>(1)</sup> | °C   |
|  | Maximum Operating Junction Temperature | 125  |       |                    | °C   |

- (1) Prolonged use at or above this junction temperature can increase the device failure-in-time (FIT) rate. Refer to [SBAA403 application note](#) for additional details

## 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |  | AFE7906  | UNIT |
|-------------------------------|--|----------|------|
|                               |  | FC-BGA   |      |
|                               |  | 400 PINS |      |
| R <sub>θ JA</sub>             | Junction-to-ambient thermal resistance       | 16.2     | °C/W |
| R <sub>θ JC(top)</sub>        | Junction-to-case (top) thermal resistance    | 0.42     | °C/W |
| R <sub>θ JB</sub>             | Junction-to-board thermal resistance         | 4.85     | °C/W |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 0.12     | °C/W |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 4.6      | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

## 6.5 RF ADC Electrical Characteristics

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1500MSPS above 6GHz input frequency,  $f_{\text{ADC}} = 2949.12\text{MHz}$ ; PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$  below 6GHz input frequency and External clock mode with  $f_{\text{CLK}} = 2949.12\text{MHz}$  above 6GHz input frequency; nominal power supplies; DSA Setting =3dB; SerDes rate =24.33Gbps; unless otherwise noted.

| PARAMETER              |  | TEST CONDITIONS  | MIN | TYP   | MAX | UNIT |
|------------------------|--|--|-----|-------|-----|------|
| ADC <sub>RES</sub>     | ADC resolution   |  |     | 14    |     | bits |
| F <sub>RFin</sub>      | RF input frequency range   |  | 5   | 12000 |     | MHz  |
| P <sub>FS_CW,min</sub> | Min Full scale input power, at device pins <sup>(1)</sup>        | f <sub>IN</sub> = 5 MHz, DSA=0dB, f <sub>ADC</sub> = 1500MSPS, f <sub>NCO</sub> = 17MHz, Decimate by 48    |     | -0.4  |     | dBm  |
|                        |  | f <sub>IN</sub> = 30 MHz, DSA=0dB, f <sub>ADC</sub> = 1500MSPS, f <sub>NCO</sub> = 30MHz, Decimate by 24   |     | -2.2  |     |      |
|                        |  | f <sub>IN</sub> = 410 MHz, DSA=0dB, f <sub>ADC</sub> = 3000MSPS, f <sub>NCO</sub> = 400MHz, Decimate by 12 |     | -2.5  |     |      |
|                        |  | f <sub>IN</sub> = 830 MHz, DSA=0dB   |     | -2.9  |     |      |
|                        |  | f <sub>IN</sub> = 1760 MHz, DSA=0dB  |     | -2.8  |     |      |
|                        |  | f <sub>IN</sub> = 2610 MHz, DSA=0dB  |     | -1.8  |     |      |
|                        |  | f <sub>IN</sub> = 3610 MHz, DSA=0dB  |     | -0.4  |     |      |
|                        |  | f <sub>IN</sub> = 4910 MHz, DSA=0dB  |     | 0.1   |     |      |
|                        |  | f <sub>IN</sub> = 8150 MHz, DSA=0dB  |     | 2.1   |     |      |
|                        |  | f <sub>IN</sub> = 9610 MHz, DSA=0dB  |     | 4.3   |     |      |
| P <sub>FS_CW,MAX</sub> | MAX Full scale input power - reliability limited, at device pins | f <sub>IN</sub> = 5 MHz, f <sub>ADC</sub> = 1500MSPS, f <sub>NCO</sub> = 17MHz, Decimate by 48             |     | 19.7  |     | dBm  |
|                        |  | f <sub>IN</sub> = 30 MHz, f <sub>ADC</sub> = 1500MSPS, f <sub>NCO</sub> = 30MHz, Decimate by 24            |     | 17.8  |     |      |
|                        |  | f <sub>IN</sub> = 410 MHz, f <sub>ADC</sub> = 3000MSPS, f <sub>NCO</sub> = 400MHz, Decimate by 24          |     | 17.6  |     |      |
|                        |  | f <sub>IN</sub> = 830 MHz  |     | 16.7  |     |      |
|                        |  | f <sub>IN</sub> = 1760 MHz   |     | 17.0  |     |      |
|                        |  | f <sub>IN</sub> = 2610 MHz   |     | 18    |     |      |
|                        |  | f <sub>IN</sub> = 3610 MHz   |     | 18.5  |     |      |
|                        |  | f <sub>IN</sub> = 4910 MHz   |     | 19.3  |     |      |
|                        |  | f <sub>IN</sub> = 8150 MHz   |     | 21.3  |     |      |
|                        |  | f <sub>IN</sub> = 9610 MHz   |     | 23.5  |     |      |
| R <sub>TERM</sub>      | Input reference impedance  |  |     | 100.0 |     | Ω    |
| ATT <sub>range</sub>   | DSA Attenuation range  |  |     | 25.0  |     | dB   |
| ATT <sub>step</sub>    | DSA Attenuation step   |  |     | 0.5   |     | dB   |
|                        | DSA Attenuation step accuracy                                    | Delta=Gatt(X)-Gatt(X-1), F <sub>in</sub> =3610MHz, after calibration                                       |     | 0.1   |     |      |
|                        | DSA Gain Steps Phase accuracy any 8dB range                      | F <sub>in</sub> =3610MHz, after calibration  |     | 0.9   |     | deg  |
|                        | DSA Gain Steps Phase accuracy any 8dB range                      | F <sub>in</sub> =4910MHz, after calibration  |     | 1.8   |     |      |
| G <sub>flat</sub>      | Gain flatness  | Measured Over 80MHz BW   |     | 0.2   |     | dB   |
|                        |  | Measured Over 200MHz BW  |     | 0.5   |     |      |
|                        |  | Measured Over 400MHz BW  |     | 1.1   |     |      |

## 6.5 RF ADC Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1500MSPS above 6GHz input frequency,  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$  below 6GHz input frequency and External clock mode with  $f_{\text{CLK}} = 2949.12\text{MHz}$  above 6GHz input frequency; nominal power supplies; DSA Setting =3dB; SerDes rate =24.33Gbps; unless otherwise noted.

|                   | PARAMETER                                 | TEST CONDITIONS  | MIN    | TYP | MAX | UNIT    |
|-------------------|---|--|--------|-----|-----|---------|
| NSD               | Noise Density<br>(small signal = -30dBFS) | $f_{\text{IN}} = 5 \text{ MHz}$ , DSA = 3dB, $f_{\text{ADC}} = 1500\text{MSPS}$ , $f_{\text{NCO}} = 17\text{MHz}$ , Decimate by 48                         | -147.1 |     |     | dBFS/Hz |
|                   |   | $f_{\text{IN}} = 30 \text{ MHz}$ , DSA = 3dB, $f_{\text{ADC}} = 1500\text{MSPS}$ , $f_{\text{NCO}} = 30\text{MHz}$ , Decimate by 24                        | -150.7 |     |     |         |
|                   |   | $f_{\text{IN}} = 410 \text{ MHz}$ , DSA = 3dB, $f_{\text{ADC}} = 3000\text{MSPS}$ , $f_{\text{NCO}} = 400\text{MHz}$ , Decimate by 24                      | -155.4 |     |     |         |
|                   |   | $f_{\text{IN}} = 830 \text{ MHz}$ , DSA = 3dB <sup>(3)</sup>   | -156.2 |     |     |         |
|                   |   | $f_{\text{IN}} = 1760 \text{ MHz}$ , DSA = 3dB <sup>(3)</sup>  | -156.0 |     |     |         |
|                   |   | $f_{\text{IN}} = 2610 \text{ MHz}$ , DSA = 3dB <sup>(3)</sup>  | -155.4 |     |     |         |
|                   |   | $f_{\text{IN}} = 3610 \text{ MHz}$ , DSA = 3dB <sup>(3)</sup>  | -155.1 |     |     |         |
|                   |   | $f_{\text{IN}} = 4910 \text{ MHz}$ , DSA = 3dB <sup>(3)</sup>  | -155.1 |     |     |         |
|                   |   | $f_{\text{IN}} = 8110 \text{ MHz}$ , DSA = 3dB <sup>(3)</sup>  | -152   |     |     |         |
|                   |   | $f_{\text{IN}} = 9610 \text{ MHz}$ , DSA = 3dB <sup>(3)</sup>  | -151   |     |     |         |
|                   |   | $f_{\text{IN}} = 5 \text{ MHz}$ , $f_{\text{ADC}} = 1500\text{MSPS}$ , $f_{\text{NCO}} = 17\text{MHz}$ , Decimate by 48, $3 \leq \text{Atten} \leq 22$     | -147.8 |     |     |         |
|                   |   | $f_{\text{IN}} = 30 \text{ MHz}$ , $f_{\text{ADC}} = 1500\text{MSPS}$ , $f_{\text{NCO}} = 30\text{MHz}$ , Decimate by 24, $3 \leq \text{Atten} \leq 22$    | -151.5 |     |     |         |
|                   |   | $f_{\text{IN}} = 410 \text{ MHz}$ , $3 \leq \text{Atten} \leq 22$ , $f_{\text{ADC}} = 3000\text{MSPS}$ , $f_{\text{NCO}} = 400\text{MHz}$ , Decimate by 24 | -156.6 |     |     |         |
|                   |   | $f_{\text{IN}} = 830 \text{ MHz}$ , $3 \leq \text{Atten} \leq 22$  | -156.0 |     |     |         |
|                   |   | $f_{\text{IN}} = 1760 \text{ MHz}$ , $3 \leq \text{Atten} \leq 25$   | -155.8 |     |     |         |
|                   |   | $f_{\text{IN}} = 2610 \text{ MHz}$ , $3 \leq \text{Atten} \leq 25$   | -155.7 |     |     |         |
|                   |   | $f_{\text{IN}} = 3610 \text{ MHz}$ , $3 \leq \text{Atten} \leq 25$   | -155.4 |     |     |         |
|                   |   | $f_{\text{IN}} = 4910 \text{ MHz}$ , $3 \leq \text{Atten} \leq 25$   | -155.8 |     |     |         |
| NF <sub>min</sub> | Noise Figure min<br>DSA Atten=0 - 3dB     | $f_{\text{IN}} = 5 \text{ MHz}$ , $f_{\text{ADC}} = 1500\text{MSPS}$ , $f_{\text{NCO}} = 17\text{MHz}$ , Decimate by 48                                    | 29.4   |     |     | dB      |
|                   |   | $f_{\text{IN}} = 30 \text{ MHz}$ , $f_{\text{ADC}} = 1500\text{MSPS}$ , $f_{\text{NCO}} = 30\text{MHz}$ , Decimate by 24                                   | 24.5   |     |     |         |
|                   |   | $f_{\text{IN}} = 410 \text{ MHz}$ , $f_{\text{ADC}} = 3000\text{MSPS}$ , $f_{\text{NCO}} = 400\text{MHz}$ , Decimate by 24                                 | 19.3   |     |     |         |
|                   |   | $f_{\text{IN}} = 830 \text{ MHz}$  | 19.1   |     |     |         |
|                   |   | $f_{\text{IN}} = 1760 \text{ MHz}$   | 19.0   |     |     |         |
|                   |   | $f_{\text{IN}} = 2610 \text{ MHz}$   | 20.9   |     |     |         |
|                   |   | $f_{\text{IN}} = 3610 \text{ MHz}$   | 22.8   |     |     |         |
|                   |   | $f_{\text{IN}} = 4910 \text{ MHz}$   | 22.4   |     |     |         |
|                   |   | $f_{\text{IN}} = 8150 \text{ MHz}$   | 27.3   |     |     |         |
|                   |   | $f_{\text{IN}} = 9610 \text{ MHz}$   | 30     |     |     |         |

## 6.5 RF ADC Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1500MSPS above 6GHz input frequency,  $f_{\text{ADC}} = 2949.12\text{MHz}$ ; PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$  below 6GHz input frequency and External clock mode with  $f_{\text{CLK}} = 2949.12\text{MHz}$  above 6GHz input frequency; nominal power supplies; DSA Setting =3dB; SerDes rate =24.33Gbps; unless otherwise noted.

| PARAMETER                |  | TEST CONDITIONS   | MIN | TYP  | MAX | UNIT |
|--------------------------|--|---|-----|------|-----|------|
| NF                       | Noise Figure <sup>(4)</sup><br>DSA Atten=4dB   | $f_{\text{IN}} = 5 \text{ MHz}, f_{\text{ADC}} = 1500\text{MSPS}, f_{\text{NCO}} = 17\text{MHz}$ , Decimate by 48                         |     | 30.6 |     | dB   |
|                          |  | $f_{\text{IN}} = 30 \text{ MHz}, f_{\text{ADC}} = 1500\text{MSPS}, f_{\text{NCO}} = 30\text{MHz}$ , Decimate by 24                        |     | 25.1 |     |      |
|                          |  | $f_{\text{IN}} = 410 \text{ MHz}, f_{\text{ADC}} = 3000\text{MSPS}, f_{\text{NCO}} = 400\text{MHz}$ , Decimate by 24                      |     | 20.1 |     |      |
|                          |  | $f_{\text{IN}} = 830 \text{ MHz}$   |     | 20.0 |     |      |
|                          |  | $f_{\text{IN}} = 1760 \text{ MHz}$  |     | 20.6 |     |      |
|                          |  | $f_{\text{IN}} = 2610 \text{ MHz}$  |     | 21.9 |     |      |
|                          |  | $f_{\text{IN}} = 3610 \text{ MHz}$  |     | 23.5 |     |      |
|                          |  | $f_{\text{IN}} = 4910 \text{ MHz}$  |     | 22.3 |     |      |
|                          |  | $f_{\text{IN}} = 8150 \text{ MHz}$  |     | 27.9 |     |      |
|                          |  | $f_{\text{IN}} = 9610 \text{ MHz}$  |     | 30.7 |     |      |
| $\text{NF}_{\text{max}}$ | Noise Figure <sup>(4)</sup><br>DSA Atten=20dB  | $f_{\text{IN}} = 5 \text{ MHz}, f_{\text{ADC}} = 1500\text{MSPS}, f_{\text{NCO}} = 17\text{MHz}$ , Decimate by 48                         |     | 45.9 |     | dB   |
|                          |  | $f_{\text{IN}} = 30 \text{ MHz}, f_{\text{ADC}} = 1500\text{MSPS}, f_{\text{NCO}} = 30\text{MHz}$ , Decimate by 24                        |     | 40.2 |     |      |
|                          |  | $f_{\text{IN}} = 410 \text{ MHz}, f_{\text{ADC}} = 3000\text{MSPS}, f_{\text{NCO}} = 400\text{MHz}$ , Decimate by 24                      |     | 35.0 |     |      |
|                          |  | $f_{\text{IN}} = 830 \text{ MHz}$   |     | 34.7 |     |      |
|                          |  | $f_{\text{IN}} = 1760 \text{ MHz}$  |     | 35.2 |     |      |
|                          |  | $f_{\text{IN}} = 2610 \text{ MHz}$  |     | 36.0 |     |      |
|                          |  | $f_{\text{IN}} = 3610 \text{ MHz}$  |     | 37.3 |     |      |
|                          |  | $f_{\text{IN}} = 4910 \text{ MHz}$  |     | 37.6 |     |      |
|                          |  | $f_{\text{IN}} = 8150 \text{ MHz}$  |     | 42.8 |     |      |
|                          |  | $f_{\text{IN}} = 9610 \text{ MHz}$  |     | 45   |     |      |
| IMD3                     | 3 <sup>rd</sup> order intermodulation 2 tones at at $f_{\text{IN}} \pm 10\text{MHz}$<br>-7dBFS each tone | $f_{\text{IN}} = 30 \pm 1 \text{ MHz}, f_{\text{ADC}} = 1500\text{MSPS}, f_{\text{NCO}} = 30\text{MHz}$ , Decimate by 24                  |     | -82  |     | dBc  |
|                          |  | $f_{\text{IN}} = 400\text{MHz}$ and $405\text{MHz}$ , $f_{\text{ADC}} = 3000\text{MSPS}, f_{\text{NCO}} = 400\text{MHz}$ , Decimate by 24 |     | -75  |     |      |
|                          |  | $f_{\text{IN}} = 840 \text{ MHz}, 3 \leq \text{Atten} \leq 12$  |     | -82  |     |      |
|                          |  | $f_{\text{IN}} = 1770 \text{ MHz}, 3 \leq \text{Atten} \leq 12$   |     | -84  |     |      |
|                          |  | $f_{\text{IN}} = 2610 \text{ MHz}, 3 \leq \text{Atten} \leq 12$   |     | -74  |     |      |
|                          |  | $f_{\text{IN}} = 3610 \text{ MHz}, 3 \leq \text{Atten} \leq 12$   |     | -77  |     |      |
|                          |  | $f_{\text{IN}} = 4920 \text{ MHz}, 3 \leq \text{Atten} \leq 12$   |     | -76  |     |      |
|                          |  | $f_{\text{IN}} = 8150 \text{ MHz}, 3 \leq \text{Atten} \leq 12$ , 25MHz tone spacing  |     | -59  |     |      |
|                          |  | $f_{\text{IN}} = 9610 \text{ MHz}, 3 \leq \text{Atten} \leq 12$ , 25MHz tone spacing  |     | -60  |     |      |

## 6.5 RF ADC Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1500MSPS above 6GHz input frequency,  $f_{\text{ADC}} = 2949.12\text{MHz}$ ; PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$  below 6GHz input frequency and External clock mode with  $f_{\text{CLK}} = 2949.12\text{MHz}$  above 6GHz input frequency; nominal power supplies; DSA Setting =3dB; SerDes rate =24.33Gbps; unless otherwise noted.

| PARAMETER |  | TEST CONDITIONS  | MIN | TYP | MAX | UNIT |
|-----------|--|--|-----|-----|-----|------|
| SFDR      | Spurious Free Dynamic Range within output bandwidth, $A_{\text{IN}} = -3 \text{ dBFS}$ | $f_{\text{IN}} = 5 \text{ MHz}, f_{\text{ADC}} = 1500\text{MSPS}, f_{\text{NCO}} = 17\text{MHz}$ , Decimate by 48    |     | 78  |     | dBFS |
|           |  | $f_{\text{IN}} = 30 \text{ MHz}, f_{\text{ADC}} = 1500\text{MSPS}, f_{\text{NCO}} = 30\text{MHz}$ , Decimate by 24   |     | 100 |     |      |
|           |  | $f_{\text{IN}} = 410 \text{ MHz}, f_{\text{ADC}} = 3000\text{MSPS}, f_{\text{NCO}} = 400\text{MHz}$ , Decimate by 24 |     | 94  |     |      |
|           |  | $f_{\text{IN}} = 830 \text{ MHz}$  |     | 88  |     |      |
|           |  | $f_{\text{IN}} = 1760 \text{ MHz}$   |     | 81  |     |      |
|           |  | $f_{\text{IN}} = 2610 \text{ MHz}$   |     | 88  |     |      |
|           |  | $f_{\text{IN}} = 3610 \text{ MHz}$   |     | 84  |     |      |
|           |  | $f_{\text{IN}} = 4910 \text{ MHz}$   |     | 79  |     |      |
|           |  | $f_{\text{IN}} = 8150 \text{ MHz}$   |     | 78  |     |      |
| HD2       | 2nd Harmonic Distortion $A_{\text{IN}} = -3 \text{ dBFS}^{(2)}$                        | $f_{\text{IN}} = 5 \text{ MHz}, f_{\text{ADC}} = 1500\text{MSPS}, f_{\text{NCO}} = 17\text{MHz}$ , Decimate by 48    |     | -84 |     | dBFS |
|           |  | $f_{\text{IN}} = 30 \text{ MHz}, f_{\text{ADC}} = 1500\text{MSPS}$ , Bypass Mode (TI only test mode)                 |     | -91 |     |      |
|           |  | $f_{\text{IN}} = 410 \text{ MHz}, f_{\text{ADC}} = 3000\text{MSPS}$ , Bypass Mode (TI only test mode)                |     | -90 |     |      |
|           |  | $f_{\text{IN}} = 830 \text{ MHz}$  |     | -86 |     |      |
|           |  | $f_{\text{IN}} = 1760 \text{ MHz}$   |     | -90 |     |      |
|           |  | $f_{\text{IN}} = 2610 \text{ MHz}$   |     | -88 |     |      |
|           |  | $f_{\text{IN}} = 3610 \text{ MHz}$   |     | -87 |     |      |
|           |  | $f_{\text{IN}} = 4910 \text{ MHz}$   |     | -84 |     |      |
|           |  | $f_{\text{IN}} = 8150 \text{ MHz}$   |     | -70 |     |      |
| HD3       | 3rd Harmonic Distortion $A_{\text{IN}} = -3 \text{ dBFS}$                              | $f_{\text{IN}} = 5 \text{ MHz}, f_{\text{ADC}} = 1500\text{MSPS}, f_{\text{NCO}} = 17\text{MHz}$ , Decimate by 48    |     | -78 |     | dBFS |
|           |  | $f_{\text{IN}} = 30 \text{ MHz}, f_{\text{ADC}} = 1500\text{MSPS}$ , Bypass Mode (TI only test mode)                 |     | -96 |     |      |
|           |  | $f_{\text{IN}} = 410 \text{ MHz}, f_{\text{ADC}} = 3000\text{MSPS}$ , Bypass Mode (TI only test mode)                |     | -94 |     |      |
|           |  | $f_{\text{IN}} = 830 \text{ MHz}$  |     | -80 |     |      |
|           |  | $f_{\text{IN}} = 1760 \text{ MHz}$   |     | -85 |     |      |
|           |  | $f_{\text{IN}} = 2610 \text{ MHz}$   |     | -86 |     |      |
|           |  | $f_{\text{IN}} = 3610 \text{ MHz}$   |     | -78 |     |      |
|           |  | $f_{\text{IN}} = 4910 \text{ MHz}$   |     | -75 |     |      |
|           |  | $f_{\text{IN}} = 8150 \text{ MHz}$   |     | -70 |     |      |
|           |  | $f_{\text{IN}} = 9610 \text{ MHz}$   |     | -70 |     |      |

## 6.5 RF ADC Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1500MSPS above 6GHz input frequency,  $f_{\text{ADC}} = 2949.12\text{MHz}$ ; PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$  below 6GHz input frequency and External clock mode with  $f_{\text{CLK}} = 2949.12\text{MHz}$  above 6GHz input frequency; nominal power supplies; DSA Setting =3dB; SerDes rate =24.33Gbps; unless otherwise noted.

| PARAMETER | TEST CONDITIONS  | MIN | TYP  | MAX | UNIT |
|-----------|--|-----|------|-----|------|
| HDn, n>3  | $f_{\text{IN}} = 5 \text{ MHz}, f_{\text{ADC}} = 1500\text{MSPS}, f_{\text{NCO}} = 17\text{MHz}$ , Decimate by 48    |     | -94  |     | dBFS |
|           | $f_{\text{IN}} = 30 \text{ MHz}, f_{\text{ADC}} = 1500\text{MSPS}, f_{\text{NCO}} = 30\text{MHz}$ , Decimate by 24   |     | -94  |     |      |
|           | $f_{\text{IN}} = 410 \text{ MHz}, f_{\text{ADC}} = 3000\text{MSPS}, f_{\text{NCO}} = 400\text{MHz}$ , Decimate by 24 |     | -94  |     |      |
|           | $f_{\text{IN}} = 830 \text{ MHz}$  |     | -88  |     |      |
|           | $f_{\text{IN}} = 1760 \text{ MHz}$   |     | -81  |     |      |
|           | $f_{\text{IN}} = 2610 \text{ MHz}$   |     | -88  |     |      |
|           | $f_{\text{IN}} = 3610 \text{ MHz}$   |     | -84  |     |      |
|           | $f_{\text{IN}} = 4910 \text{ MHz}$   |     | -82  |     |      |
|           | $f_{\text{IN}} = 8150 \text{ MHz}$   |     | -78  |     |      |
| SFDR      | $f_{\text{IN}} = 9610 \text{ MHz}$   |     | -71  |     | dBFS |
|           | $f_{\text{IN}} = 5 \text{ MHz}, f_{\text{ADC}} = 1500\text{MSPS}, f_{\text{NCO}} = 17\text{MHz}$ , Decimate by 48    |     | 101  |     |      |
|           | $f_{\text{IN}} = 30 \text{ MHz}, f_{\text{ADC}} = 1500\text{MSPS}, f_{\text{NCO}} = 30\text{MHz}$ , Decimate by 24   |     | 105  |     |      |
|           | $f_{\text{IN}} = 410 \text{ MHz}, f_{\text{ADC}} = 3000\text{MSPS}, f_{\text{NCO}} = 400\text{MHz}$ , Decimate by 24 |     | 95   |     |      |
|           | $f_{\text{IN}} = 830 \text{ MHz}$  |     | 89   |     |      |
|           | $f_{\text{IN}} = 1760 \text{ MHz}$   |     | 89   |     |      |
|           | $f_{\text{IN}} = 2610 \text{ MHz}$   |     | 95   |     |      |
|           | $f_{\text{IN}} = 3610 \text{ MHz}$   |     | 87   |     |      |
|           | $f_{\text{IN}} = 4910 \text{ MHz}$   |     | 90   |     |      |
| HD2       | $f_{\text{IN}} = 8150 \text{ MHz}$   |     | 83   |     | dBFS |
|           | $f_{\text{IN}} = 9610 \text{ MHz}$   |     | 80   |     |      |
|           | $f_{\text{IN}} = 5 \text{ MHz}, f_{\text{ADC}} = 1500\text{MSPS}, f_{\text{NCO}} = 17\text{MHz}$ , Decimate by 48    |     | -104 |     |      |
|           | $f_{\text{IN}} = 30 \text{ MHz}, f_{\text{ADC}} = 1500\text{MSPS}$ , Bypass Mode (TI only test mode)                 |     | -91  |     |      |
|           | $f_{\text{IN}} = 410 \text{ MHz}, f_{\text{ADC}} = 3000\text{MSPS}$ , Bypass Mode (TI only test mode)                |     | -104 |     |      |
|           | $f_{\text{IN}} = 830 \text{ MHz}$ , with board trim  |     | -79  |     |      |
|           | $f_{\text{IN}} = 1760 \text{ MHz}$ , with board trim   |     | -102 |     |      |
|           | $f_{\text{IN}} = 2610 \text{ MHz}$ , with board trim   |     | -100 |     |      |
|           | $f_{\text{IN}} = 3610 \text{ MHz}$ , with board trim   |     | -101 |     |      |
|           | $f_{\text{IN}} = 4910 \text{ MHz}$ , with board trim   |     | -99  |     |      |
|           | $f_{\text{IN}} = 8150 \text{ MHz}$ , with board trim   |     | -107 |     |      |
|           | $f_{\text{IN}} = 9610 \text{ MHz}$ , with board trim   |     | -107 |     |      |

## 6.5 RF ADC Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; RX Output Rate = 491.52MSPS below 6GHz input frequency and 1500MSPS above 6GHz input frequency,  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$  below 6GHz input frequency and External clock mode with  $f_{\text{CLK}} = 2949.12\text{MHz}$  above 6GHz input frequency; nominal power supplies; DSA Setting =3dB; SerDes rate =24.33Gbps; unless otherwise noted.

| PARAMETER             |   | TEST CONDITIONS   | MIN | TYP  | MAX | UNIT |
|-----------------------|---|---|-----|------|-----|------|
| HD3                   | 3rd Harmonic Distortion<br>$A_{\text{IN}} = -13 \text{ dBFS}$                         | $f_{\text{IN}} = 5 \text{ MHz}, f_{\text{ADC}} = 1500\text{MSPS}, f_{\text{NCO}} = 17\text{MHz}$ , Decimate by 48       |     | -103 |     | dBFS |
|                       |   | $f_{\text{IN}} = 30 \text{ MHz}, f_{\text{ADC}} = 1500\text{MSPS}$ , Bypass Mode (TI only test mode)                    |     | -84  |     |      |
|                       |   | $f_{\text{IN}} = 381 \text{ MHz}, f_{\text{ADC}} = 3000\text{MSPS}$ , Bypass Mode (TI only test mode)                   |     | -91  |     |      |
|                       |   | $f_{\text{IN}} = 830 \text{ MHz}$   |     | -95  |     |      |
|                       |   | $f_{\text{IN}} = 1760 \text{ MHz}$  |     | -95  |     |      |
|                       |   | $f_{\text{IN}} = 2610 \text{ MHz}$  |     | -98  |     |      |
|                       |   | $f_{\text{IN}} = 3610 \text{ MHz}$  |     | -97  |     |      |
|                       |   | $f_{\text{IN}} = 4910 \text{ MHz}$  |     | -94  |     |      |
|                       |   | $f_{\text{IN}} = 8150 \text{ MHz}$  |     | -100 |     |      |
| HD <sub>n</sub> , n>3 | SFDR excl. HD2 and HD3<br>$A_{\text{IN}} = -13 \text{ dBFS}$                          | $f_{\text{IN}} = 5 \text{ MHz}, f_{\text{ADC}} = 1500\text{MSPS}, f_{\text{NCO}} = 17\text{MHz}$ , Decimate by 48       |     | -104 |     | dBFS |
|                       |   | $f_{\text{IN}} = 30 \text{ MHz}, f_{\text{ADC}} = 1500\text{MSPS}, f_{\text{NCO}} = 30\text{MHz}$ , Decimate by 24      |     | -105 |     |      |
|                       |   | $f_{\text{IN}} = 410 \text{ MHz}, f_{\text{ADC}} = 3000\text{MSPS}$ , $f_{\text{NCO}} = 400\text{MHz}$ , Decimate by 24 |     | -95  |     |      |
|                       |   | $f_{\text{IN}} = 830 \text{ MHz}$   |     | -89  |     |      |
|                       |   | $f_{\text{IN}} = 1760 \text{ MHz}$  |     | -89  |     |      |
|                       |   | $f_{\text{IN}} = 2610 \text{ MHz}$  |     | -95  |     |      |
|                       |   | $f_{\text{IN}} = 3610 \text{ MHz}$  |     | -90  |     |      |
|                       |   | $f_{\text{IN}} = 4910 \text{ MHz}$  |     | -90  |     |      |
|                       |   | $f_{\text{IN}} = 8150 \text{ MHz}$  |     | -83  |     |      |
| RX-RX/FB Isolation    | Near Channel:<br>1RXIN to 2RXIN<br>3RXIN to 4RXIN<br>1FBIN to 1RXIN<br>2FBIN to 3RXIN | $f_{\text{IN}} = 5 \text{ MHz}, f_{\text{ADC}} = 1500\text{MSPS}, f_{\text{NCO}} = 17\text{MHz}$ , Decimate by 48       |     | -98  |     | dB   |
|                       |   | $f_{\text{IN}} = 30 \text{ MHz}, f_{\text{ADC}} = 1500\text{MSPS}, f_{\text{NCO}} = 30\text{MHz}$ , Decimate by 24      |     | -98  |     |      |
|                       |   | $f_{\text{IN}} = 400 \text{ MHz}$   |     | -88  |     |      |
|                       |   | $f_{\text{IN}} = 830 \text{ MHz}$   |     | -77  |     |      |
|                       |   | $f_{\text{IN}} = 1760 \text{ MHz}$  |     | -71  |     |      |
|                       |   | $f_{\text{IN}} = 2610 \text{ MHz}$  |     | -74  |     |      |
|                       |   | $f_{\text{IN}} = 3610 \text{ MHz}$  |     | -77  |     |      |
|                       |   | $f_{\text{IN}} = 4910 \text{ MHz}$  |     | -65  |     |      |
|                       |   | $f_{\text{IN}} = 8150 \text{ MHz}$  |     | -68  |     |      |
|                       |   | $f_{\text{IN}} = 9610 \text{ MHz}$  |     | -68  |     |      |

- (1) The input fullscale at minimum attenuation can be reduced by adding a digital gain range to the DSA, extending the useful range of the DSA. The noise figure remains constant over the digital gain range.
- (2) After HD2 trim on specific printed circuit board.
- (3) From DSA = 3dB down to 0dB, NSD increases 1dB per DSA dB
- (4) NF increase 1dB per DSA 1dB above DSA = 3dB

## 6.6 PLL/VCO/Clock Electrical Characteristics

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; Reference clock input frequency 491.52MHz (unless otherwise noted), phase noise normalized to  $f_{\text{VCO}}$ .

| PARAMETER                      |  | TEST CONDITIONS                                       | MIN                   | TYP     | MAX | UNIT                   |
|--------------------------------|--|---|-----------------------|---------|-----|------------------------|
| $f_{\text{VCO}1}$              | VCO1 min frequency   |   |                       | 7.2     |     | GHz                    |
|                                | VCO1 max frequency   |   | 7.68                  |         |     | GHz                    |
| $f_{\text{VCO}2}$              | VCO2 min frequency   |   |                       | 8.848   |     | GHz                    |
|                                | VCO2 max frequency   |   | 9.216                 |         |     | GHz                    |
| $f_{\text{VCO}3}$              | VCO3 min frequency   |   |                       | 9.8304  |     | GHz                    |
|                                | VCO3 max frequency   |   | 10.24                 |         |     | GHz                    |
| $f_{\text{VCO}4}$              | VCO4 min frequency   |   |                       | 11.7965 |     | GHz                    |
|                                | VCO4 max frequency   |   | 12.288                |         |     | GHz                    |
| $\text{DIV}_{\text{FBADC}}$    | ADC sample rate divider from VCO rate  |   | 1, 2, 3,<br>4, 6 or 8 |         |     |                        |
| $\text{DIV}_{\text{RXADC}}$    | ADC sample rate divider  |   | 1, 2, 3,<br>4, 6 or 8 |         |     |                        |
| $\text{PN}_{\text{VCO}}$       | Closed Loop Phase Noise $F_{\text{PLL}} = 11.79848 \text{ GHz } F_{\text{REF}}=491.52\text{MHz}$ | 600kHz  | -113                  |         |     | $\text{dBc}/\text{Hz}$ |
|                                |  | 800kHz  | -116                  |         |     | $\text{dBc}/\text{Hz}$ |
|                                |  | 1MHz  | -119                  |         |     | $\text{dBc}/\text{Hz}$ |
|                                |  | 1.8MHz  | -125                  |         |     | $\text{dBc}/\text{Hz}$ |
|                                |  | 5MHz  | -133                  |         |     | $\text{dBc}/\text{Hz}$ |
|                                |  | 50MHz   | -141                  |         |     | $\text{dBc}/\text{Hz}$ |
|                                | Closed Loop Phase Noise $F_{\text{PLL}}=8.84736 \text{ GHz } F_{\text{REF}}=491.52\text{MHz}$    | 600kHz  | -114                  |         |     | $\text{dBc}/\text{Hz}$ |
|                                |  | 800kHz  | -118                  |         |     | $\text{dBc}/\text{Hz}$ |
|                                |  | 1MHz  | -120                  |         |     | $\text{dBc}/\text{Hz}$ |
|                                |  | 1.8MHz  | -127                  |         |     | $\text{dBc}/\text{Hz}$ |
|                                |  | 5MHz  | -135                  |         |     | $\text{dBc}/\text{Hz}$ |
|                                |  | 50MHz   | -142                  |         |     | $\text{dBc}/\text{Hz}$ |
| $F_{\text{rms}}$               | Clock PLL integrated phase error <sup>(1)</sup>  | $f_{\text{PLL}}=11.79848 \text{ GHz, [1KHz, 100MHz]}$ | -43.4                 |         |     | $\text{dBc}/\text{Hz}$ |
|                                |  | $f_{\text{PLL}}=8.8536 \text{ GHz, [1KHz, 100MHz]}$   | -47.6                 |         |     | $\text{dBc}/\text{Hz}$ |
|                                |  | $f_{\text{PLL}}=9.8304 \text{ GHz, [1KHz, 100MHz]}$   | -46.2                 |         |     | $\text{dBc}/\text{Hz}$ |
| $f_{\text{PFD}}$               | PFD frequency  |   | 100                   | 500     |     | MHz                    |
| $\text{PN}_{\text{pll\_flat}}$ | Normalized PLL flat Noise  | $f_{\text{VCO}} = 11796.48\text{MHz}$                 | -                     | 226.5   |     | $\text{dBc}/\text{Hz}$ |
| $F_{\text{REF}}$               | Input Clock frequency  |   | 0.1                   | 12      |     | GHz                    |

## 6.6 PLL/VCO/Clock Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ; Reference clock input frequency 491.52MHz (unless otherwise noted), phase noise normalized to  $f_{\text{VCO}}$ .

| PARAMETER       |                                       | TEST CONDITIONS                             | MIN                    | TYP | MAX | UNIT                |
|-----------------|---------------------------------------|---|------------------------|-----|-----|---------------------|
| V <sub>SS</sub> | Input Clock level                     |   | 0.6                    |     | 1.8 | V <sub>ppdiff</sub> |
| Coupling        |                                       |   | AC<br>Coupling<br>Only |     |     |                     |
|                 | REFCLK input impedance <sup>(2)</sup> | Parallel resistance<br>Parallel capacitance | 100<br>0.5             |     |     | $\Omega$<br>pF      |

(1) Single Sideband, not including the reference clock contribution

(2) Refer to S11 data available from TI for impedance vs frequency

## 6.7 Digital Electrical Characteristics

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$  (unless otherwise noted)

| PARAMETER  | TEST CONDITIONS                          | MIN                              | TYP                         | MAX                         | UNIT                   |
|--|--|----------------------------------|-----------------------------|-----------------------------|------------------------|
| <b>CML SerDes Outputs [8:1]STX+/-</b>  |  |                                  |                             |                             |                        |
| $F_{\text{SerDes}}$  | SerDes Bit Rate                          | Full rate mode                   | 19                          | 29.5                        | Gbps                   |
|  |  | Half rate mode                   | 9.5                         | 16.25                       |                        |
|  |  | Quarter rate mode                | 4.75                        | 8.125                       |                        |
|  |  | 1/8 <sup>th</sup> rate mode      | 2.375                       | 4.062                       |                        |
|  |  | 1/16 <sup>th</sup> rate mode     | 1.1875                      | 2.031                       |                        |
| $T_J$  | Total Jitter Tolerance                   |                                  |                             | 0.42                        | UI                     |
| $V_{\text{STDIFF}}$  | SerDes Transmitter Output Amplitude      | differential                     | 500                         | 1000                        | mVpp                   |
| $V_{\text{STCOM}}$   | SerDes Output Common Mode                |                                  | 0.4                         | 0.45                        | 0.55                   |
| $Z_{\text{STdiff}}$  | SerDes Output Impedance                  |                                  |                             | 100                         | $\Omega$               |
| TRF  | Output rise and fall time                | 20-80%                           | 8                           |                             | ps                     |
| TTJ  | Output total jitter                      |                                  |                             | 0.21                        | UI                     |
| <b>CMOS I/O: GPIO{B/C/D/E}x, SPICLK, SPISDIO, SPISDO, SPISEN, RESETZ, BISTB0, BISTB1</b> |  |                                  |                             |                             |                        |
| $V_{\text{IH}}$  | High-Level Input Voltage                 |                                  | 0.6 $\times$ VDD1<br>P8GPIO |                             | V                      |
| $V_{\text{IL}}$  | Low-Level Input Voltage                  |                                  |                             | 0.4 $\times$ VDD1<br>P8GPIO | V                      |
| $I_{\text{IH}}$  | High-Level Input Current                 |                                  | - 250                       | 250                         | $\mu\text{A}$          |
| $I_{\text{IL}}$  | Low-Level Input Current                  |                                  | - 250                       | 250                         | $\mu\text{A}$          |
| $C_L$  | CMOS input capacitance                   |                                  |                             | 2                           | pF                     |
| $V_{\text{OH}}$  | High-Level Output Voltage                |                                  | VDD1P8G<br>PIO - 0.2        |                             | V                      |
| $V_{\text{OL}}$  | Low-Level Output Voltage                 |                                  |                             | 0.2                         | V                      |
| <b>Differential Inputs: SYSREF+/- Mode A</b>   |  |                                  |                             |                             |                        |
| $F_{\text{SYSREFMAX}}$   | SYSREF Input Frequency Maximum           |                                  | 40                          |                             | MHz                    |
| $V_{\text{SWINGSRMAX}}$  | SYSREF Input Swing Maximum               |                                  | 1.8                         |                             | Vppdiff <sup>(2)</sup> |
| $V_{\text{SWINGSRMIN}}$  | SYSREF Input Swing Minimum               | $f_{\text{REF}} < 500\text{MHz}$ | 0.3                         |                             | Vppdiff <sup>(2)</sup> |
| $V_{\text{SWINGSRMIN}}$  | SYSREF Input Swing Minimum               | $f_{\text{REF}} > 500\text{MHz}$ | 0.6                         |                             | Vppdiff <sup>(2)</sup> |
| $V_{\text{COMSRMAX}}$  | SYSREF Input Common Mode Voltage Maximum |                                  | 0.8                         |                             | V                      |
| $V_{\text{COMSRMIN}}$  | SYSREF Input Common Mode Voltage Minimum |                                  | 0.6                         |                             | V                      |
| $Z_T$  | Input termination                        | differential                     | 100 <sup>(1)</sup>          |                             | $\Omega$               |
| $C_L$  | Input capacitance                        | Each pin to GND                  | 0.5                         |                             | pF                     |
| <b>LVDS Inputs: 0SYNCIN+/- and 1SYNCIN+/-</b>  |  |                                  |                             |                             |                        |
| $V_{\text{ICOM}}$  | Input Common Voltage                     |                                  | 1.2                         |                             | V                      |
| $V_{\text{ID}}$  | Differential Input Voltage swing         |                                  | 450                         |                             | Vppdiff <sup>(2)</sup> |
| $Z_T$  | Input termination                        | differential                     | 100                         |                             | $\Omega$               |
| <b>LVDS Outputs: 0SYNCOUT+/- and 1SYNCOUT+/-</b>   |  |                                  |                             |                             |                        |
| $V_{\text{OCOM}}$  | Output Common Voltage                    |                                  | 1.2                         |                             | V                      |
| $V_{\text{OD}}$  | Differential Output Voltage swing        |                                  | 500                         |                             | Vppdiff <sup>(2)</sup> |
| $Z_T$  | Internal Termination                     |                                  | 100                         |                             | $\Omega$               |

(1) SYSREF termination is programmable between  $100\ \Omega$ ,  $150\ \Omega$  and  $300\ \Omega$

(2) Vppdiff is the difference between the maximum differential voltage (positive value) and minimum differential voltage (negative value).

## 6.8 Power Supply Electrical Characteristics

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ;  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

| PARAMETER         | TEST CONDITIONS   | MIN  | TYP  | MAX | UNIT |
|-------------------|---|--|------|-----|------|
| $I_{VDD1P8}$      | Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX                                |  | 673  |     | mA   |
|                   |   |  |      |     |      |
|                   |   |  |      |     |      |
| $I_{VDD1P2}$      | Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8 | Mode 1: 4R, $f_{\text{ADC}} = 3\text{ GSPS}$ , $\text{DDC}_{\text{RX}} = 6x$ Decimation, $f_{\text{RX}} = 1.85\text{ GHz}$ , 8b/10b coding, 20 Gbps, RX: 4-8-4-1   | 376  |     | mA   |
|                   | Group 3C: VDD1P8PLL + VDD1P8PLLVCO                                      |  |      |     |      |
|                   | Group 2A: VDD1P2FB + VDD1P2RX   |  | 17.5 |     | mA   |
|                   | Group 2B: VDD1P2TXCLK + VDD1P2TXENC                                     |  |      |     |      |
| $I_{VDD0P9}$      | Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF                   |  | 557  |     | mA   |
|                   | Group 1A: DVDD0P9 + VDDT0P9   |  |      |     |      |
| $P_{\text{diss}}$ | Power Dissipation   |  | 75   |     | mA   |
| $I_{VDD1P8}$      | Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX                                |  | 68   |     | mA   |
|                   | Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8 |  |      |     |      |
|                   | Group 3C: VDD1P8PLL + VDD1P8PLLVCO                                      |  |      |     |      |
| $I_{VDD1P2}$      | Group 2A: VDD1P2FB + VDD1P2RX   | Mode 2: 4R2F, $f_{\text{ADC}} = 3\text{ GSPS}$ , $\text{DDC}_{\text{FB}} = \text{DDC}_{\text{RX}} = 6x$ Decimation, $f_{\text{RX}} = 1.85\text{ GHz}$ , 8b/10b coding, 20 Gbps, RX: 4-8-4-1, FB: 2-4-4-1 | 1582 |     | mA   |
|                   | Group 2B: VDD1P2TXCLK + VDD1P2TXENC                                     |  |      |     |      |
|                   | Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF                   |  | 4208 |     | mW   |
|                   | Group 1A: DVDD0P9 + VDDT0P9   |  |      |     |      |
| $P_{\text{diss}}$ | Power Dissipation   |  | 1006 |     | mA   |
| $I_{VDD1P8}$      | Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX                                |  | 548  |     | mA   |
|                   | Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8 |  |      |     |      |
|                   | Group 3C: VDD1P8PLL + VDD1P8PLLVCO                                      |  |      |     |      |
| $I_{VDD1P2}$      | Group 2A: VDD1P2FB + VDD1P2RX   |  | 17.5 |     | mA   |
|                   | Group 2B: VDD1P2TXCLK + VDD1P2TXENC                                     |  |      |     |      |
|                   | Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF                   |  | 839  |     | mA   |
|                   | Group 1A: DVDD0P9 + VDDT0P9   |  |      |     |      |
| $P_{\text{diss}}$ | Power Dissipation   |  | 92   |     | mA   |
| $I_{VDD1P8}$      | Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX                                |  | 68   |     | mA   |
|                   | Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8 |  |      |     |      |
|                   | Group 3C: VDD1P8PLL + VDD1P8PLLVCO                                      |  |      |     |      |
| $I_{VDD1P2}$      | Group 2A: VDD1P2FB + VDD1P2RX   | Mode 4: 4R, $f_{\text{ADC}} = 3\text{ GSPS}$ , $\text{DDC}_{\text{RX}} = 2x$ Decimation , $f_{\text{RX}} = 2.25\text{ GHz}$ , 64/66 coding, 24.75 Gbps, RX: 8-8-2-1                                      | 2174 |     | mA   |
|                   | Group 2B: VDD1P2TXCLK + VDD1P2TXENC                                     |  |      |     |      |
|                   | Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF                   |  | 5996 |     | mW   |
|                   | Group 1A: DVDD0P9 + VDDT0P9   |  |      |     |      |
| $P_{\text{diss}}$ | Power Dissipation   |  | 672  |     | mA   |
| $I_{VDD1P8}$      | Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX                                |  | 506  |     | mA   |
|                   | Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TXDAC+ VDD1P8GPIO + VDDA1P8 |  |      |     |      |
|                   | Group 3C: VDD1P8PLL + VDD1P8PLLVCO                                      |  |      |     |      |
| $I_{VDD1P2}$      | Group 2A: VDD1P2FB + VDD1P2RX   |  | 17.5 |     | mA   |
|                   | Group 2B: VDD1P2TXCLK + VDD1P2TXENC                                     |  |      |     |      |
|                   | Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF                   |  | 552  |     | mA   |
|                   | Group 1A: DVDD0P9 + VDDT0P9   |  |      |     |      |
| $P_{\text{diss}}$ | Power Dissipation   |  | 76   |     | mA   |
| $I_{VDD0P9}$      | Group 2A: VDD1P2FB + VDD1P2RX   |  | 68   |     | mA   |
|                   | Group 2B: VDD1P2TXCLK + VDD1P2TXENC                                     |  |      |     |      |
| $P_{\text{diss}}$ | Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF                   |  | 1613 |     | mA   |
|                   | Group 1A: DVDD0P9 + VDDT0P9   |  |      |     |      |
| $P_{\text{diss}}$ | Power Dissipation   |  | 4468 |     | mW   |

## 6.8 Power Supply Electrical Characteristics (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ;  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

|                   | PARAMETER   | TEST CONDITIONS   | MIN  | TYP | MAX | UNIT |
|-------------------|---|---|------|-----|-----|------|
| $I_{VDD1P8}$      | Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX                                | Mode 5: 4R2F, $f_{\text{ADC}} = 3\text{ GSPS}$ , $\text{DDC}_{\text{RX}} = 12x$ Decimation Dual Channel, $\text{DDC}_{\text{FB}} = 3x$ Decimation, $f_{\text{RX}} = 1.85$ and $2.65\text{ GHz}$ , 8b/10b coding, 20 Gbps, RX: 4-16-8-1, FB: 4-4-4-1 | 1005 |     |     | mA   |
|                   | Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TxDAC+ VDD1P8GPIO + VDDA1P8 |   | 562  |     |     | mA   |
|                   | Group 3C: VDD1P8PLL + VDD1P8PLLVCO                                      |   | 17.5 |     |     | mA   |
| $I_{VDD1P2}$      | Group 2A: VDD1P2FB + VDD1P2RX   | Mode 5: 4R2F, $f_{\text{ADC}} = 3\text{ GSPS}$ , $\text{DDC}_{\text{RX}} = 12x$ Decimation Dual Channel, $\text{DDC}_{\text{FB}} = 3x$ Decimation, $f_{\text{RX}} = 1.85$ and $2.65\text{ GHz}$ , 8b/10b coding, 20 Gbps, RX: 4-16-8-1, FB: 4-4-4-1 | 837  |     |     | mA   |
|                   | Group 2B: VDD1P2TXCLK + VDD1P2TXENC                                     |   | 92   |     |     | mA   |
|                   | Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF                   |   | 68   |     |     | mA   |
|                   | $I_{VDD0P9}$  |   | 2359 |     |     | mA   |
| $P_{\text{diss}}$ | Power Dissipation   |   | 6195 |     |     | mW   |
| $I_{VDD1P8}$      | Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX                                | Mode 6: 4R, $f_{\text{ADC}} = 3\text{ GSPS}$ , $\text{DDC}_{\text{RX}} = 12x$ Decimation Dual Channel, $f_{\text{RX}} = 1.85$ and $2.65\text{ GHz}$ , 8b/10b coding, 20 Gbps, RX: 4-16-8-1  | 671  |     |     | mA   |
|                   | Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TxDAC+ VDD1P8GPIO + VDDA1P8 |   | 374  |     |     | mA   |
|                   | Group 3C: VDD1P8PLL + VDD1P8PLLVCO                                      |   | 17.5 |     |     | mA   |
| $I_{VDD1P2}$      | Group 2A: VDD1P2FB + VDD1P2RX   | Mode 6: 4R, $f_{\text{ADC}} = 3\text{ GSPS}$ , $\text{DDC}_{\text{RX}} = 12x$ Decimation Dual Channel, $f_{\text{RX}} = 1.85$ and $2.65\text{ GHz}$ , 8b/10b coding, 20 Gbps, RX: 4-16-8-1  | 555  |     |     | mA   |
|                   | Group 2B: VDD1P2TXCLK + VDD1P2TXENC                                     |   | 75   |     |     | mA   |
|                   | Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF                   |   | 67   |     |     | mA   |
|                   | $I_{VDD0P9}$  |   | 1702 |     |     | mA   |
| $P_{\text{diss}}$ | Power Dissipation   |   | 4305 |     |     | mW   |
| $I_{VDD1P8}$      | Group 3A: VDD1P8FB + VDD1P8RX + VDD1P8TX                                | Mode 7: same configuration as mode 2, Sleep Mode. SLEEP pin is pull high.   | 16   |     |     | mA   |
|                   | Group 3B: VDD1P8FBCLK + VDD1P8RXCLK + VDD1P8TxDAC+ VDD1P8GPIO + VDDA1P8 |   | 295  |     |     | mA   |
|                   | Group 3C: VDD1P8PLL + VDD1P8PLLVCO                                      |   | 12   |     |     | mA   |
| $I_{VDD1P2}$      | Group 2A: VDD1P2FB + VDD1P2RX   | Mode 7: same configuration as mode 2, Sleep Mode. SLEEP pin is pull high.   | 4    |     |     | mA   |
|                   | Group 2B: VDD1P2TXCLK + VDD1P2TXENC                                     |   | 24   |     |     | mA   |
|                   | Group 2C: VDD1P2FBCML + VDD1P2RXCML + VDD1P2PLLCLKREF                   |   | 45   |     |     | mA   |
|                   | $I_{VDD0P9}$  |   | 156  |     |     | mA   |
| $P_{\text{diss}}$ | Power Dissipation   |   | 818  |     |     | mW   |

## 6.9 Timing Requirements

Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ;  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

|                             |   | MIN | NOM                   | MAX | UNIT |
|-----------------------------|---|-----|-----------------------|-----|------|
| <b>Timing: SYSREF+/-</b>    |   |     |                       |     |      |
| $t_s(\text{SYSREF})$        | Setup Time, SYSREF+/- Valid to Rising Edge of CLK+/-          |     | 50                    |     | ps   |
| $t_h(\text{SYSREF})$        | Hold Time, SYSREF+/- Valid after Rising Edge of CLK+/-        |     | 50                    |     | ps   |
| <b>Timing: Serial ports</b> |   |     |                       |     |      |
| $t_s(\text{SENB})$          | Setup Time, SENB to Rising Edge of SCLK                       |     | 15                    |     | ns   |
| $t_h(\text{SENB})$          | Hold Time, SENB after last Rising Edge of SCLK <sup>(1)</sup> |     | $5 + t_{\text{SCLK}}$ |     | ns   |
| $t_s(\text{SDIO})$          | Setup Time, SDIO valid to Rising Edge of SCLK                 |     | 15                    |     | ns   |
| $t_h(\text{SDIO})$          | Hold Time, SDIO valid after Rising Edge of SCLK               |     | 5                     |     | ns   |
| $t_{(\text{SCLK})_W}$       | Minimum SCLK period: registers write                          |     | 25                    |     | ns   |
| $t_{(\text{SCLK})_R}$       | Minimum SCLK period: registers read                           |     | 50                    |     | ns   |
| $t_d(\text{data\_out})$     | Minimum Data Output delay after Falling Edge of SCLK          |     | 0                     |     | ns   |
|                             | Maximum Data Output delay after Falling Edge of SCLK          |     | 15                    |     | ns   |
| $t_{\text{RESET}}$          | Minimum RESETZ Pulse Width                                    |     | 1                     |     | ms   |

(1) SDEN\ need to be held one more extra clock cycle with the last SCLK edge

## 6.10 Switching Characteristics

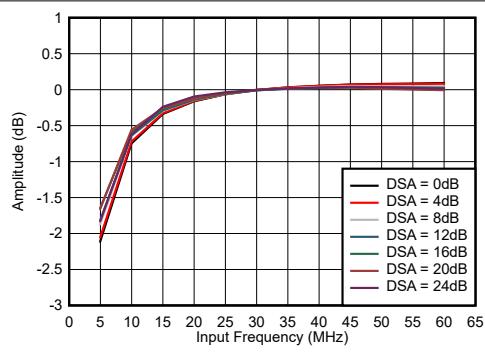
Typical values at  $T_A = +25^\circ\text{C}$ , full temperature range is  $T_{A,\text{MIN}} = -40^\circ\text{C}$  to  $T_{J,\text{MAX}} = +110^\circ\text{C}$ ;  $f_{\text{ADC}} = 2949.12\text{MSPS}$ ; nominal power supplies; 1 tone at -1 dBFS; DSA Attenuation =0dB; SerDes rate = 24.33Gbps; unless otherwise noted.

| PARAMETER                 | TEST CONDITIONS                 | MIN   | TYP | MAX | UNIT                                  |
|---------------------------|---------------------------------|---|-----|-----|---------------------------------------|
| <b>RX Channel Latency</b> |                                 |   |     |     |                                       |
| $t_{\text{JESDRX}}$       | RX input to JESD output Latency | LMFS=2-16-16-1, 122.88 MSPS, 24x Decimation, Serdes rate = 16.22Gbps (JESD204C) | 92  |     | interface clock cycles <sup>(1)</sup> |
|                           |                                 | LMFS=4-16-8-1, 245.76 MSPS, 12x Decimation, Serdes rate = 16.22Gbps (JESD204C)  | 108 |     |                                       |
|                           |                                 | LMFS=2-8-8-1, 368.64 MSPS, 8x Decimation, Serdes rate = 16.22Gbps (JESD204C)    | 118 |     |                                       |
|                           |                                 | LMFS=4-8-4-1, 491.52 MSPS, 6x Decimation, Serdes rate = 16.22Gbps (JESD204C)    | 153 |     |                                       |
| <b>FB Channel Latency</b> |                                 |   |     |     |                                       |
|                           | SerDes Transmitter Analog Delay |   | 3.6 |     | ns                                    |
| $t_{\text{JESDFB}}$       | FB input to JESD output Latency | LMFS=1-2-8-1, 368.64 MSPS, 8x Decimation  | 151 |     | interface clock cycles <sup>(1)</sup> |
|                           |                                 | LMFS=2-4-4-1, 491.52 MSPS, 6x Decimation  | 177 |     |                                       |

(1) Interface clock cycles is the period of the digital interface clock rate, e.g. 1GSPS = 1ns.

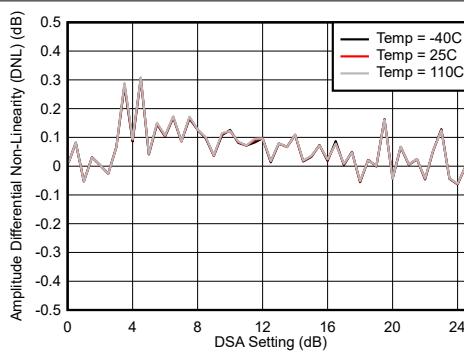
### 6.11.1 RX Typical Characteristics 30 MHz and 400 MHz

Typical values at  $T_A = +25^\circ\text{C}$ . Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with  $f_{\text{REF}} = 500 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with  $f_{\text{REF}} = 500 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 3 dB.



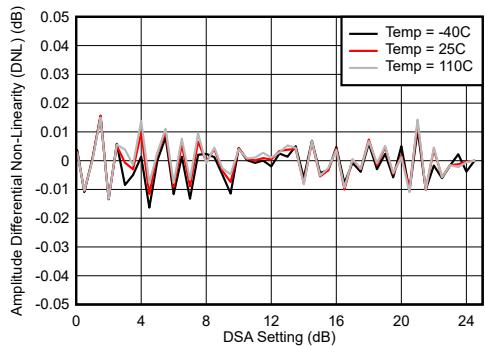
Normalized to 30 MHz

图 6-1. RX In-Band Gain Flatness,  $f_{\text{IN}} = 30 \text{ MHz}$



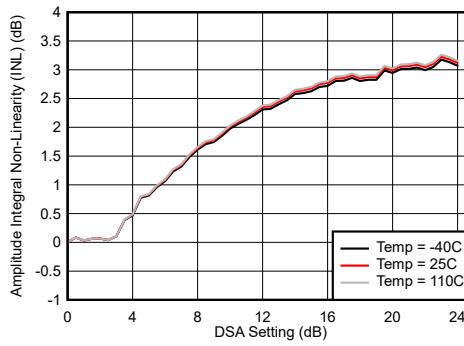
$$\text{Differential Amplitude Error} = P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$$

图 6-2. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 30 MHz



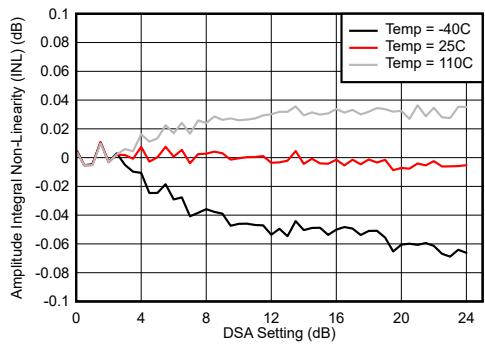
$$\text{Differential Amplitude Error} = P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$$

图 6-3. RX Calibrated Differential Amplitude Error vs DSA Setting at 30 MHz



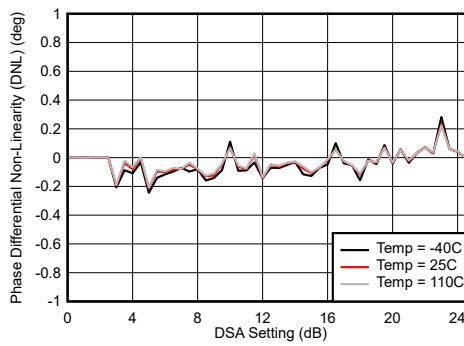
$$\text{Integrated Amplitude Error} = P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$$

图 6-4. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 30 MHz



$$\text{Integrated Amplitude Error} = P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$$

图 6-5. RX Calibrated Integrated Amplitude Error vs DSA Setting at 30 MHz

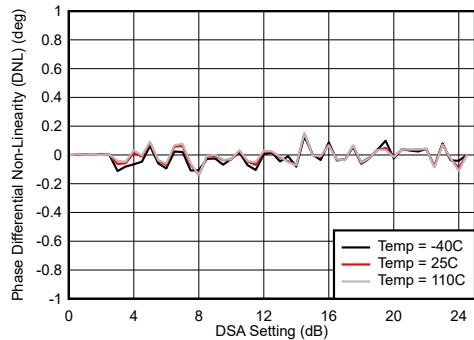


$$\text{Differential Phase Error} = \text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$$

图 6-6. RX Uncalibrated Differential Phase Error vs DSA Setting at 30 MHz

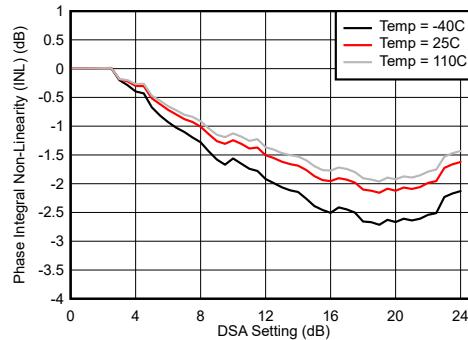
### 6.11.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ . Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with  $f_{\text{REF}} = 500 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with  $f_{\text{REF}} = 500 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 3 dB.



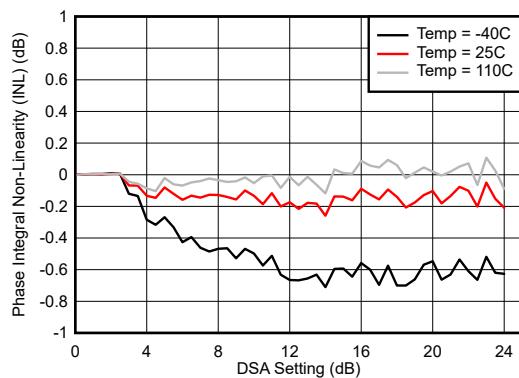
Differential Phase Error =  $\text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$

图 6-7. RX Calibrated Differential Phase Error vs DSA Setting at 30 MHz



Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

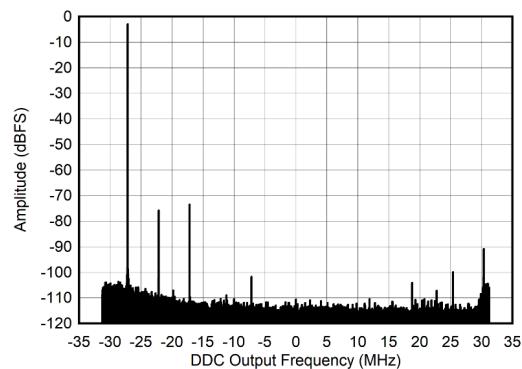
图 6-8. RX Uncalibrated Integrated Phase Error vs DSA Setting at 30 MHz



With 0.8 GHz matching

Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

图 6-9. RX Calibrated Integrated Phase Error vs DSA Setting at 30 MHz

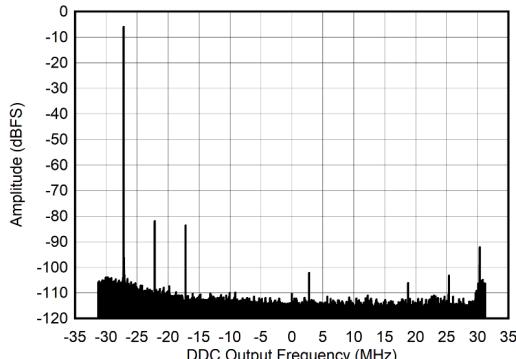


$A_{\text{IN}} = -3 \text{ dBFS}$ ,  $f_{\text{ADC}} = 1500 \text{ MSPS}$ ,  $f_{\text{NCO}} = 32.13 \text{ MHz}$ , Decimate by 24x

图 6-10. RX Output FFT at 5 MHz

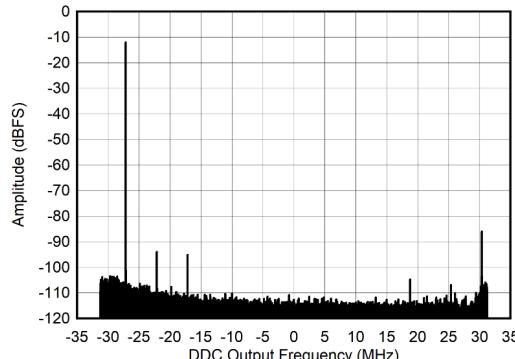
### 6.11.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ . Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with  $f_{\text{REF}} = 500 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with  $f_{\text{REF}} = 500 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 3 dB.



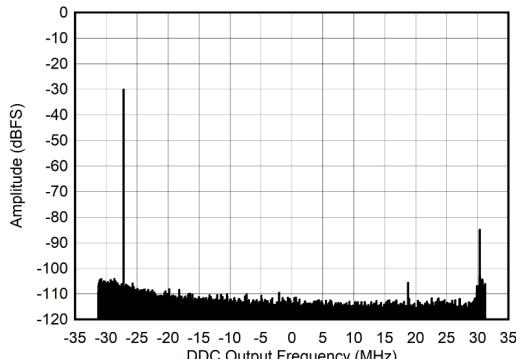
$A_{\text{IN}} = -6 \text{ dBFS}$ ,  $f_{\text{ADC}} = 1500 \text{ MSPS}$ ,  $f_{\text{NCO}} = 32.13 \text{ MHz}$ , Decimate by 24x

图 6-11. RX Output FFT at 5 MHz



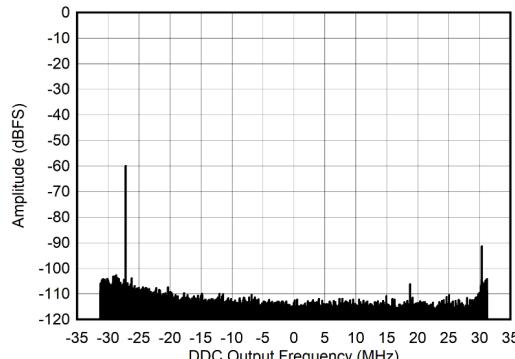
$A_{\text{IN}} = -12 \text{ dBFS}$ ,  $f_{\text{ADC}} = 1500 \text{ MSPS}$ ,  $f_{\text{NCO}} = 32.13 \text{ MHz}$ , Decimate by 24x

图 6-12. RX Output FFT at 5 MHz



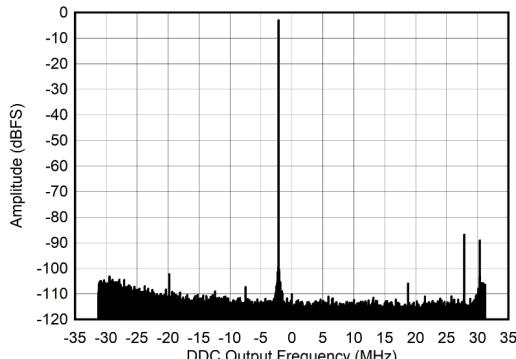
$A_{\text{IN}} = -30 \text{ dBFS}$ ,  $f_{\text{ADC}} = 1500 \text{ MSPS}$ ,  $f_{\text{NCO}} = 32.13 \text{ MHz}$ , Decimate by 24x

图 6-13. RX Output FFT at 5 MHz



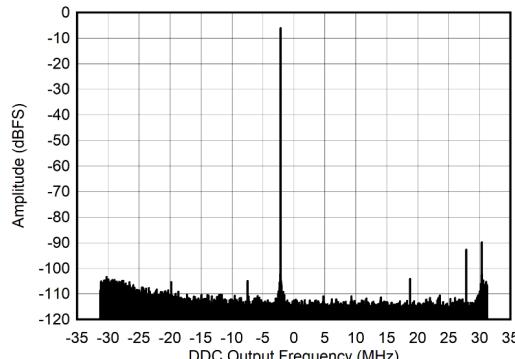
$A_{\text{IN}} = -60 \text{ dBFS}$ ,  $f_{\text{ADC}} = 1500 \text{ MSPS}$ ,  $f_{\text{NCO}} = 32.13 \text{ MHz}$ , Decimate by 24x

图 6-14. RX Output FFT at 5 MHz



$A_{\text{IN}} = -3 \text{ dBFS}$ ,  $f_{\text{ADC}} = 1500 \text{ MSPS}$ ,  $f_{\text{NCO}} = 32.13 \text{ MHz}$ , Decimate by 24x

图 6-15. RX Output FFT at 30 MHz

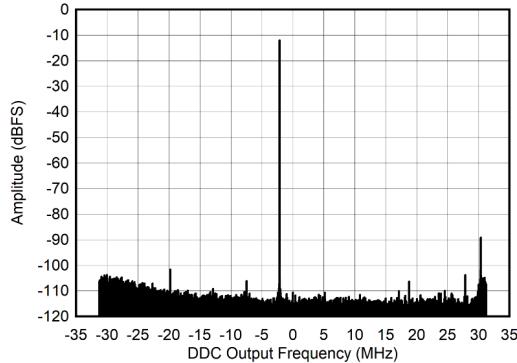


$A_{\text{IN}} = -6 \text{ dBFS}$ ,  $f_{\text{ADC}} = 1500 \text{ MSPS}$ ,  $f_{\text{NCO}} = 32.13 \text{ MHz}$ , Decimate by 24x

图 6-16. RX Output FFT at 30 MHz

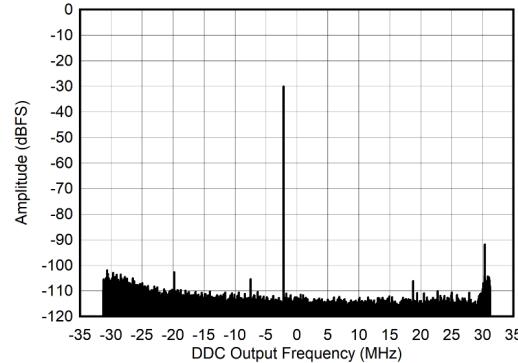
### 6.11.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ . Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with  $f_{\text{REF}} = 500 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with  $f_{\text{REF}} = 500 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 3 dB.



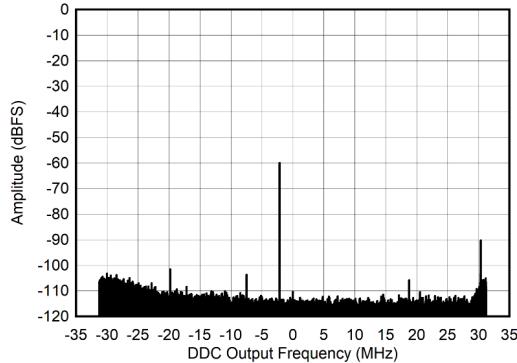
$A_{\text{IN}} = -12 \text{ dBFS}$ ,  $f_{\text{ADC}} = 1500 \text{ MSPS}$ ,  $f_{\text{NCO}} = 32.13 \text{ MHz}$ ,  
Decimate by 24x

图 6-17. RX Output FFT at 30 MHz



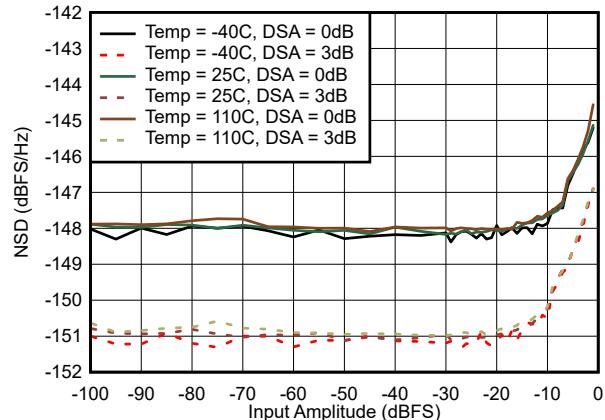
$A_{\text{IN}} = -30 \text{ dBFS}$ ,  $f_{\text{ADC}} = 1500 \text{ MSPS}$ ,  $f_{\text{NCO}} = 32.13 \text{ MHz}$ ,  
Decimate by 24x

图 6-18. RX Output FFT at 30 MHz



$A_{\text{IN}} = -60 \text{ dBFS}$ ,  $f_{\text{ADC}} = 1500 \text{ MSPS}$ ,  $f_{\text{NCO}} = 32.13 \text{ MHz}$ ,  
Decimate by 24x

图 6-19. RX Output FFT at 30 MHz

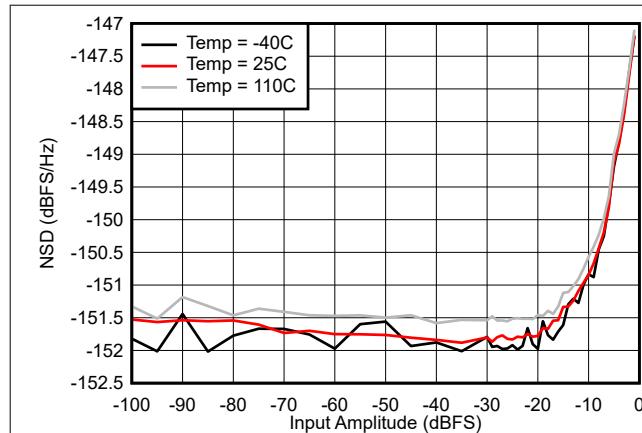


$f_{\text{ADC}} = 1500 \text{ MSPS}$ ,  $f_{\text{NCO}} = 32.13 \text{ MHz}$ , Decimate by 24x

图 6-20. NSD vs Input Amplitude at 30 MHz with DSA = 0 and 3dB

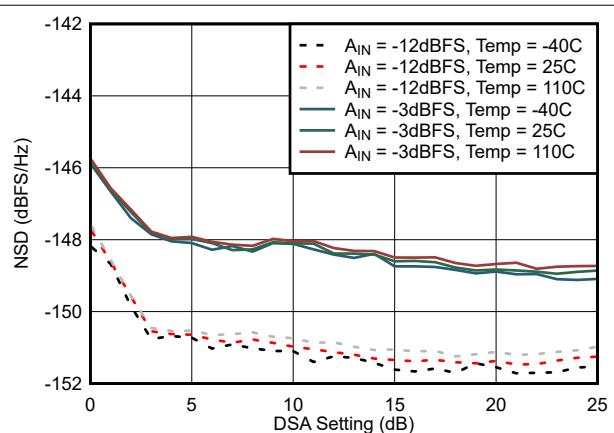
### 6.11.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ . Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with  $f_{\text{REF}} = 500 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with  $f_{\text{REF}} = 500 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 3 dB.



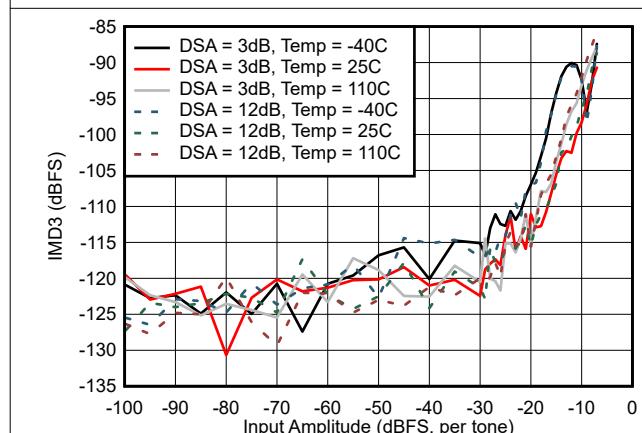
$f_{\text{ADC}} = 1500 \text{ MSPS}$ ,  $f_{\text{NCO}} = 32.13 \text{ MHz}$ , Decimate by 24x

图 6-21. NSD vs Input Amplitude at 30 MHz with DSA = 12



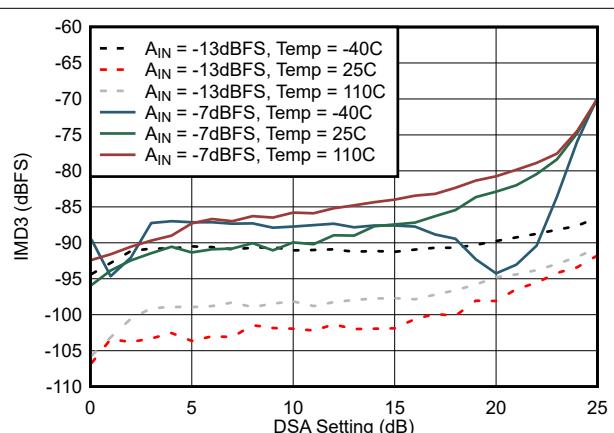
$f_{\text{ADC}} = 1500 \text{ MSPS}$ ,  $f_{\text{NCO}} = 32.13 \text{ MHz}$ , Decimate by 24x

图 6-22. NSD vs DSA Attenuation at 30 MHz



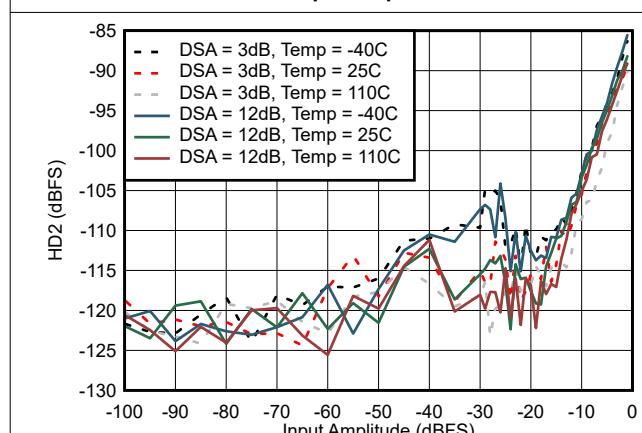
$f_{\text{ADC}} = 1500 \text{ MSPS}$ ,  $f_{\text{NCO}} = 32.13 \text{ MHz}$ , Decimate by 24x

图 6-23. IMD3 vs Input Amplitude at 30 MHz



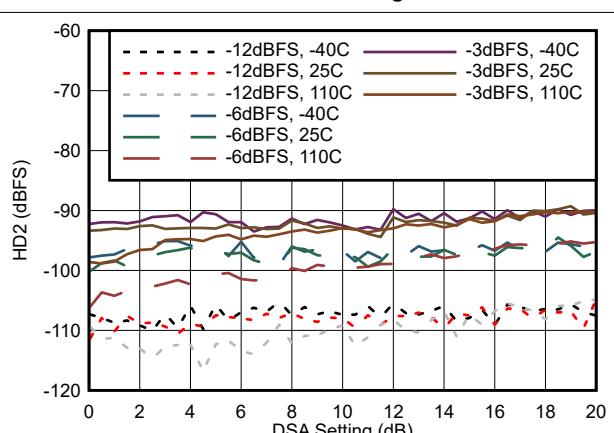
$f_{\text{ADC}} = 1500 \text{ MSPS}$ ,  $f_{\text{NCO}} = 32.13 \text{ MHz}$ , Decimate by 24x

图 6-24. IMD3 vs DSA Setting at 30 MHz



$f_{\text{ADC}} = 1500 \text{ MSPS}$ ,  $f_{\text{NCO}} = 32.13 \text{ MHz}$ , Decimate by 24x

图 6-25. HD2 vs Input Amplitude at 30 MHz



$f_{\text{ADC}} = 1500 \text{ MSPS}$ ,  $f_{\text{NCO}} = 32.13 \text{ MHz}$ , Decimate by 24x

图 6-26. HD2 vs DSA Setting at 30 MHz

### 6.11.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ . Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with  $f_{\text{REF}} = 500 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with  $f_{\text{REF}} = 500 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 3 dB.

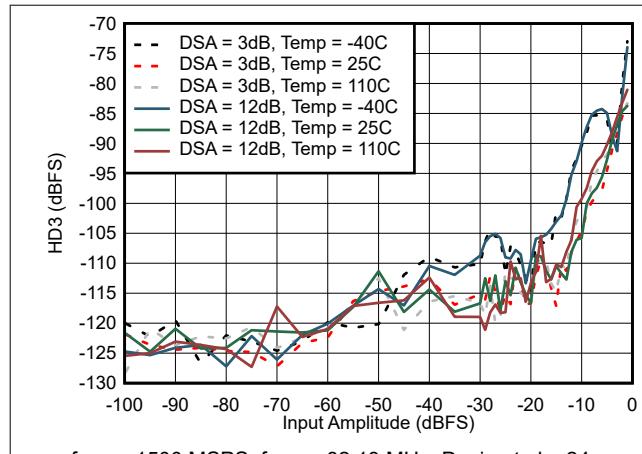


图 6-27. HD3 vs Input Amplitude at 30 MHz

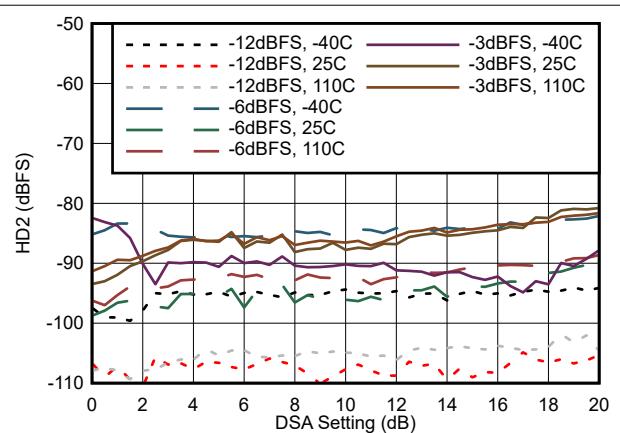


图 6-28. HD2 vs DSA Setting at 30 MHz

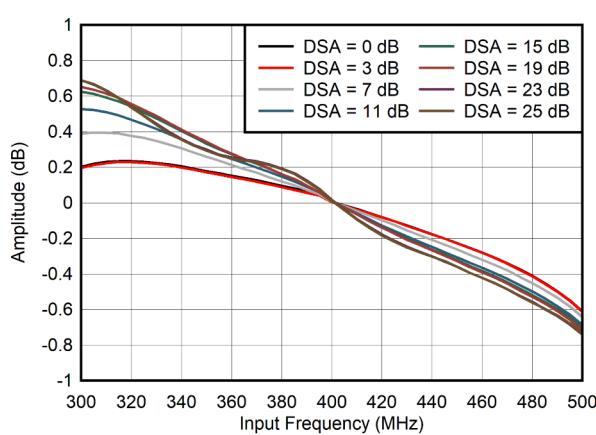


图 6-29. RX In-Band Gain Flatness,  $f_{\text{IN}} = 400 \text{ MHz}$

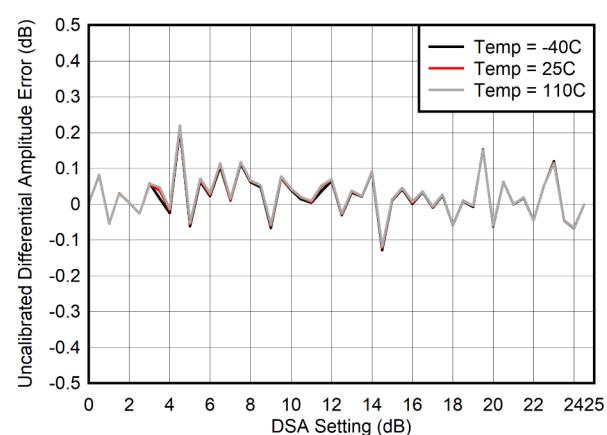
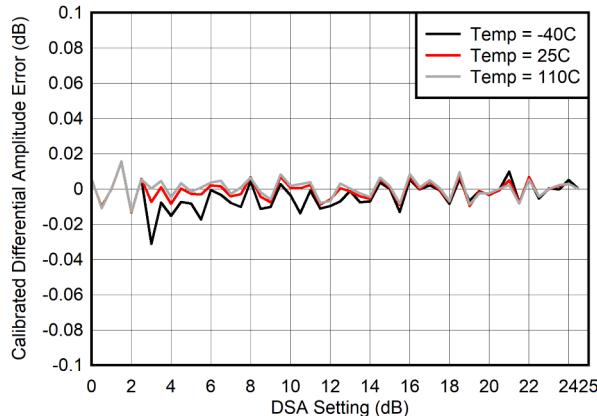


图 6-30. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 30 MHz

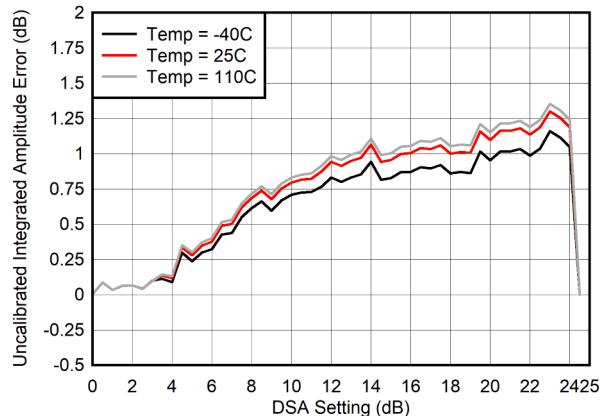
### 6.11.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ . Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with  $f_{\text{REF}} = 500 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with  $f_{\text{REF}} = 500 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 3 dB.



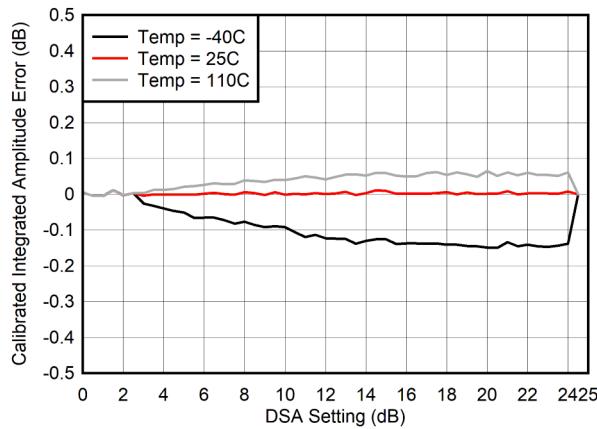
$$\text{Differential Amplitude Error} = P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$$

图 6-31. RX Calibrated Differential Amplitude Error vs DSA Setting at 400 MHz



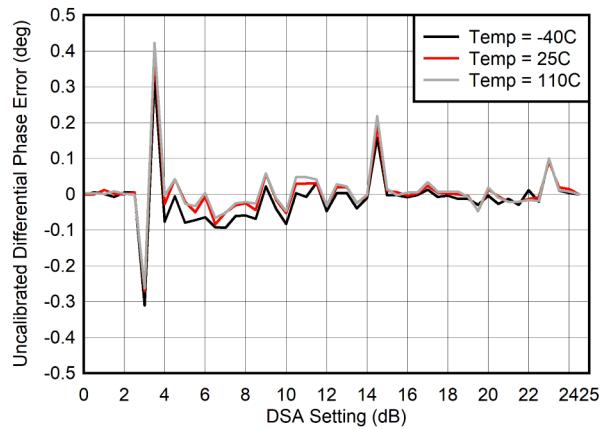
$$\text{Integrated Amplitude Error} = P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$$

图 6-32. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 400 MHz



$$\text{Integrated Amplitude Error} = P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$$

图 6-33. RX Calibrated Integrated Amplitude Error vs DSA Setting at 400 MHz

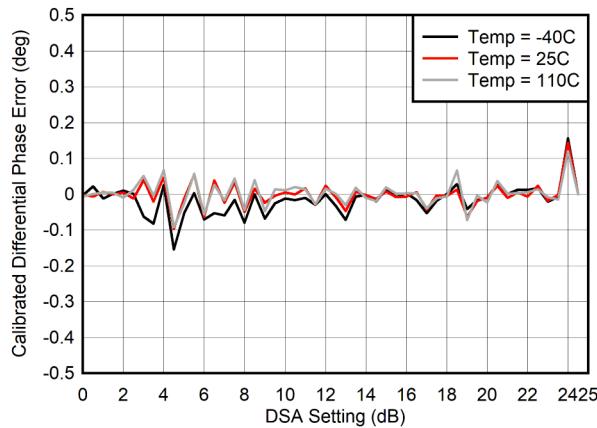


$$\text{Differential Phase Error} = \text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$$

图 6-34. RX Uncalibrated Differential Phase Error vs DSA Setting at 400 MHz

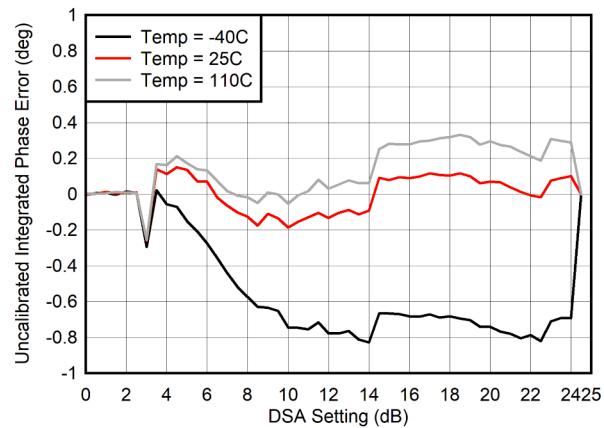
### 6.11.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ . Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with  $f_{\text{REF}} = 500 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with  $f_{\text{REF}} = 500 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 3 dB.



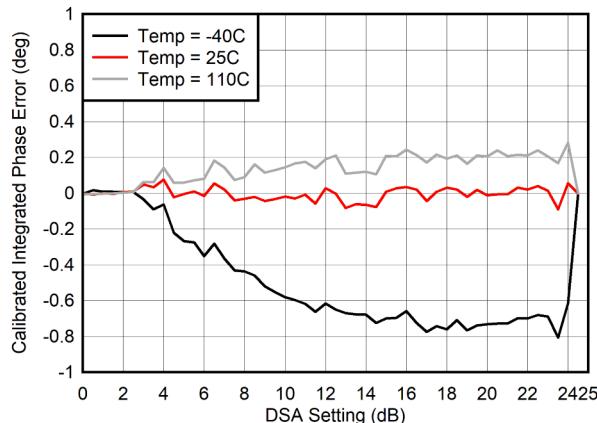
$$\text{Differential Phase Error} = \text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$$

图 6-35. RX Calibrated Differential Phase Error vs DSA Setting at 400 MHz



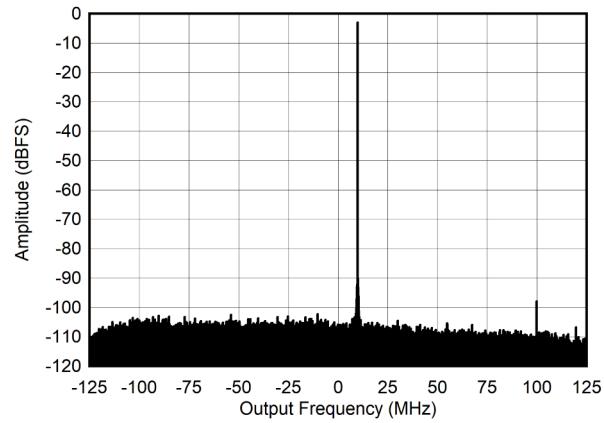
$$\text{Integrated Phase Error} = \text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$$

图 6-36. RX Uncalibrated Integrated Phase Error vs DSA Setting at 400 MHz



$$\text{Integrated Phase Error} = \text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$$

图 6-37. RX Calibrated Integrated Phase Error vs DSA Setting at 400 MHz

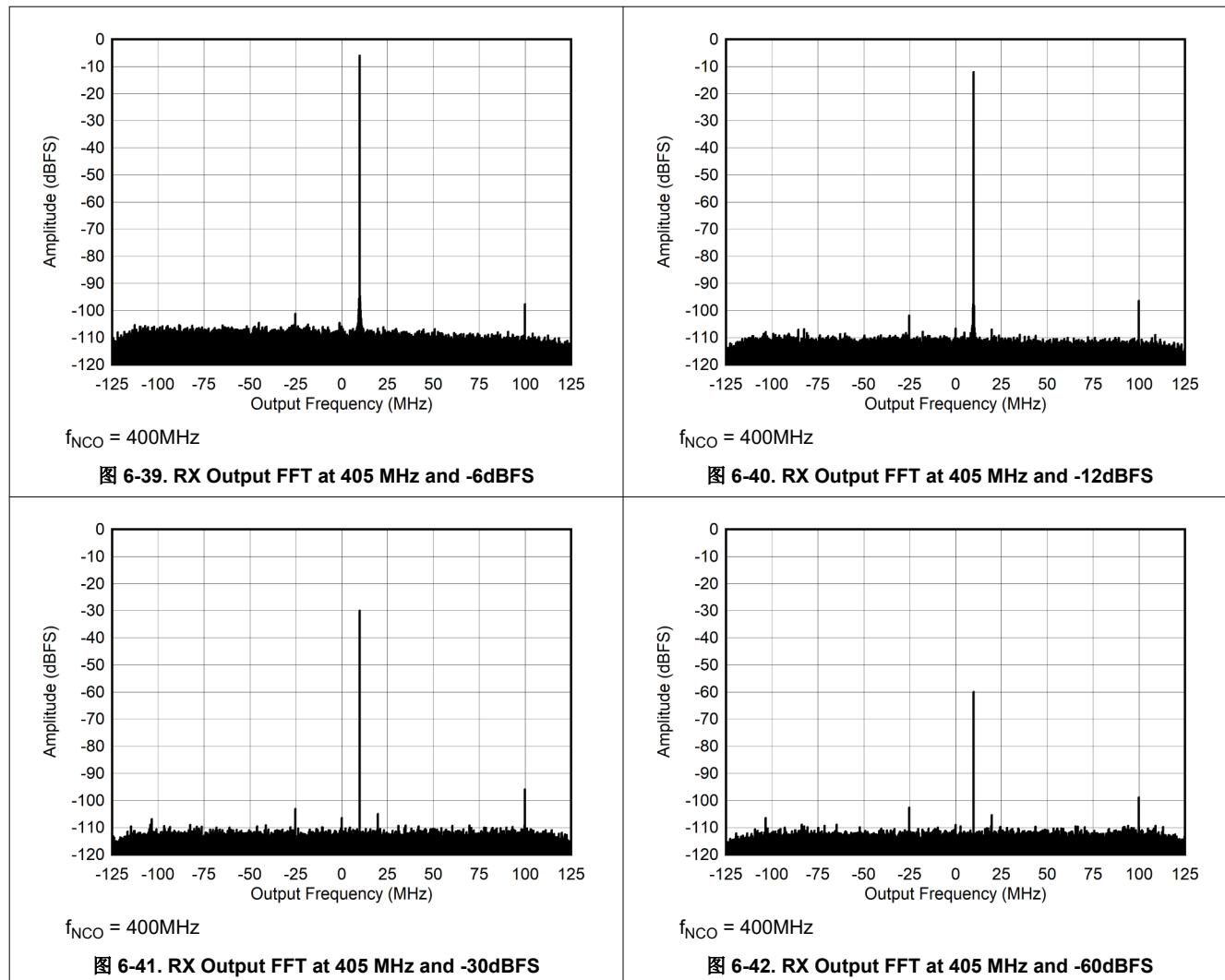


$$f_{\text{NCO}} = 400 \text{ MHz}$$

图 6-38. RX Output FFT at 405 MHz and -3dBFS

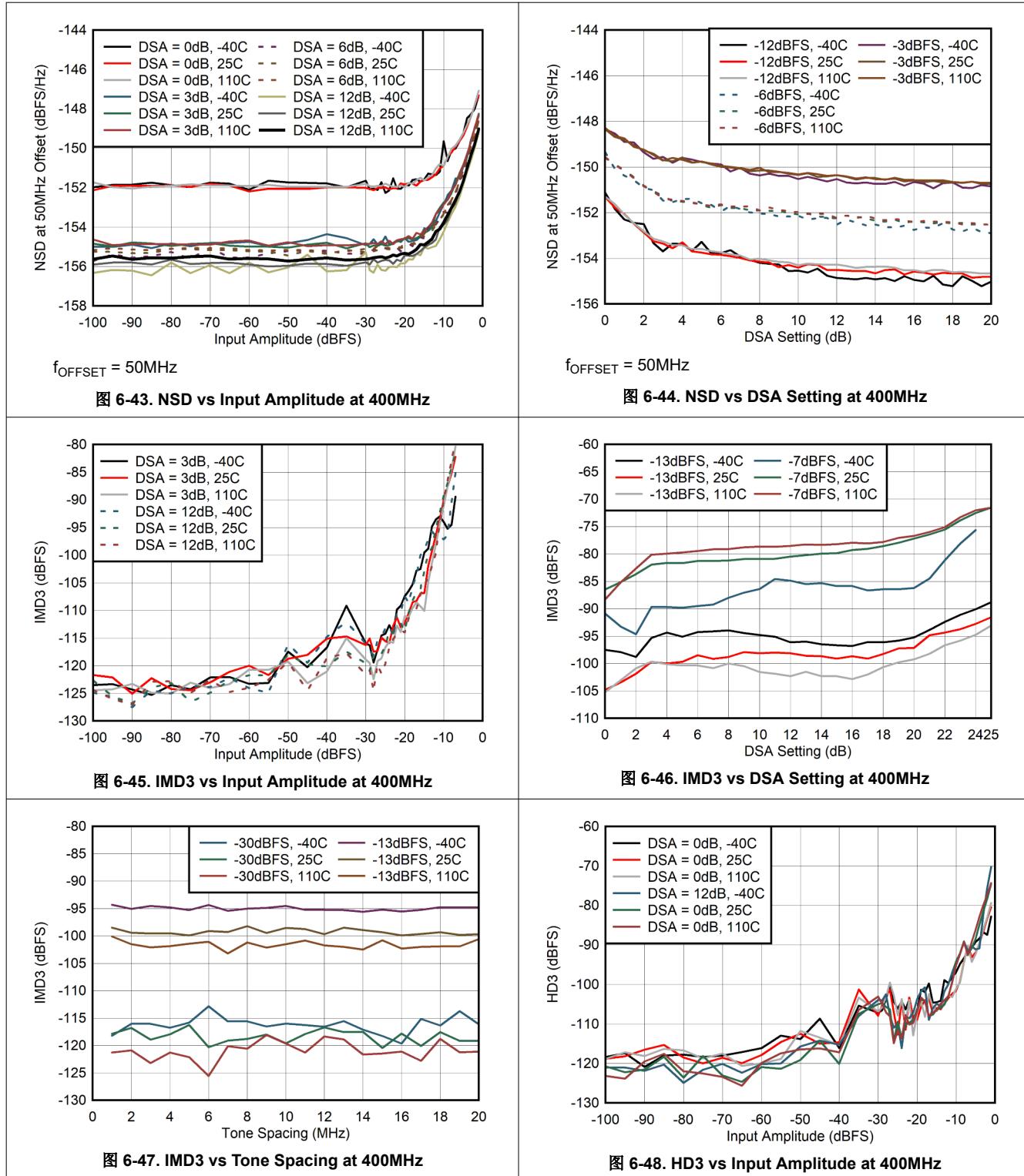
### 6.11.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ . Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with  $f_{\text{REF}} = 500 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with  $f_{\text{REF}} = 500 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 3 dB.



### 6.11.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ . Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with  $f_{\text{REF}} = 500 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with  $f_{\text{REF}} = 500 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 3 dB.



### 6.11.1 RX Typical Characteristics 30 MHz and 400 MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ . Default conditions at 30MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 62.5 MSPS (decimate by 24x), PLL clock mode with  $f_{\text{REF}} = 500 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 3 dB. Default conditions at 400 MHz: ADC Sampling Rate = 1500 MSPS, output sample rate = 125 MSPS (decimate by 12x), PLL clock mode with  $f_{\text{REF}} = 500 \text{ MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 3 dB.

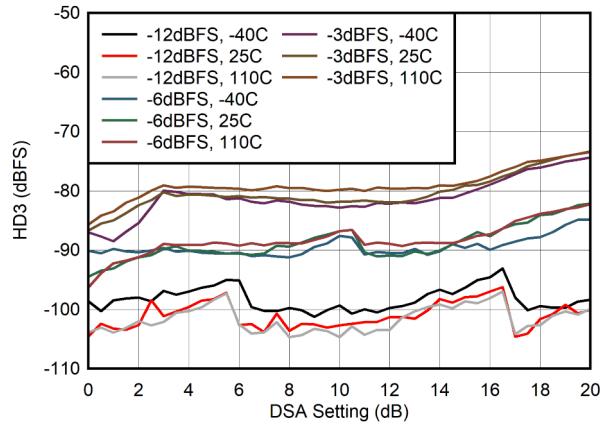
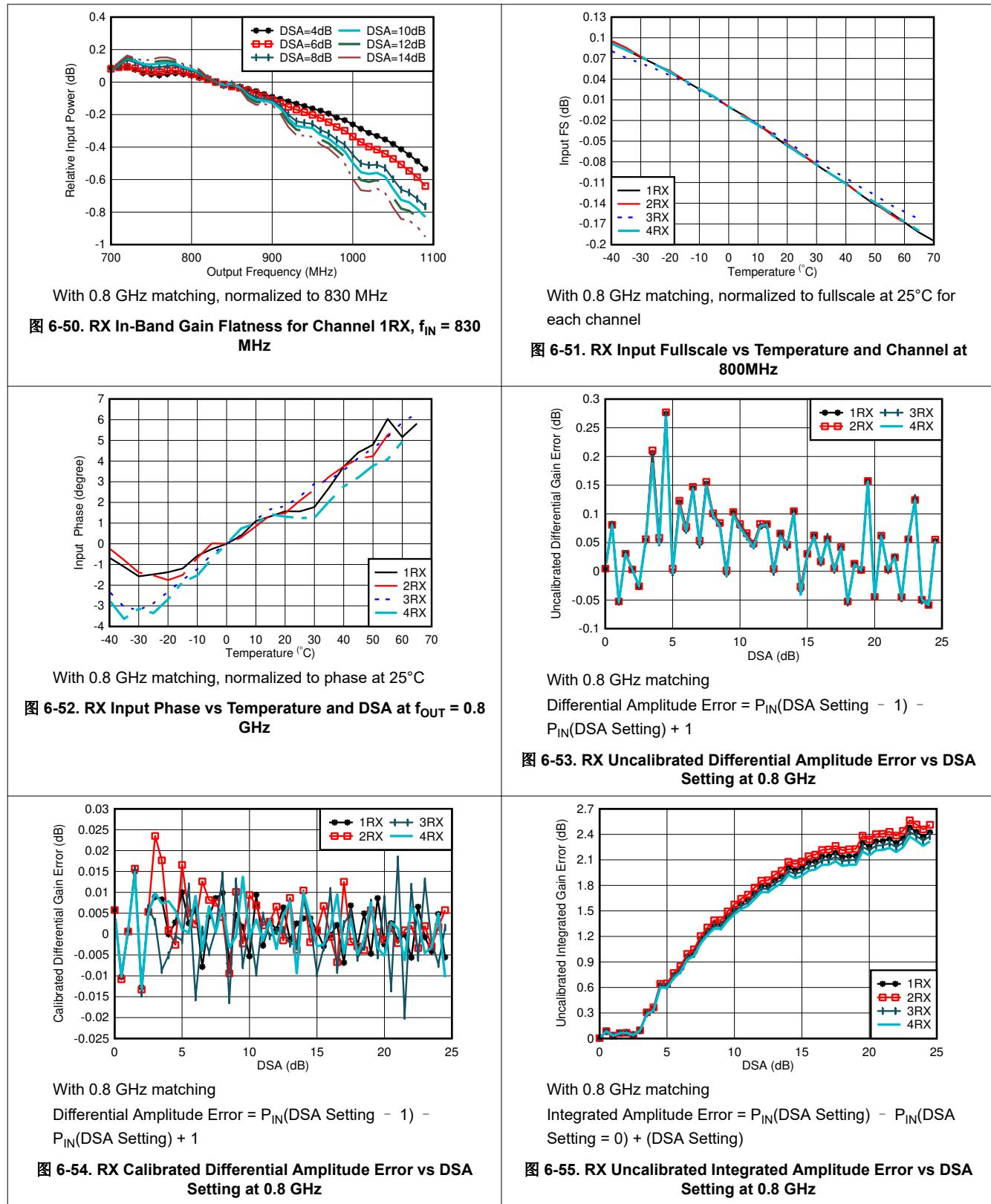


图 6-49. HD3 vs DSA Setting at 400MHz

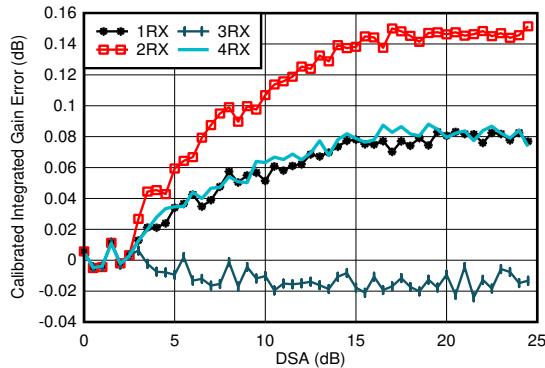
### 6.11.2 RX Typical Characteristics at 800MHz

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{IN}} = -3\text{ dBFS}$ , DSA setting = 4 dB.



### 6.11.2 RX Typical Characteristics at 800MHz (continued)

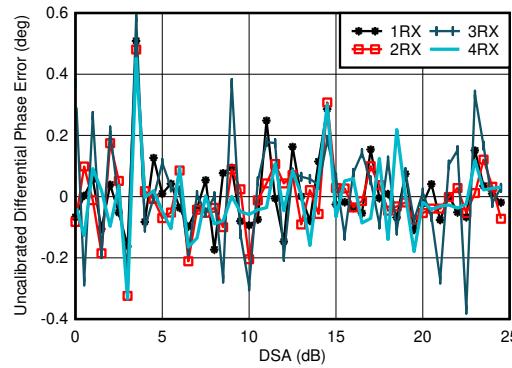
Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{IN}} = -3\text{ dBFS}$ , DSA setting = 4 dB.



With 0.8 GHz matching

Integrated Amplitude Error =  $P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

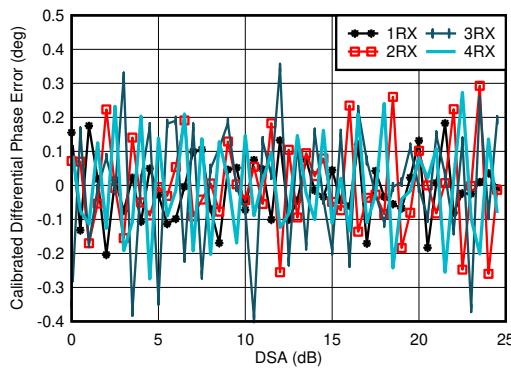
图 6-56. RX Calibrated Integrated Amplitude Error vs DSA Setting at 2.6 GHz



With 0.8 GHz matching

Differential Phase Error =  $\text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$

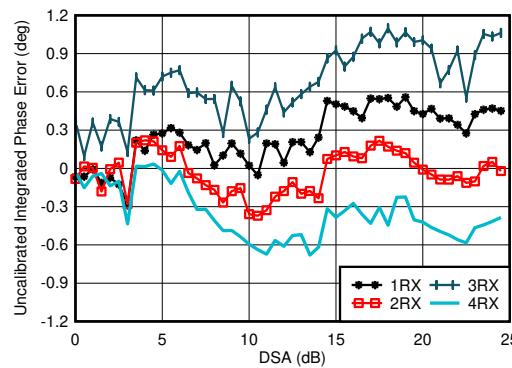
图 6-57. RX Uncalibrated Differential Phase Error vs DSA Setting at 0.8 GHz



With 0.8 GHz matching

Differential Phase Error =  $\text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$

图 6-58. RX Calibrated Differential Phase Error vs DSA Setting at 0.8 GHz



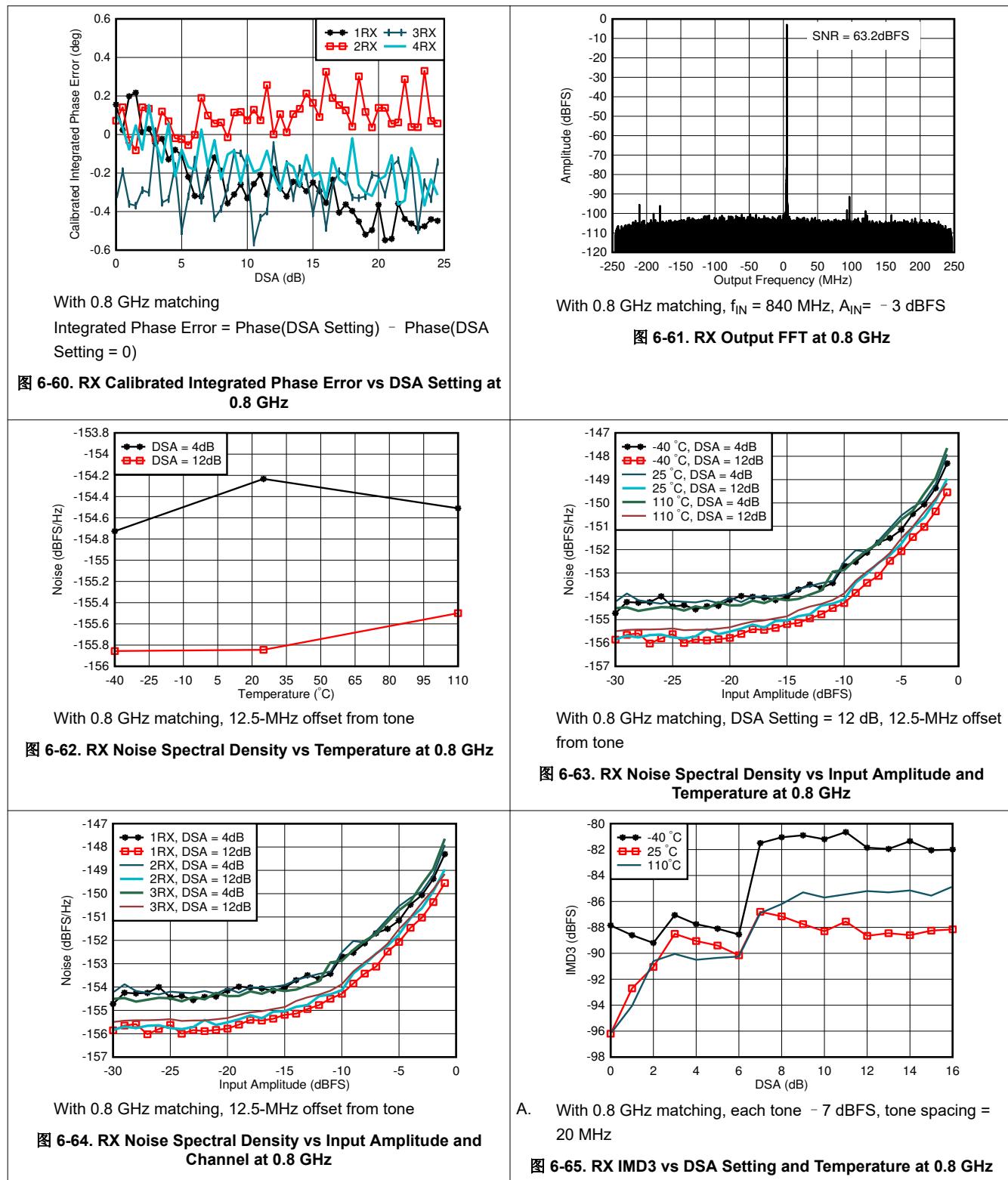
With 0.8 GHz matching

Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

图 6-59. RX Uncalibrated Integrated Phase Error vs DSA Setting at 0.8 GHz

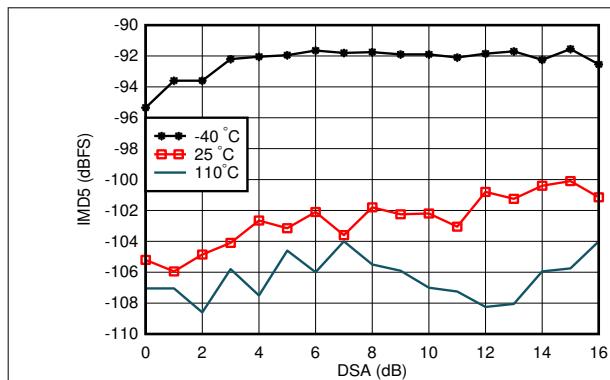
### 6.11.2 RX Typical Characteristics at 800MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{IN}} = -3\text{ dBFS}$ , DSA setting = 4 dB.



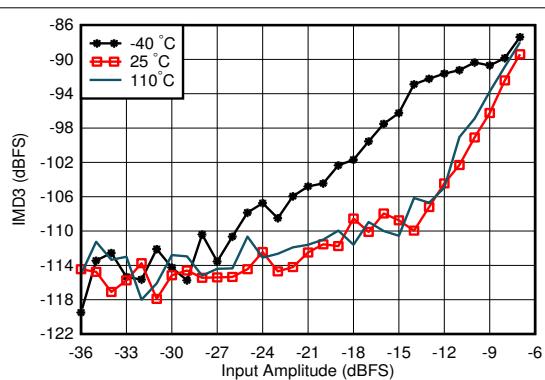
### 6.11.2 RX Typical Characteristics at 800MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{IN}} = -3\text{ dBFS}$ , DSA setting = 4 dB.



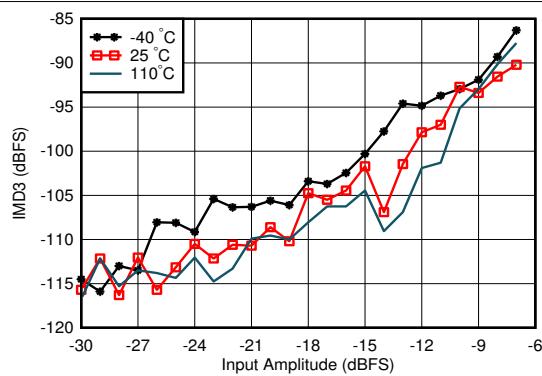
With 0.8 GHz matching, each tone  $-7\text{ dBFS}$ , tone spacing = 20 MHz

图 6-66. RX IMD5 vs DSA Setting and Temperature at 0.8 GHz



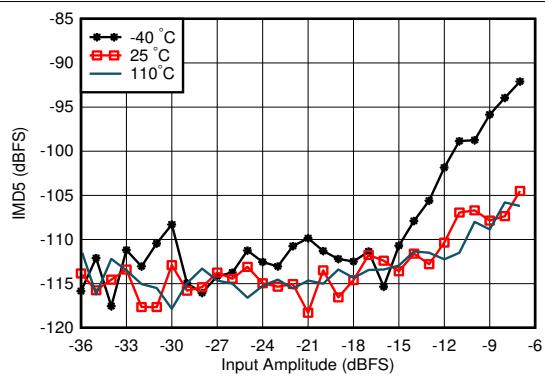
With 0.8 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

图 6-67. RX IMD3 vs Input Level and Temperature at 0.8 GHz



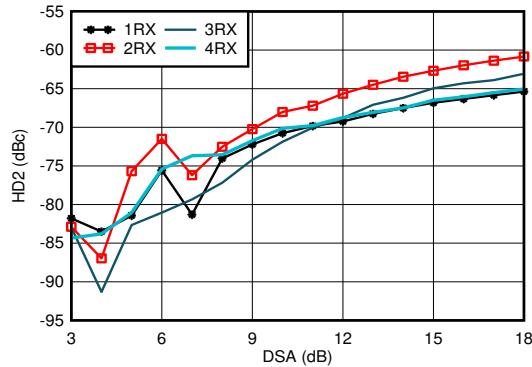
With 0.8 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

图 6-68. RX IMD3 vs Input Level and Temperature at 0.8 GHz



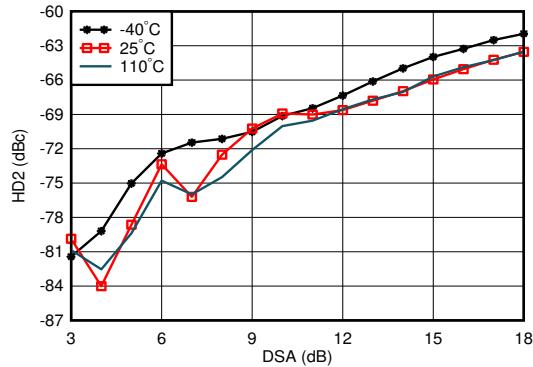
With 0.8 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

图 6-69. RX IMD5 vs Input Level and Temperature at 0.8 GHz



With 0.8 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

图 6-70. RX HD2 vs DSA Setting and Channel at 0.8 GHz

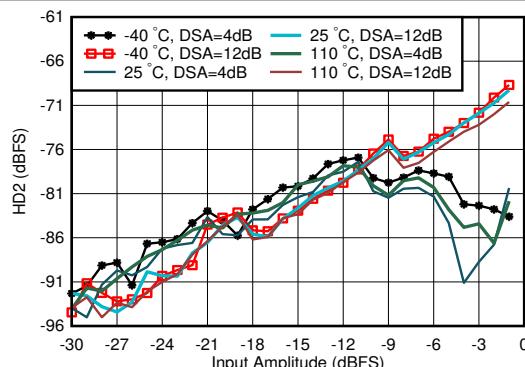


With 0.8 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

图 6-71. RX HD2 vs DSA Setting and Temperature at 0.8 GHz

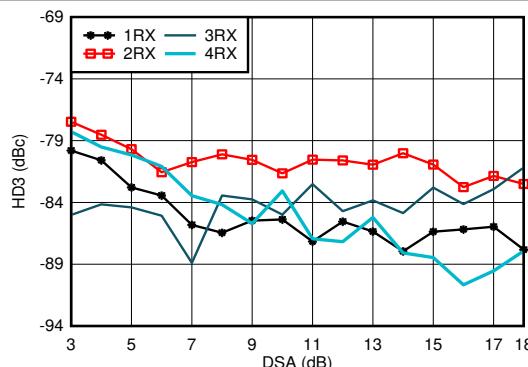
### 6.11.2 RX Typical Characteristics at 800MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{IN}} = -3\text{ dBFS}$ , DSA setting = 4 dB.



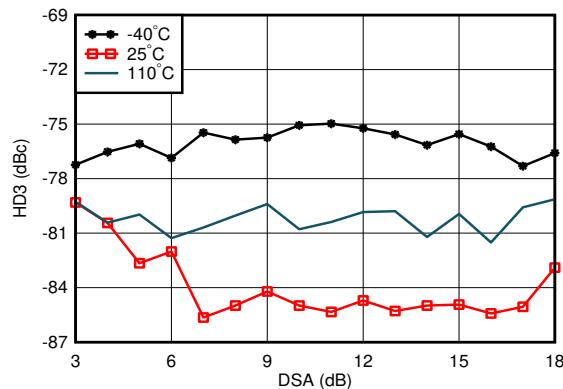
With 0.8 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

图 6-72. RX HD2 vs Input Level and Temperature at 0.8 GHz



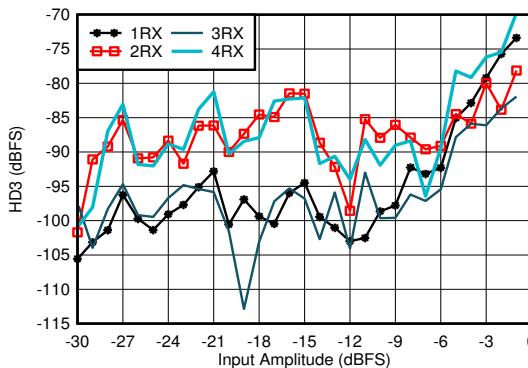
With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

图 6-73. RX HD3 vs DSA Setting and Channel at 0.8 GHz



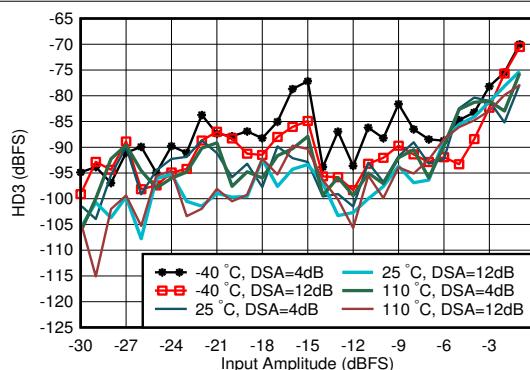
With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

图 6-74. RX HD3 vs DSA Setting and Temperature at 0.8 GHz



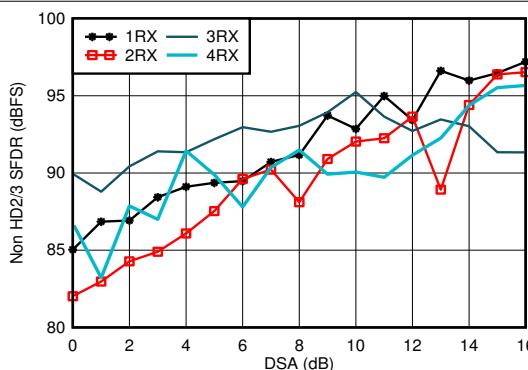
With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

图 6-75. RX HD3 vs Input Level and Channel at 0.8 GHz



With 0.8 GHz matching, DDC bypass mode (TI only mode for characterization)

图 6-76. RX HD3 vs Input Level and Temperature at 0.8 GHz

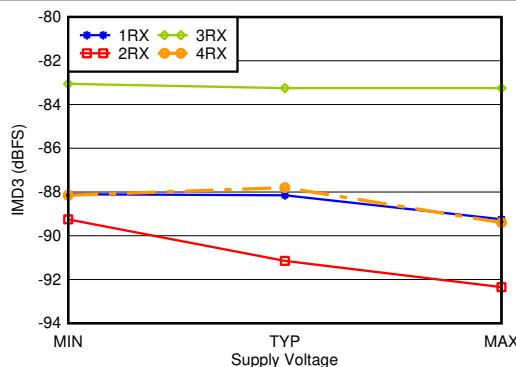


With 0.8 GHz matching

图 6-77. RX Non-HD2/3 vs DSA Setting at 0.8 GHz

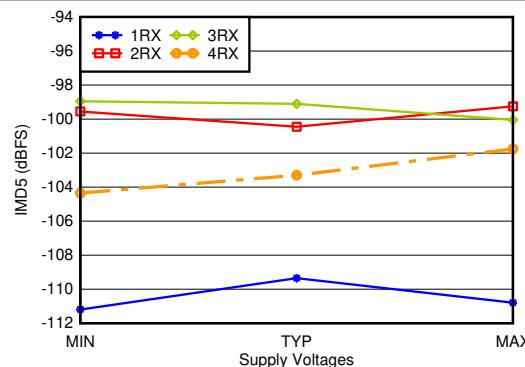
### 6.11.2 RX Typical Characteristics at 800MHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{IN}} = -3\text{ dBFS}$ , DSA setting = 4 dB.



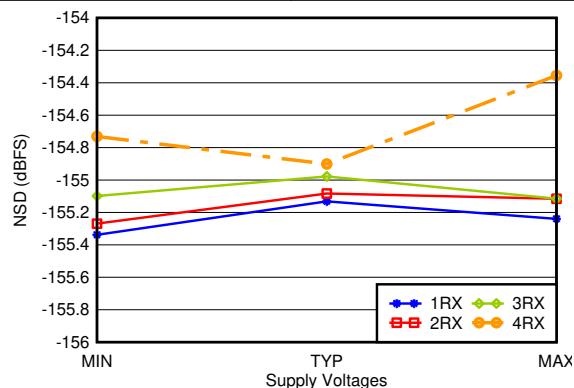
With 0.8 GHz matching,  $-7\text{ dBFS}$  each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

图 6-78. RX IMD3 vs Supply and Channel at 0.8 GHz



With 0.8 GHz matching,  $-7\text{ dBFS}$  each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

图 6-79. RX IMD5 vs Supply and Channel at 0.8 GHz

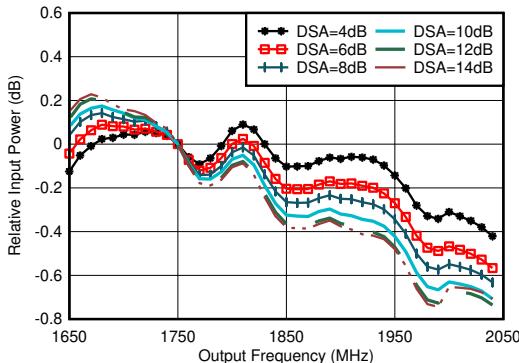


With 0.8 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

图 6-80. RX Noise Spectral Density vs Supply and Channel at 0.8 GHz

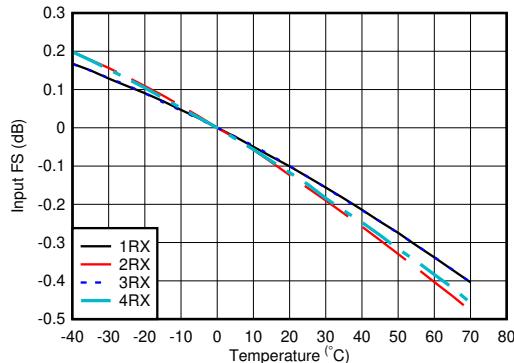
### 6.11.3 RX Typical Characteristics 1.75GHz to 1.9GHz

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{IN}} = -3\text{ dBFS}$ , DSA setting = 4 dB.



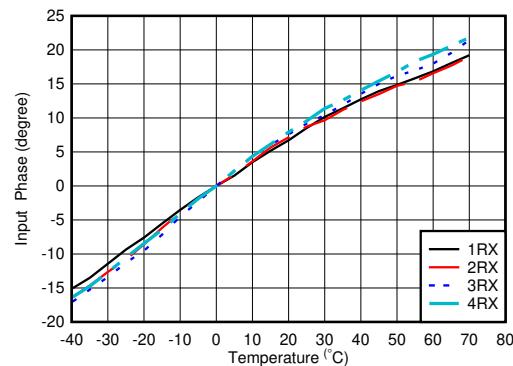
With 1.8 GHz matching, normalized to 1.75 GHz

图 6-81. RX In-Band Gain Flatness,  $f_{\text{IN}} = 1750\text{ MHz}$



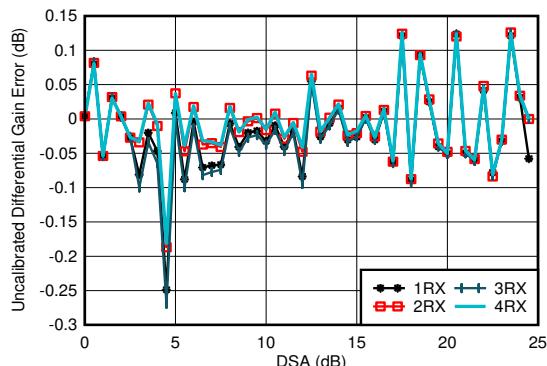
With 1.8 GHz matching, normalized to fullscale at  $25^\circ\text{C}$  for each channel

图 6-82. RX Input Fullscale vs Temperature and Channel at 1.75 GHz



With 2.6 GHz matching, normalized to phase at  $25^\circ\text{C}$

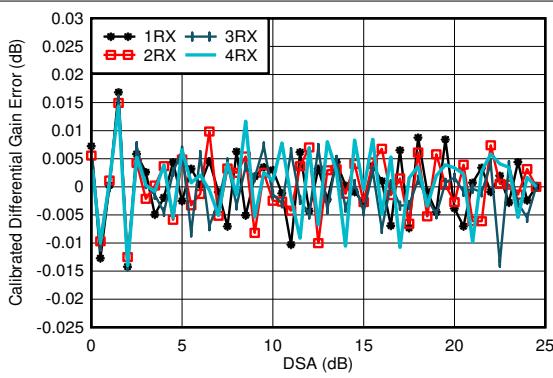
图 6-83. RX Input Phase vs Temperature and DSA at  $f_{\text{IN}} = 1.75\text{ GHz}$



With 1.8 GHz matching

Differential Amplitude Error =  $P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$

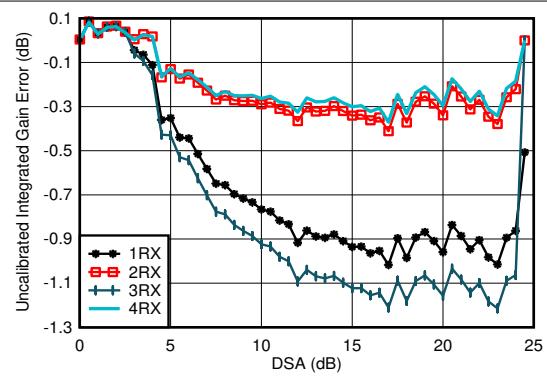
图 6-84. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching

Differential Amplitude Error =  $P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$

图 6-85. RX Calibrated Differential Amplitude Error vs DSA Setting at 1.75 GHz



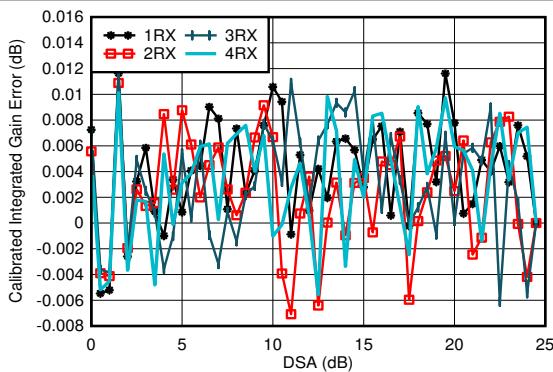
With 1.8 GHz matching

Integrated Amplitude Error =  $P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

图 6-86. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 1.75 GHz

### 6.11.3 RX Typical Characteristics 1.75GHz to 1.9GHz (continued)

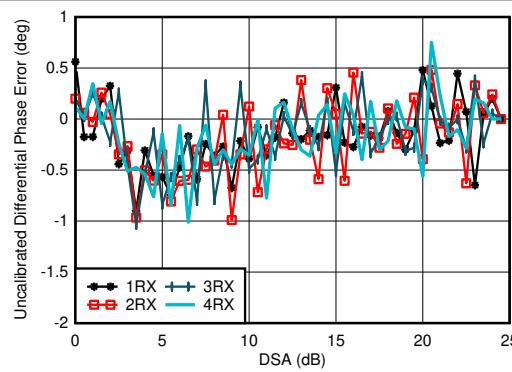
Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{IN}} = -3\text{ dBFS}$ , DSA setting = 4 dB.



With 1.8 GHz matching

Integrated Amplitude Error =  $P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$

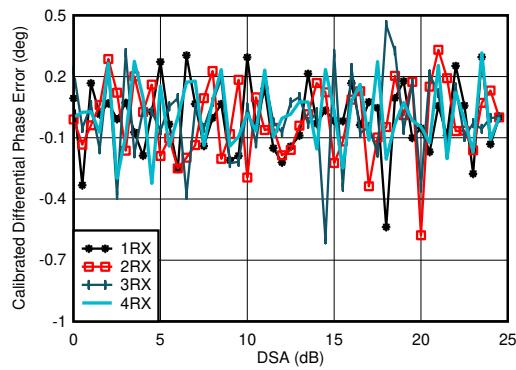
图 6-87. RX Calibrated Integrated Amplitude Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching

Differential Phase Error =  $\text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$

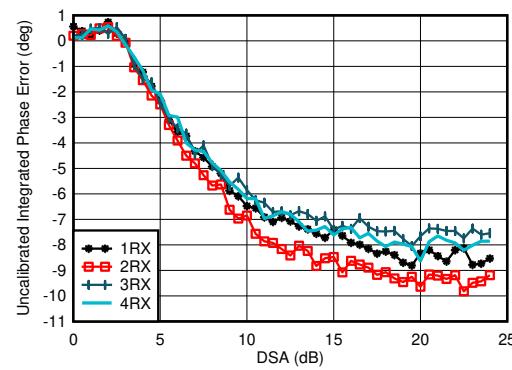
图 6-88. RX Uncalibrated Differential Phase Error vs DSA Setting at 1.75 GHz



With 1.8 GHz matching

Differential Phase Error =  $\text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$

图 6-89. RX Calibrated Differential Phase Error vs DSA Setting at 1.75 GHz



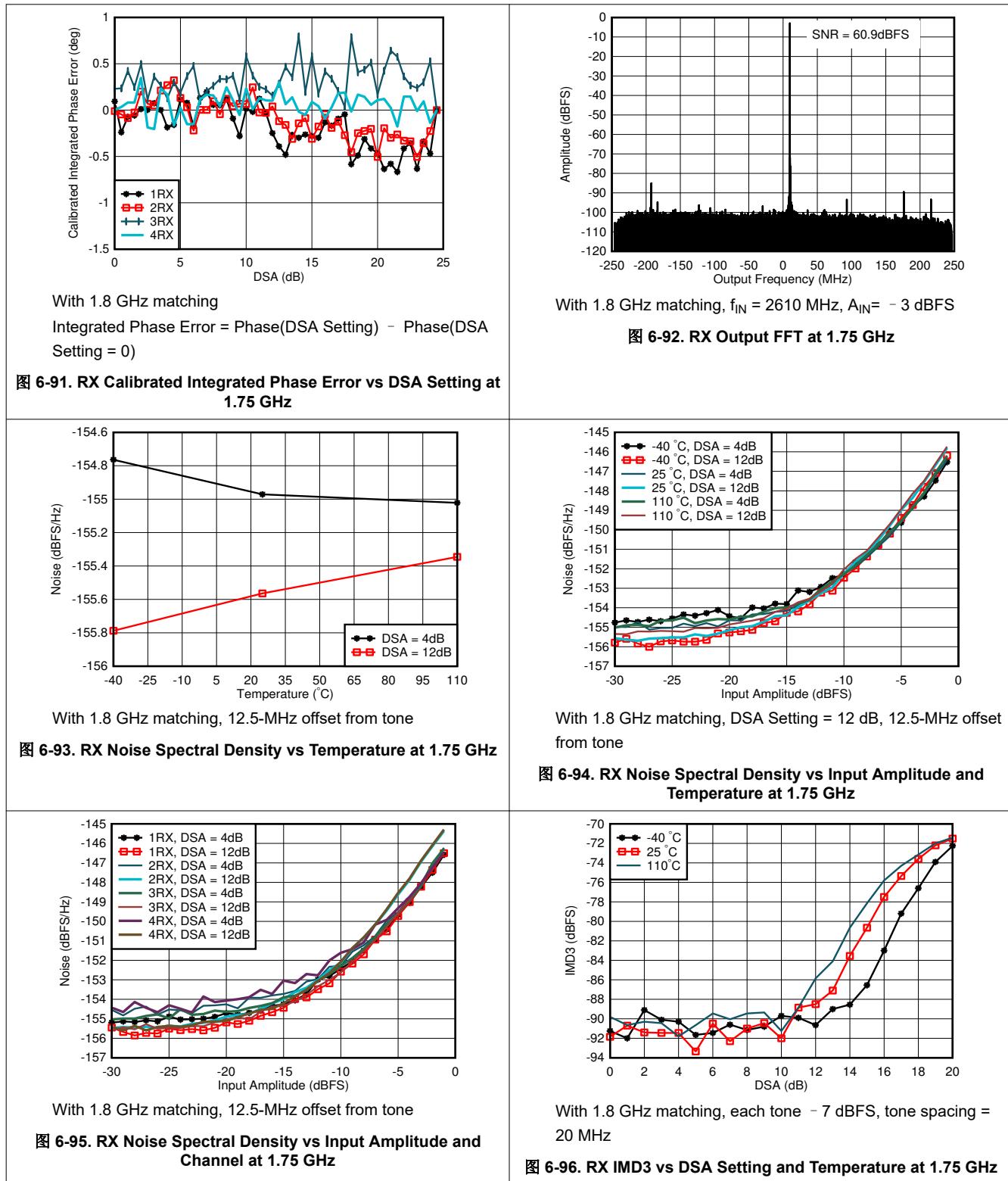
With 1.8 GHz matching

Integrated Phase Error =  $\text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$

图 6-90. RX Uncalibrated Integrated Phase Error vs DSA Setting at 1.75 GHz

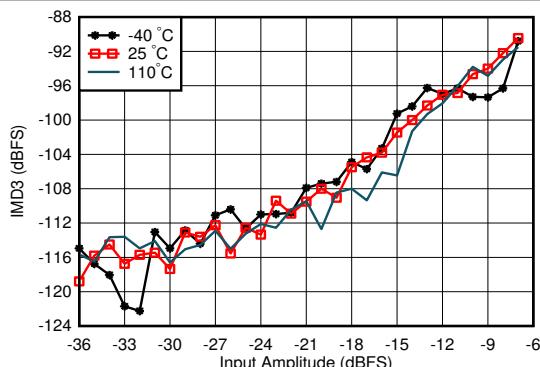
### 6.11.3 RX Typical Characteristics 1.75GHz to 1.9GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{IN}} = -3\text{ dBFS}$ , DSA setting = 4 dB.



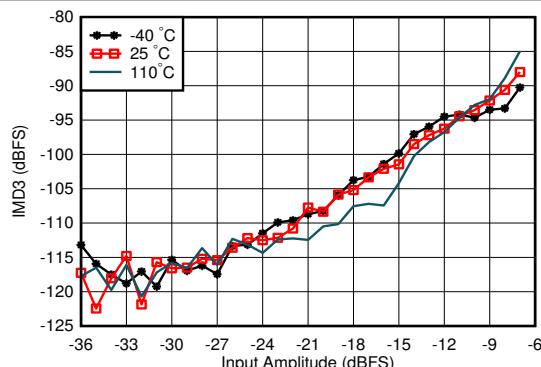
### 6.11.3 RX Typical Characteristics 1.75GHz to 1.9GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{IN}} = -3\text{ dBFS}$ , DSA setting = 4 dB.



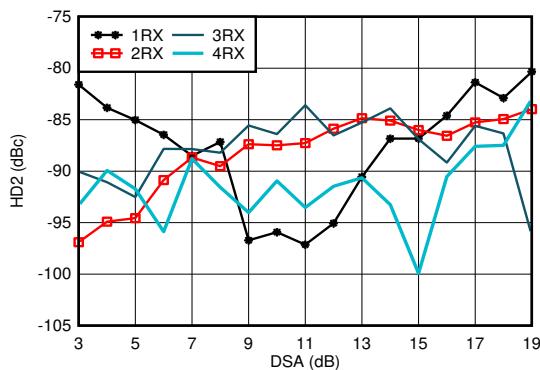
With 1.8 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

图 6-97. RX IMD3 vs Input Level and Temperature at 1.75 GHz



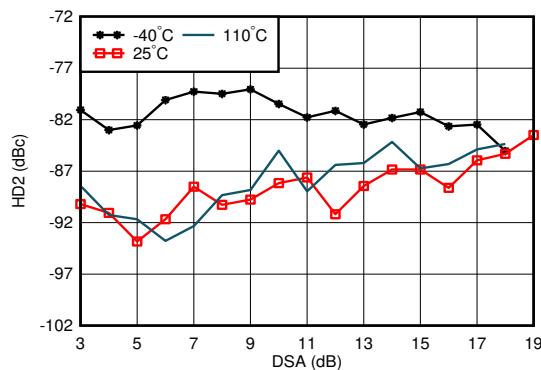
With 1.8 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

图 6-98. RX IMD3 vs Input Level and Temperature at 1.75 GHz



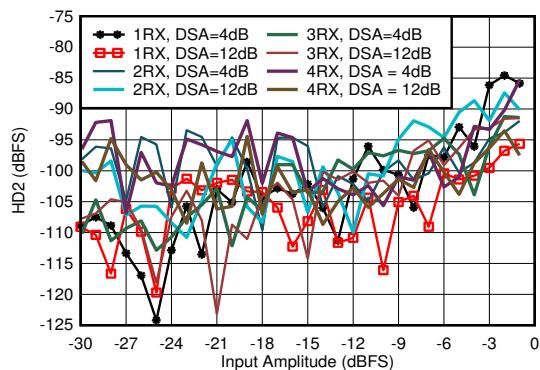
With 1.8 GHz matching,  $f_{\text{in}} = 1900\text{MHz}$ , measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

图 6-99. RX HD2 vs DSA Setting and Channel at 1.9 GHz



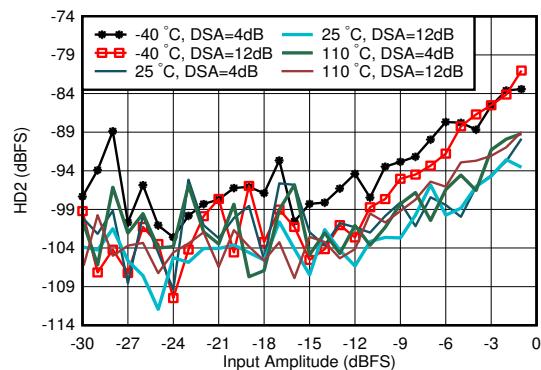
With 1.8 GHz matching,  $f_{\text{in}} = 1900\text{MHz}$ , measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

图 6-100. RX HD2 vs DSA Setting and Temperature at 1.9 GHz



With 1.8 GHz matching,  $f_{\text{in}} = 1900\text{MHz}$ , measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

图 6-101. RX HD2 vs Input Amplitude and Channel at 1.9 GHz

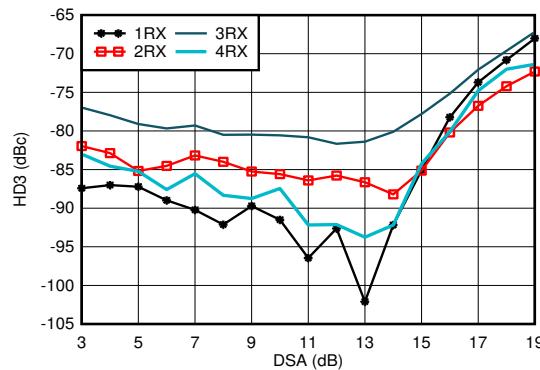


With 1.8 GHz matching,  $f_{\text{in}} = 1900\text{MHz}$ , measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

图 6-102. RX HD2 vs Input Amplitude and Temperature at 1.9 GHz

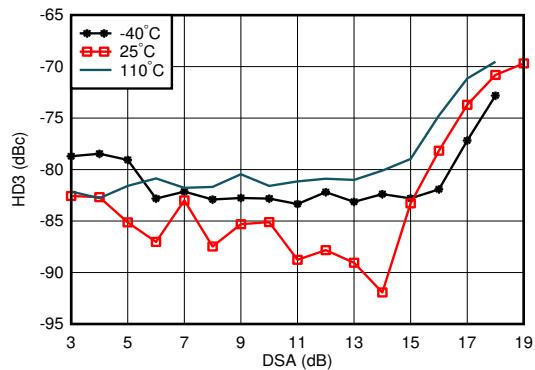
### 6.11.3 RX Typical Characteristics 1.75GHz to 1.9GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{IN}} = -3\text{ dBFS}$ , DSA setting = 4 dB.



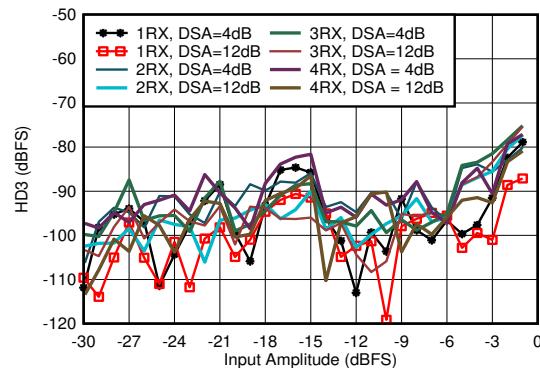
With 1.8 GHz matching,  $f_{\text{in}} = 1900\text{MHz}$ , DDC bypass mode (TI only mode for characterization)

图 6-103. RX HD3 vs DSA Setting and Channel at 1.9 GHz



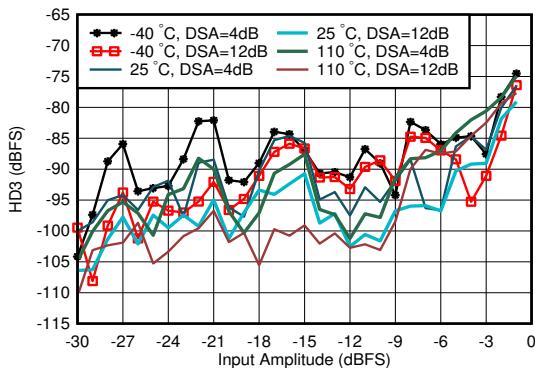
With 1.8 GHz matching,  $f_{\text{in}} = 1900\text{MHz}$ , DDC bypass mode (TI only mode for characterization)

图 6-104. RX HD3 vs DSA Setting and Temperature at 1.9 GHz



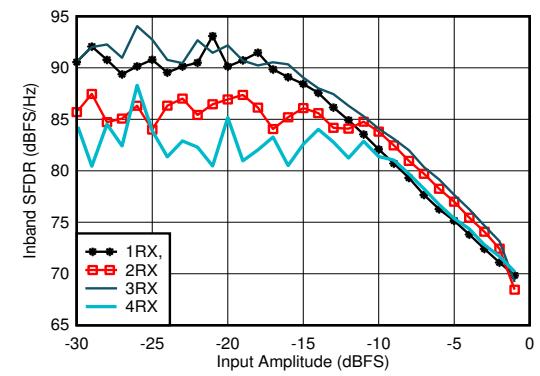
With 1.8 GHz matching,  $f_{\text{in}} = 1900\text{MHz}$ , DDC bypass mode (TI only mode for characterization)

图 6-105. RX HD3 vs Input Level and Channel at 1.9 GHz



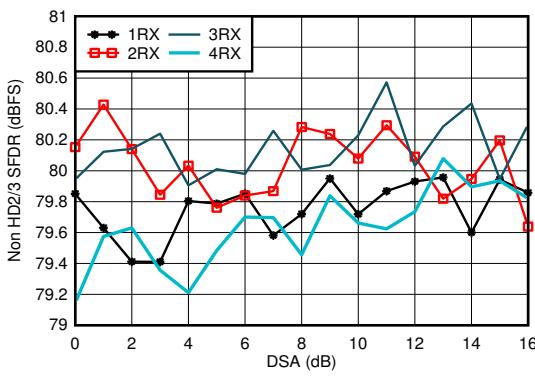
With 1.8 GHz matching,  $f_{\text{in}} = 1900\text{MHz}$ , DDC bypass mode (TI only mode for characterization)

图 6-106. RX HD3 vs Input Level and Temperature at 1.9 GHz



With 1.8 GHz matching, decimated by 3

图 6-107. RX In-Band SFDR (±400 MHz) vs Input Amplitude at 1.75 GHz

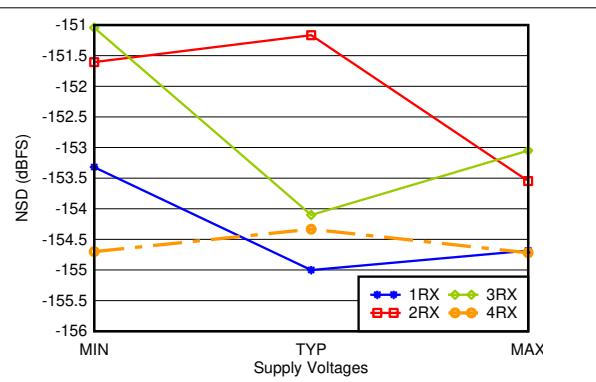
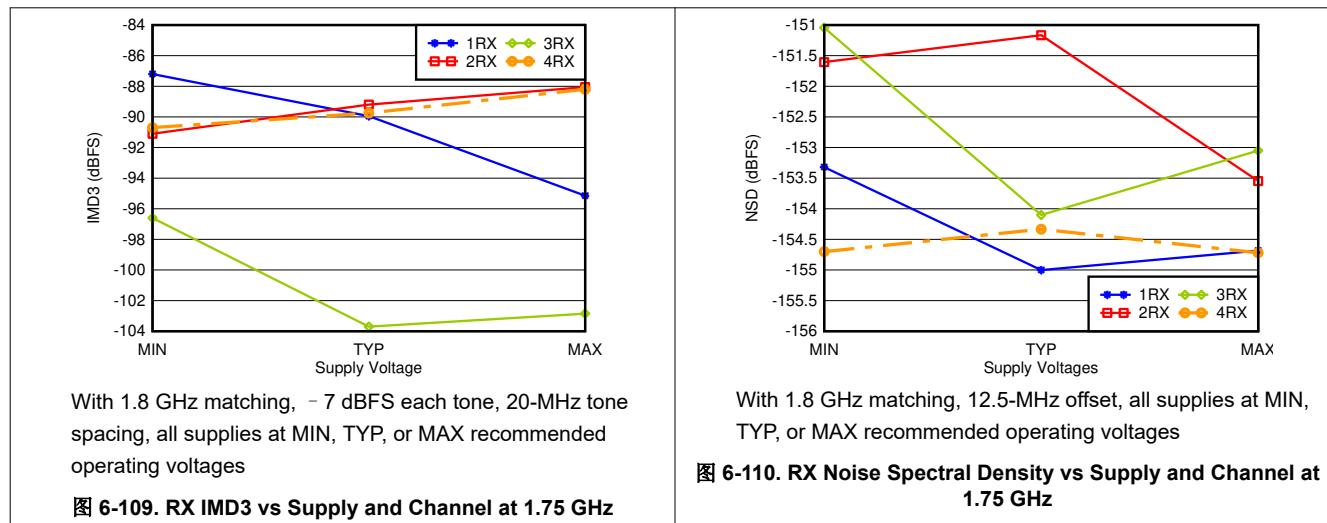


With 1.8 GHz matching

图 6-108. RX Non-HD2/3 vs DSA Setting at 1.75 GHz

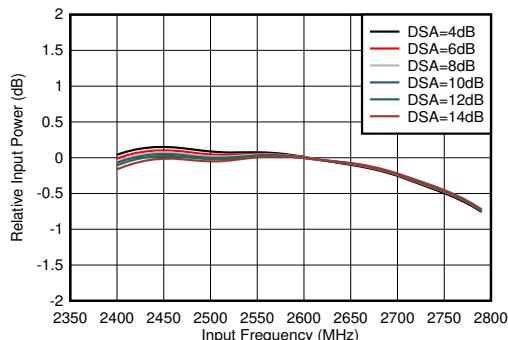
### 6.11.3 RX Typical Characteristics 1.75GHz to 1.9GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{IN}} = -3\text{ dBFS}$ , DSA setting = 4 dB.



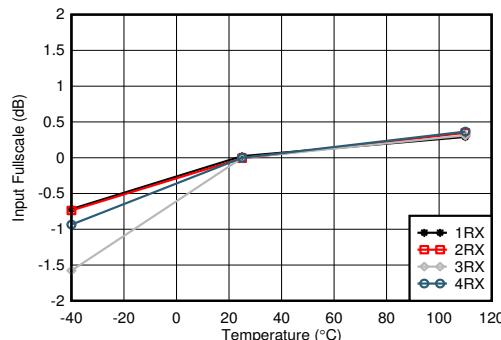
### 6.11.4 RX Typical Characteristics 2.6GHz

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{IN}} = -3\text{ dBFS}$ , DSA setting = 4 dB.



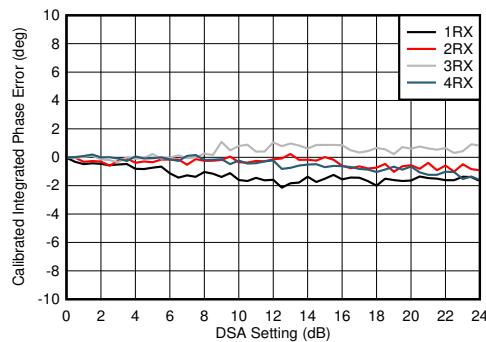
With matching, normalized to power at 2.6 GHz for each DSA setting

图 6-111. RX Inband Gain Flatness,  $f_{\text{IN}} = 2600\text{ MHz}$



With 2.6 GHz matching, normalized to fullscale at  $25^\circ\text{C}$  for each channel

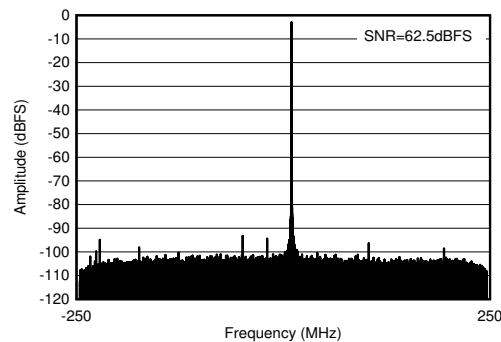
图 6-112. RX Input Fullscale vs Temperature and Channel at 2.6 GHz



With 2.6 GHz matching

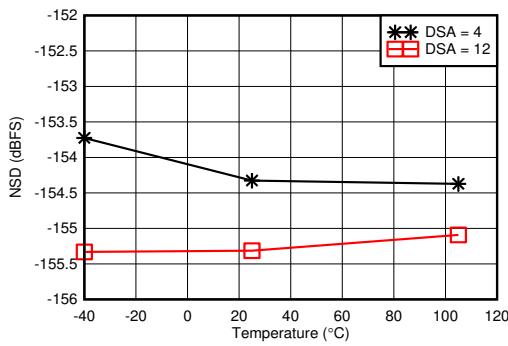
Integrated Phase Error = Phase(DSA Setting) - Phase(DSA Setting = 0)

图 6-113. RX Calibrated Integrated Phase Error vs DSA Setting at 2.6 GHz



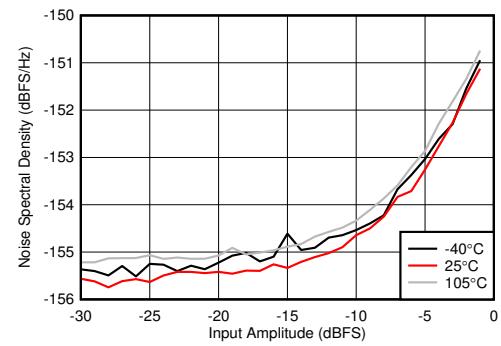
With 2.6 GHz matching,  $f_{\text{IN}} = 2610\text{ MHz}$ ,  $A_{\text{IN}} = -3\text{ dBFS}$

图 6-114. RX Output FFT at 2.6 GHz



With 2.6 GHz matching, 12.5-MHz offset from tone

图 6-115. RX Noise Spectral Density vs Temperature at 2.6 GHz



With 2.6 GHz matching, DSA Setting = 12 dB, 12.5-MHz offset from tone

图 6-116. RX Noise Spectral Density vs Input Amplitude and Temperature at 2.6 GHz

#### 6.11.4 RX Typical Characteristics 2.6GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{IN}} = -3\text{ dBFS}$ , DSA setting = 4 dB.

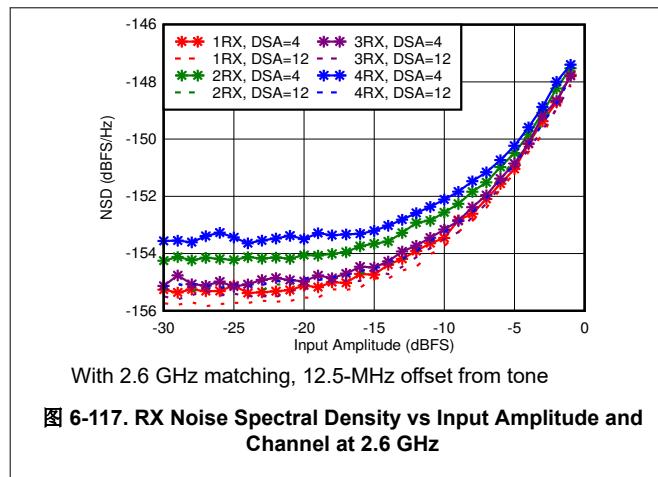


图 6-117. RX Noise Spectral Density vs Input Amplitude and Channel at 2.6 GHz

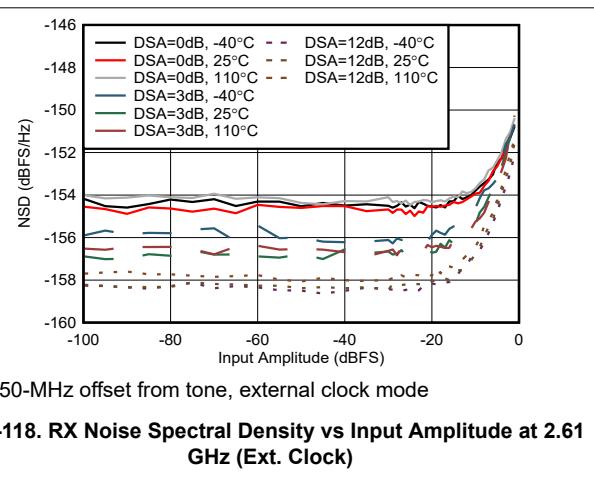


图 6-118. RX Noise Spectral Density vs Input Amplitude at 2.6 GHz (Ext. Clock)

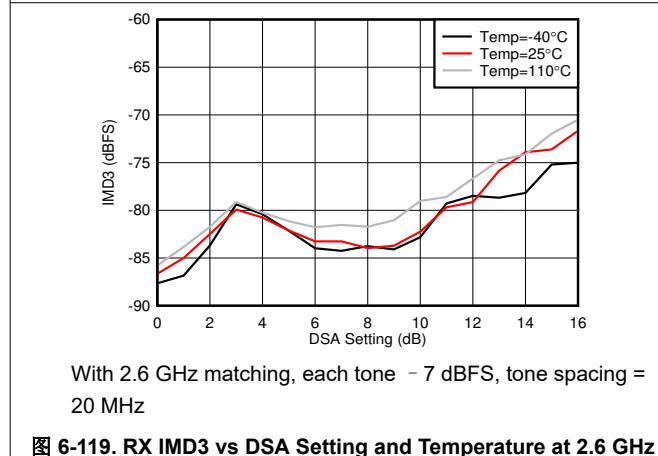


图 6-119. RX IMD3 vs DSA Setting and Temperature at 2.6 GHz

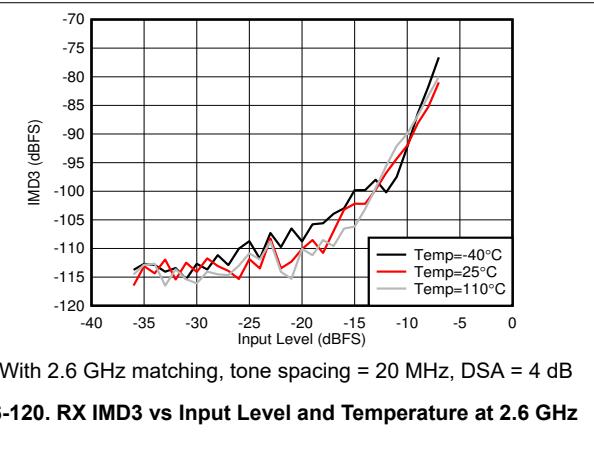


图 6-120. RX IMD3 vs Input Level and Temperature at 2.6 GHz

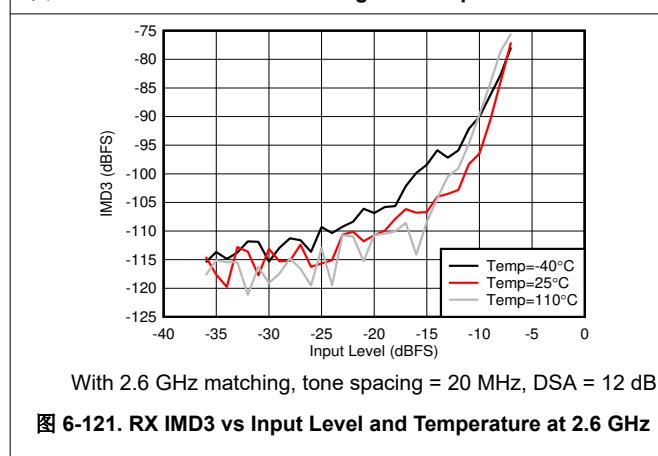


图 6-121. RX IMD3 vs Input Level and Temperature at 2.6 GHz

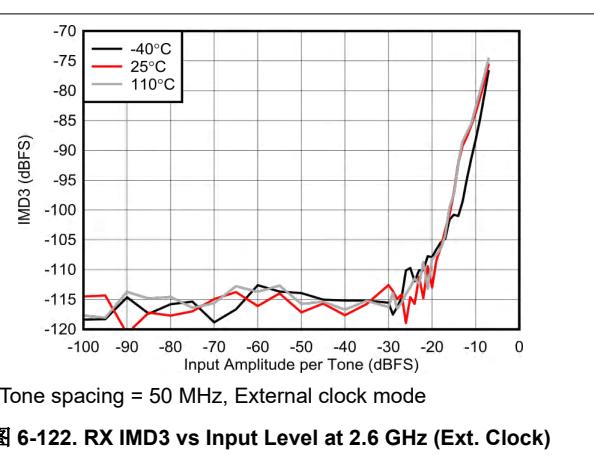
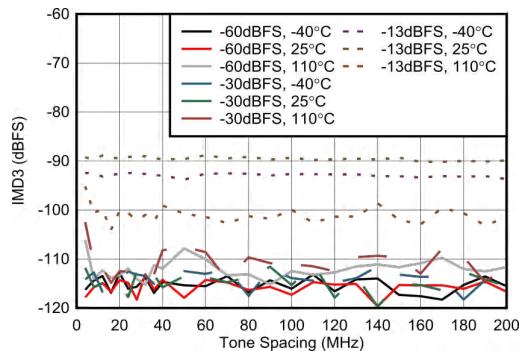


图 6-122. RX IMD3 vs Input Level at 2.6 GHz (Ext. Clock)

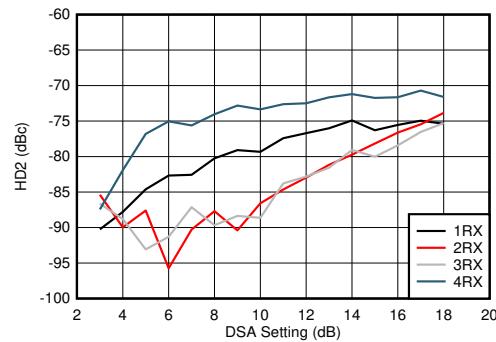
### 6.11.4 RX Typical Characteristics 2.6GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{IN}} = -3\text{ dBFS}$ , DSA setting = 4 dB.



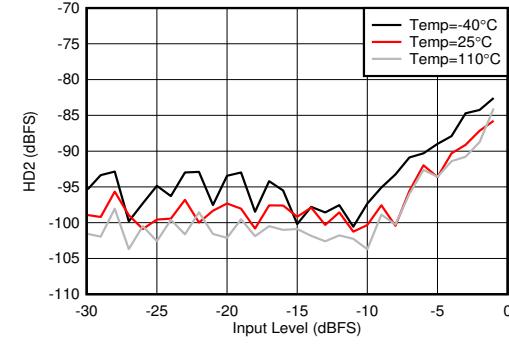
External clock mode

图 6-123. RX IMD3 vs Tone Spacing at 2.6 GHz (Ext. Clock)



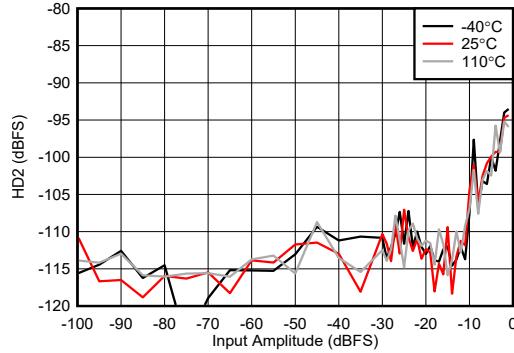
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

图 6-124. RX HD2 vs DSA Setting and Channel at 2.6 GHz



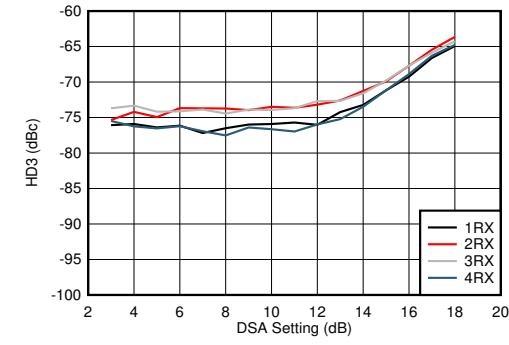
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

图 6-125. RX HD2 vs Input Level and Temperature at 2.6 GHz



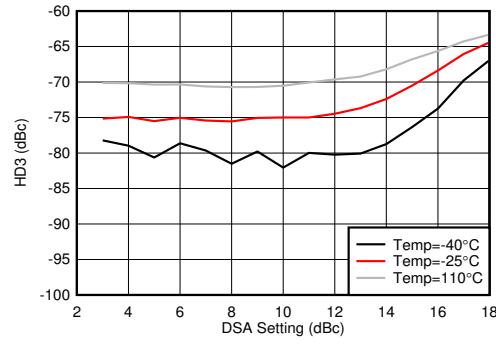
External clock mode

图 6-126. RX HD2 vs Input Level and Temperature at 2.6 GHz



With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

图 6-127. RX HD3 vs DSA Setting and Channel at 2.6 GHz

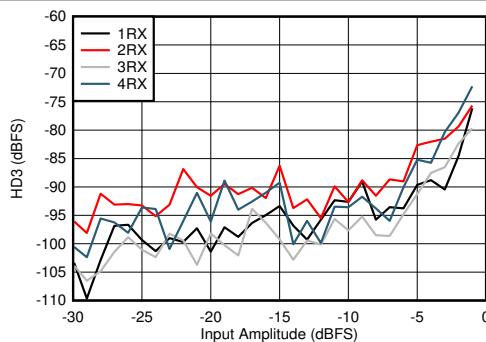


With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

图 6-128. RX HD3 vs DSA Setting and Temperature at 2.6 GHz

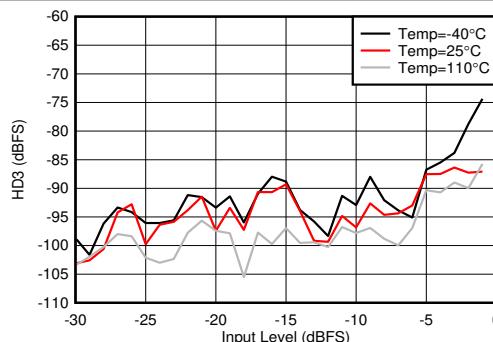
#### 6.11.4 RX Typical Characteristics 2.6GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{IN}} = -3\text{ dBFS}$ , DSA setting = 4 dB.



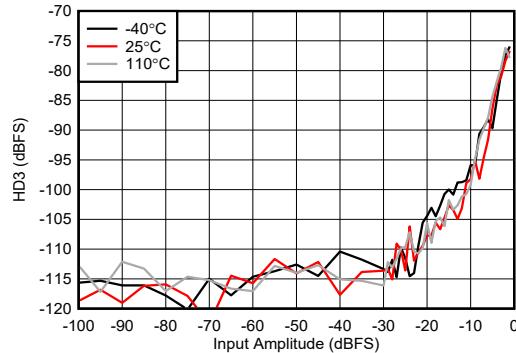
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

图 6-129. RX HD3 vs Input Level and Channel at 2.6 GHz



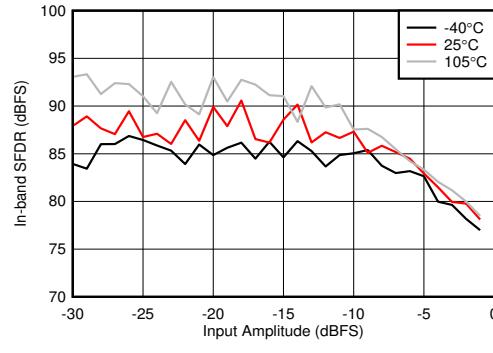
With 2.6 GHz matching, DDC bypass mode (TI only mode for characterization)

图 6-130. RX HD3 vs Input Level and Temperature at 2.6 GHz



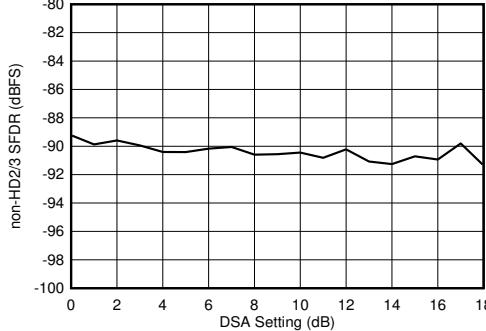
External clock mode

图 6-131. RX HD3 vs Input Level and Temperature at 2.6 GHz



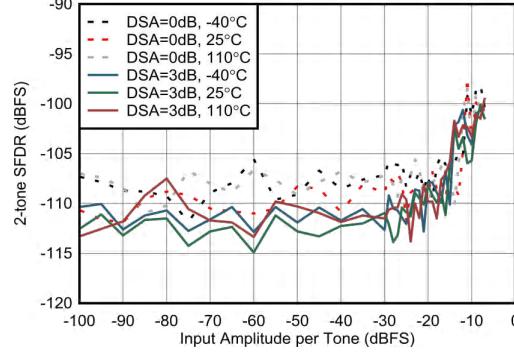
With 2.6 GHz matching, decimate by 4

图 6-132. RX In-Band SFDR (\pm300 MHz) vs Input Amplitude and Temperature at 2.6 GHz



With 2.6 GHz matching

图 6-133. RX Non-HD2/3 vs DSA Setting at 2.6 GHz

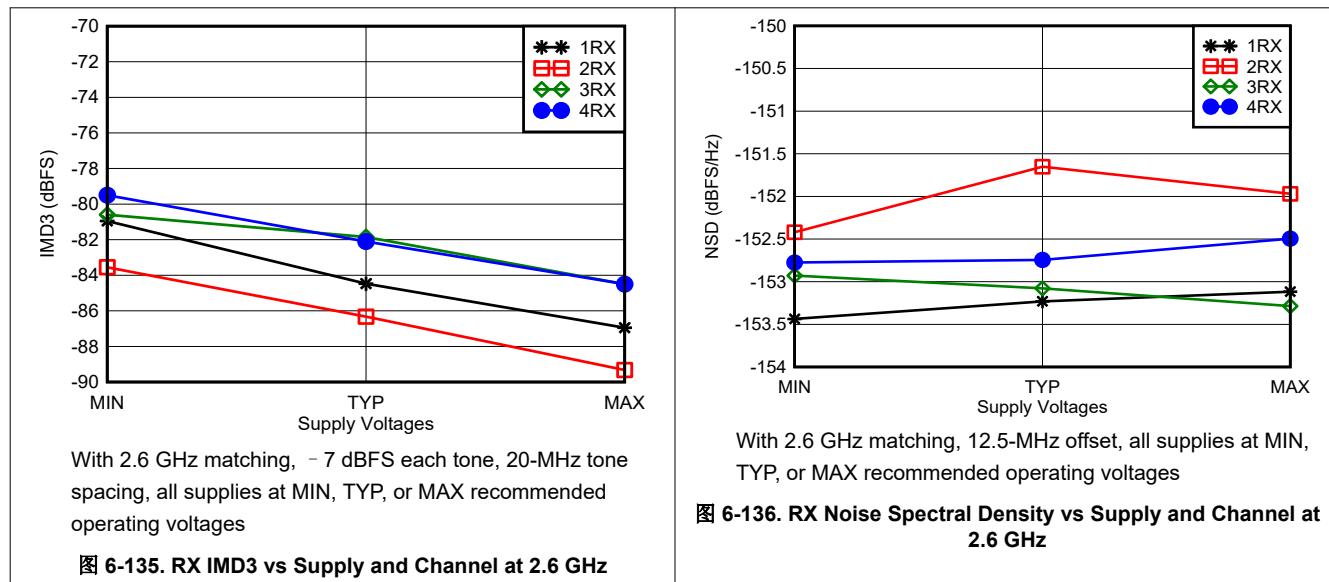


External clock mode, 50MHz tone spacing, excluding 3rd order distortion

图 6-134. RX 2-tone SFDR vs Input Amplitude at 2.6 GHz

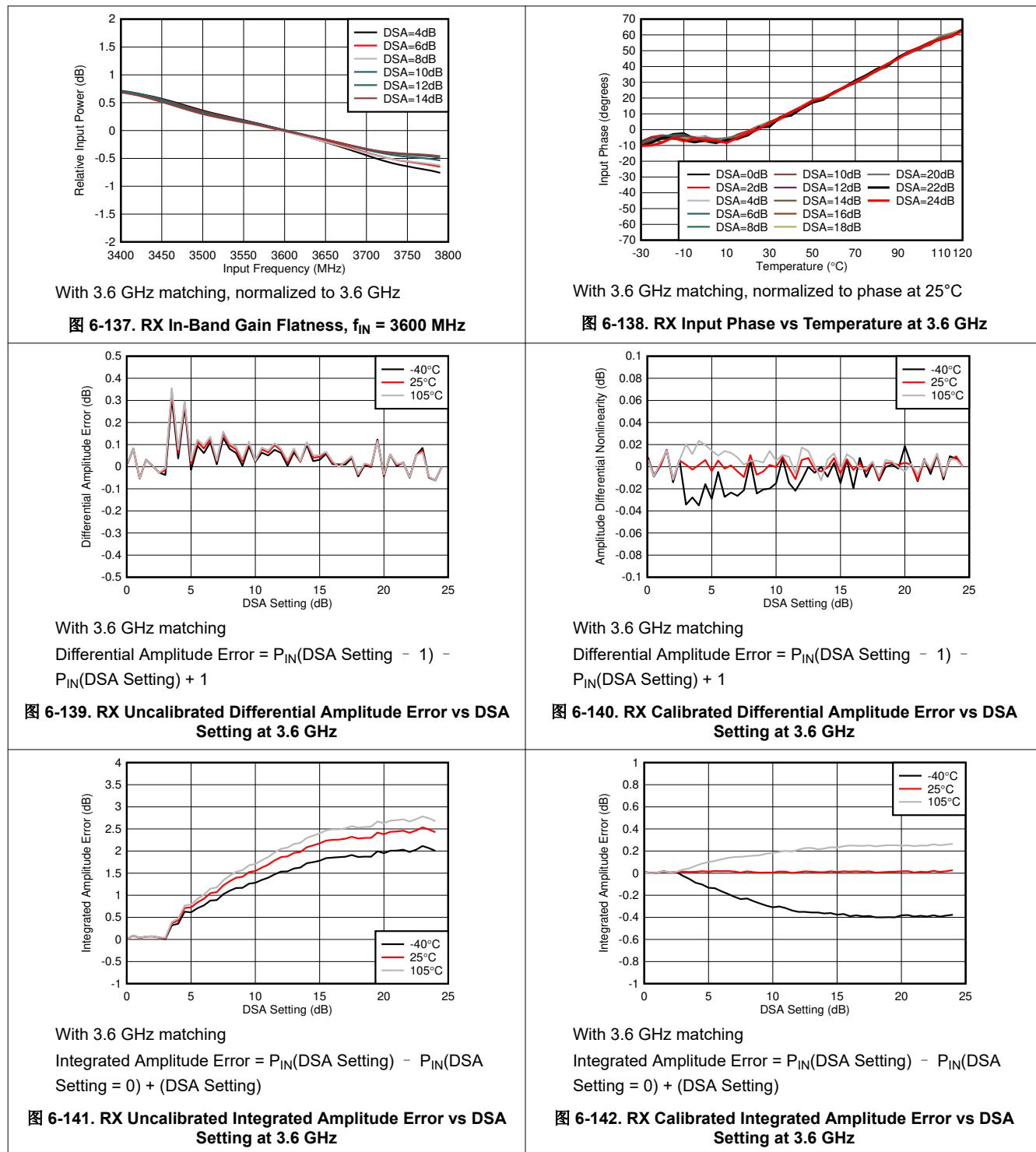
#### 6.11.4 RX Typical Characteristics 2.6GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{IN}} = -3\text{ dBFS}$ , DSA setting = 4 dB.



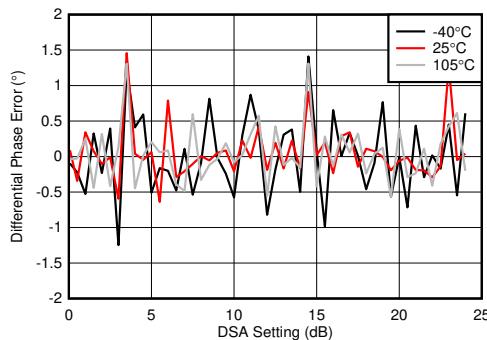
### 6.11.5 RX Typical Characteristics 3.5GHz

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{IN}} = -3\text{ dBFS}$ , DSA setting = 4 dB.



### 6.11.5 RX Typical Characteristics 3.5GHz (continued)

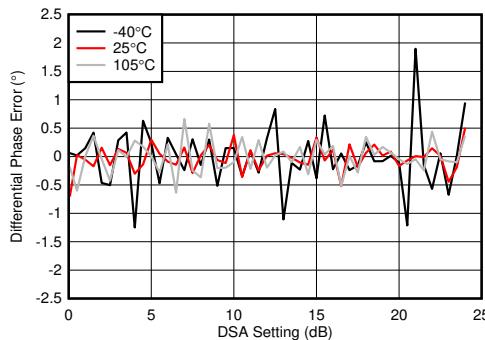
Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{IN}} = -3\text{ dBFS}$ , DSA setting = 4 dB.



With 3.6 GHz matching

$$\text{Differential Phase Error} = \text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$$

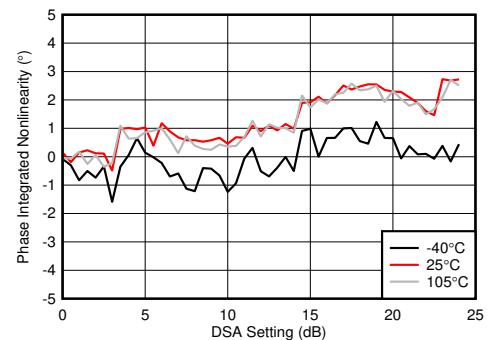
图 6-143. RX Uncalibrated Phase Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching

$$\text{Differential Phase Error} = \text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$$

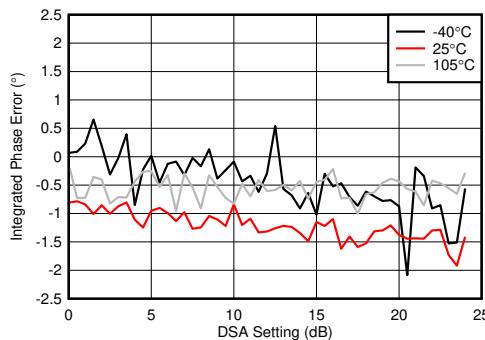
图 6-144. RX Calibrated Differential Phase Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching

$$\text{Integrated Phase Error} = \text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$$

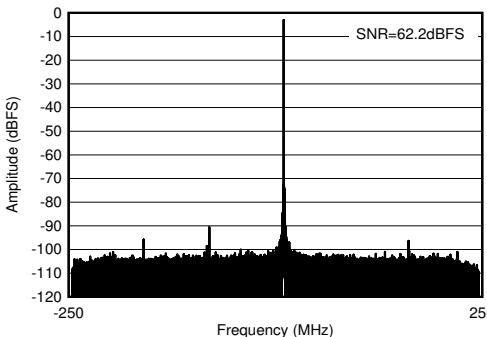
图 6-145. RX Uncalibrated Integrated Phase Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching

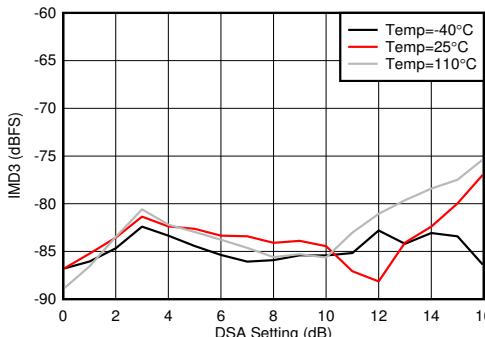
$$\text{Integrated Phase Error} = \text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$$

图 6-146. RX Calibrated Integrated Phase Error vs DSA Setting at 3.6 GHz



With 3.6 GHz matching,  $f_{\text{IN}} = 3610\text{ MHz}$ ,  $A_{\text{IN}} = -3\text{ dBFS}$

图 6-147. RX Output FFT at 3.6 GHz

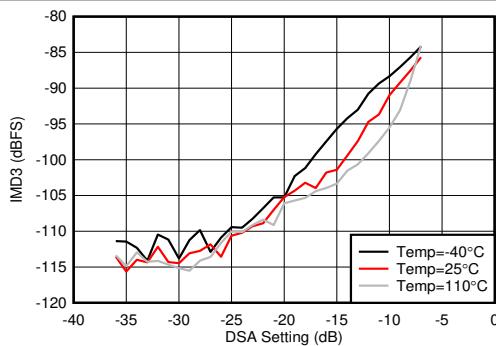


With 3.5 GHz matching, each tone at  $-7\text{ dBFS}$ , 20-MHz tone spacing

图 6-148. RX IMD3 vs DSA Setting and Temperature at 3.6 GHz

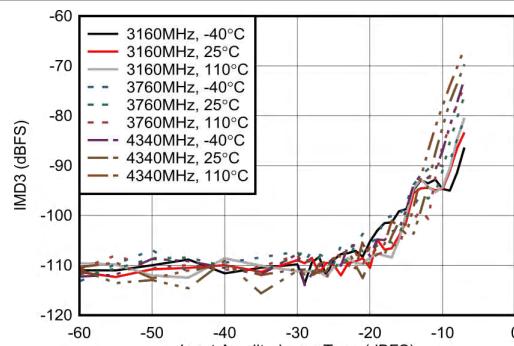
### 6.11.5 RX Typical Characteristics 3.5GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{IN}} = -3\text{ dBFS}$ , DSA setting = 4 dB.



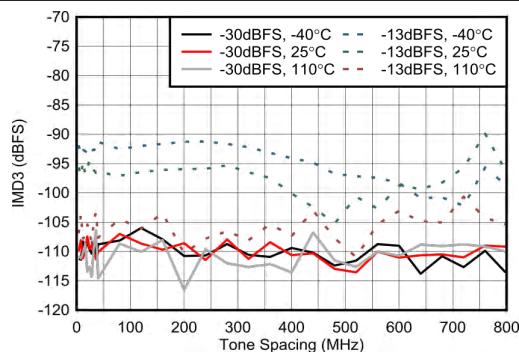
With 3.5 GHz matching, 20-MHz tone spacing

图 6-149. RX IMD3 vs Input Level and Temperature at 3.6 GHz



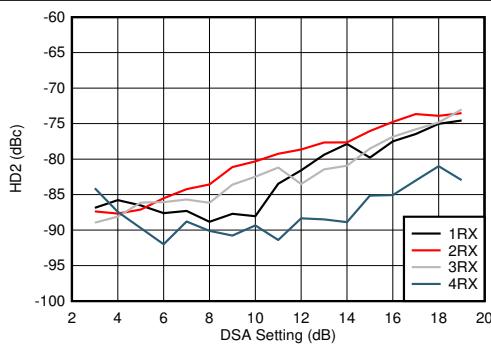
External clock mode, 20-MHz tone spacing, 2x Decimation

图 6-150. RX IMD3 vs Input Level



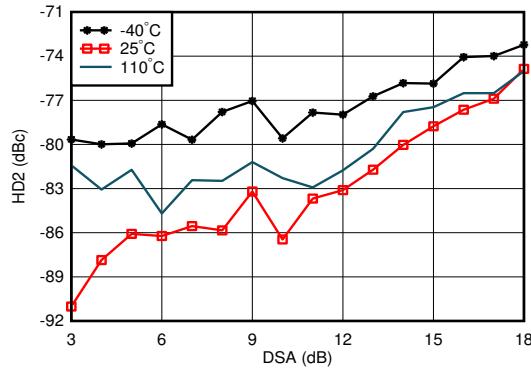
External clock mode, 2x Decimation

图 6-151. RX IMD3 vs Tone Spacing at 3.76GHz



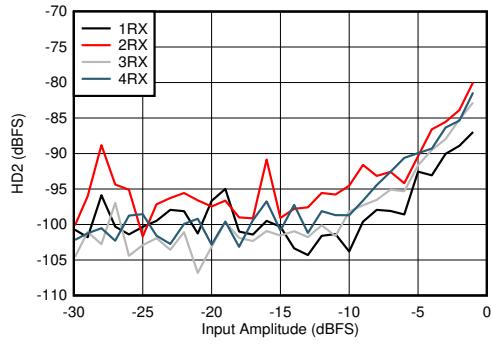
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

图 6-152. RX HD2 vs DSA Setting and Channel at 3.6 GHz



With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

图 6-153. RX HD2 vs DSA Setting and Temperature at 3.6 GHz

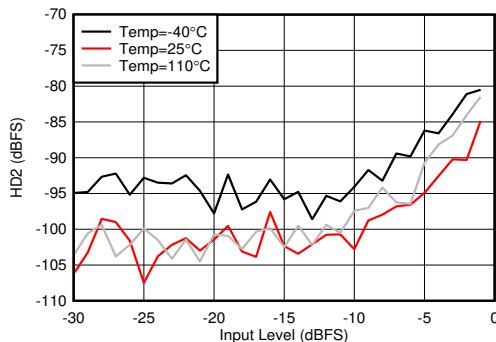


With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

图 6-154. RX HD2 vs Input Level and Channel at 3.6 GHz

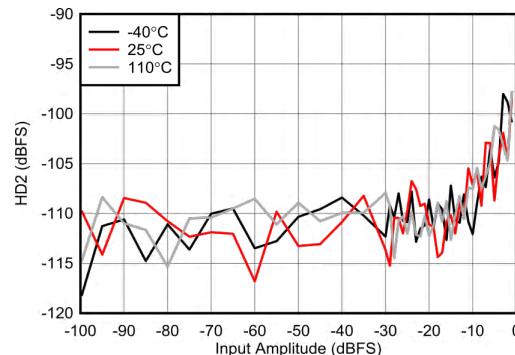
### 6.11.5 RX Typical Characteristics 3.5GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 4 dB.



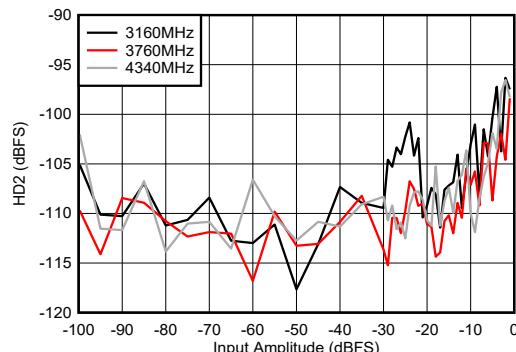
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

图 6-155. RX HD2 vs Input Level and Temperature at 3.6 GHz



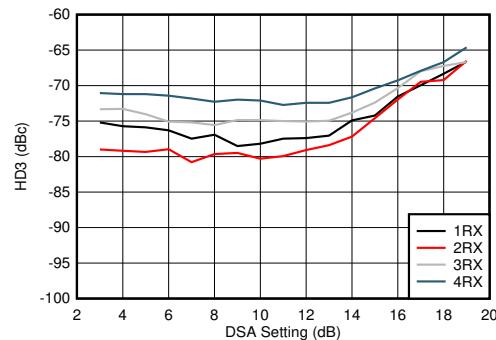
External clock mode, 2x Decimation

图 6-156. RX HD2 vs Input Level at 3.76 GHz



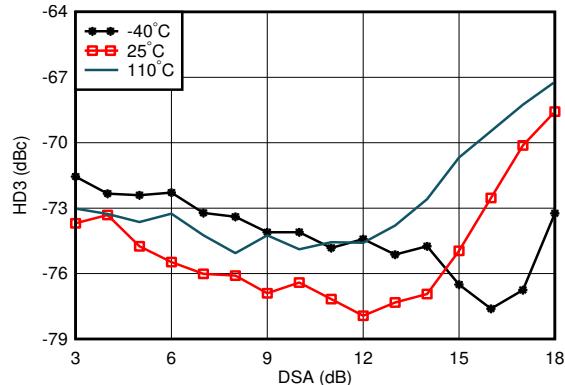
External clock mode, 25°C, 2x Decimation

图 6-157. RX HD2 vs Input Level



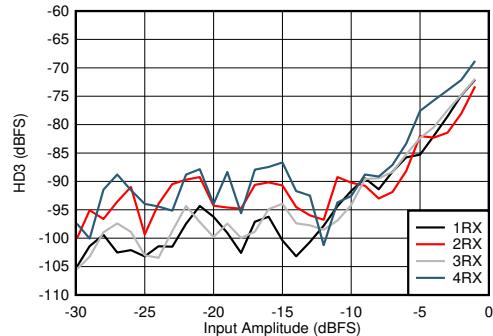
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

图 6-158. RX HD3 vs DSA Setting and Channel at 3.6 GHz



With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

图 6-159. RX HD3 vs DSA Setting and Temperature at 3.6 GHz

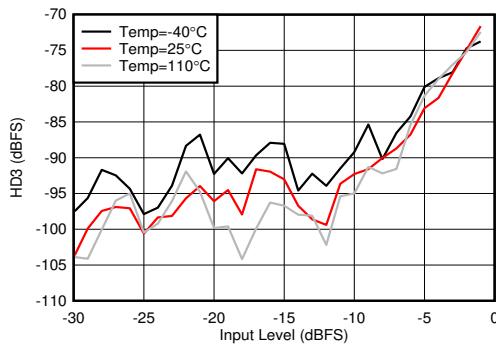


With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

图 6-160. RX HD3 vs Input Level and Channel at 3.6 GHz

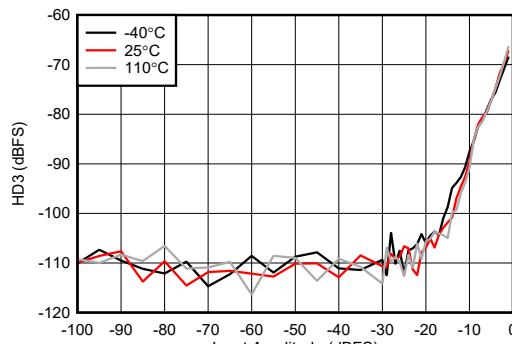
### 6.11.5 RX Typical Characteristics 3.5GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 4 dB.



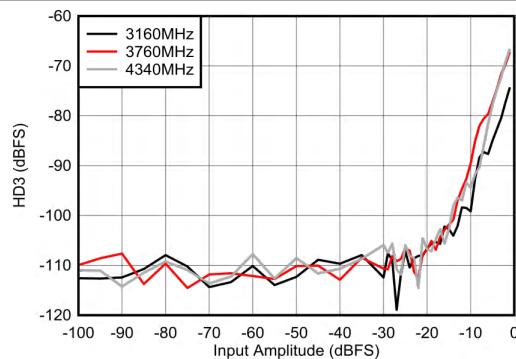
With 3.5 GHz matching, DDC bypass mode (TI only mode for characterization)

图 6-161. RX HD3 vs Input Level and Temperature at 3.6 GHz



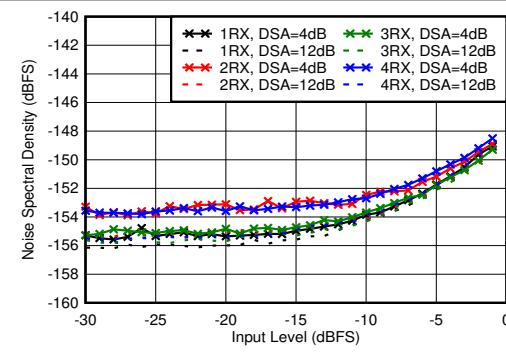
External clock mode, 2x Decimation

图 6-162. RX HD3 vs Input Level at 3.76GHz



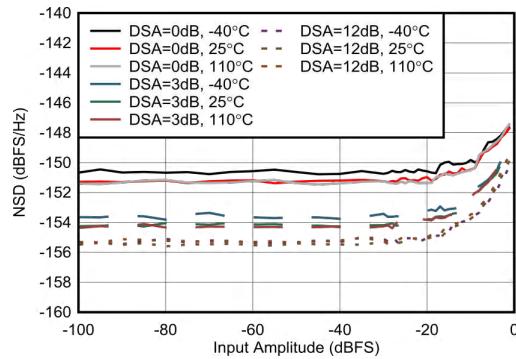
External clock mode, 25°C, 2x Decimation

图 6-163. RX HD3 vs Input Level



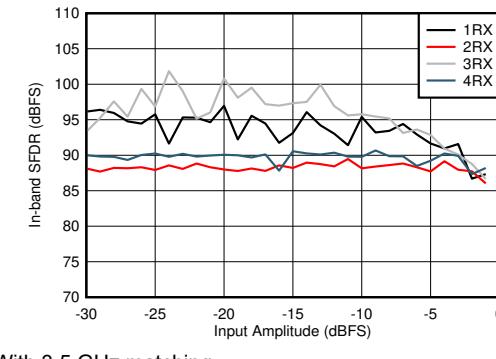
With 3.5 GHz matching, 12.5-MHz offset from tone

图 6-164. RX Noise Spectral Density vs Input Level and DSA Setting at 3.6 GHz



External clock mode, 25°C, 2x Decimation

图 6-165. RX Noise Spectral Density vs Input Level at 3.76GHz

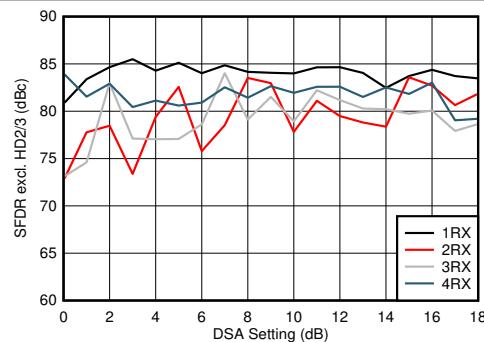


With 3.5 GHz matching

图 6-166. RX In-Band SFDR (±200 MHz) vs Input Level and Channel at 3.6 GHz

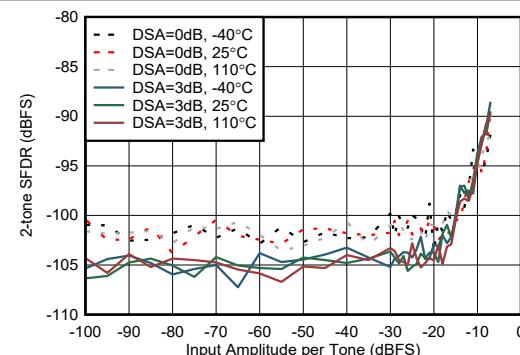
### 6.11.5 RX Typical Characteristics 3.5GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 4 dB.



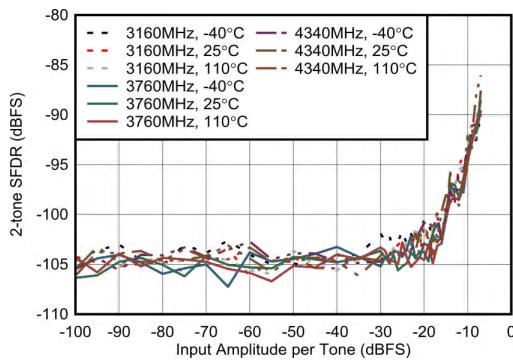
With 3.5 GHz matching

图 6-167. RX SFDR Excluding HD2/3 vs DSA Setting and Channel at 3.6 GHz



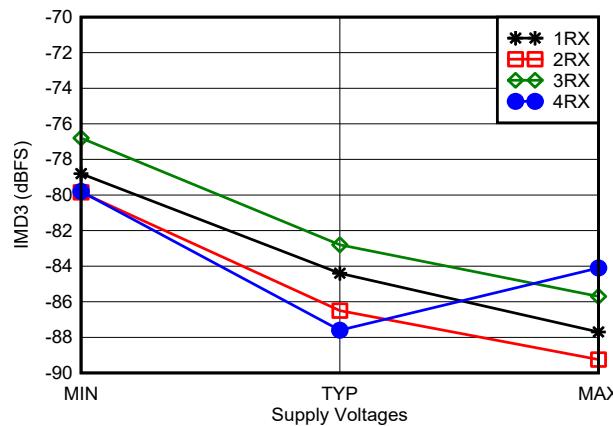
External clock mode, 20MHz tone spacing, excluding 3<sup>rd</sup> order distortion

图 6-168. RX 2-tone SFDR vs Input Amplitude and DSA Setting at 3.7 GHz



External clock mode, 20MHz tone spacing, excluding 3<sup>rd</sup> order distortion

图 6-169. RX 2-tone SFDR vs Input Amplitude and Frequency at 3.7 GHz

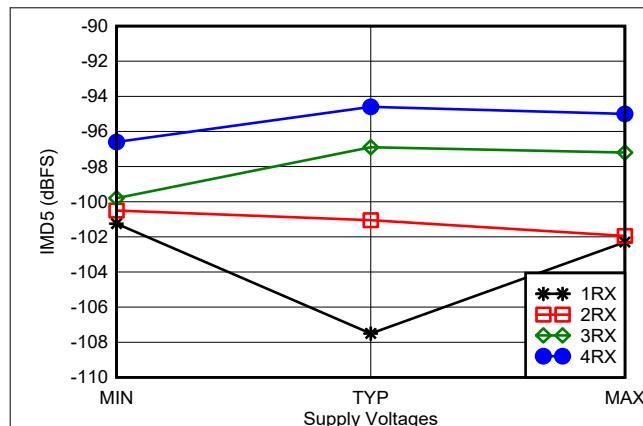


With 3.6 GHz matching, -7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

图 6-170. RX IMD3 vs Supply Voltage and Channel at 3.6 GHz

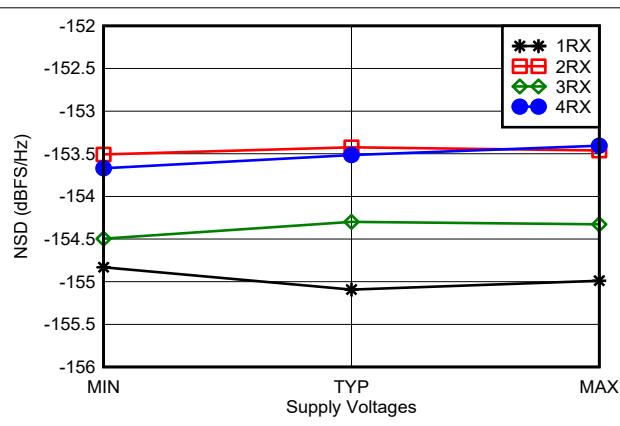
### 6.11.5 RX Typical Characteristics 3.5GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 4 dB.



With 3.6 GHz matching, -7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

图 6-171. RX IMD5 vs Supply Voltage and Channel at 3.6 GHz

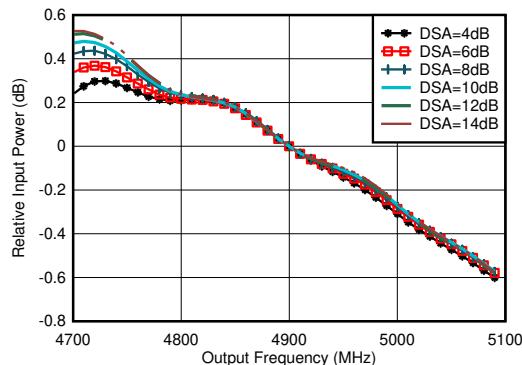


With 3.6 GHz matching, tone at -20 dBFS, 12.5-MHz offset frequency, all supplies at MIN, TYP, or MAX recommended operating voltages

图 6-172. RX Noise Spectral Density vs Supply Voltage and Channel at 3.6 GHz

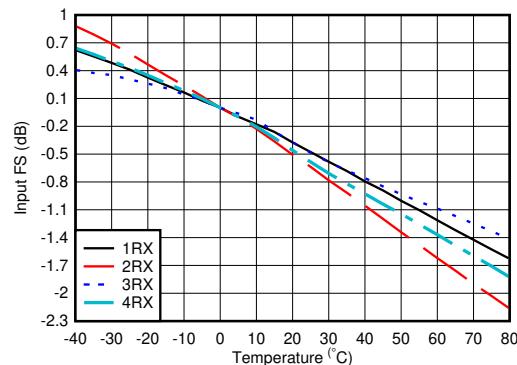
### 6.11.6 RX Typical Characteristics 4.9GHz

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{IN}} = -3\text{ dBFS}$ , DSA setting = 4 dB.



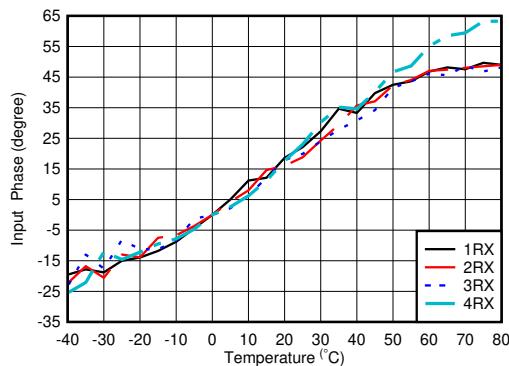
With matching, normalized to power at 4.9GHz for each DSA setting

图 6-173. RX Inband Gain Flatness,  $f_{\text{IN}} = 4900\text{ MHz}$



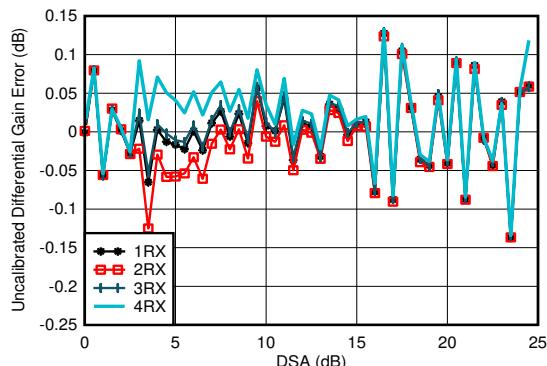
With 4.9 GHz matching, normalized to fullscale at  $25^\circ\text{C}$  for each channel

图 6-174. RX Input Fullscale vs Temperature and Channel at 4.9 GHz



With 4.9 GHz matching, normalized to phase at  $25^\circ\text{C}$

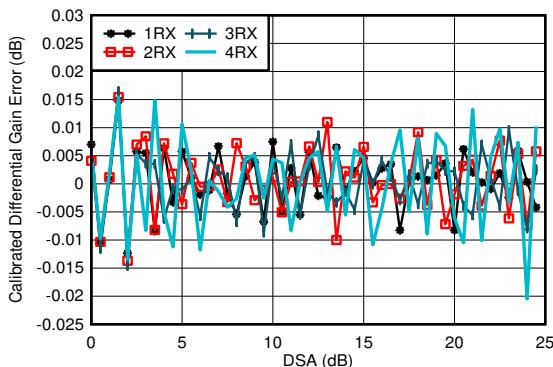
图 6-175. RX Input Phase vs Temperature and DSA at  $f_{\text{OUT}} = 4.9\text{ GHz}$



With 4.9 GHz matching

$$\text{Differential Amplitude Error} = P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$$

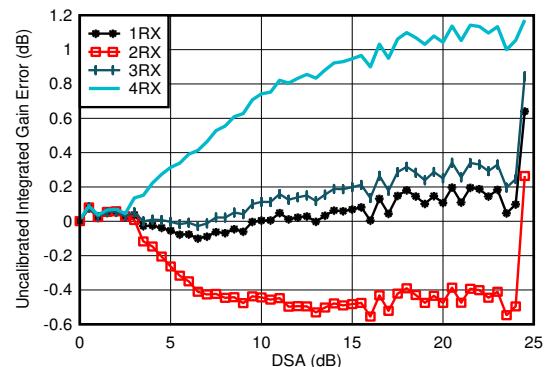
图 6-176. RX Uncalibrated Differential Amplitude Error vs DSA Setting at 4.9 GHz



With 4.9 GHz matching

$$\text{Differential Amplitude Error} = P_{\text{IN}}(\text{DSA Setting} - 1) - P_{\text{IN}}(\text{DSA Setting}) + 1$$

图 6-177. RX Calibrated Differential Amplitude Error vs DSA Setting at 4.9 GHz



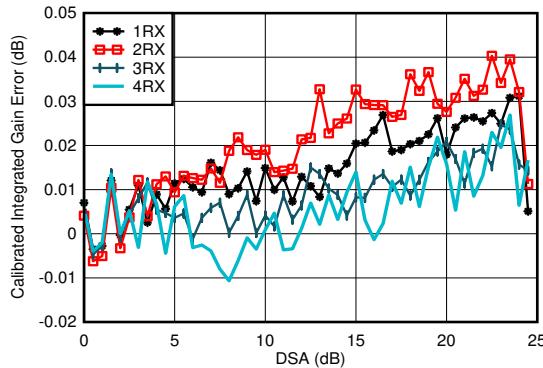
With 4.9 GHz matching

$$\text{Integrated Amplitude Error} = P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$$

图 6-178. RX Uncalibrated Integrated Amplitude Error vs DSA Setting at 4.9 GHz

### 6.11.6 RX Typical Characteristics 4.9GHz (continued)

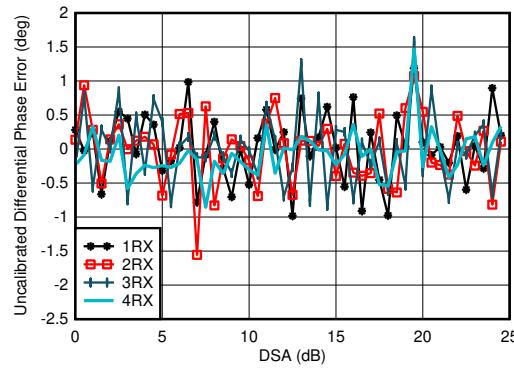
Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{IN}} = -3\text{ dBFS}$ , DSA setting = 4 dB.



With 4.9 GHz matching

$$\text{Integrated Amplitude Error} = P_{\text{IN}}(\text{DSA Setting}) - P_{\text{IN}}(\text{DSA Setting} = 0) + (\text{DSA Setting})$$

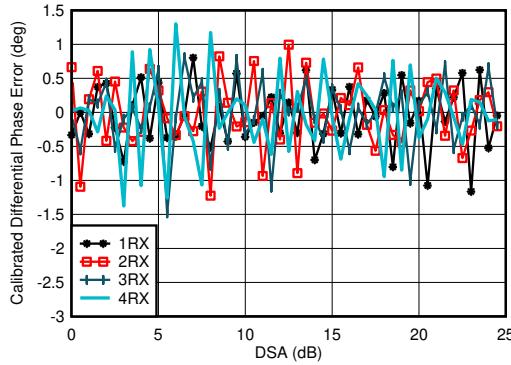
**图 6-179. RX Calibrated Integrated Amplitude Error vs DSA Setting at 4.9 GHz**



With 4.9 GHz matching

$$\text{Differential Phase Error} = \text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$$

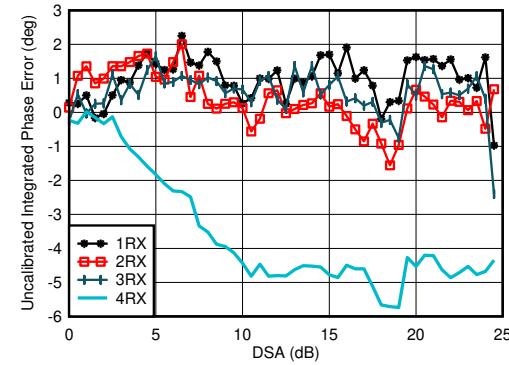
**图 6-180. RX Uncalibrated Differential Phase Error vs DSA Setting at 4.9 GHz**



With 4.9 GHz matching

$$\text{Differential Phase Error} = \text{Phase}_{\text{IN}}(\text{DSA Setting} - 1) - \text{Phase}_{\text{IN}}(\text{DSA Setting})$$

**图 6-181. RX Calibrated Differential Phase Error vs DSA Setting at 4.9 GHz**



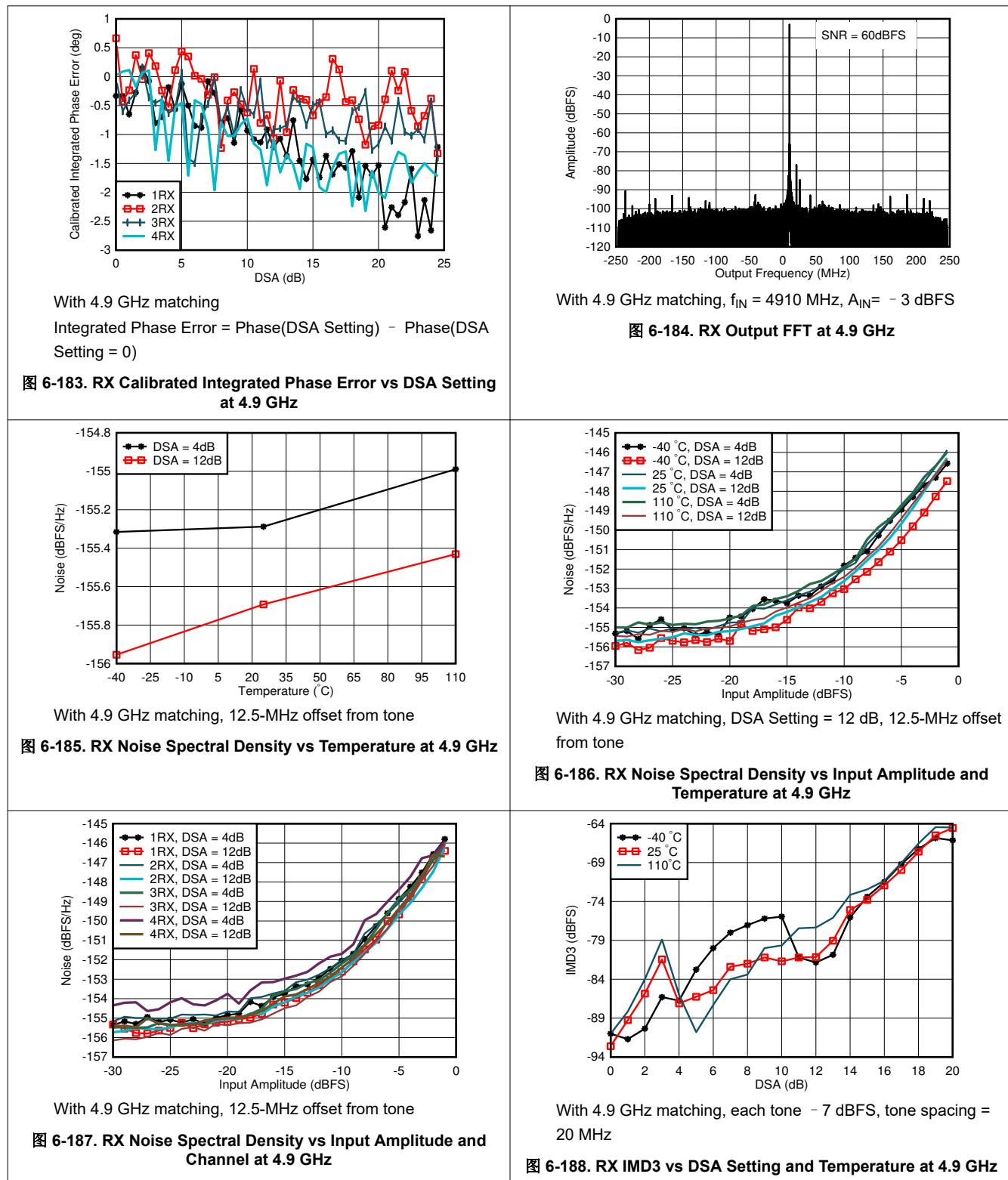
With 4.9 GHz matching

$$\text{Integrated Phase Error} = \text{Phase}(\text{DSA Setting}) - \text{Phase}(\text{DSA Setting} = 0)$$

**图 6-182. RX Uncalibrated Integrated Phase Error vs DSA Setting at 4.9 GHz**

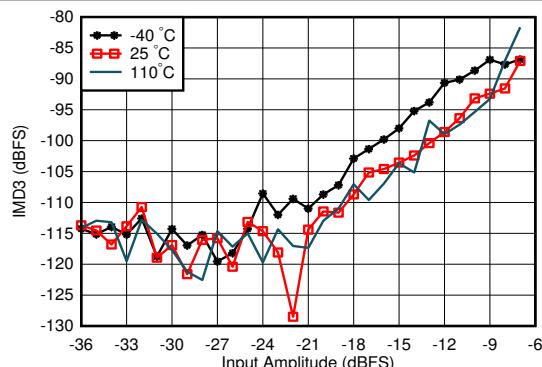
### 6.11.6 RX Typical Characteristics 4.9GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{IN}} = -3\text{ dBFS}$ , DSA setting = 4 dB.



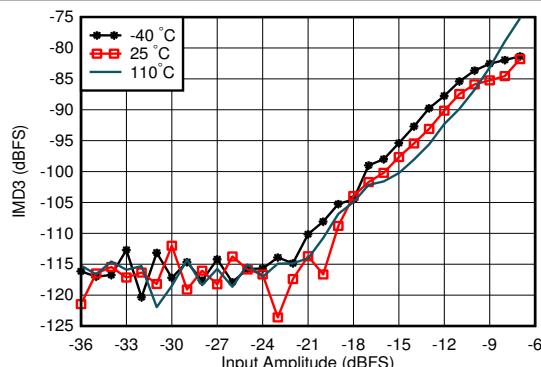
### 6.11.6 RX Typical Characteristics 4.9GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{IN}} = -3\text{ dBFS}$ , DSA setting = 4 dB.



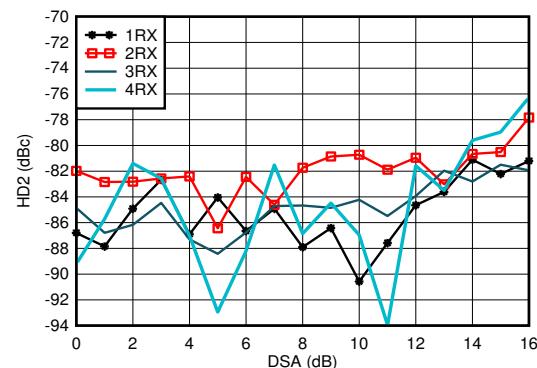
With 4.9 GHz matching, tone spacing = 20 MHz, DSA = 4 dB

图 6-189. RX IMD3 vs Input Level and Temperature at 4.9 GHz



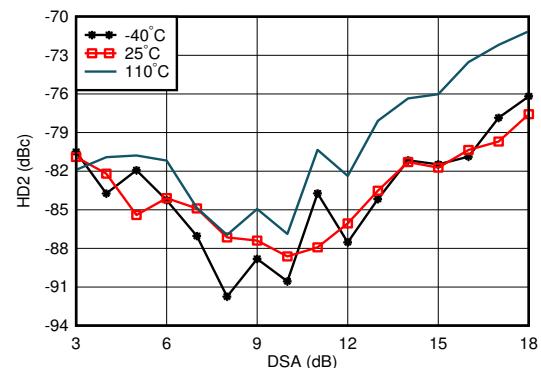
With 4.9 GHz matching, tone spacing = 20 MHz, DSA = 12 dB

图 6-190. RX IMD3 vs Input Level and Temperature at 4.9 GHz



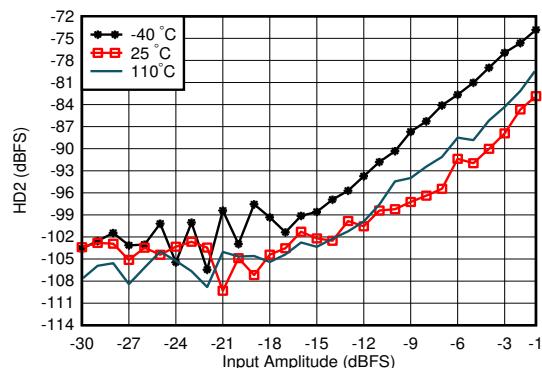
With 4.9 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

图 6-191. RX HD2 vs DSA Setting and Channel at 4.9 GHz



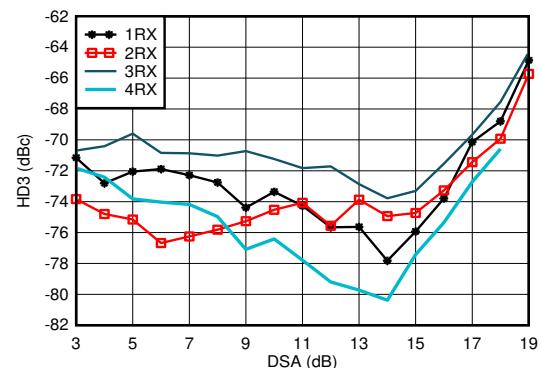
With 4.9 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

图 6-192. RX HD2 vs DSA and Temperature at 4.9 GHz



With 4.9 GHz matching, measured after HD2 trim, DDC bypass mode (TI only mode for characterization)

图 6-193. RX HD2 vs Input Level and Temperature at 4.9 GHz

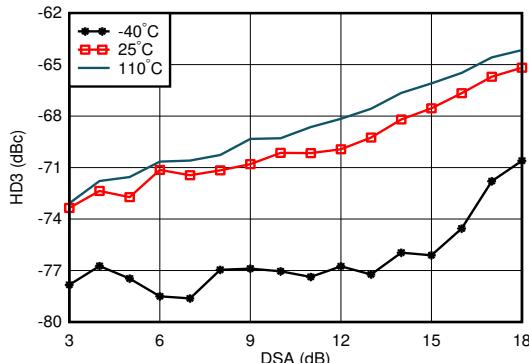


With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

图 6-194. RX HD3 vs DSA Setting and Channel at 4.9 GHz

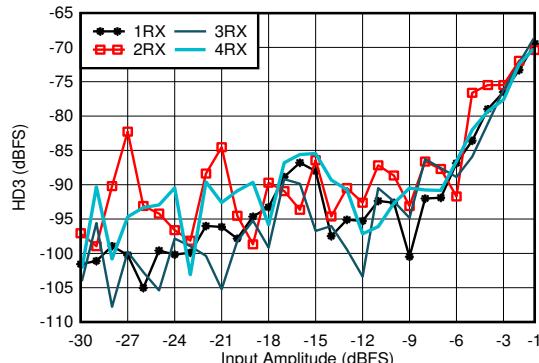
### 6.11.6 RX Typical Characteristics 4.9GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{IN}} = -3\text{ dBFS}$ , DSA setting = 4 dB.



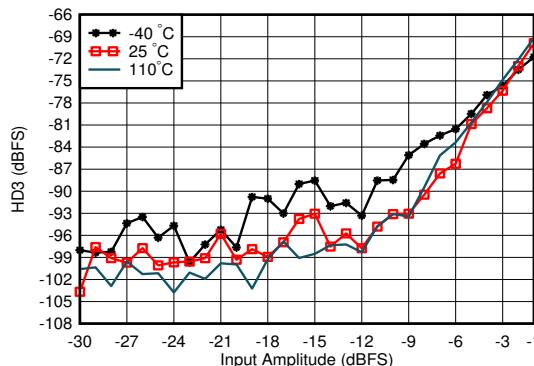
With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

图 6-195. RX HD3 vs DSA Setting and Temperature at 4.9 GHz



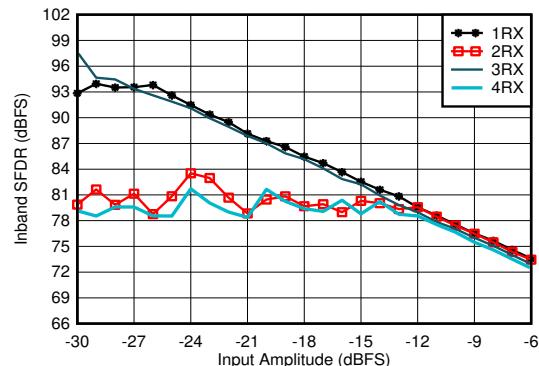
With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

图 6-196. RX HD3 vs Input Level and Channel at 4.9 GHz



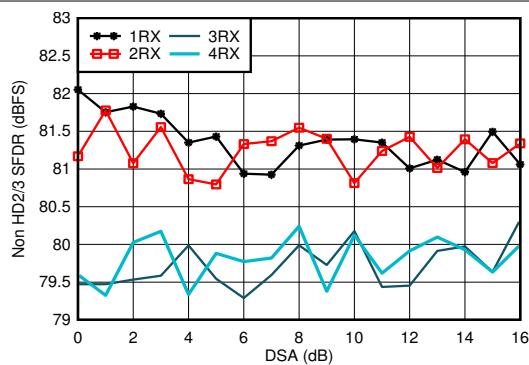
With 4.9 GHz matching, DDC bypass mode (TI only mode for characterization)

图 6-197. RX HD3 vs Input Level and Temperature at 4.9 GHz



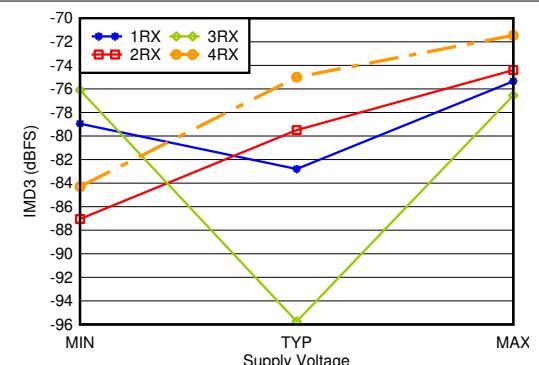
With 4.9 GHz matching, decimate by 3

图 6-198. RX In-Band SFDR (±400 MHz) vs Input Amplitude and Channel at 4.9 GHz



With 4.9 GHz matching

图 6-199. RX Non-HD2/3 vs DSA Setting at 4.9 GHz

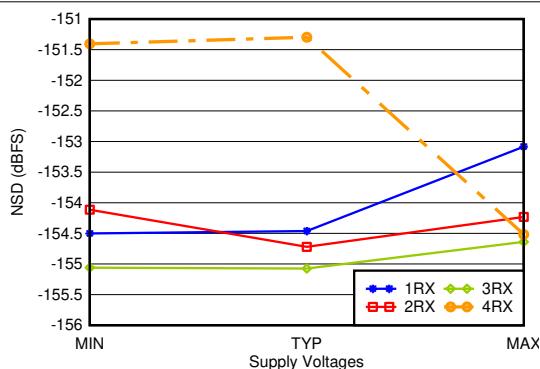


With 4.9 GHz matching, -7 dBFS each tone, 20-MHz tone spacing, all supplies at MIN, TYP, or MAX recommended operating voltages

图 6-200. RX IMD3 vs Supply and Channel at 4.9 GHz

### 6.11.6 RX Typical Characteristics 4.9GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ , ADC Sampling Rate = 2949.12 GHz. Default conditions: output sample rate = 491.52MSPS (decimate by 6), PLL clock mode with  $f_{\text{REF}} = 491.52\text{MHz}$ ,  $A_{\text{IN}} = -3\text{ dBFS}$ , DSA setting = 4 dB.



With 4.9 GHz matching, 12.5-MHz offset, all supplies at MIN, TYP, or MAX recommended operating voltages

图 6-201. RX Noise Spectral Density vs Supply and Channel at 4.9 GHz

### 6.11.7 RX Typical Characteristics 6.8GHz

Typical values at  $T_A = +25^\circ\text{C}$ . Default conditions at 30MHz: ADC Sampling Rate = 3000MSPS, output sample rate = 1500MSPS (decimate by 2x), External clock mode ,  $A_{\text{IN}} = -3\text{ dBFS}$ , DSA setting = 3 dB.

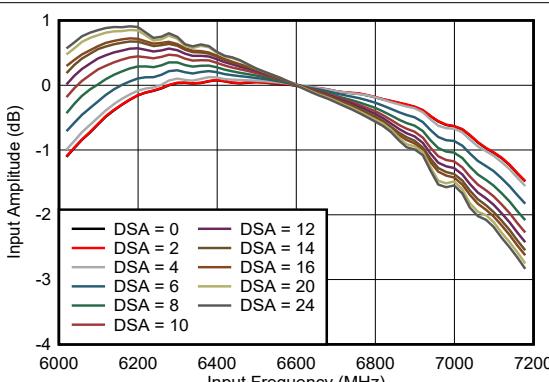


图 6-202. RX In-Band Gain Flatness

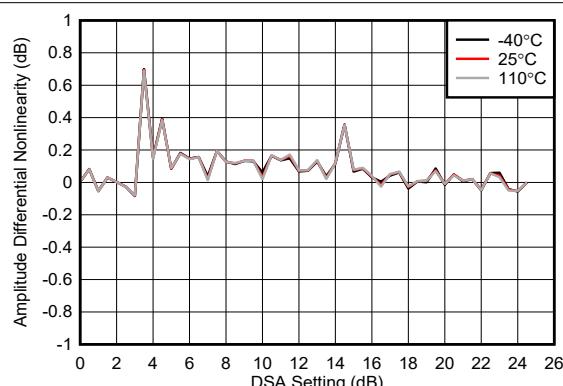
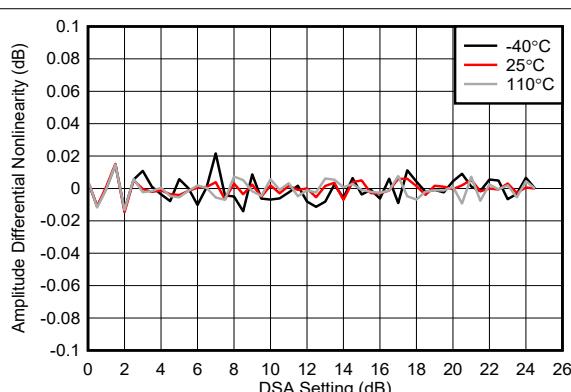


图 6-203. RX Uncalibrated Differential Amplitude Error at 6.851GHz



Calibrated at 25°C, held at -40 and 110°C

图 6-204. RX Calibrated Differential Amplitude Error at 6.851GHz

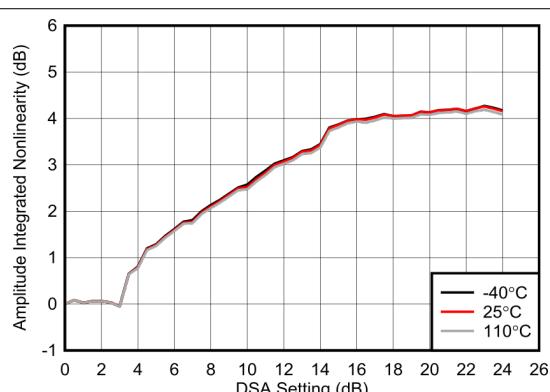
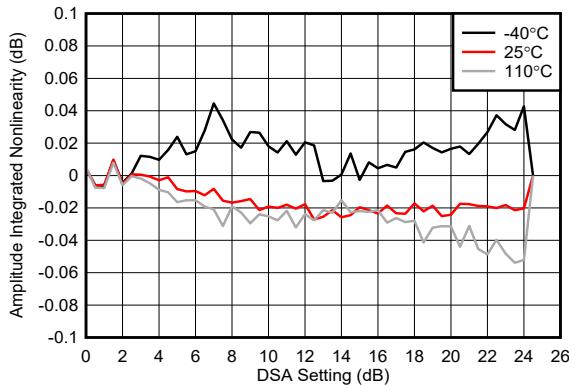


图 6-205. RX Uncalibrated Integrated Amplitude Error at 6.851GHz

### 6.11.7 RX Typical Characteristics 6.8GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ . Default conditions at 30MHz: ADC Sampling Rate = 3000MSPS, output sample rate = 1500MSPS (decimate by 2x), External clock mode,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 3 dB.



Calibrated at 25°C, held at -40 and 110°C

图 6-206. RX Calibrated Integrated Amplitude Error at 6.851GHz

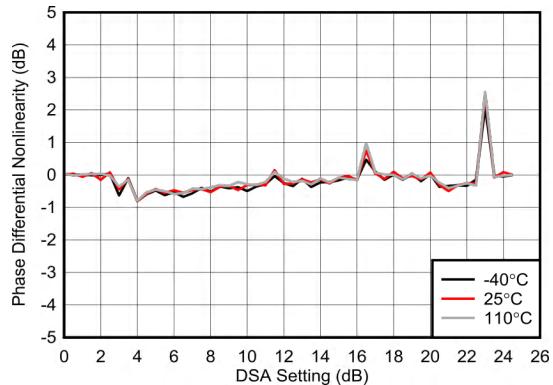
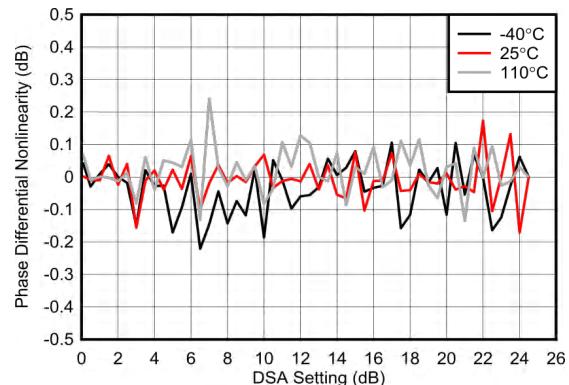


图 6-207. RX Uncalibrated Differential Phase Error at 6.851GHz



Calibrated at 25°C, held at -40 and 110°C

图 6-208. RX Calibrated Differential Phase Error at 6.851GHz

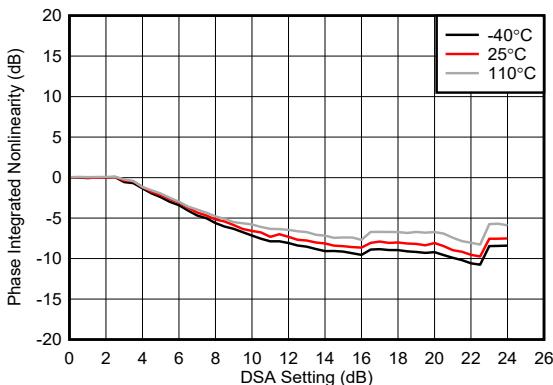
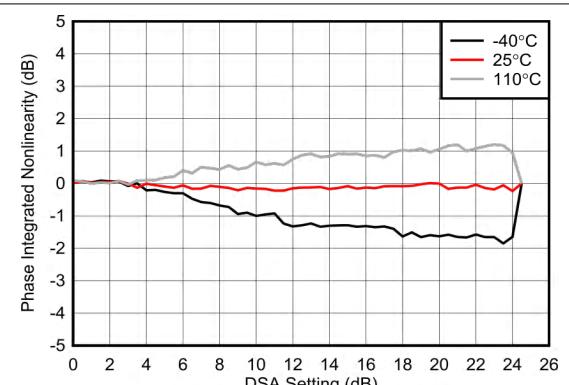
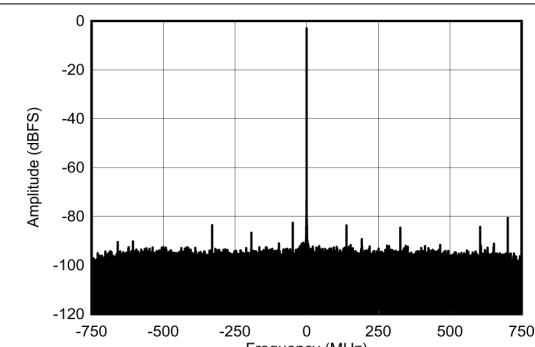


图 6-209. RX Uncalibrated Integrated Phase Error at 6.851GHz



Calibrated at 25°C, held at -40 and 110°C

图 6-210. RX Calibrated Integrated Phase Error at 6.851GHz



$F_{\text{NCO}} = 6.851\text{GHz}$ ,  $F_{\text{IN}}$  offset -130kHz

图 6-211. RX Output FFT at 6.851GHz and -3dBFS

### 6.11.7 RX Typical Characteristics 6.8GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ . Default conditions at 30MHz: ADC Sampling Rate = 3000MSPS, output sample rate = 1500MSPS (decimate by 2x), External clock mode,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 3 dB.

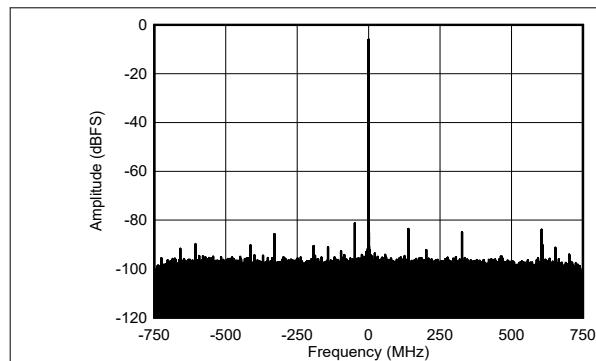


图 6-212. RX Output FFT at 6.851GHz and -6dBFS

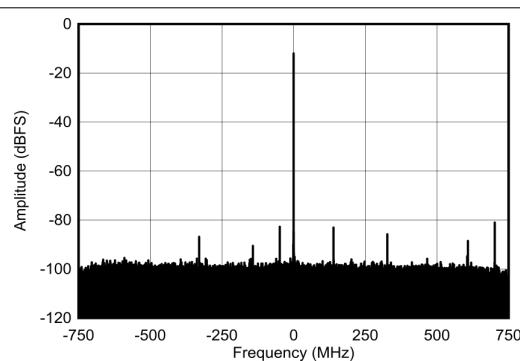


图 6-213. RX Output FFT at 6.851GHz and -12dBFS

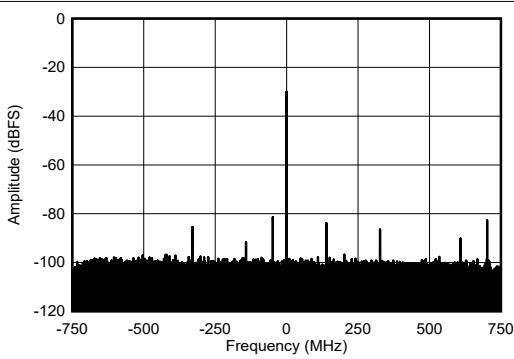


图 6-214. RX Output FFT at 6.851GHz and -30dBFS

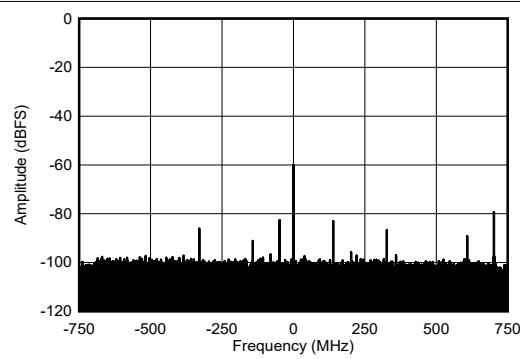


图 6-215. RX Output FFT at 6.851GHz and -60dBFS

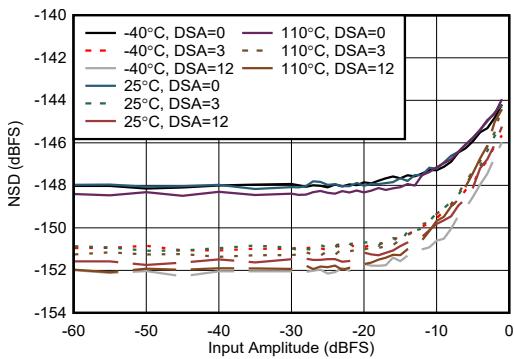


图 6-216. RX NSD vs Input Amplitude at 6.851GHz

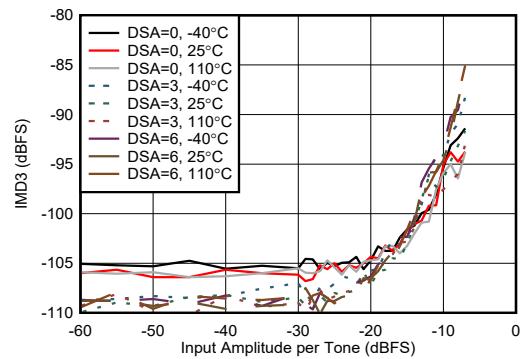
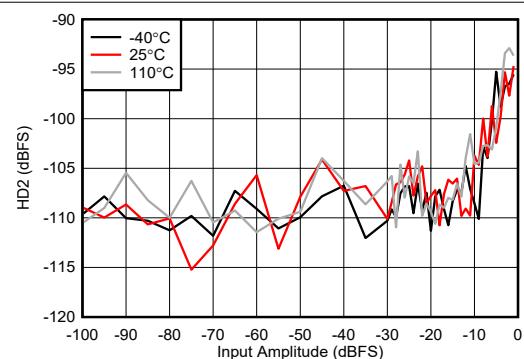
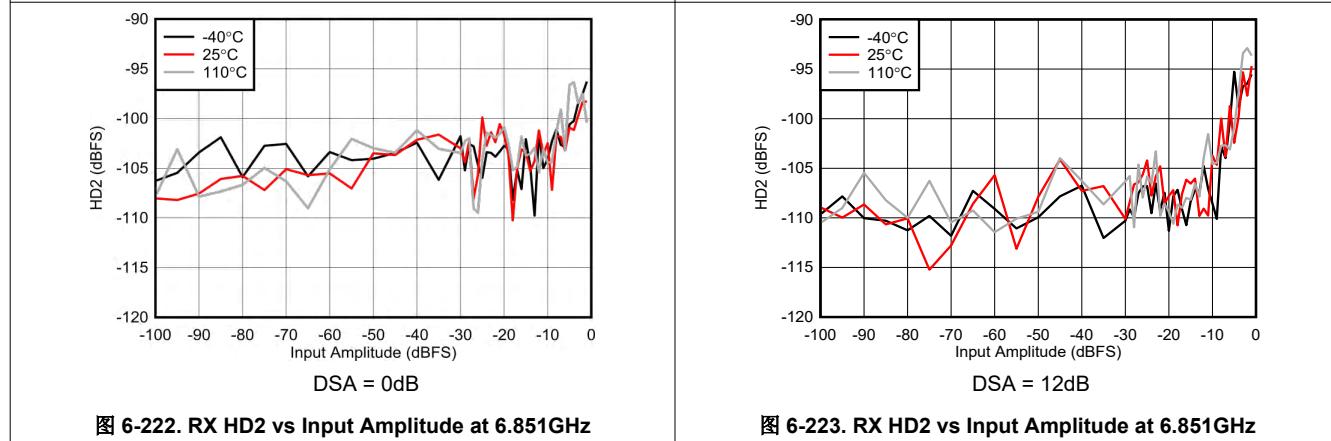
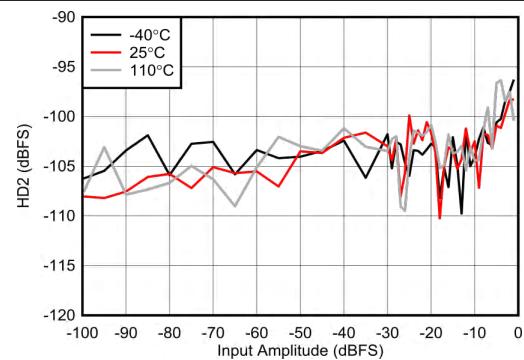
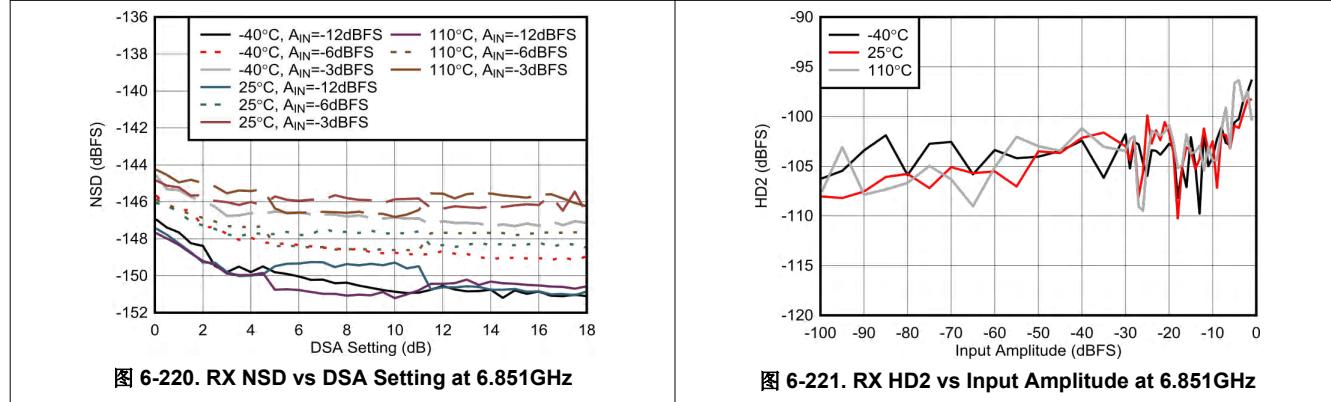
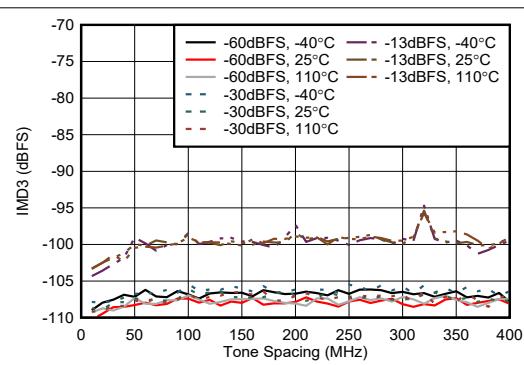
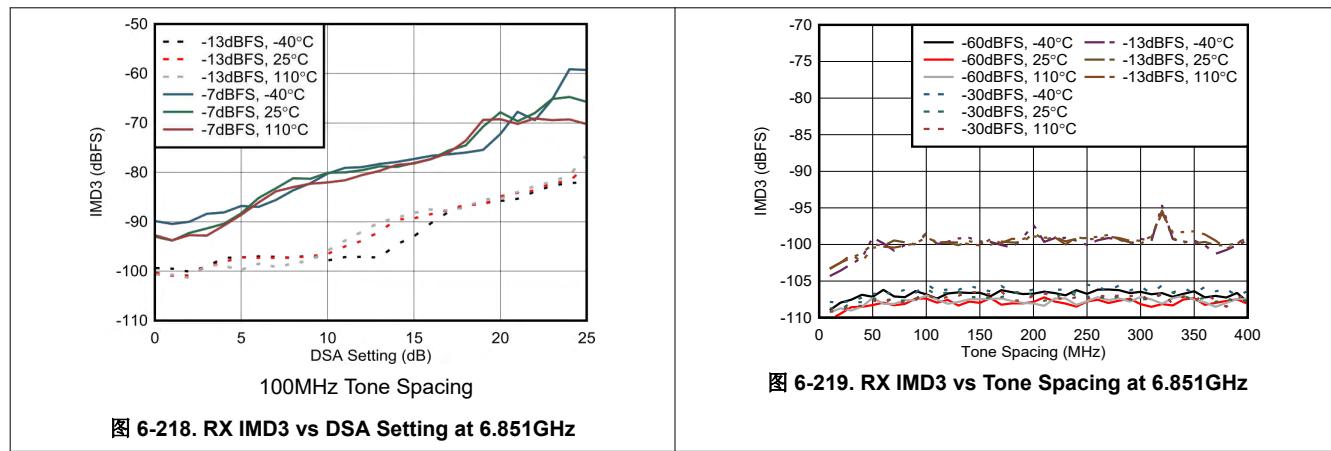


图 6-217. RX IMD3 vs Input Amplitude at 6.851GHz

### 6.11.7 RX Typical Characteristics 6.8GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ . Default conditions at 30MHz: ADC Sampling Rate = 3000MSPS, output sample rate = 1500MSPS (decimate by 2x), External clock mode,  $A_{IN} = -3 \text{ dBFS}$ , DSA setting = 3 dB.



### 6.11.7 RX Typical Characteristics 6.8GHz (continued)

Typical values at  $T_A = +25^\circ\text{C}$ . Default conditions at 30MHz: ADC Sampling Rate = 3000MSPS, output sample rate = 1500MSPS (decimate by 2x), External clock mode,  $A_{\text{IN}} = -3 \text{ dBFS}$ , DSA setting = 3 dB.

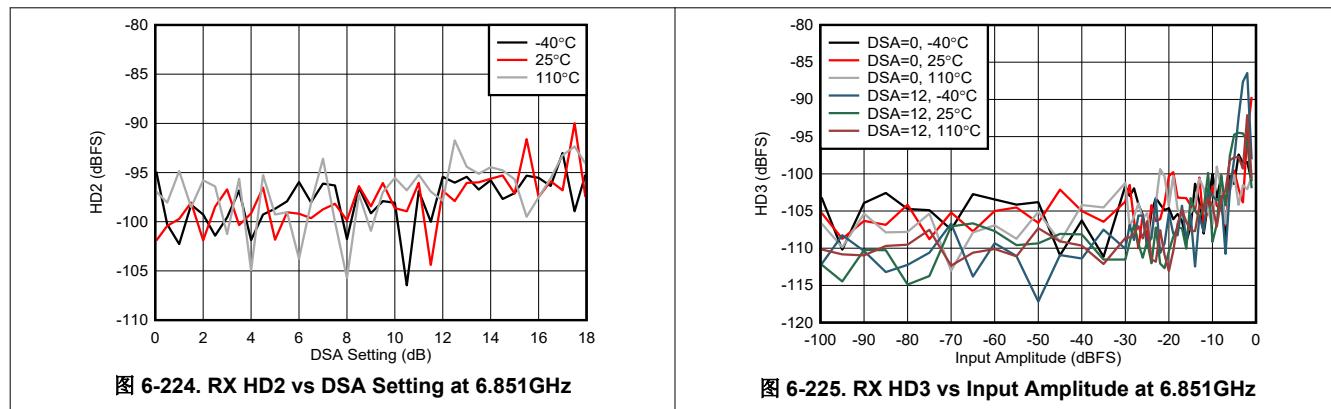


图 6-224. RX HD2 vs DSA Setting at 6.851GHz

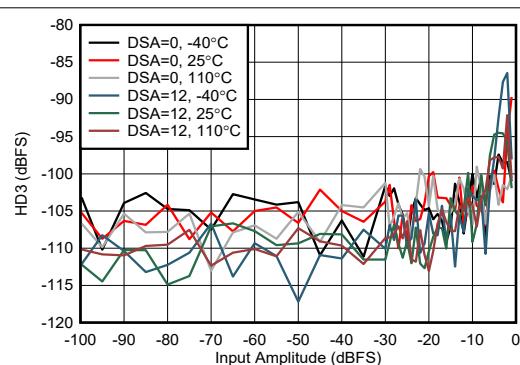


图 6-225. RX HD3 vs Input Amplitude at 6.851GHz

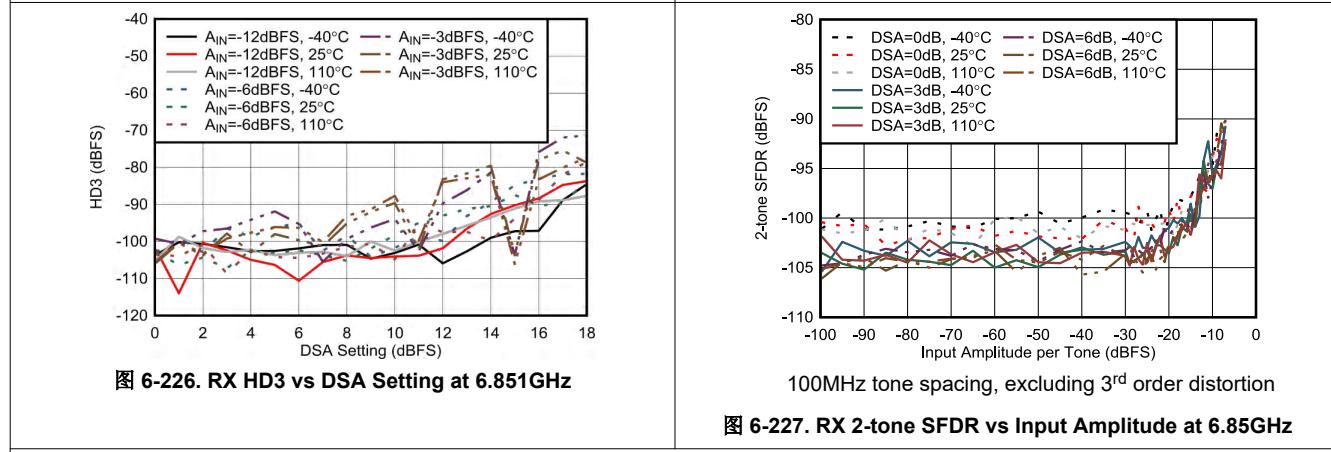
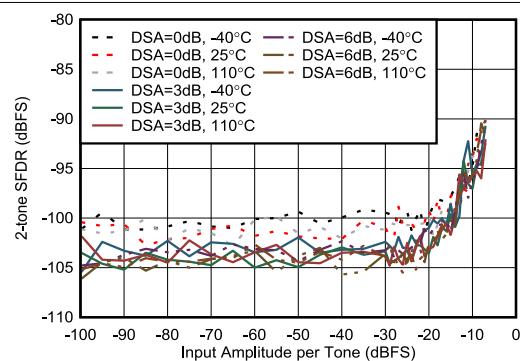


图 6-226. RX HD3 vs DSA Setting at 6.851GHz



100MHz tone spacing, excluding 3<sup>rd</sup> order distortion

图 6-227. RX 2-tone SFDR vs Input Amplitude at 6.85GHz

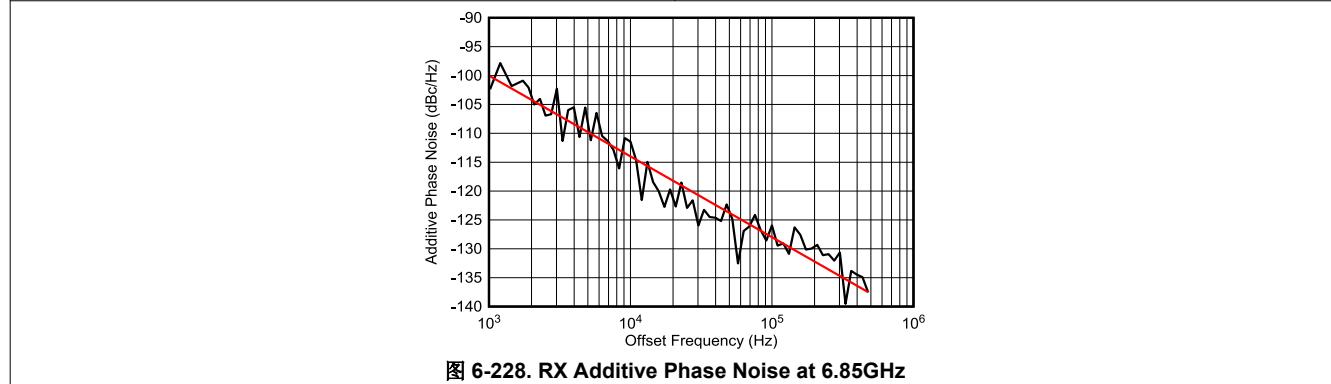
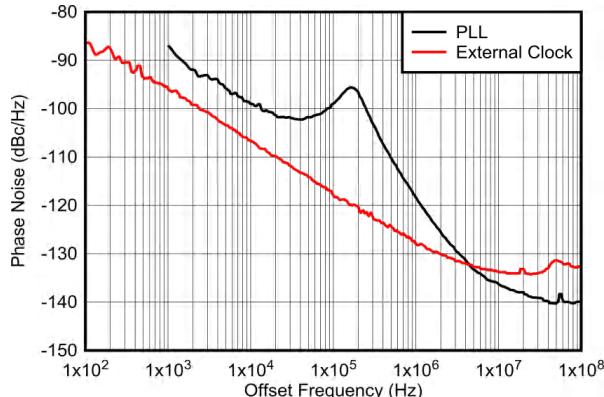


图 6-228. RX Additive Phase Noise at 6.85GHz

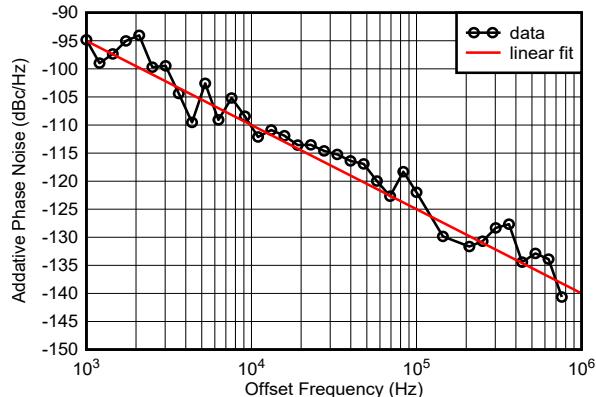
### 6.11.8 PLL and Clock Typical Characteristics

Typical values at  $T_A = +25^\circ\text{C}$  with nominal supplies. Unless otherwise noted,  $f_{\text{REF}} = 491.52 \text{ MHz}$ , Phase noise measured at TX output

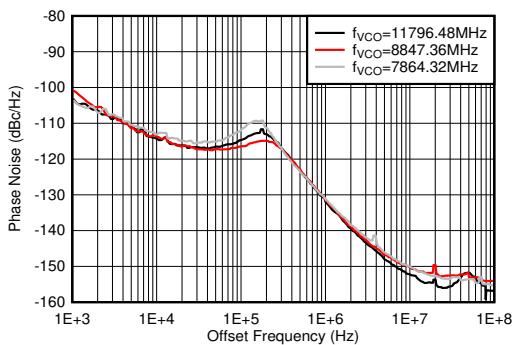


measured at TX output, normalized to 12GHz by  
 $20 \times \log_{10}(12\text{GHz}/F_{\text{OUT}})$

**图 6-229. Phase Noise vs Offset Frequency for PLL and External Clock at 12GHz**

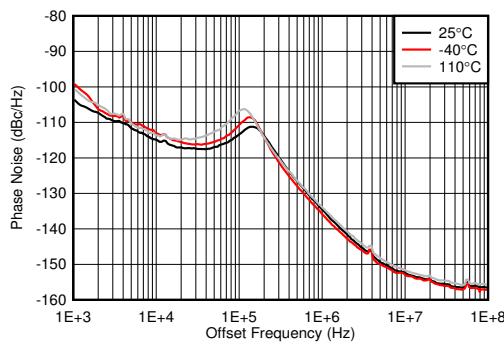


**图 6-230. RX Additive Phase Noise at 9.61GHz**



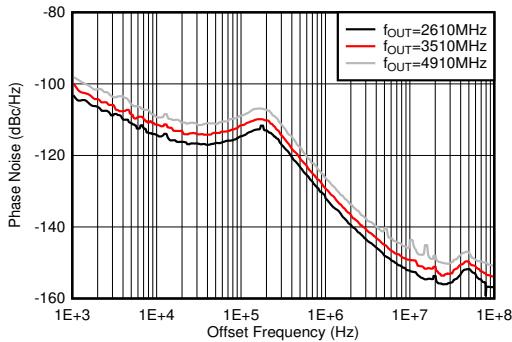
PLL enabled,  $f_{\text{REF}} = 491.52 \text{ MSPS}$ , measured at 2TXOUT

**图 6-231. Phase Noise vs Offset Frequency and fVCO at fOUT = 2610 MHz**



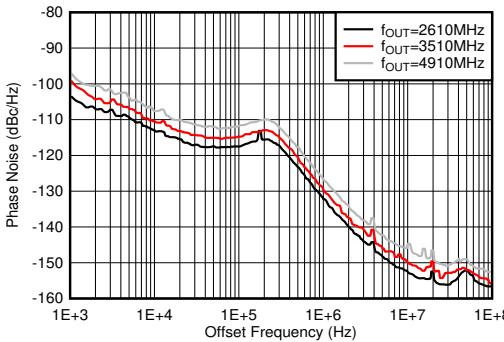
PLL enabled,  $f_{\text{VCO}} = 11796.48 \text{ MHz}$ ,  $f_{\text{REF}} = 491.52 \text{ MSPS}$ , measured at 2TXOUT

**图 6-232. Phase Noise for 12-GHz VCO vs Offset Frequency and Temperature at fOUT = 1910 MHz**



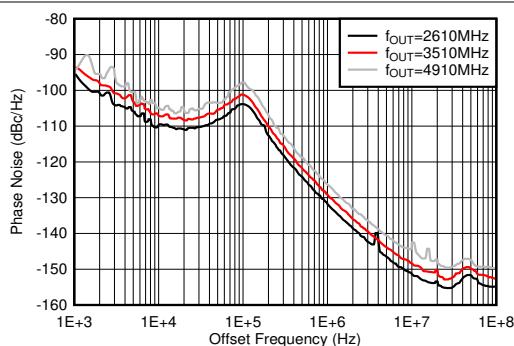
PLL enabled,  $f_{\text{VCO}} = 11796.48 \text{ MHz}$ ,  $f_{\text{REF}} = 491.52 \text{ MSPS}$ , measured at 2TXOUT

**图 6-233. Phase Noise for 12-GHz VCO vs Offset Frequency and fOUT at 25°C**



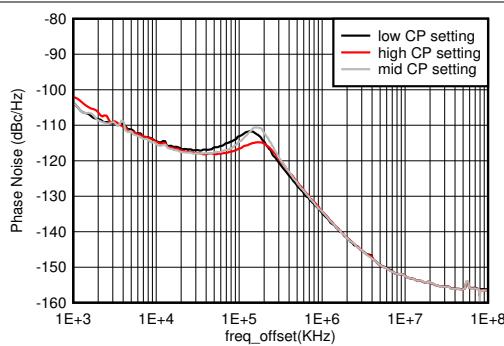
PLL enabled,  $f_{\text{VCO}} = 11796.48 \text{ MHz}$ ,  $f_{\text{REF}} = 491.52 \text{ MSPS}$ , measured at 2TXOUT

**图 6-234. Phase Noise for 12-GHz VCO vs Offset Frequency and fOUT at -40°C**



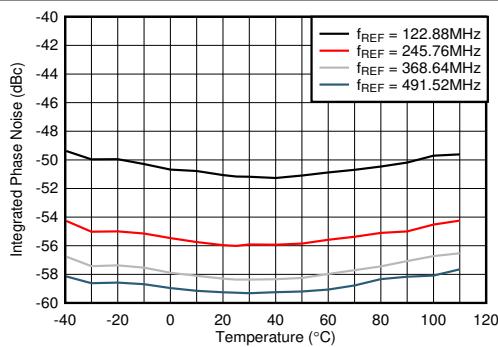
PLL enabled,  $f_{VCO} = 11796.48$  MHz,  $f_{REF} = 491.52$  MSPS,  
measured at 2TXOUT

图 6-235. Phase Noise for 12-GHz VCO vs Offset Frequency and  $f_{OUT}$  at 110°C



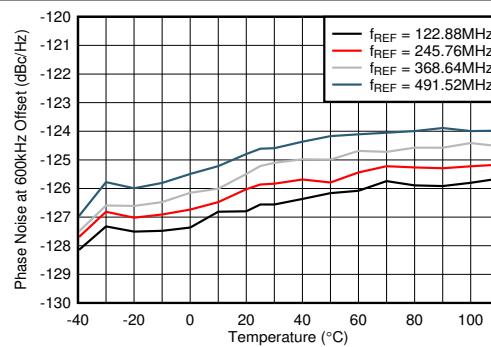
PLL enabled,  $f_{VCO} = 11796.48$  MHz,  $f_{REF} = 491.52$  MSPS,  
measured at 2TXOUT

图 6-236. Phase Noise for 12-GHz VCO vs Offset Frequency and CP Setting at  $f_{OUT} = 2.6$  GHz



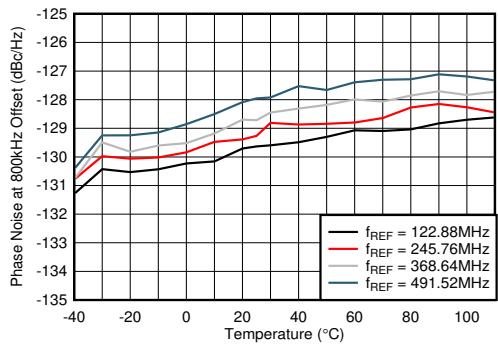
PLL enabled,  $f_{VCO} = 11796.48$  MHz, 1-kHz to 100-MHz,  
single-sided integration bandwidth, measured at 2TXOUT

图 6-237. Integrated Phase Noise for 12-GHz VCO vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz



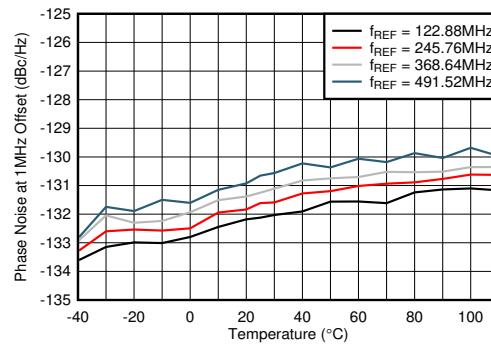
PLL enabled,  $f_{VCO} = 11796.48$  MHz, measured at 2TXOUT

图 6-238. Phase Noise for 12-GHz VCO at 600kHz Offset vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz



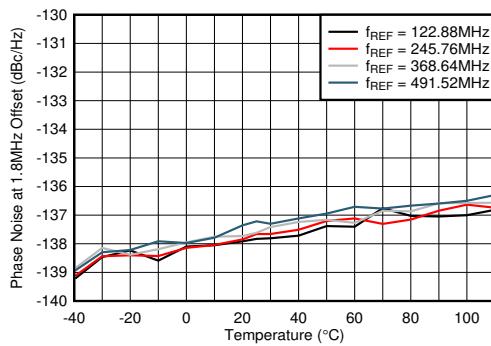
A. PLL enabled,  $f_{VCO} = 11796.48$  MHz, measured at 2TXOUT

图 6-239. Phase Noise for 12-GHz VCO at 800-kHz Offset vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz



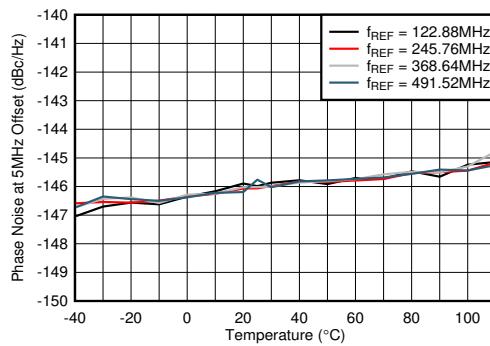
PLL enabled,  $f_{VCO} = 11796.48$  MHz, measured at 2TXOUT

图 6-240. Phase Noise for 12-GHz VCO at 1-MHz Offset vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz



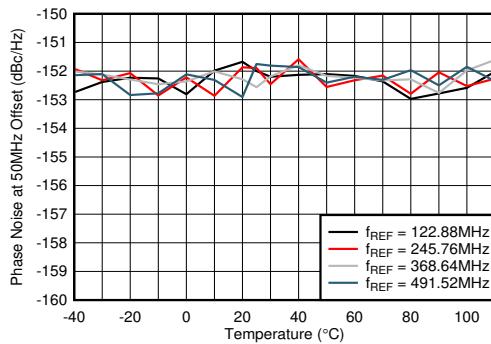
PLL enabled,  $f_{VCO} = 11796.48$  MHz, measured at 2TXOUT

**图 6-241. Phase Noise for 12-GHz VCO at 1.8-MHz Offset vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



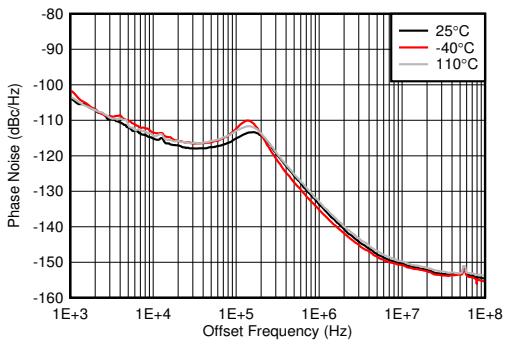
PLL enabled,  $f_{VCO} = 11796.48$  MHz, measured at 2TXOUT

**图 6-242. Phase Noise for 12-GHz VCO at 5-MHz Offset vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



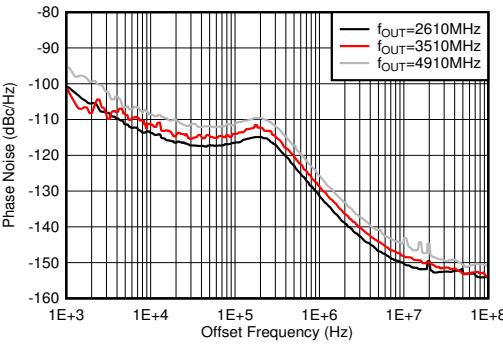
PLL enabled,  $f_{VCO} = 11796.48$  MHz, measured at 2TXOUT

**图 6-243. Phase Noise for 12-GHz VCO at 50-MHz Offset vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



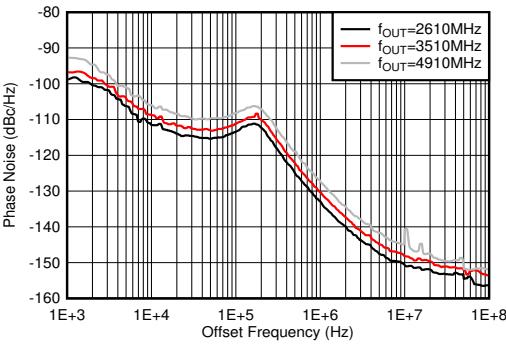
PLL enabled,  $f_{VCO} = 9830.4$  MHz,  $f_{REF} = 491.52$  MSPS, measured at 2TXOUT

**图 6-244. Phase Noise for 10-GHz VCO vs Offset Frequency and Temperature at  $f_{OUT} = 1910$  MHz**



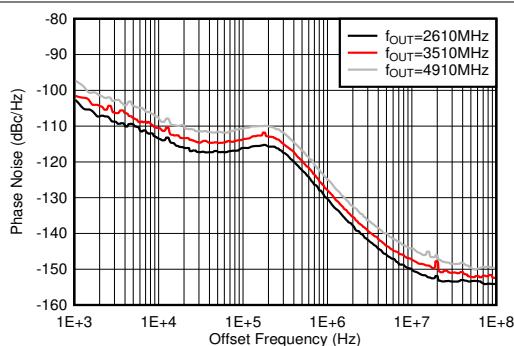
PLL enabled,  $f_{VCO} = 9830.4$  MHz,  $f_{REF} = 491.52$  MSPS, measured at 2TXOUT

**图 6-245. Phase Noise for 10-GHz VCO vs Offset Frequency and  $f_{OUT}$  at  $25^{\circ}\text{C}$**



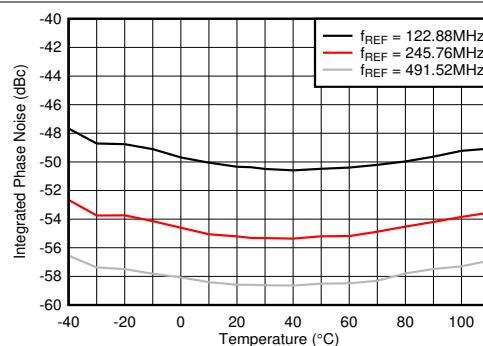
PLL enabled,  $f_{VCO} = 9830.4$  MHz,  $f_{REF} = 491.52$  MSPS, measured at 2TXOUT

**图 6-246. Phase Noise for 10-GHz VCO vs Offset Frequency and  $f_{OUT}$  at  $-40^{\circ}\text{C}$**



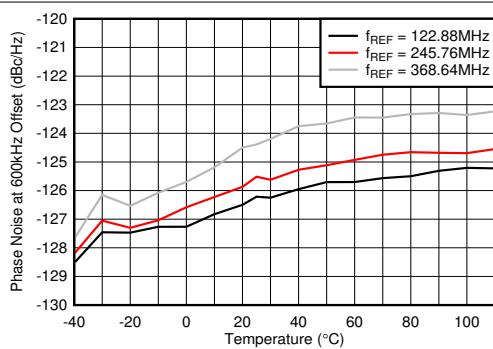
PLL enabled,  $f_{VCO} = 9830.4$  MHz,  $f_{REF} = 491.52$  MSPS, measured at 2TXOUT

**图 6-247. Phase Noise for 10-GHz VCO vs Offset Frequency and  $f_{OUT}$  at 110°C**



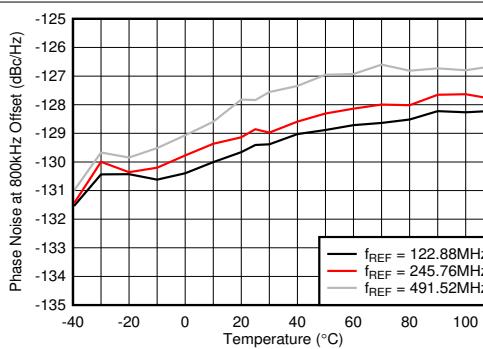
PLL enabled,  $f_{VCO} = 9830.4$  MHz, 1-kHz to 100-MHz, single-sided integration bandwidth, measured at 2TXOUT

**图 6-248. Integrated Phase Noise for 10-GHz VCO vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



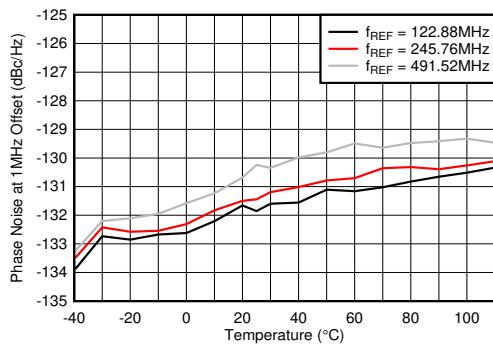
PLL enabled,  $f_{VCO} = 9830.4$  MHz, measured at 2TXOUT

**图 6-249. Phase Noise for 10-GHz VCO at 600 kHz vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



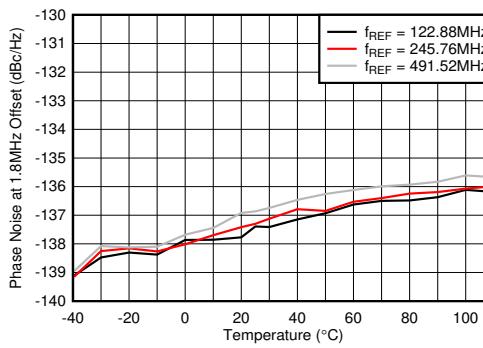
PLL enabled,  $f_{VCO} = 9830.4$  MHz, measured at 2TXOUT

**图 6-250. Phase Noise for 10-GHz VCO at 800 kHz vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



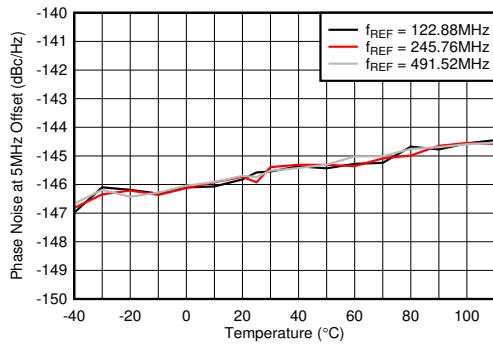
PLL enabled,  $f_{VCO} = 9830.4$  MHz, measured at 2TXOUT

**图 6-251. Phase Noise for 10-GHz VCO at 1 MHz vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



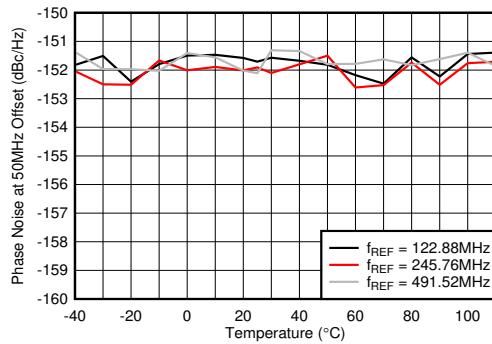
PLL enabled,  $f_{VCO} = 9830.4$  MHz, measured at 2TXOUT

**图 6-252. Phase Noise for 10-GHz VCO at 1.8 MHz vs Temperature and  $f_{REF}$  at  $f_{OUT} = 2.6$  GHz**



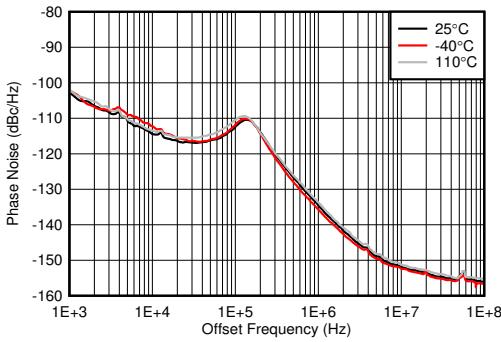
PLL enabled, f<sub>VCO</sub> = 9830.4 MHz, measured at 2TXOUT

**图 6-253. Phase Noise for 10-GHz VCO at 5 MHz vs Temperature and f<sub>REF</sub> at f<sub>OUT</sub> = 2.6 GHz**



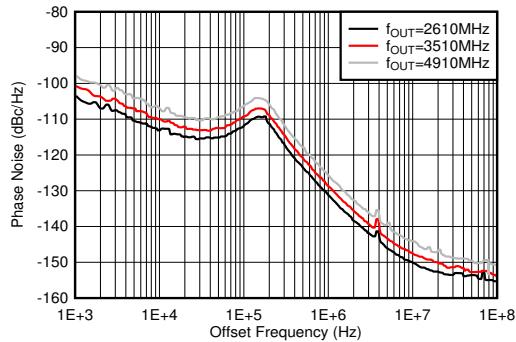
PLL enabled, f<sub>VCO</sub> = 9830.4 MHz, measured at 2TXOUT

**图 6-254. Phase Noise for 10-GHz VCO at 50 MHz vs Temperature and f<sub>REF</sub> at f<sub>OUT</sub> = 2.6 GHz**



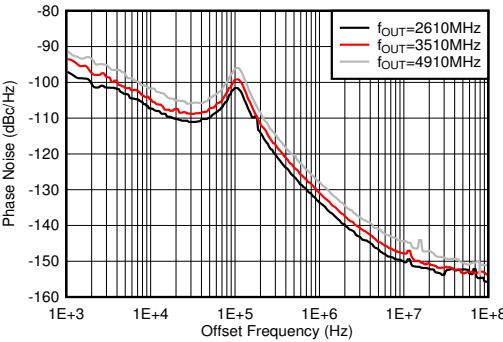
PLL enabled, f<sub>VCO</sub> = 8847.36 MHz, f<sub>REF</sub> = 491.52MSPS, measured at 2TXOUT

**图 6-255. Phase Noise for 9-GHz VCO vs Offset Frequency and Temperature at f<sub>OUT</sub> = 1910 MHz**



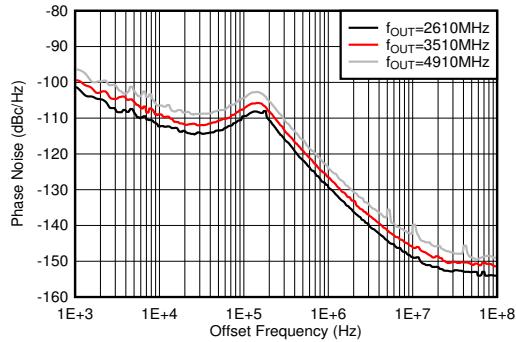
PLL enabled, f<sub>VCO</sub> = 8847.36 MHz, f<sub>REF</sub> = 491.52MSPS, measured at 2TXOUT

**图 6-256. Phase Noise for 9-GHz VCO vs Offset Frequency and f<sub>OUT</sub> at 25°C**



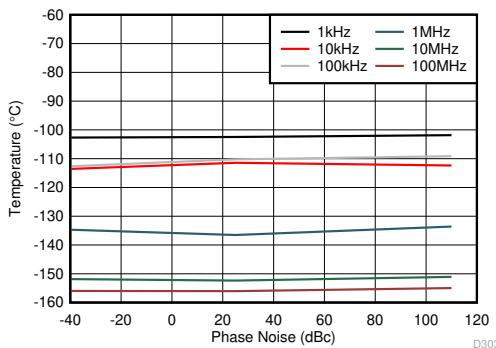
PLL enabled, f<sub>VCO</sub> = 8847.36 MHz, f<sub>REF</sub> = 491.52MSPS, measured at 2TXOUT

**图 6-257. Phase Noise for 9-GHz VCO vs Offset Frequency and f<sub>OUT</sub> at -40°C**



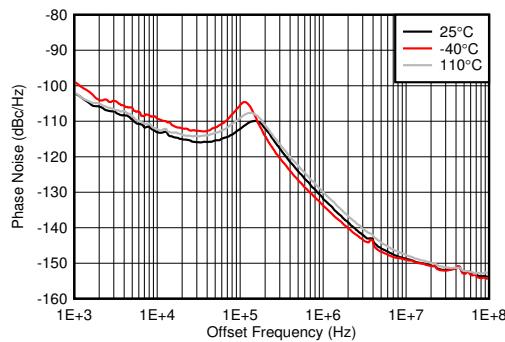
PLL enabled, f<sub>VCO</sub> = 8847.36 MHz, f<sub>REF</sub> = 491.52MSPS, measured at 2TXOUT

**图 6-258. Phase Noise for 9-GHz VCO vs Offset Frequency and f<sub>OUT</sub> at 110°C**



PLL enabled,  $f_{VCO} = 8847.36$  MHz,  $f_{REF} = 491.52$  MSPS,  
minimum LPF BW, measured at 2TXOUT

**图 6-259. Phase Noise for 9-GHz VCO vs  
Temperature Over Offset Frequency at  $f_{OUT} = 2.6$   
GHz**



PLL enabled,  $f_{VCO} = 7864.32$  MHz,  $f_{REF} = 491.52$  MSPS,  
measured at 2TXOUT

**图 6-260. Phase Noise for 8-GHz VCO vs Offset  
Frequency and Temperature at  $f_{OUT} = 1910$  MHz**

## 7 Device and Documentation Support

### 7.1 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](#) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 7.2 支持资源

[TI E2E™ 支持论坛](#)是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

### 7.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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### 7.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能导致器件与其发布的规格不相符。

### 7.5 术语表

#### [TI 术语表](#)

本术语表列出并解释了术语、首字母缩略词和定义。

## 8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)  | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| AFE7906IABJ      | ACTIVE        | FCBGA        | ABJ             | 400  | 90          | RoHS & Green     | SNAGCU                               | Level-3-260C-168 HR  | -40 to 85    | AFE7906I                | Samples |
| AFE7906IALK      | ACTIVE        | FCBGA        | ALK             | 400  | 90          | Non-RoHS & Green | Call TI                              | Level-3-220C-168 HR  | -40 to 85    | AFE7906 SNPB            | Samples |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

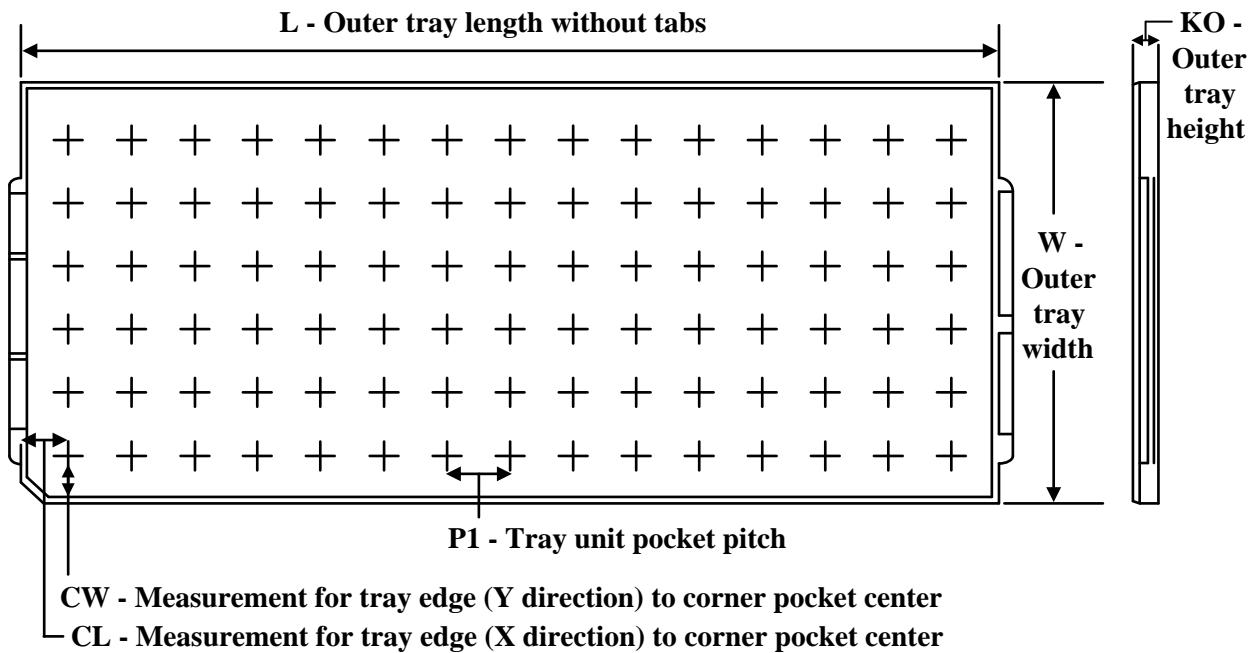
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



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**TRAY**


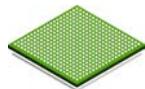
Chamfer on Tray corner indicates Pin 1 orientation of packed units.

\*All dimensions are nominal

| Device      | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|-------------|--------------|--------------|------|-----|-------------------|----------------------|--------|--------|---------|---------|---------|---------|
| AFE7906IABJ | ABJ          | FCBGA        | 400  | 90  | 6 x 15            | 150                  | 315    | 135.9  | 7620    | 19.5    | 21      | 19.2    |
| AFE7906IALK | ALK          | FCBGA        | 400  | 90  | 6 x 15            | 150                  | 315    | 135.9  | 7620    | 19.5    | 21      | 19.2    |

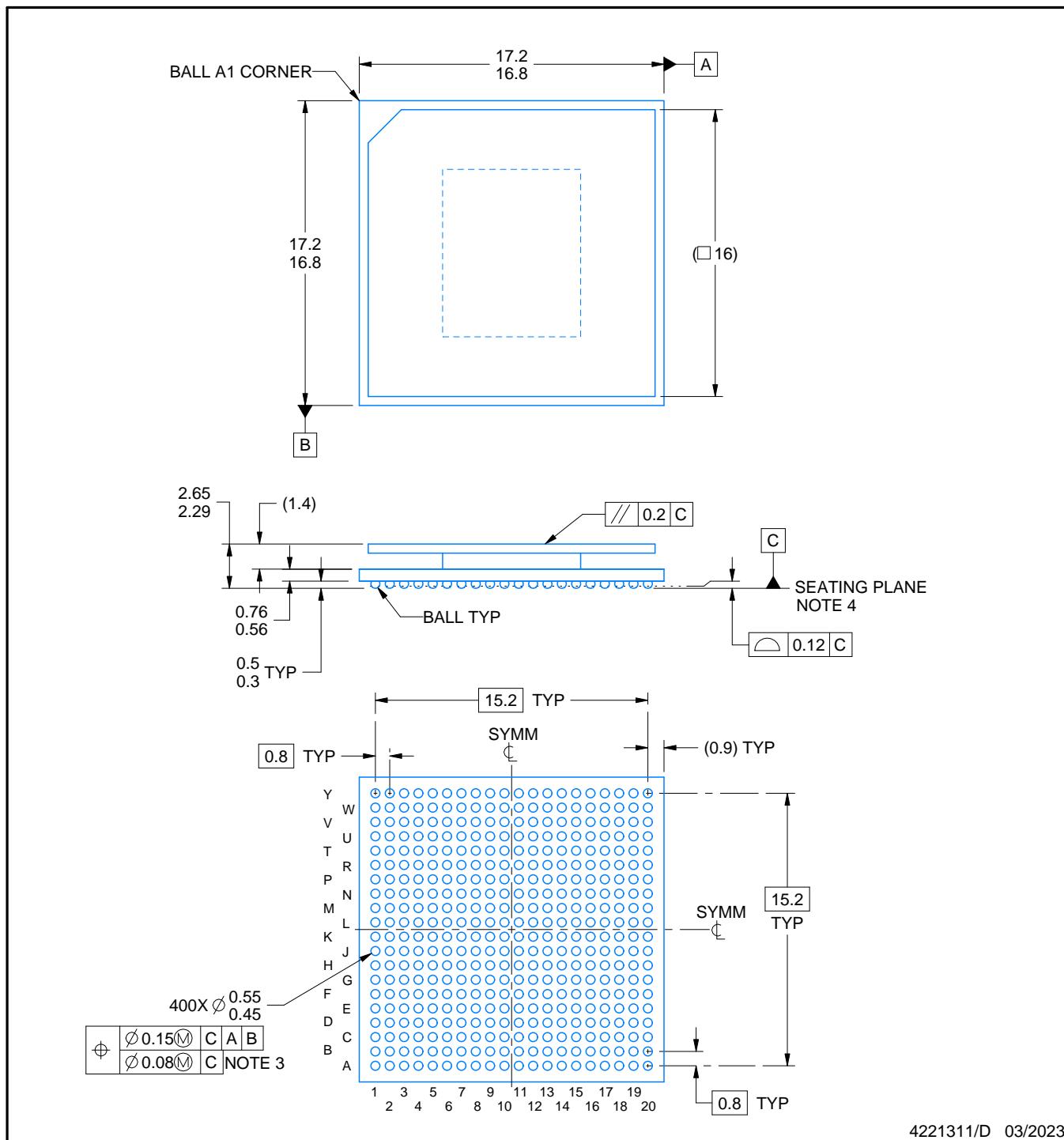
# PACKAGE OUTLINE

**ABJ0400A**



**FCCBGA - 2.65 mm max height**

BALL GRID ARRAY



4221311/D 03/2023

## NOTES:

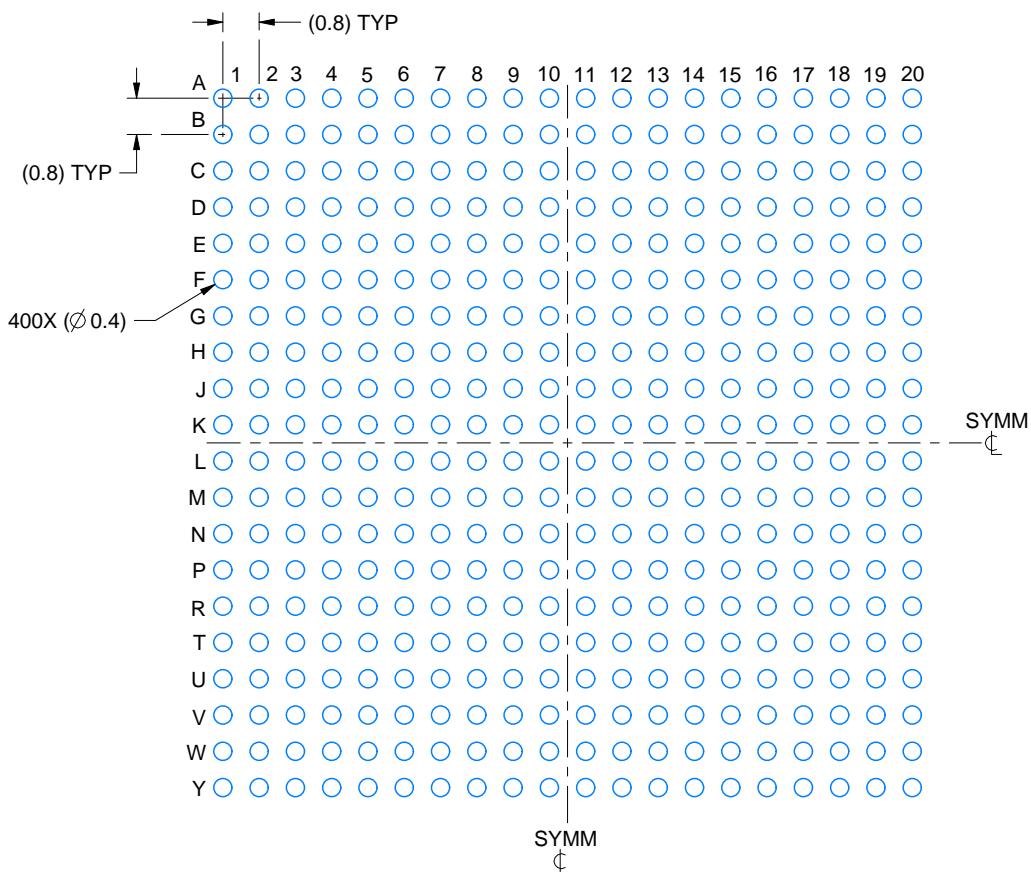
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
5. The lids are electrically floating (e.g. not tied to GND).

# EXAMPLE BOARD LAYOUT

ABJ0400A

FCBGA - 2.65 mm max height

BALL GRID ARRAY



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:6X



4221311/D 03/2023

NOTES: (continued)

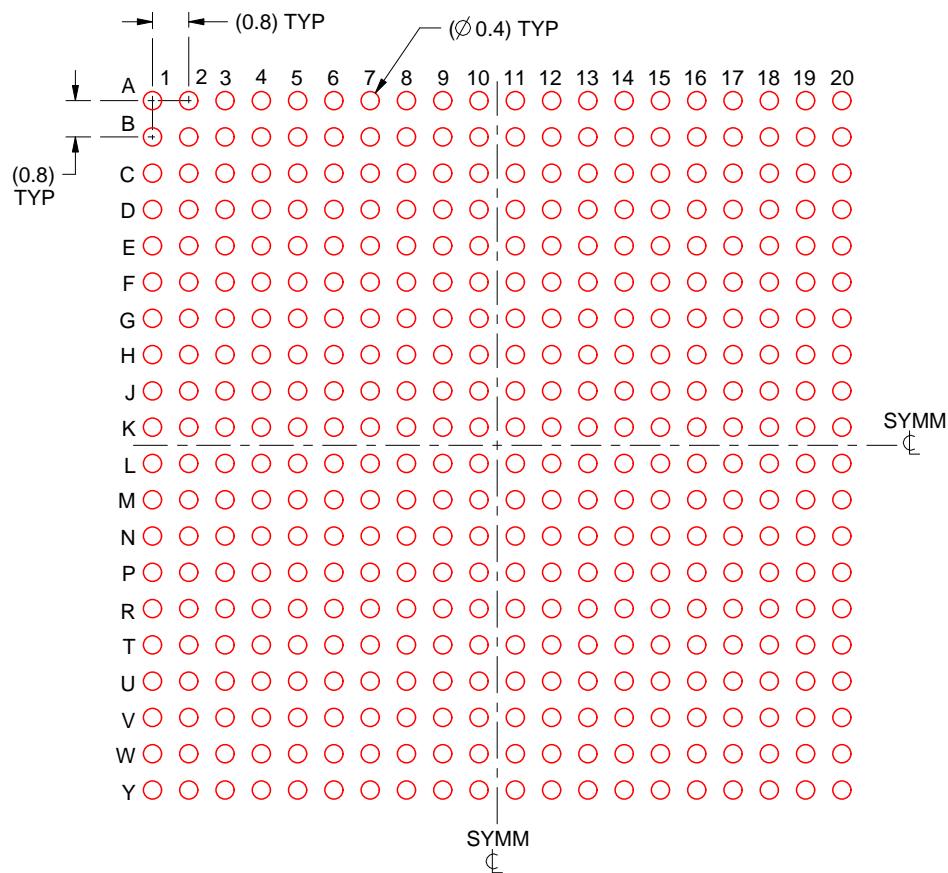
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.  
For more information, see Texas Instruments literature number SPRU811 ([www.ti.com/lit/spru811](http://www.ti.com/lit/spru811)).

# EXAMPLE STENCIL DESIGN

ABJ0400A

FCBGA - 2.65 mm max height

BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.15 mm THICK STENCIL  
SCALE:6X

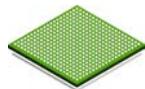
4221311/D 03/2023

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

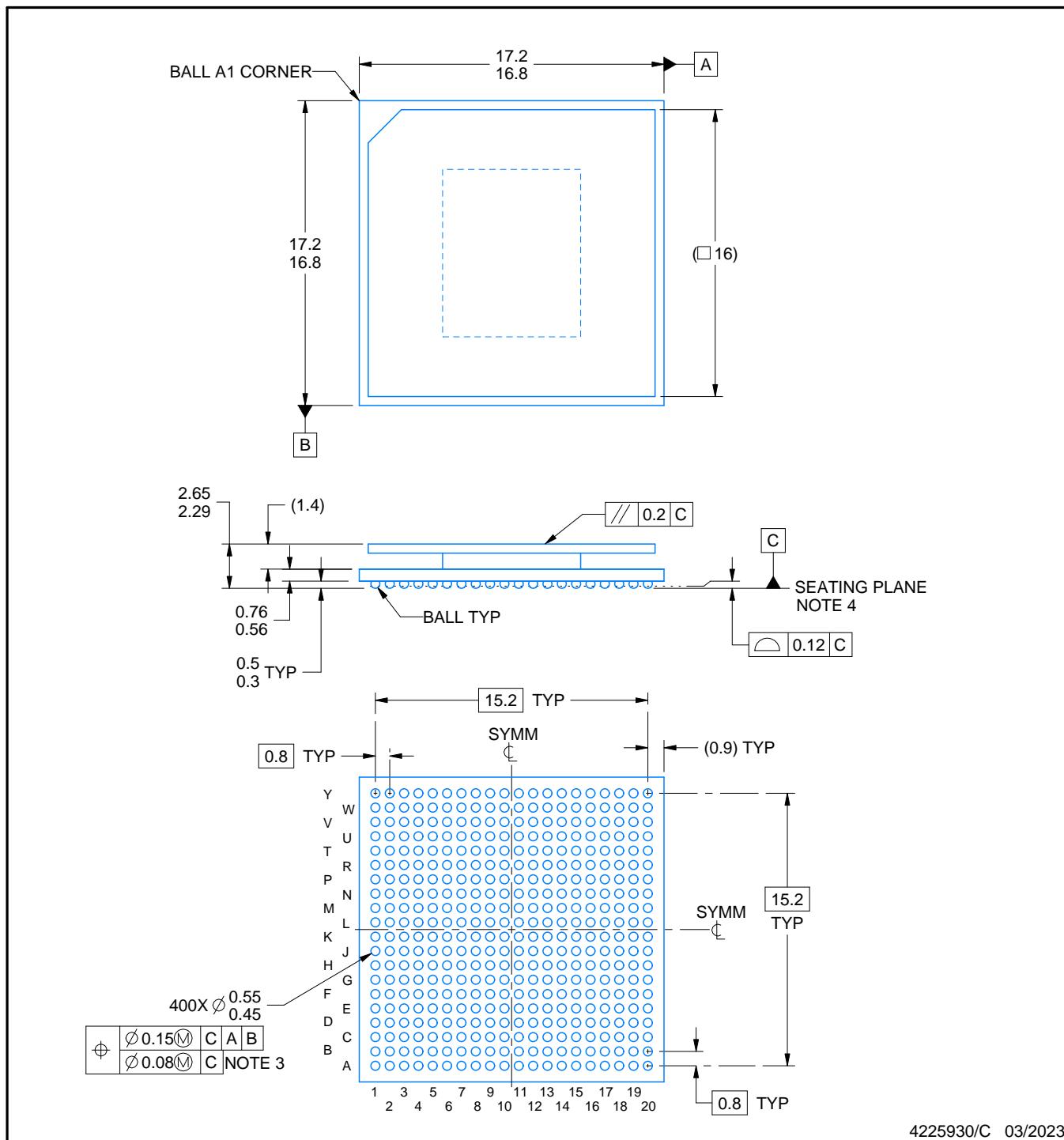
# PACKAGE OUTLINE

**ALK0400A**



**FCCBGA - 2.65 mm max height**

BALL GRID ARRAY



4225930/C 03/2023

**NOTES:**

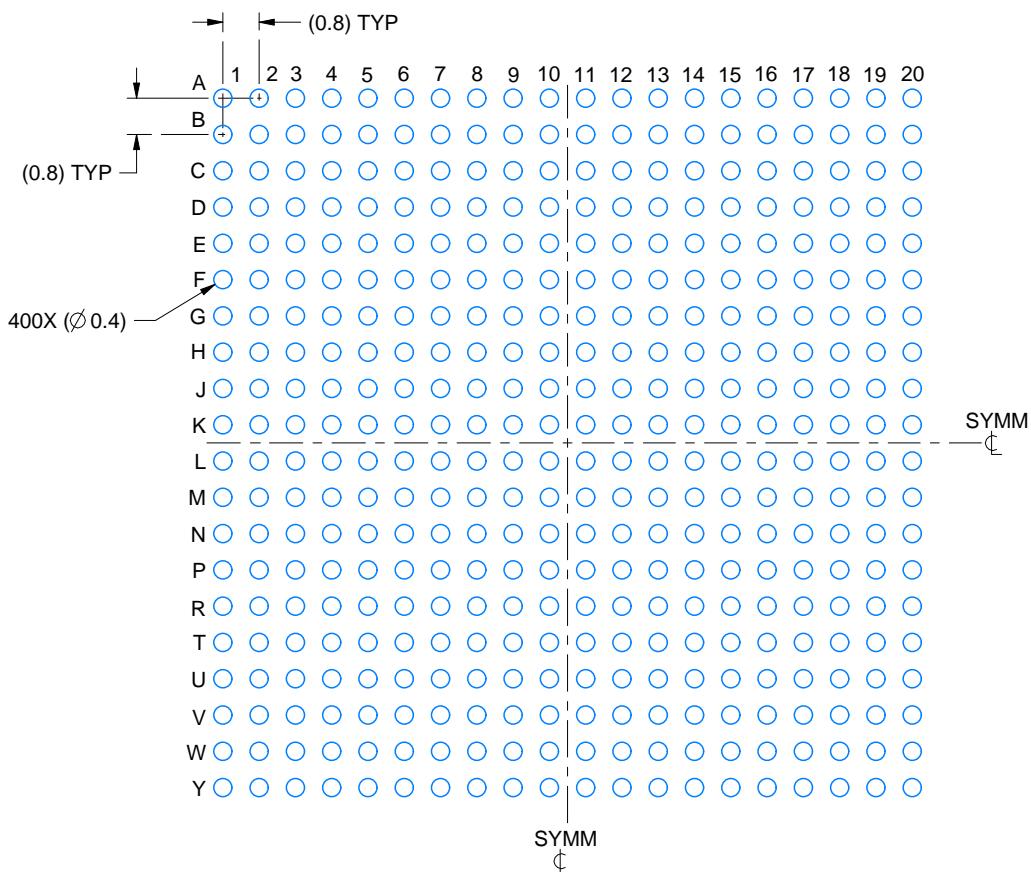
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
5. Pb-Free die bump and SnPb solder ball.
6. The lids are electrically floating (e.g. not tied to GND).

# EXAMPLE BOARD LAYOUT

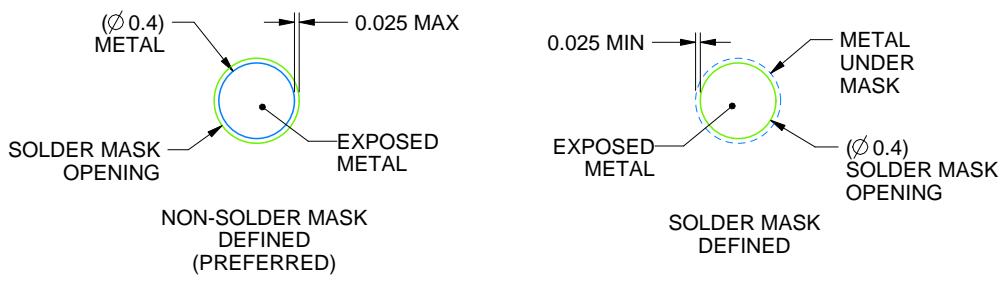
ALK0400A

FCBGA - 2.65 mm max height

BALL GRID ARRAY



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:6X



SOLDER MASK DETAILS  
NOT TO SCALE

4225930/C 03/2023

NOTES: (continued)

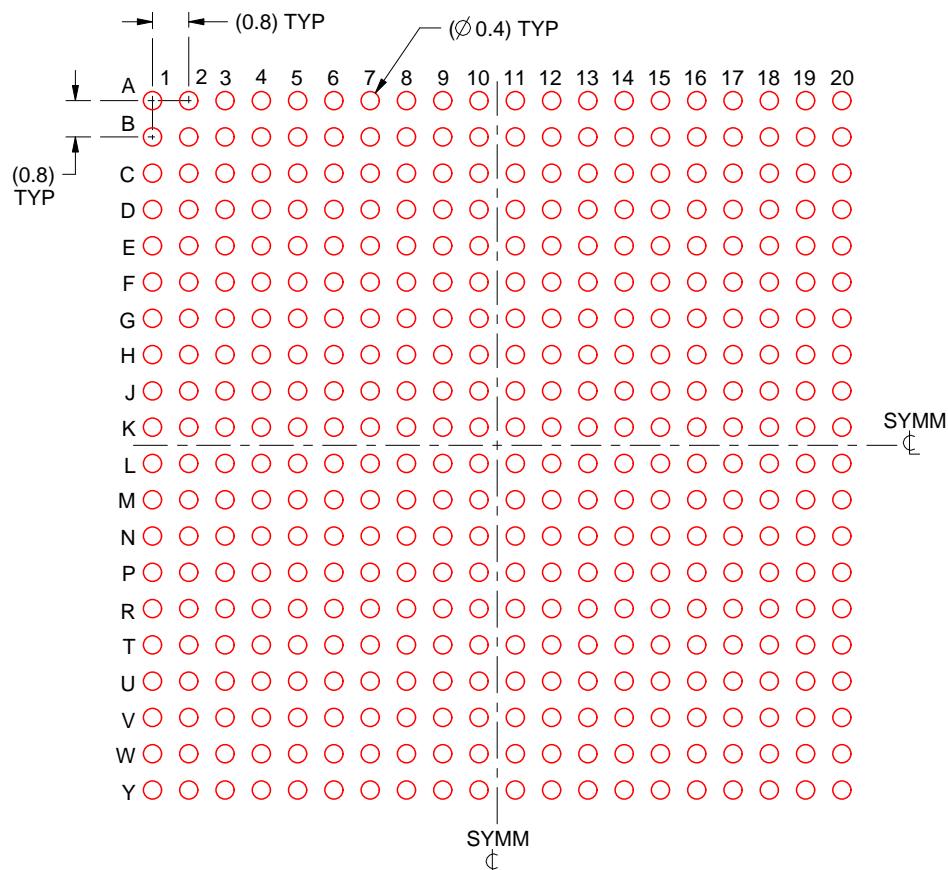
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.  
For more information, see Texas Instruments literature number SPRU811 ([www.ti.com/lit/spru811](http://www.ti.com/lit/spru811)).

# EXAMPLE STENCIL DESIGN

**ALK0400A**

**FCBGA - 2.65 mm max height**

BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.15 mm THICK STENCIL  
SCALE:6X

4225930/C 03/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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