Ajay KumarGargEngineeringCollege, Ghaziabad

Department of CSE

ST-1 Solution-OddSemester (2022-23)

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AJAY KUMAR GARG ENGINEERING COLLEGE

SESSIONAL TEST - I

SUB :- COMPUTER ORGANISATION & ARCHITECTURE CODE :- KCS-302

SECTION - A

Q.1) Define the term computer organization and computer architecture.

Ans) Computer organization ↴

It is concerned with the way the hardware components operate and the way they are connected together to form the computer system.

Analogy: Civil engineer's task during building construction (cement, bricks, iron rods & other building materials).

Computer Architecture ↴

It is concerned with the structure and behaviour of the computer as seen by the user.

Analogy: Architecht's task during the planning of a building. (overall layout, floor plan etc)

Q.2) A digital computer has a common bus system for 16 registers of 16 bits each. If the bus is constructed with multiplexers. Draw a schematic diagram and find following.

(i) How many selection inputs are there in each multiplexer?

(ii) What size of multiplexers are needed?

(iii) How many multiplexers are there in the bus?

Ans) (i) 4 selection inputs are there. ↴

(ii) Size of Multiplexers = $2^{(4)} \times 1$.

as no. of registers are = $16 = 2^4$

∴ size of each multiplexer is = 16×1 or $2^4 \times 1$

(iii) Given,

No. of bits in each register = 16.

∴ No. of multiplexers = 16

Q.3) Represent the following conditional control statements by two register transfer statements with control functions
if (P=1) then (R1 ← R2) else if (Q=1) then (R1 ← R3)

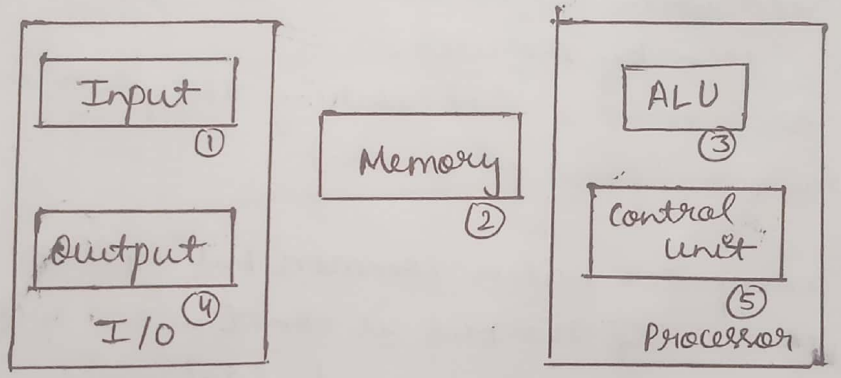
Ans)
P : R1 ← R2
P'Q : R1 ← R3

SECTION - B

Q.4) Explain the functional unit of digital computer at different levels with suitable diagram.

Ans) A computer consists of five functionally independent units.

1. Input
2. Memory unit
3. ALU
4. Output
5. Control Unit.



1. **Input unit** :- The input unit accepts coded information from human operators using devices such as keyboards. Many other kinds of input devices for human-computer interactions are available, including the mouse, joystick etc.

2. **Memory** :- The information received is stored in the computer's memory, either for later use or to be processed immediately by the arithmetic and logic unit. Memory is a medium that stores the binary information.

3. **ALU (Arithmetic and Logical unit)** :- ALU is a group of circuits that performs arithmetic (addition, increament/decreament or complement) and logic (AND, OR, NOT, XOR etc) operations.

Control Unit: The control unit controls the movement of data and instructions into and out of the processor and controls the operation of the ALU. A control unit is a group of circuits that provides timing and signals to all the operations in the computer and controls the data flow.

(5) **Output Unit:** The output unit is the counter part of the input unit. The data that is processed by the CPU is displayed to the user via output unit such as speaker, monitor etc.

Q.5) Evaluate the arithmetic statement using stack organized computer with zero-address instruction:

$$X = (A - B + C \cdot (D \cdot E - F)) / (G + H \cdot K)$$

Ans)
$$X = (A - B + C \cdot (D \cdot E - F)) / (G + H \cdot K)$$
$$= (AB - + C \cdot (DE \cdot F -)) / (GHK \cdot +)$$
$$= (AB - + C \cdot DE \cdot F - *) / (GHK \cdot +)$$
$$= (AB - CDE \cdot F - \cdot +) / (GHK \cdot +)$$
$$X = AB - CDE \cdot F - \cdot + GHK \cdot + /$$

Operation	Operand	
PUSH	A	TOS ← A
PUSH	B	TOS ← B
SUB		TOS ← (A - B)
PUSH	C	TOS ← C
PUSH	D	TOS ← D
PUSH	E	TOS ← E
MUL		TOS ← (D · E)
PUSH	F	TOS ← F
SUB		TOS ← (D · E - F)
MUL		TOS ← (C · (D · E - F))
ADD		TOS ← (A - B + C · (D · E - F))
PUSH	G	
PUSH	H	
PUSH	K	

Operation	Operand	
MUL		$TOS \leftarrow (H \cdot K)$
ADD		$TOS \leftarrow (G + H \cdot K)$
DIV		$TOS \leftarrow \frac{(A - B + C \cdot (D \cdot E - F))}{(G + H \cdot K)}$
POP	X	$X = \frac{(A - B + C \cdot (D \cdot E - F))}{(G + H \cdot K)}$

Q.6) What is the bus arbitration? Explain Distributed arbitration scheme with the help of an example.

Ans) * Bus Arbitration is a process which decides among a number of devices requesting to use the system bus, which one to grant access.

* Bus Arbitration refers to the process by which the current bus master accesses and then leaves the control of the bus and passes it to the another bus requesting processor unit.

* It is of two types.

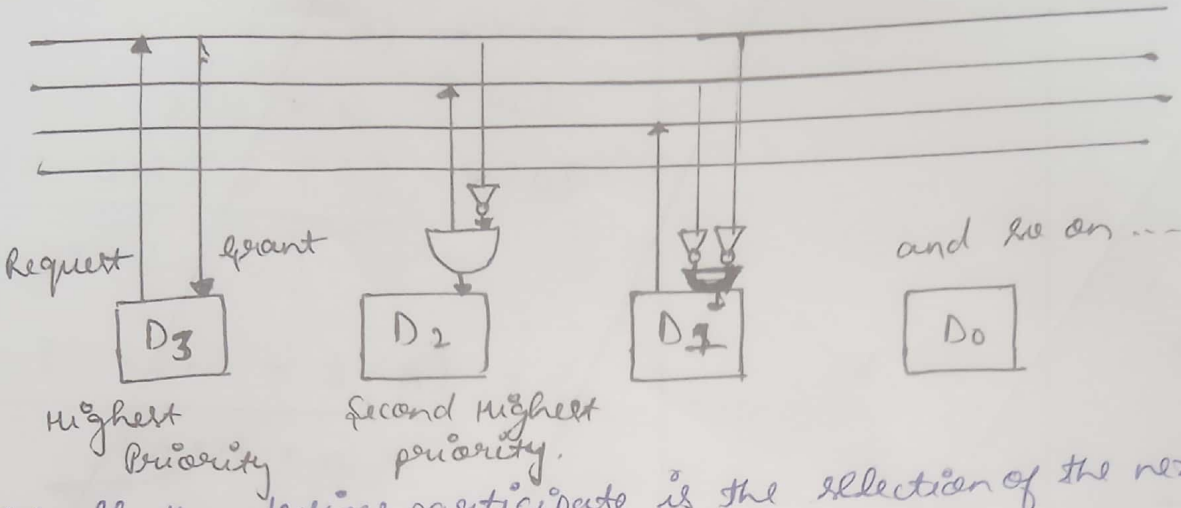
① Centralized Bus Arbitration :- In this a single bus arbiter performs the required arbitration.
It is further divided as :

a) Daisy Chaining :- In this method the device which is "physically closer" to the bus controller / arbiter will be allowed to use the bus first.

b) Polling :- The controller is used to generate the address for the devices (unique priority) requesting for bus. The controller generates a sequence of ~~master~~ device addresses. When the requesting ~~master~~ device recognized its address, it activates the busy line and begins to use the bus.

c) Independent Request Method :- In this, each device has a seperate pair of bus request and bus grant lines and each pair has a priority alligned to it.

② Distributed Arbitration :-



* Here all the devices participate is the selection of the next bus master.
* Each device on the bus is assigned a 4-bit identification number.
* When one or more devices request a control of the bus, they assert the start arbitration signal and place their 4-bit identification no.s on arbitration lines.
* Each device compares the code and changes its bit position, accordingly.
  It does so by placing a 0 at the input of their drive.

SECTION - C

Q.7> An instruction is stored at location 400 with its address field at location 401. The address field has the value 500. A processor registers R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is (a) direct (b) immediate (c) relative (d) register indirect (e) index with R1 as the ~~index~~ index Register.

R1	200
PC	402

Memory

400	Instruction
401	Adress field, 500
402	Next instruction

(a) direct mode.
In this the address field contains the operand address
∴ E.A. = ~~401~~ 500

(b) Immediate Method.

Address field contains the operand.

∴ E.A. = 401

c) Relative.

E.A. = A + (R)

= A + (R1)

= 500 + ~~402~~ 200

= 700

d) Register Indirect.

The register content points to effective address of operand.

∴ E.A. = 200

e) Index with R1 as Index

EA. = A + (Index Register)

= 500 + 200

= 700