US012419127B2

(12) **United States Patent**
Umebayashi et al.

(10) **Patent No.: US 12,419,127 B2**
(45) **Date of Patent: *Sep. 16, 2025**

(54) **SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME, AND ELECTRONIC APPARATUS**

(71) Applicant: **SONY GROUP CORPORATION**, Tokyo (JP)

(72) Inventors: **Taku Umebayashi**, Kanagawa (JP); **Hiroshi Takahashi**, Kanagawa (JP); **Reijiroh Shohji**, Nagasaki (JP)

(73) Assignee: **Sony Group Corporation**, Tokyo (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **18/615,151**

(22) Filed: **Mar. 25, 2024**

(65) **Prior Publication Data**

US 2024/0234468 A1 Jul. 11, 2024

Related U.S. Application Data

(63) Continuation of application No. 18/321,439, filed on May 22, 2023, now Pat. No. 12,166,061, which is a (Continued)

(30) **Foreign Application Priority Data**

Mar. 19, 2009 (JP) 2009-068582
Jan. 22, 2010 (JP) 2010-012586

(51) **Int. Cl.**
H01L 27/146 (2006.01)
H01L 21/768 (2006.01)
(Continued)

(52) **U.S. Cl.**
CPC ***H10F 39/809*** (2025.01); ***H01L 21/76898*** (2013.01); ***H01L 23/481*** (2013.01);
(Continued)

(58) **Field of Classification Search**
CPC H01L 27/14634; H01L 21/76898; H01L 23/481
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,667,499 B1 * 12/2003 Furumiya H10F 39/151 257/E27.152
7,531,884 B2 5/2009 Kim
(Continued)

FOREIGN PATENT DOCUMENTS

FR 2910707 6/2008
JP H05-048057 2/1993
(Continued)

OTHER PUBLICATIONS

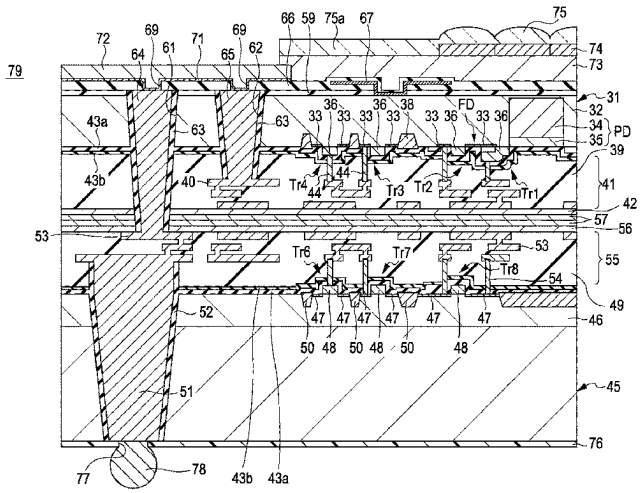
Official Action for U.S. Appl. No. 18/321,439, dated May 2, 2024, 10 pages.
(Continued)

Primary Examiner — Dale E Page
Assistant Examiner — Wilner Jean Baptiste
(74) *Attorney, Agent, or Firm* — SHERIDAN ROSS P.C.

(57) **ABSTRACT**

A semiconductor device is provided as a back-illuminated solid-state imaging device. The device is manufactured by bonding a first semiconductor wafer with a pixel array in a half-finished product state and a second semiconductor wafer with a logic circuit in a half-finished product state together, making the first semiconductor wafer into a thin film, electrically connecting the pixel array and the logic circuit, making the pixel array and the logic circuit into a finished product state, and dividing the first semiconductor wafer and the second semiconductor being bonded together into microchips.

20 Claims, 29 Drawing Sheets



Related U.S. Application Data

continuation of application No. 17/110,145, filed on Dec. 2, 2020, now Pat. No. 11,764,243, which is a continuation of application No. 16/913,075, filed on Jun. 26, 2020, now Pat. No. 10,950,647, which is a continuation of application No. 16/358,348, filed on Mar. 19, 2019, now Pat. No. 10,916,577, which is a continuation of application No. 15/814,177, filed on Nov. 15, 2017, now Pat. No. 10,403,670, which is a continuation of application No. 15/713,226, filed on Sep. 22, 2017, now Pat. No. 10,141,361, which is a continuation of application No. 15/374,864, filed on Dec. 9, 2016, now Pat. No. 9,799,695, which is a continuation of application No. 15/087,695, filed on Mar. 31, 2016, now Pat. No. 9,530,812, which is a continuation of application No. 14/834,010, filed on Aug. 24, 2015, now Pat. No. 9,319,569, which is a continuation of application No. 12/722,069, filed on Mar. 11, 2010, now Pat. No. 9,451,131.

(51) **Int. Cl.**

H01L 23/48	(2006.01)
H04N 23/00	(2023.01)
H04N 25/76	(2023.01)
H04N 25/79	(2023.01)
H10F 39/00	(2025.01)
H10F 39/12	(2025.01)
H10F 39/18	(2025.01)

(52) **U.S. Cl.**

CPC ***H04N 23/00*** (2023.01); ***H04N 25/76*** (2023.01); ***H04N 25/79*** (2023.01); ***H10F 39/018*** (2025.01); ***H10F 39/026*** (2025.01); ***H10F 39/18*** (2025.01); ***H10F 39/182*** (2025.01); ***H10F 39/199*** (2025.01); ***H10F 39/8037*** (2025.01); ***H10F 39/8053*** (2025.01); ***H10F 39/8063*** (2025.01); ***H10F 39/811*** (2025.01); *H01L 2224/11* (2013.01)

(56) **References Cited**

U.S. PATENT DOCUMENTS

7,791,012	B2	9/2010	Hirose	
8,031,249	B2	10/2011	McKee	
8,541,878	B2	9/2013	Takahashi et al.	
8,716,054	B2 *	5/2014	Jeong	H10F 39/024 438/69
8,946,798	B2	2/2015	Horiike et al.	
9,319,569	B2	4/2016	Umebayashi et al.	
9,324,753	B2	4/2016	Kato	
9,451,131	B2	9/2016	Umebayashi et al.	
9,530,812	B2	12/2016	Umebayashi et al.	
9,799,695	B2	10/2017	Umebayashi et al.	
9,936,153	B1	4/2018	Mao et al.	
10,141,361	B2 *	11/2018	Umebayashi	H04N 25/76
10,403,670	B2	9/2019	Umebayashi et al.	
10,916,577	B2	2/2021	Umebayashi et al.	
10,950,647	B2	3/2021	Umebayashi et al.	
11,764,243	B2	9/2023	Umebayashi et al.	
2001/0005153	A1	6/2001	Ueda et al.	
2002/0020862	A1	2/2002	Livengood et al.	
2002/0025623	A1	2/2002	Yamamichi et al.	
2002/0084513	A1	7/2002	Siniaguine	
2002/0089595	A1	7/2002	Orava et al.	
2003/0049925	A1	3/2003	Layman et al.	
2003/0162386	A1	8/2003	Ogawa et al.	
2004/0087109	A1	5/2004	McCann et al.	
2005/0127535	A1	6/2005	Takahashi et al.	
2005/0227403	A1	10/2005	Muramatsu	
2006/0091290	A1	5/2006	Yoshihara et al.	
2006/0146233	A1	7/2006	Park	
2006/0197007	A1	9/2006	Iwabuchi et al.	
2006/0286767	A1	12/2006	Clarke et al.	
2007/0128828	A1	6/2007	Chen et al.	
2007/0170574	A1	7/2007	Lauxtermann et al.	
2007/0194397	A1	8/2007	Adkisson et al.	
2007/0215971	A1	9/2007	Yamamoto et al.	
2008/0083939	A1	4/2008	Guidash	
2008/0093708	A1	4/2008	Noma et al.	
2008/0157148	A1	7/2008	Han	
2008/0217713	A1	9/2008	Tokuda et al.	
2009/0185060	A1	7/2009	Akiyama	
2009/0190016	A1	7/2009	Iida	
2009/0275165	A1	11/2009	Pourquier	
2009/0294814	A1	12/2009	Assefa et al.	
2010/0176271	A1	7/2010	Rim et al.	
2011/0024858	A1	2/2011	Yoshihara et al.	
2011/0168434	A1	7/2011	Farooq et al.	
2019/0273879	A1	9/2019	Xu	
2023/0290800	A1	9/2023	Umebayashi et al.	

FOREIGN PATENT DOCUMENTS

JP	H09-191097	7/1997
JP	2001-168046	6/2001
JP	2001-189423	7/2001
JP	2001-511608	8/2001
JP	2001-339057	12/2001
JP	2003-031785	1/2003
JP	2003-264280	9/2003
JP	2003-338615	11/2003
JP	2005-044861	2/2005
JP	2005-079353	3/2005
JP	2005-285988	10/2005
JP	2005-322745	11/2005
JP	2005-347707	12/2005
JP	2006-032497	2/2006
JP	2006-049361	2/2006
JP	2006-191081	7/2006
JP	2006-261510	9/2006
JP	2006-261638	9/2006
JP	2006-270292	10/2006
JP	2007-013089	1/2007
JP	2007-042933	2/2007
JP	2007-088450	4/2007
JP	2007-115994	5/2007
JP	2007-234725	9/2007
JP	2007-250561	9/2007
JP	4000507	10/2007
JP	2007-311385	11/2007
JP	2008-053430	3/2008
JP	2008-130603	6/2008
JP	2008-140819	6/2008
JP	2008-227253	9/2008
JP	2008-536330	9/2008
JP	2008-235478	10/2008
JP	2008-300614	12/2008
JP	2008-306154	12/2008
JP	2008-544571	12/2008
JP	2009-021568	1/2009
JP	2009-505401	2/2009
JP	2009-541990	11/2009
JP	2010-506404	2/2010
JP	2010-514177	4/2010
JP	2010-530633	9/2010
JP	2017-161412	8/2017
JP	2018-011068	1/2018
JP	2019-233337	1/2020
KR	10-2006-0096924	9/2006
KR	10-2006-0108378	10/2006
KR	10-2007-0120255	12/2007
KR	10-2007-0120456	12/2007
KR	100801447	2/2008
WO	WO 99/49509	9/1999
WO	WO 03/041174	5/2003
WO	WO 2006/109937	10/2006
WO	WO 2007/127825	11/2007
WO	WO 2007/148891	12/2007
WO	WO 2008/045356	4/2008

(56) **References Cited**

FOREIGN PATENT DOCUMENTS

WO	WO 2008/074688	6/2008
WO	WO 2008/146211	12/2008
WO	WO 2008/156274	12/2008

OTHER PUBLICATIONS

Notice of Allowance for U.S. Appl. No. 18/321,439, dated Aug. 14, 2024, 9 pages.
European Search Report for European Patent Application No. 10156350.0 dated Jul. 29, 2013, 4 pages.
Extended European Search Report for European Patent Application No. 16167541.8 dated Dec. 19, 2016, 11 pages.
Official Action (with English translation) for Chinese Patent Application No. 201310092864.6 dated Feb. 17, 2015, 11 pages.
Official Action (with English translation) for Chinese Patent Application No. 201310092864.6 dated Oct. 13, 2015, 20 pages.
Official Action (no English translation available) for Japanese Patent Application No. 2010-012586 mailed Sep. 30, 2014, 3 pages.
Official Action (with English translation) for Japanese Patent Application No. 2010-012586 dated Feb. 25, 2015, 7 pages.
Official Action (no English translation available) for Japanese Patent Application No. 2010-012586 mailed Feb. 2, 2016, 8 pages.
Official Action (no English translation available) for Japanese Patent Application No. 2014-260268 mailed Apr. 14, 2015, 8 pages.
Official Action (with English translation) for Japanese Patent Application No. 2014-260268 mailed Jun. 2, 2015, 10 pages.
Official Action (no English translation available) for Japanese Patent Application No. 2015-101103 mailed Sep. 29, 2015, 7 pages.
Official Action (no English translation available) for Japanese Patent Application No. 2015-101103 mailed Feb. 23, 2016, 2 pages.
Official Action (no English translation available) for Japanese Patent Application No. 2016-101517 mailed Apr. 4, 2017, 5 pages.
Official Action (with English translation) for Japanese Patent Application No. 2017-161412, dated Jun. 5, 2018, 8 pages.
Official Action (with English translation) for Korean Patent Application No. 10-2010-0019306 mailed Mar. 15, 2016, 21 pages.
Official Action (with English translation) for Korean Patent Application No. 10-2017-0023487 mailed May 8, 2017, 9 pages.
Official Action (with English translation) for Korean Patent Application No. 10-2018-0003807, dated Apr. 16, 2018, 11 pages.
Decision to Refuse European Patent Application No. 10156350.0, dated Nov. 29, 2018, 26 pages.
Summons to Attend Oral Proceedings for European Patent Application No. 16167541.8, dated Dec. 12, 2018, 11 pages.
Official Action (with English translation) for Japanese Patent Application No. 2017-161412, dated Feb. 5, 2019, 10 pages.
Official Action (with English translation) for Korean Patent Application No. 10-2019-0007329, dated Mar. 23, 2019, 11 pages.
Official Action (no English translation available) for Japanese Patent Application No. 2017-161412, dated Sep. 24, 2019, 5 pages.
Official Action (no English translation available) for Japanese Patent Application No. 2017-161412, dated Sep. 24, 2019, 2 pages.
Extended European Search Report for European Patent Application No. 19192125.3, dated Dec. 12, 2019, 11 pages.
Official Action (with English translation) for Korean Patent Application No. 10-2019-0158069, dated Feb. 25, 2020, 9 pages.
Official Action (no English translation available) for Japanese Patent Application No. 2017-161412, dated Mar. 17, 2020, 1 page.
Official Action for European Patent Application No. 19192125.3, dated Sep. 18, 2020, 8 pages.
Official Action (no English translation available) for Japan Patent Application No. 2019-233337, dated Jan. 26, 2021, 9 pages.
Official Action (no English translation available) for Japan Patent Application No. 2019-233338, dated Jan. 26, 2021, 7 pages.
Official Action (with English translation) for Korea Patent Application No. 10-2020-0143062, dated Feb. 21, 2021, 11 pages.
Official Action (English translation) for Korea Patent Application No. 10-2021-0186159, dated May 10, 2023, 7 pages.
Official Action (with English translation) for Japan Patent Application No. 2021-198680, dated Jul. 25, 2023, 6 pages.
Official Action for U.S. Appl. No. 12/722,069, dated Feb. 2, 2012, 6 pages. Restriction Requirement.
Official Action for U.S. Appl. No. 12/722,069, dated Mar. 20, 2012, 11 pages.
Official Action for U.S. Appl. No. 12/722,069, dated Oct. 24, 2012, 10 pages.
Official Action for U.S. Appl. No. 12/722,069, dated Jun. 18, 2013, 12 pages.
Official Action for U.S. Appl. No. 12/722,069, dated Jan. 8, 2014, 12 pages.
Official Action for U.S. Appl. No. 12/722,069, dated May 8, 2014, 12 pages.
Official Action for U.S. Appl. No. 12/722,069, dated Nov. 5, 2014, 12 pages.
Official Action for U.S. Appl. No. 12/722,069, dated Aug. 6, 2015, 11 pages.
Official Action for U.S. Appl. No. 12/722,069, dated Feb. 11, 2016, 13 pages.
Notice of Allowance for U.S. Appl. No. 12/722,069, dated May 24, 2016, 11 pages.
Official Action for U.S. Appl. No. 14/834,010, dated Oct. 29, 2015, 14 pages.
Notice of Allowance for U.S. Appl. No. 14/834,010, dated Feb. 29, 2016, 10 pages.
Official Action for U.S. Appl. No. 15/087,695, dated Jul. 14, 2016, 17 pages.
Notice of Allowance for U.S. Appl. No. 15/087,695, dated Aug. 16, 2016, 11 pages.
Official Action for U.S. Appl. No. 15/374,864, dated Jan. 27, 2017, 6 pages. Restriction Requirement.
Official Action for U.S. Appl. No. 15/374,864, dated Jun. 6, 2017, 13 pages.
Notice of Allowance for U.S. Appl. No. 15/374,864, dated Aug. 16, 2017, 11 pages.
Official Action for U.S. Appl. No. 15/713,226, dated Feb. 28, 2018, 13 pages.
Notice of Allowance for U.S. Appl. No. 15/713,226, dated Jul. 18, 2018, 10 pages.
Corrected Notice of Allowance for U.S. Appl. No. 15/713,226, dated Aug. 16, 2018, 3 pages.
Official Action for U.S. Appl. No. 15/814,177, dated Dec. 18, 2018, 13 pages.
Notice of Allowance for U.S. Appl. No. 15/814,177, dated Apr. 16, 2019, 8 pages.
Official Action for U.S. Appl. No. 16/358,348, dated Apr. 3, 2020, 15 pages.
Notice of Allowance for U.S. Appl. No. 16/358,348, dated Sep. 4, 2020, 9 pages.
Corrected Notice of Allowance for U.S. Appl. No. 16/358,348, dated Jan. 1, 2021, 2 pages.
Official Action for U.S. Appl. No. 16/913,075, dated Sep. 3, 2020, 10 pages.
Notice of Allowance for U.S. Appl. No. 16/913,075, dated Nov. 13, 2020, 10 pages.
Notice of Allowance for U.S. Appl. No. 16/913,075, dated Feb. 8, 2021, 9 pages.
Official Action for U.S. Appl. No. 17/110,145, dated Oct. 17, 2022, 11 pages.
Notice of Allowance for U.S. Appl. No. 17/110,145, dated Feb. 23, 2023, 9 pages.
Corrected Notice of Allowance for U.S. Appl. No. 17/110,145, dated Jun. 7, 2023, 2 pages.
Corrected Notice of Allowance for U.S. Appl. No. 17/110,145, dated Aug. 16, 2023, 2 pages.

* cited by examiner

FIG. 1

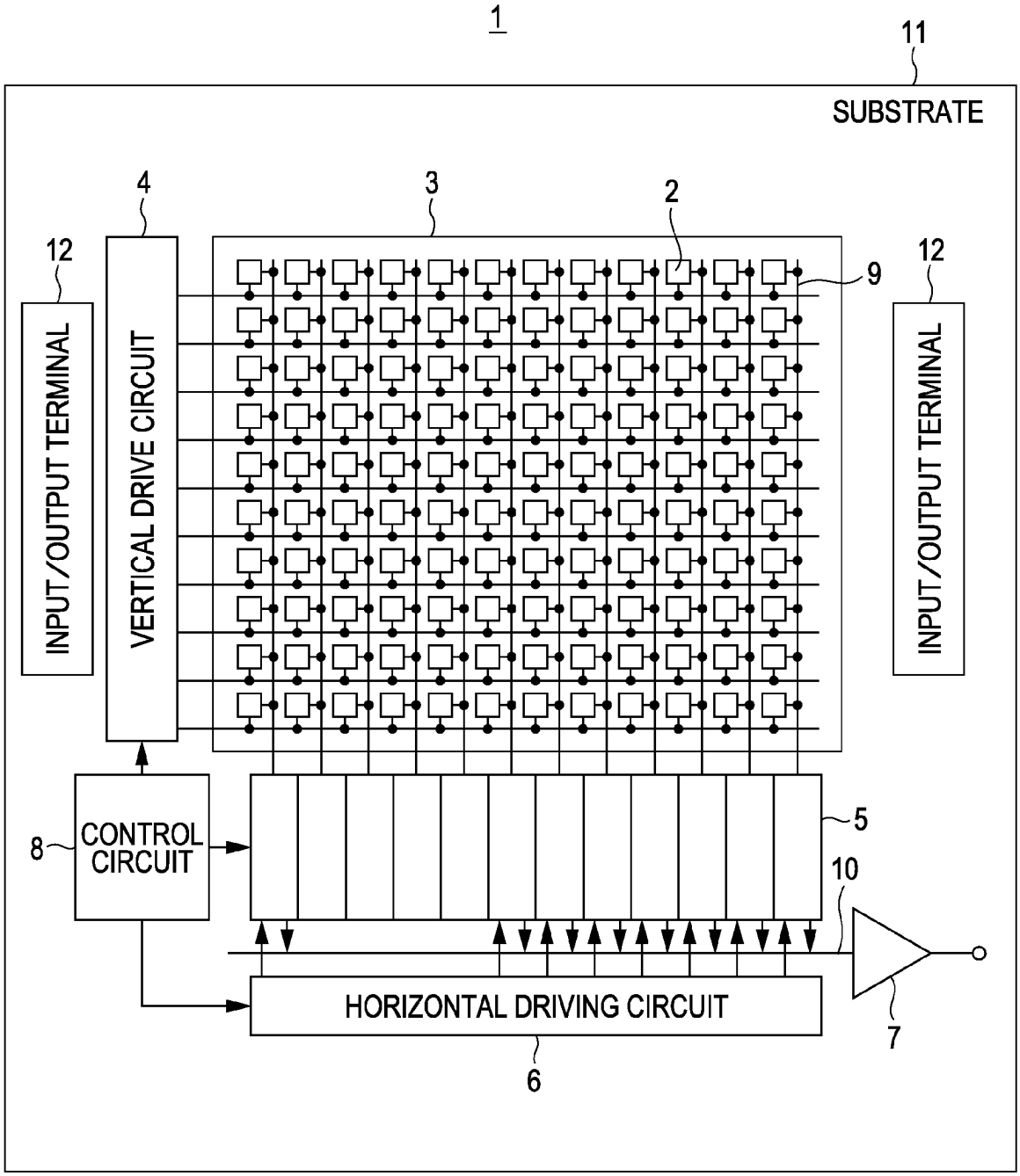

1
11
SUBSTRATE
4
3
2
12
9
12
INPUT/OUTPUT TERMINAL
VERTICAL DRIVE CIRCUIT
INPUT/OUTPUT TERMINAL
8
CONTROL CIRCUIT
5
10
HORIZONTAL DRIVING CIRCUIT
7
6

FIG. 2A

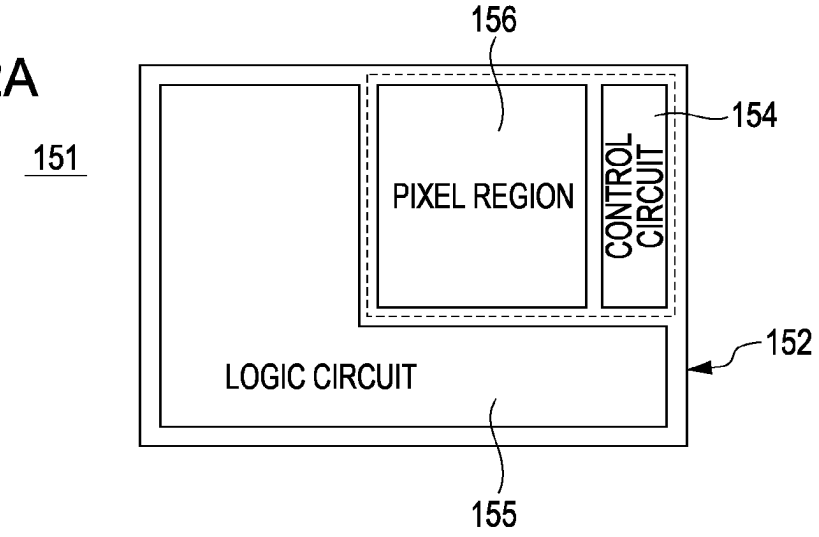


FIG. 2B

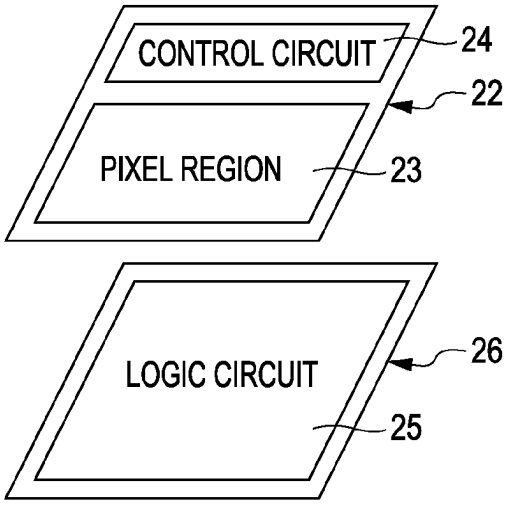
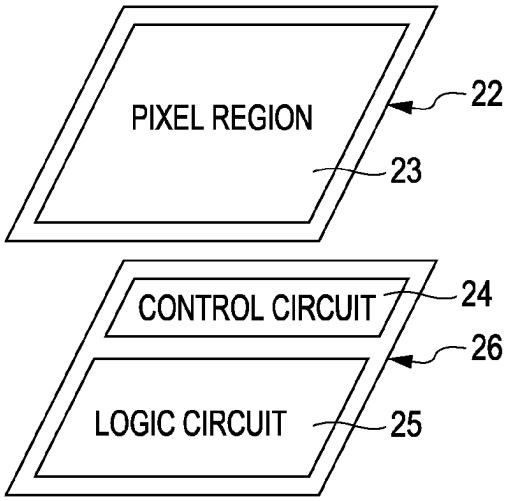


FIG. 2C



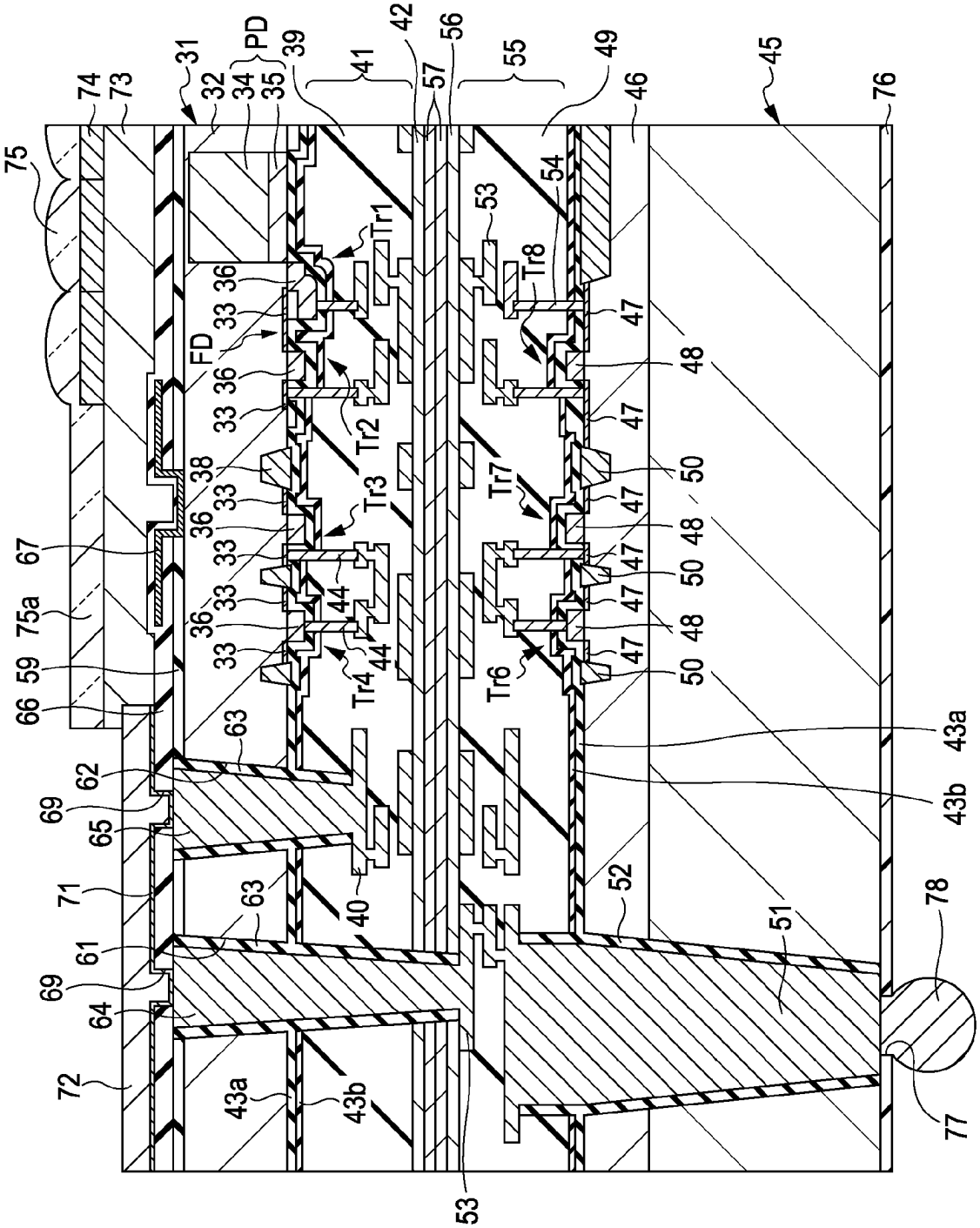

74
73
75
31
32
34
PD
35
39
41
42
56
57
55
49
46
45
76
54
53
Tr1
Tr8
36
33
FD
Tr2
38
Tr3
Tr7
67
75a
59
66
44
Tr4
Tr6
47
48
50
43a
43b
63
62
69
65
71
40
61
64
72
52
51
78
77
79

FIG. 3

FIG. 4

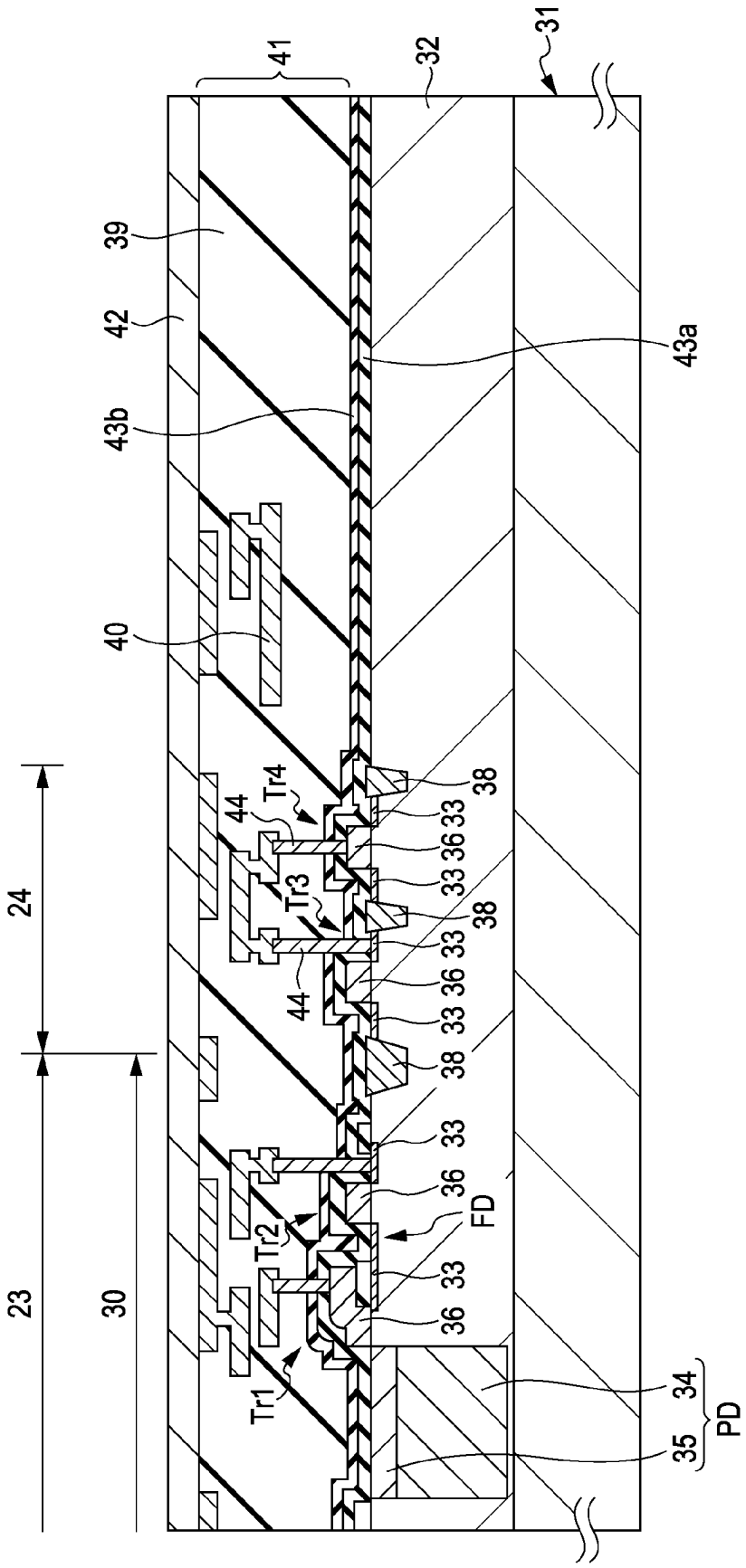

31
32
41
39
42
43a
43b
40
38
33
36
Tr4
44
Tr3
Tr2
Tr1
FD
34
35
PD
24
23
30

FIG. 5

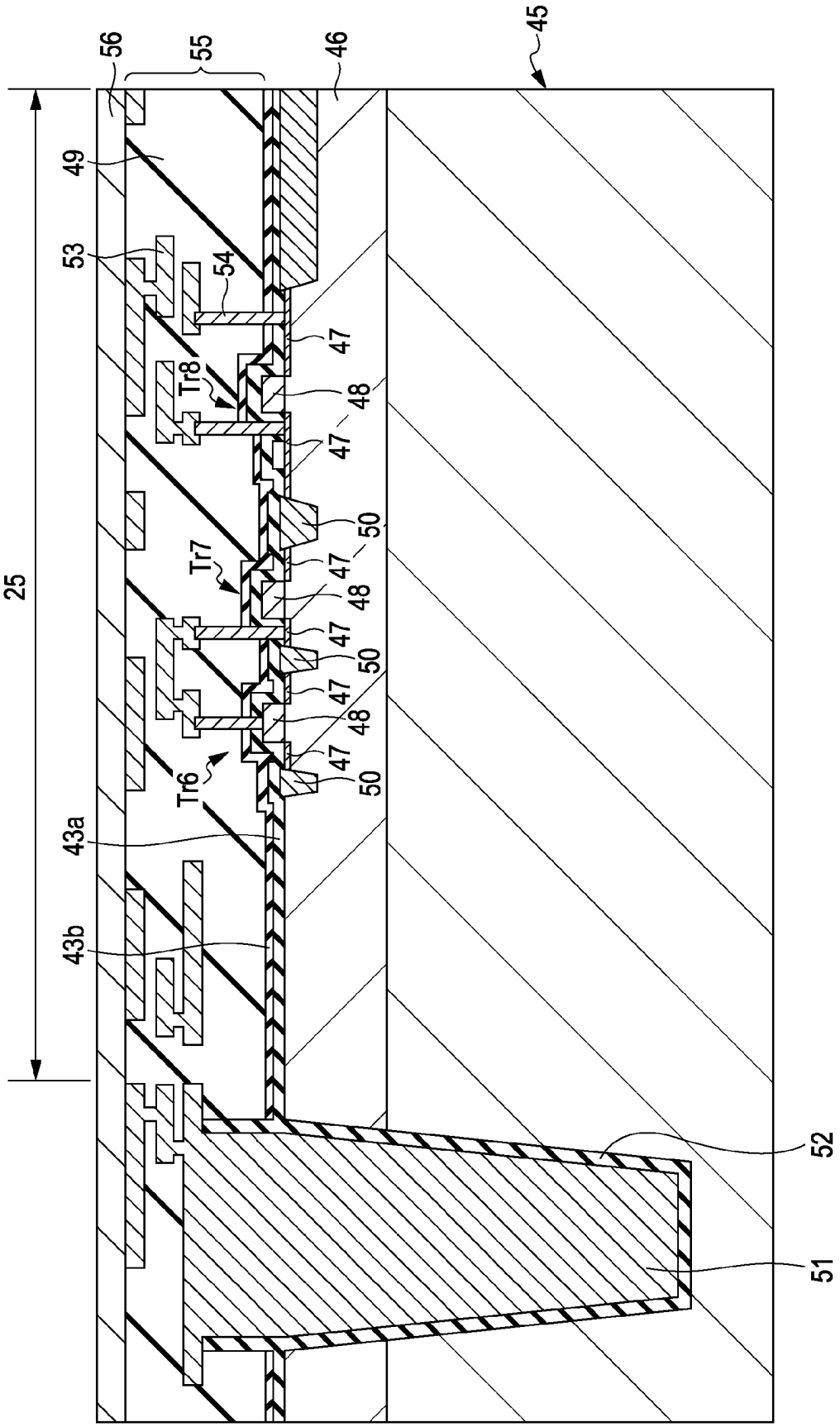


FIG. 6

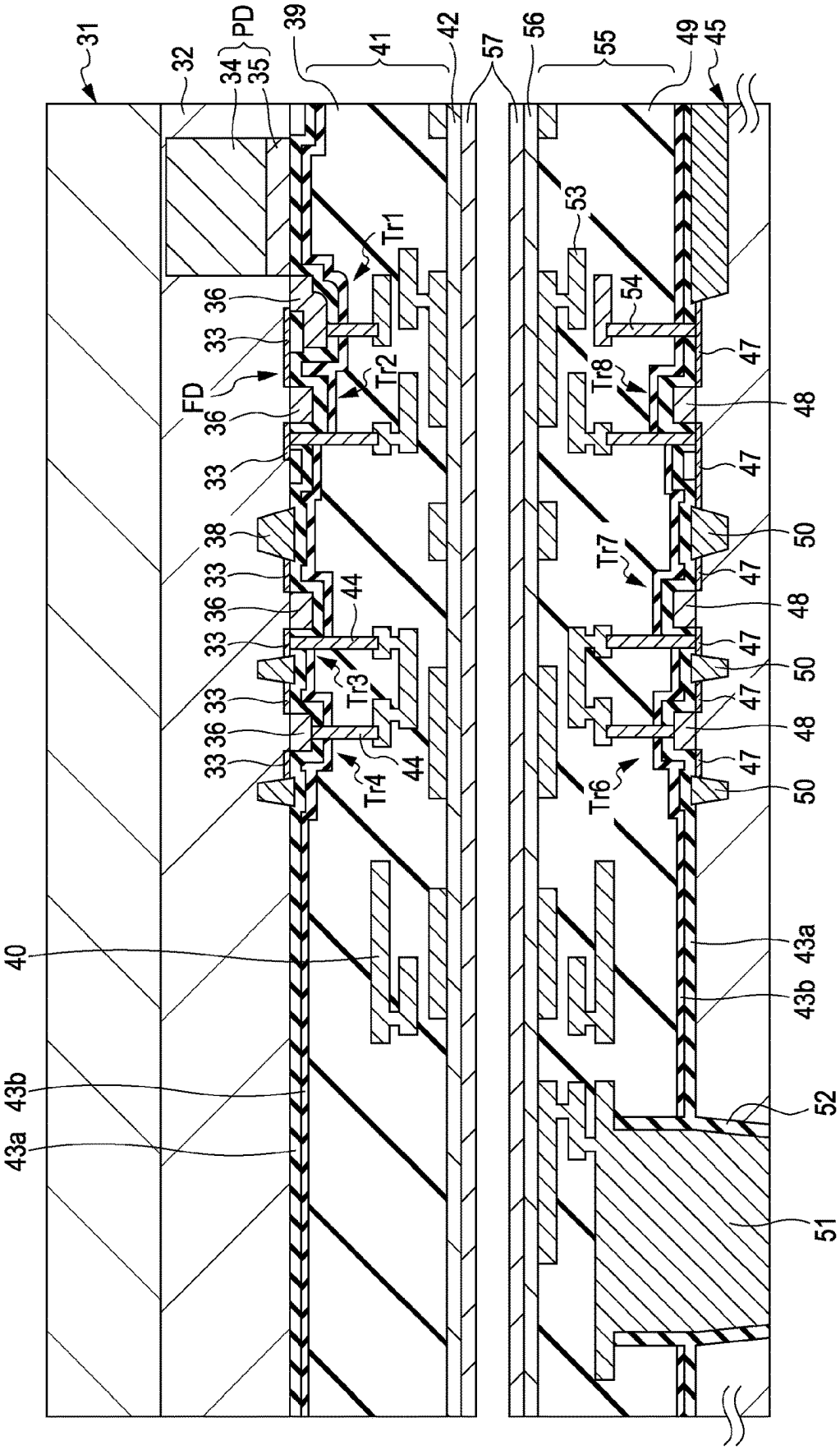

31
32
34
35
PD
39
41
42
57
56
55
49
45
53
54
Tr1
Tr2
Tr3
Tr4
Tr6
Tr7
Tr8
36
33
FD
38
44
47
48
50
40
43a
43b
52
51

FIG. 7

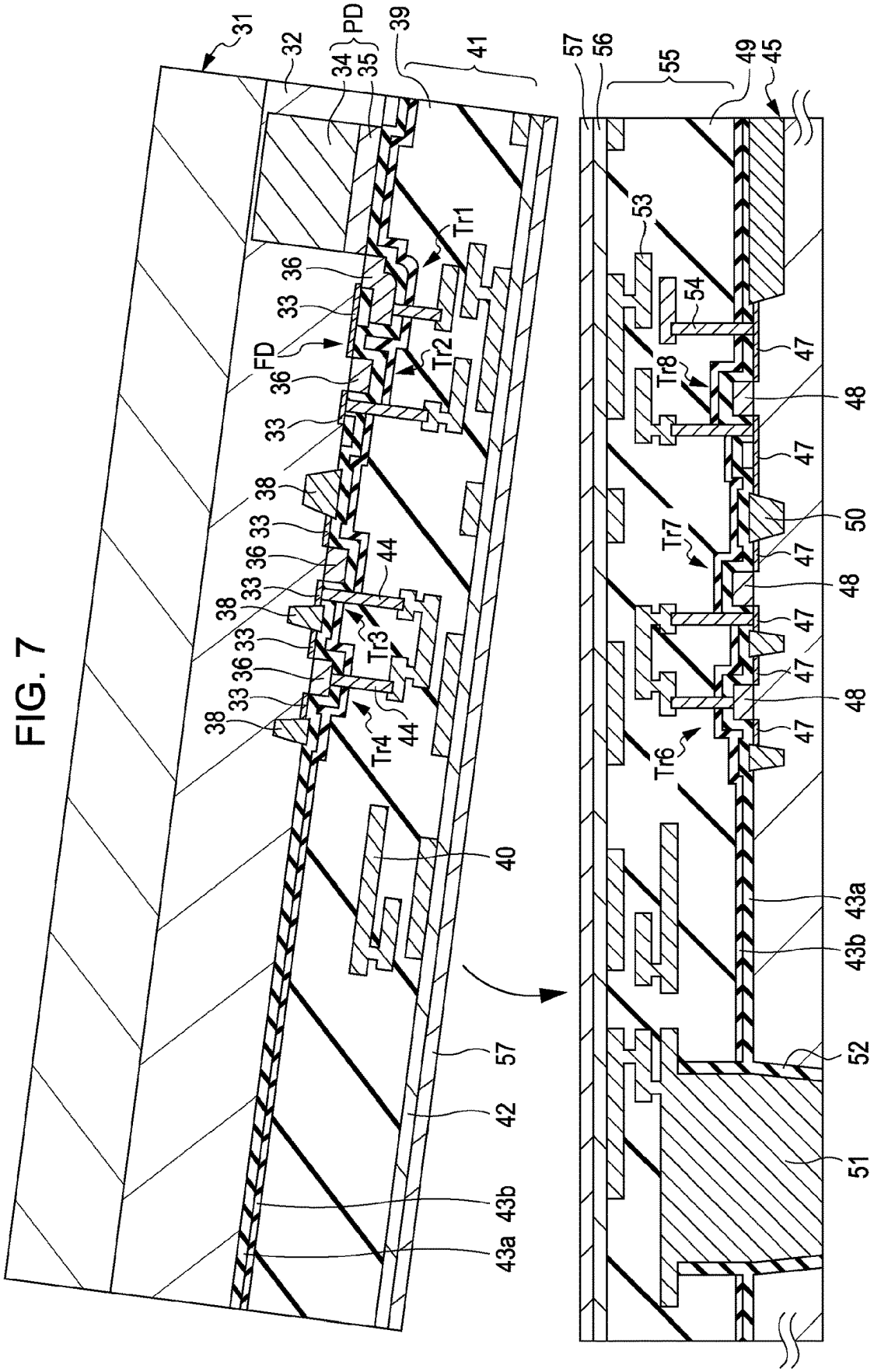

31
32
34
35
PD
39
41
57
56
55
49
45
53
54
Tr1
Tr2
Tr3
Tr4
Tr6
Tr7
Tr8
36
33
FD
38
44
40
47
48
50
43a
43b
52
51
42

FIG. 8

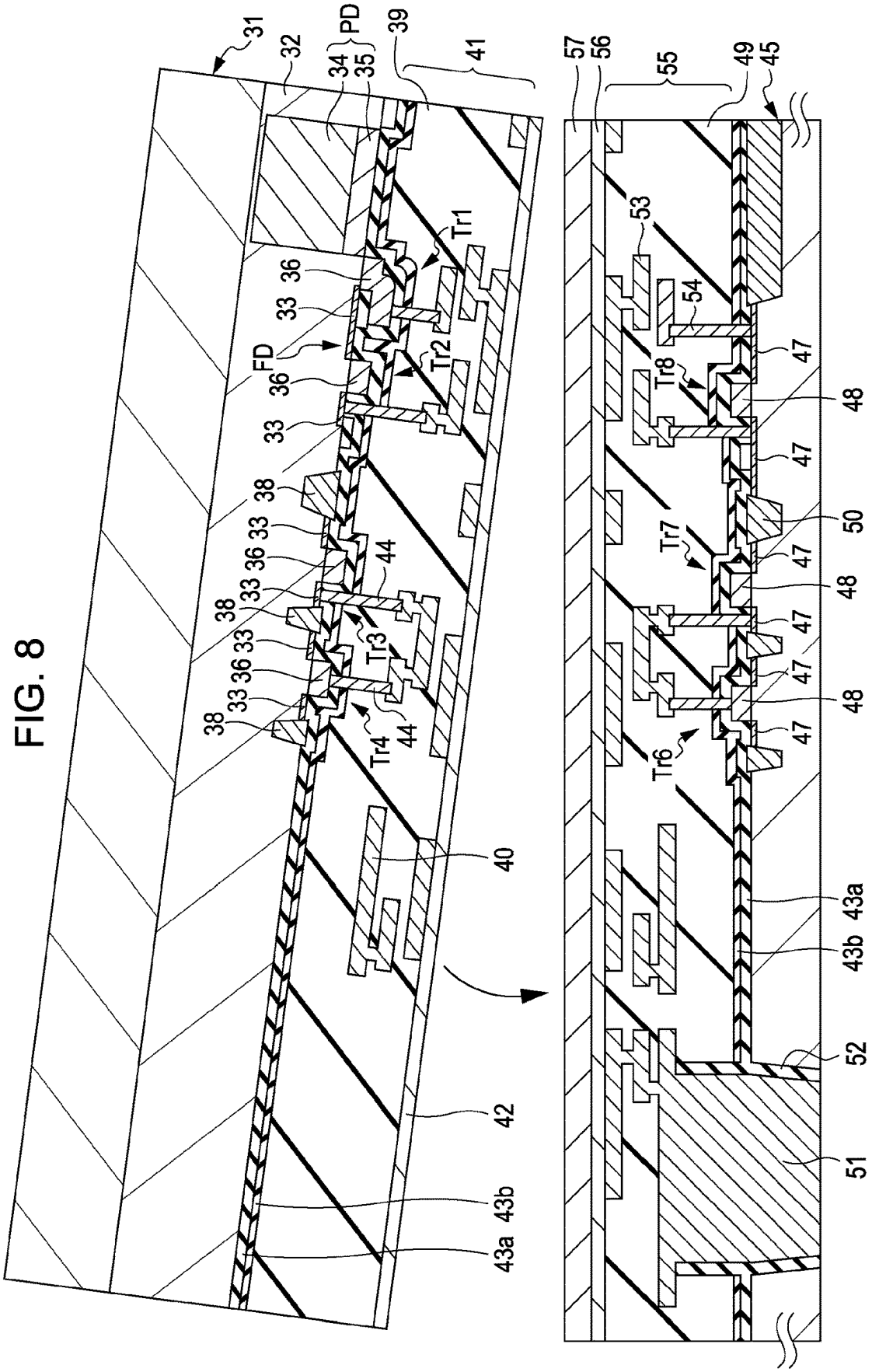

31
32
34
35
PD
39
41
57
56
55
49
45
Tr1
36
33
FD
Tr2
38
44
Tr3
Tr4
40
42
43b
43a
53
54
Tr8
47
48
50
Tr7
Tr6
52
51

FIG. 9

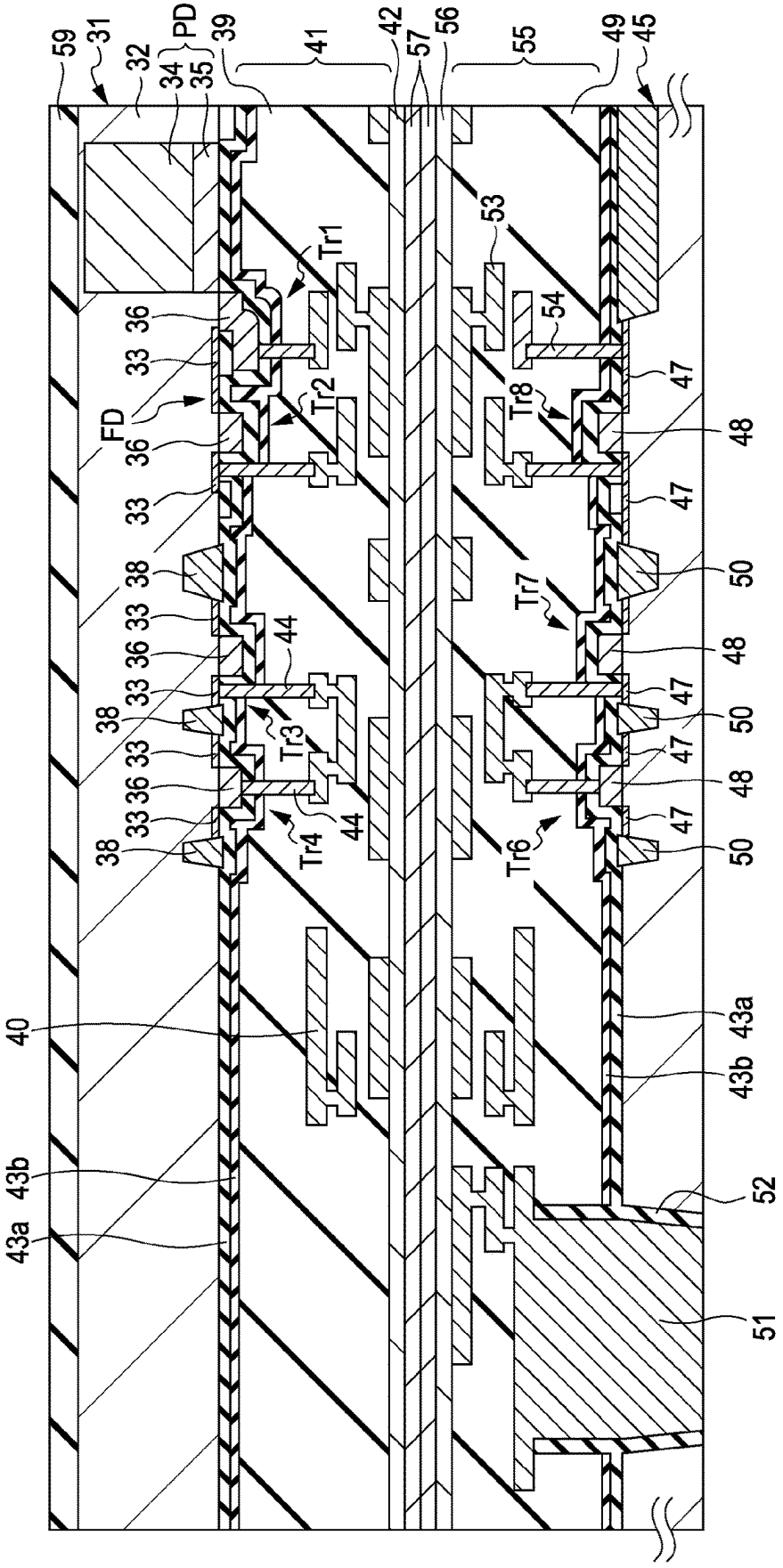

59
31
32
34
PD
35
39
41
42
57
56
55
49
45
53
Tr1
54
36
33
FD
Tr2
Tr8
48
47
38
Tr7
50
44
Tr3
Tr4
Tr6
40
43a
43b
52
51

FIG. 10

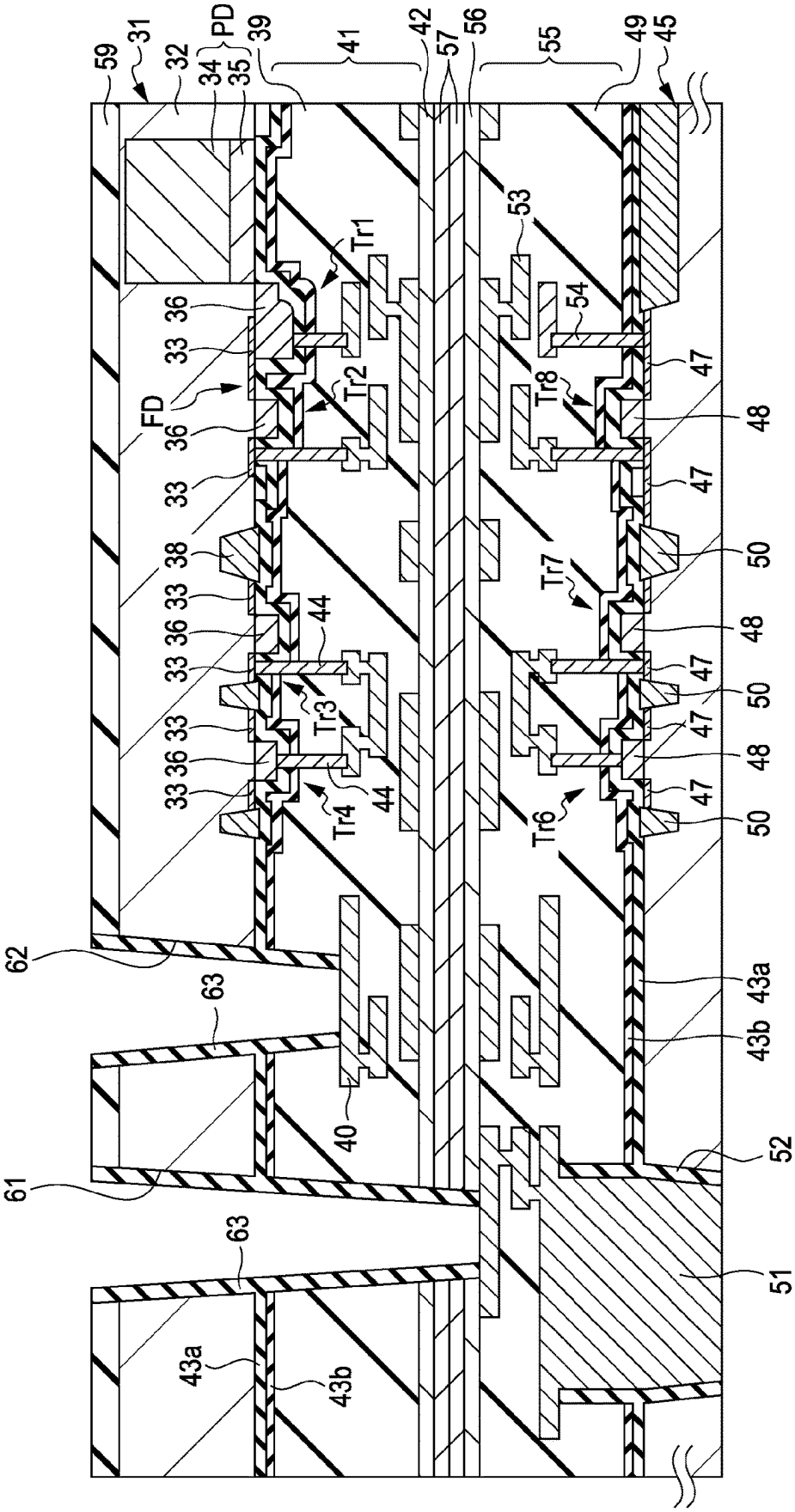

59
31
32
34
PD
35
39
41
42
57
56
55
49
45
53
Tr1
54
36
33
FD
Tr2
Tr8
47
48
38
Tr7
50
44
Tr3
Tr4
Tr6
62
63
43a
43b
40
61
52
51

FIG. 11

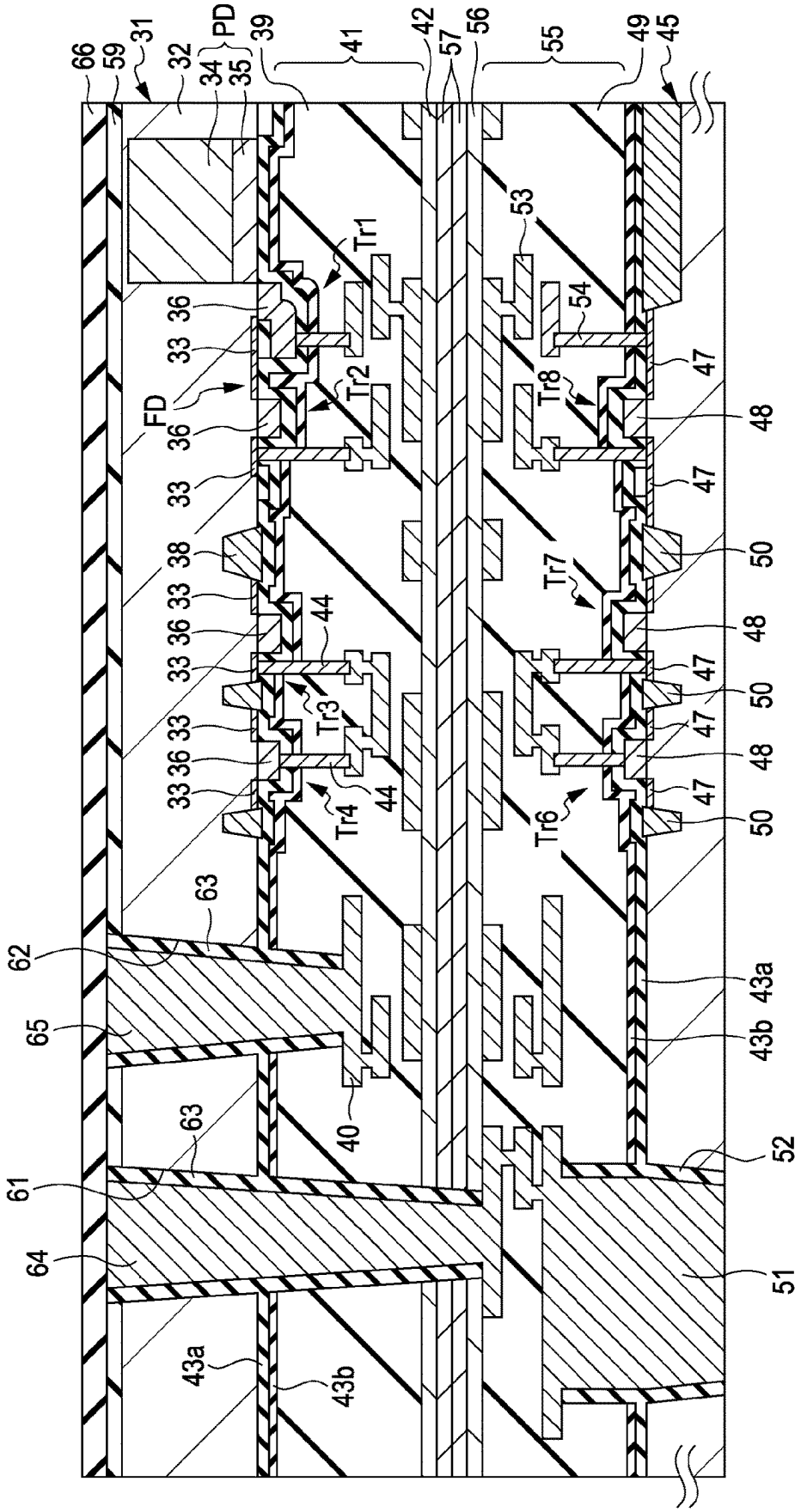

66
59
31
32
34
35
PD
39
41
42
57
56
55
49
45
53
54
Tr1
Tr2
Tr3
Tr4
Tr6
Tr7
Tr8
FD
36
33
38
44
47
48
50
62
63
65
61
64
40
43a
43b
52
51

FIG. 12

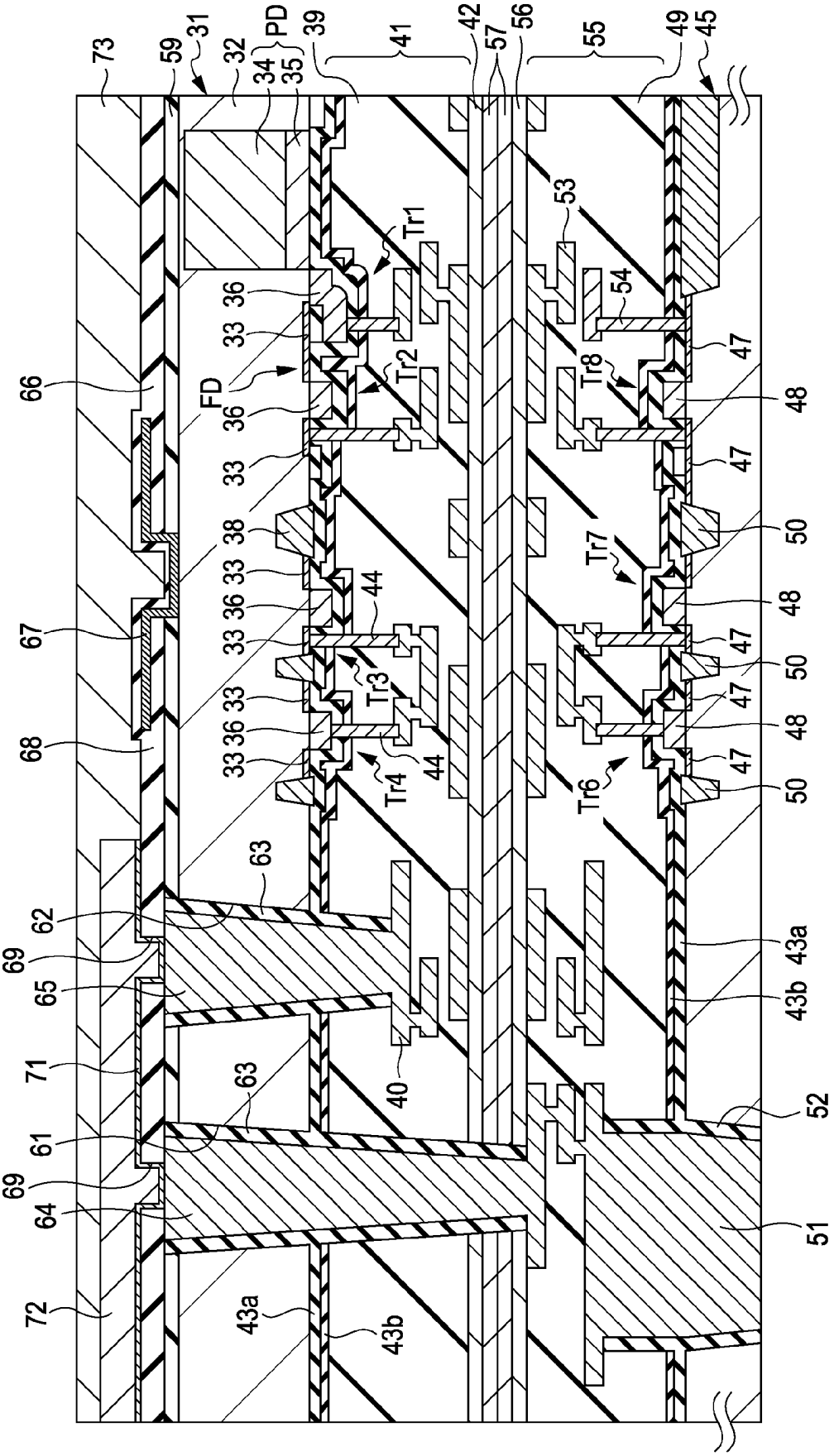
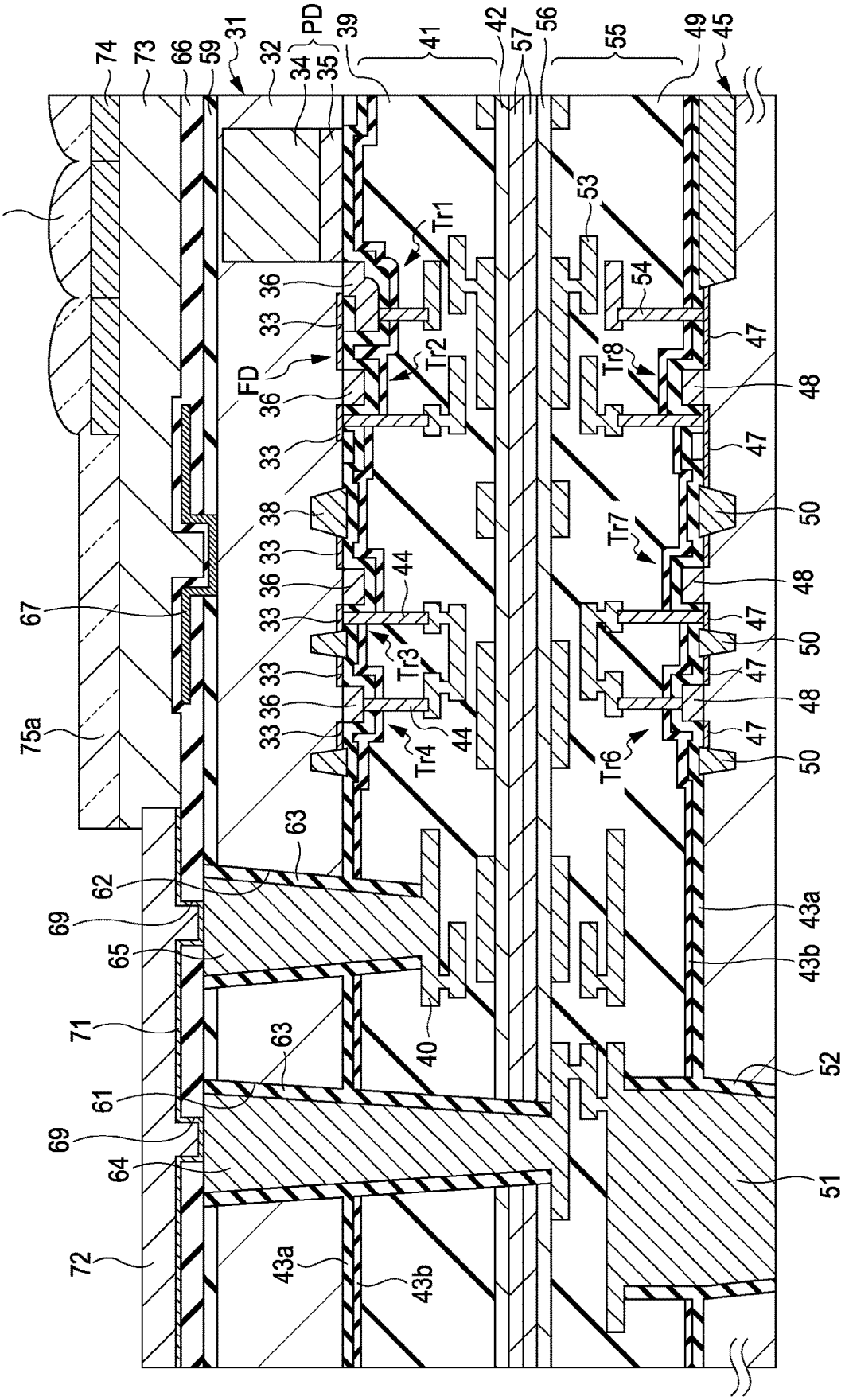

73
59
31
32
34
35
PD
39
41
42
57
56
55
49
45
53
54
Tr1
Tr2
Tr3
Tr4
Tr6
Tr7
Tr8
36
33
FD
38
44
47
48
50
66
67
68
62
63
69
65
71
61
64
72
40
43a
43b
52
51

FIG. 13


74
73
66
59
31
32
34
PD
35
39
41
42
57
56
55
49
45
75
53
Tr1
36
33
54
47
FD
Tr2
Tr8
48
38
Tr7
50
44
67
Tr3
75a
Tr4
Tr6
63
62
69
65
71
40
61
64
72
43a
43b
52
51

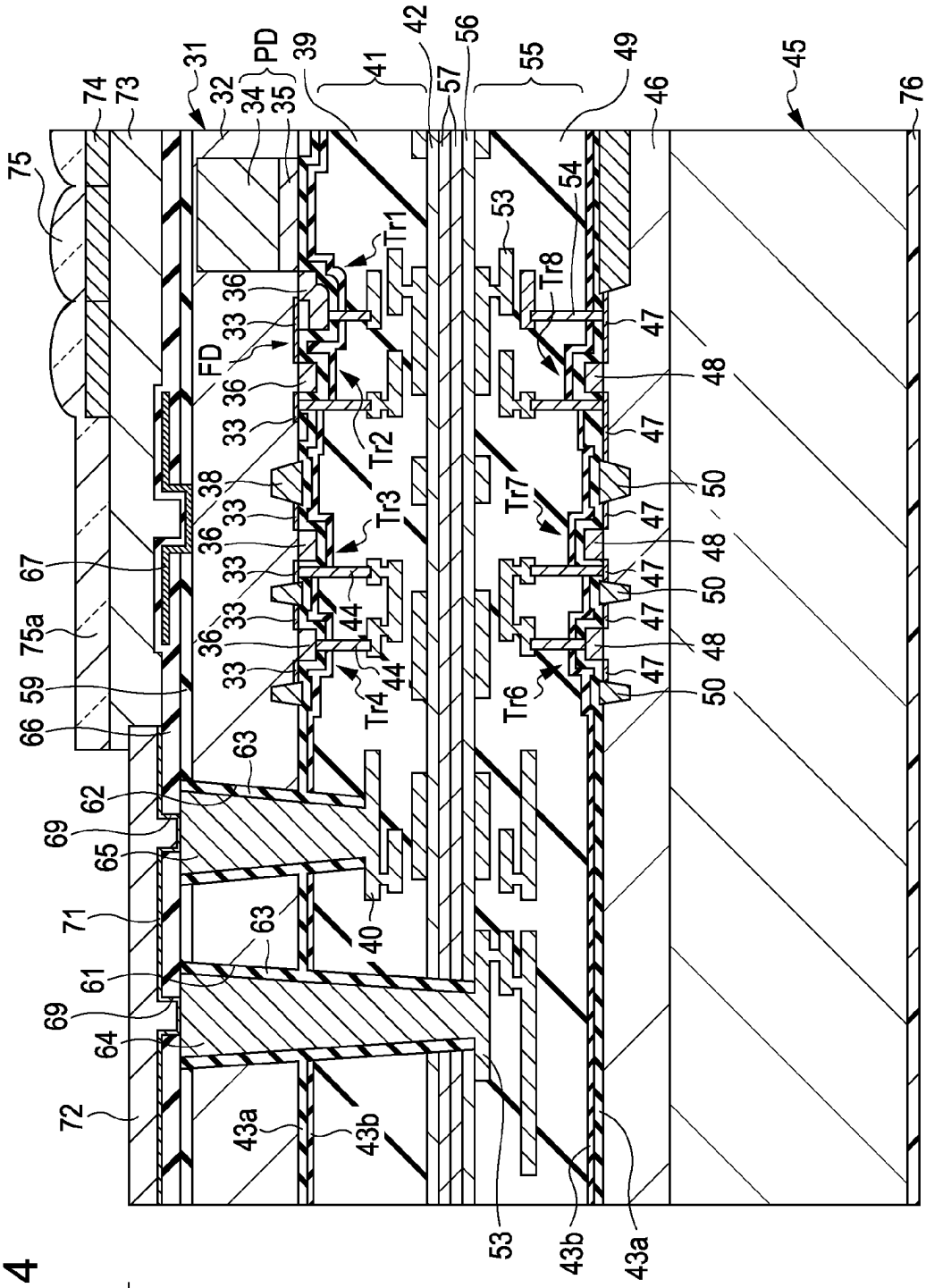

31
32
34
PD
35
39
41
42
56
57
55
49
46
45
76
74
73
75
75a
67
59
66
62
69
65
71
61
64
72
63
40
43a
43b
53
54
Tr1
Tr2
Tr3
Tr4
Tr6
Tr7
Tr8
FD
36
33
38
44
47
48
50
81

FIG. 14

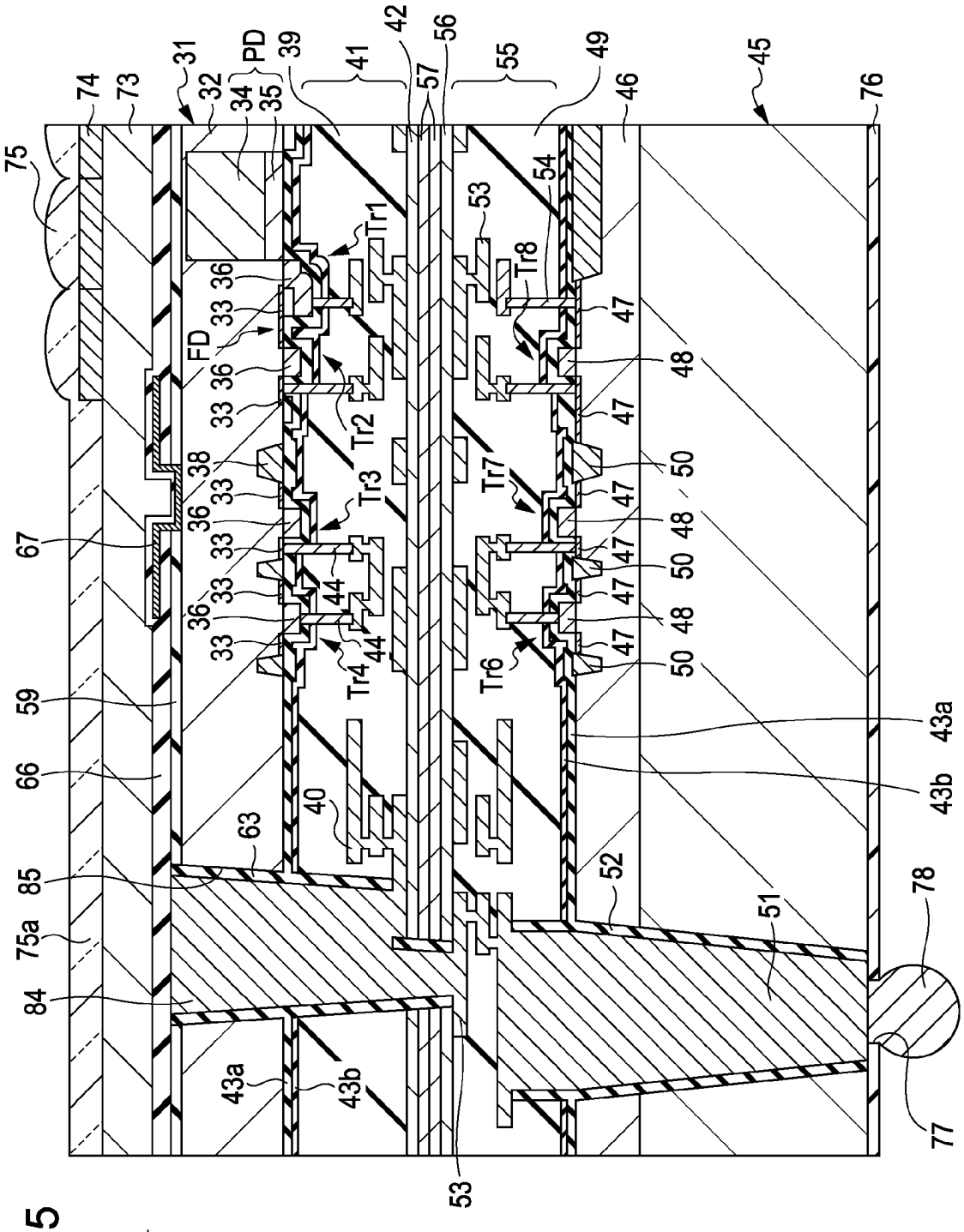

74
73
31
32
34
PD
35
39
41
42
56
57
55
49
46
45
76
75
54
53
Tr1
Tr8
36
33
FD
47
48
Tr2
38
Tr3
Tr7
50
67
44
Tr4
Tr6
59
66
43a
43b
63
40
85
52
51
78
75a
84
77
83

FIG. 15

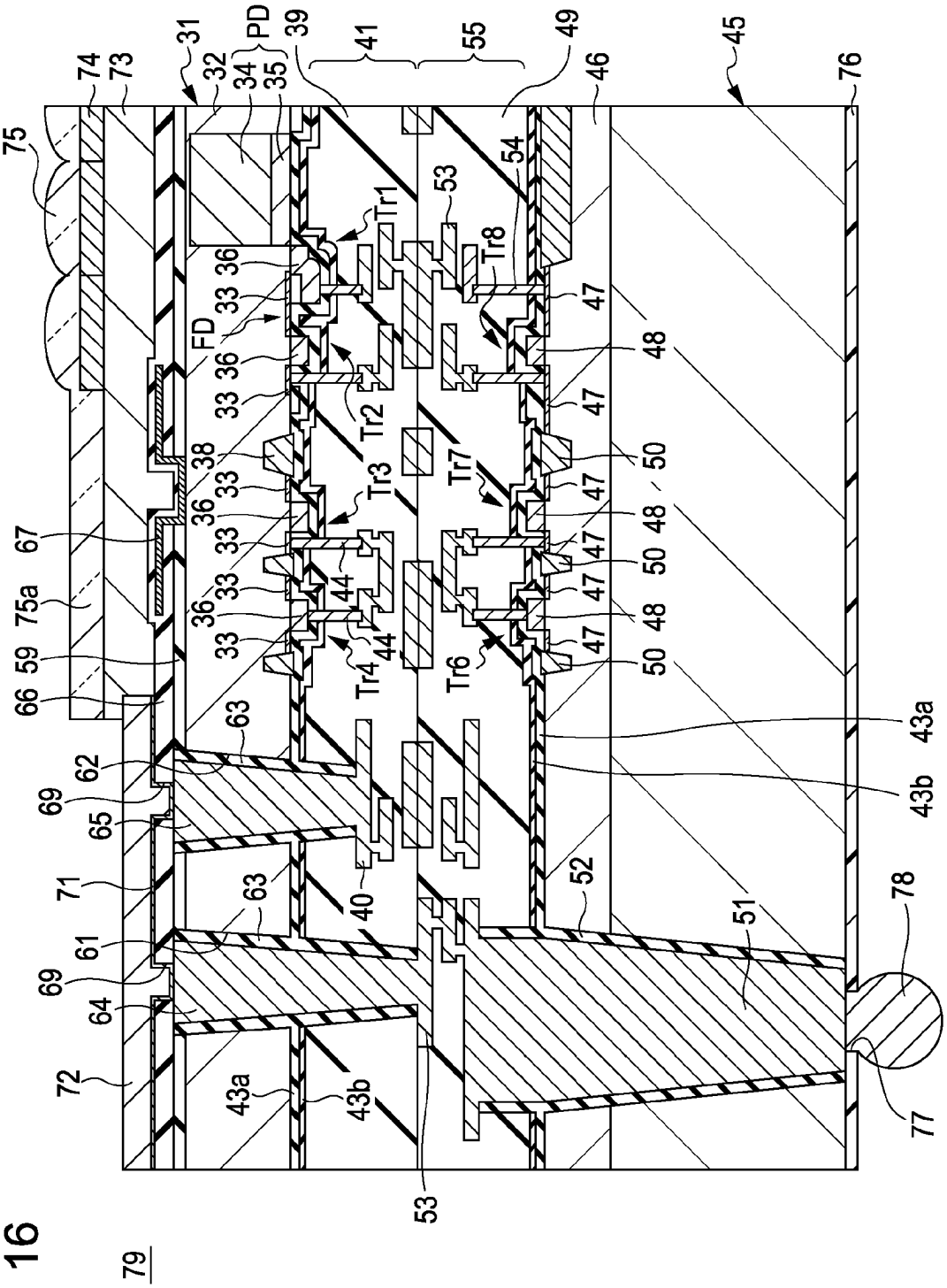

74
73
31
32
PD
34
35
39
41
55
49
46
45
76
75
54
53
Tr1
Tr8
36
33
FD
47
48
Tr2
38
Tr3
Tr7
50
67
75a
44
Tr4
Tr6
59
66
63
43a
62
43b
69
65
71
40
52
51
78
61
64
72
77
79

FIG. 16

FIG. 17

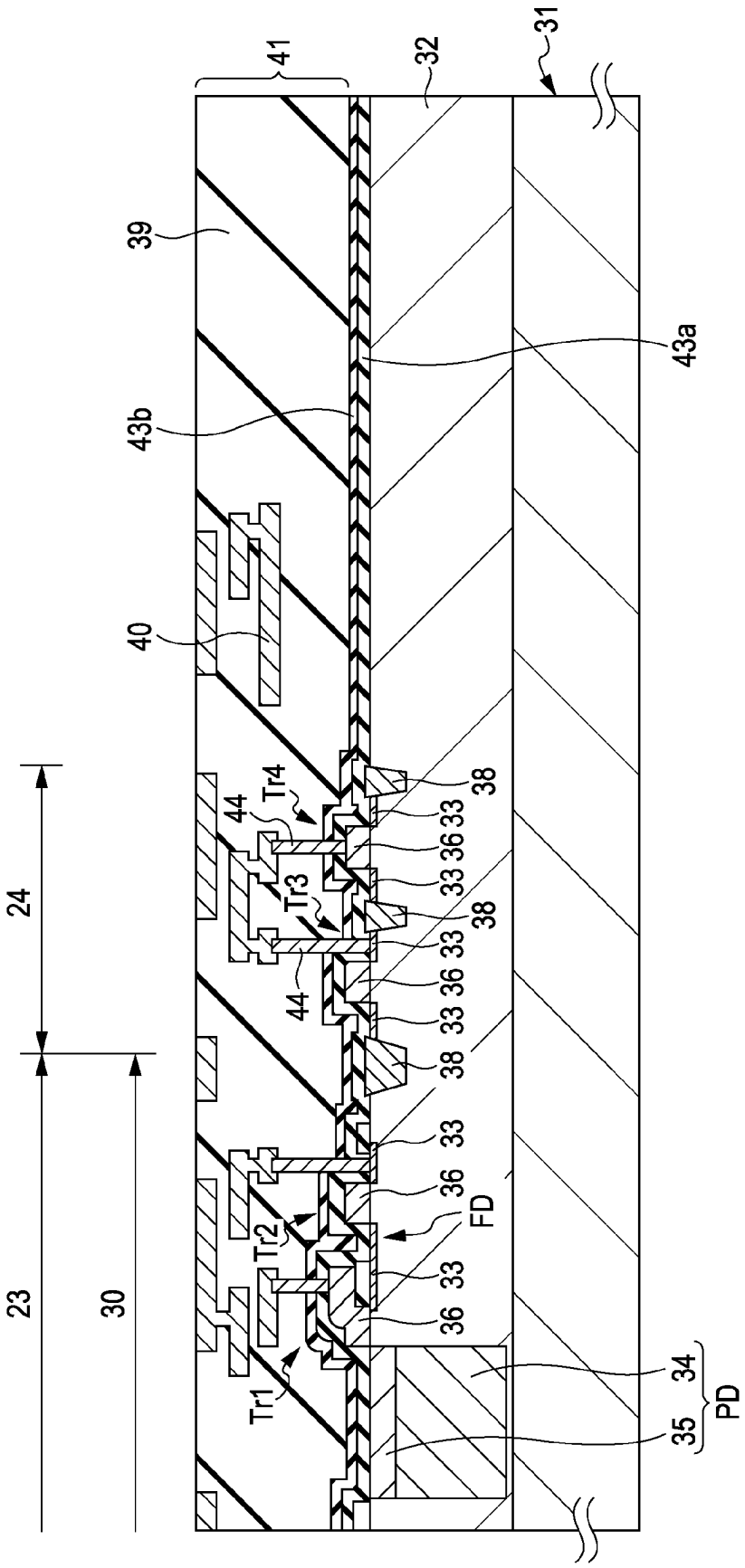

31
32
41
39
43a
43b
40
38
33
36
Tr4
44
Tr3
Tr2
Tr1
FD
34
35
PD
23
24
30

FIG. 18

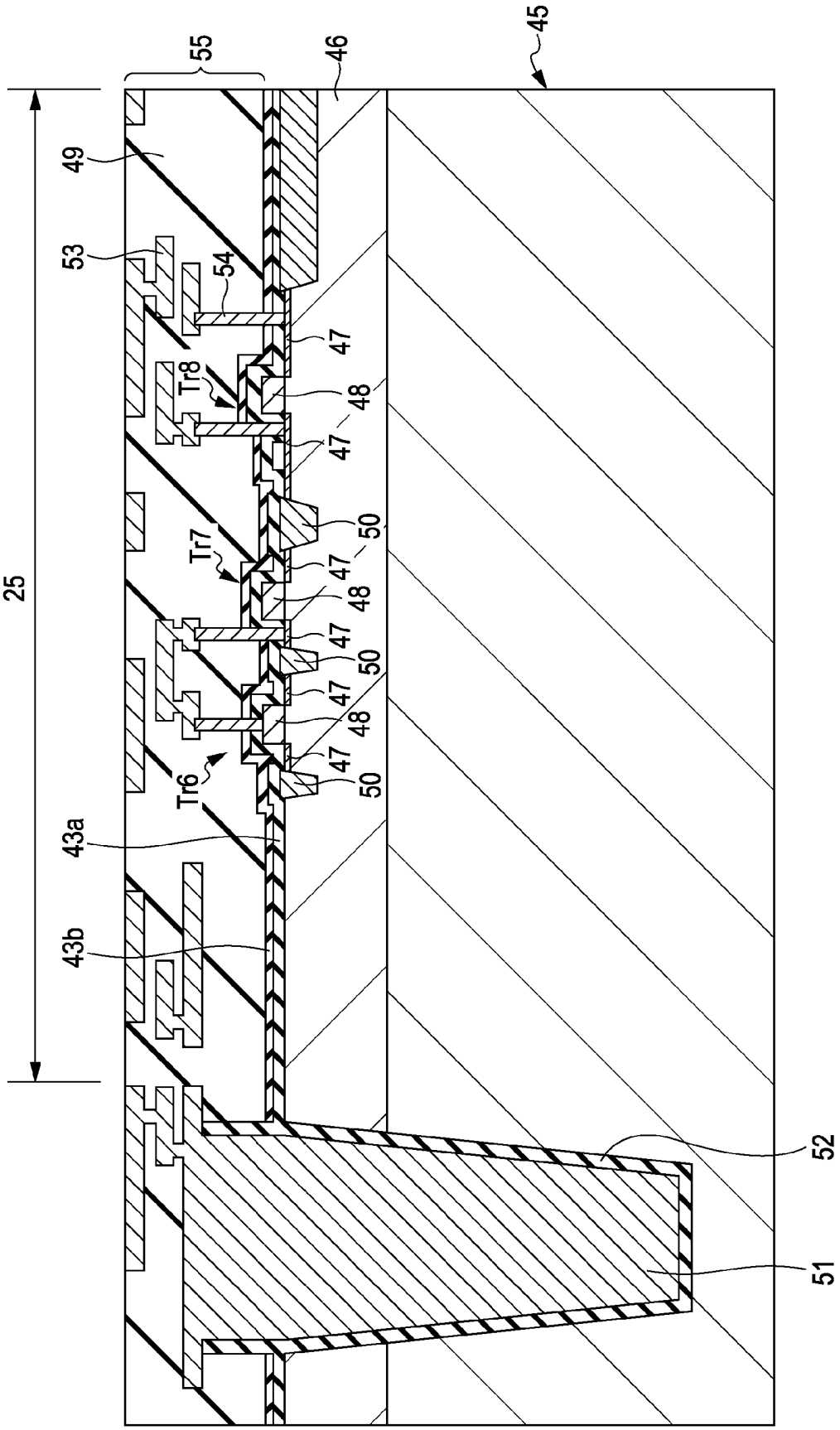

45
46
55
49
53
54
47
Tr8
48
47
50
Tr7
47
48
47
50
47
48
47
Tr6
50
25
43a
43b
52
51

FIG. 19

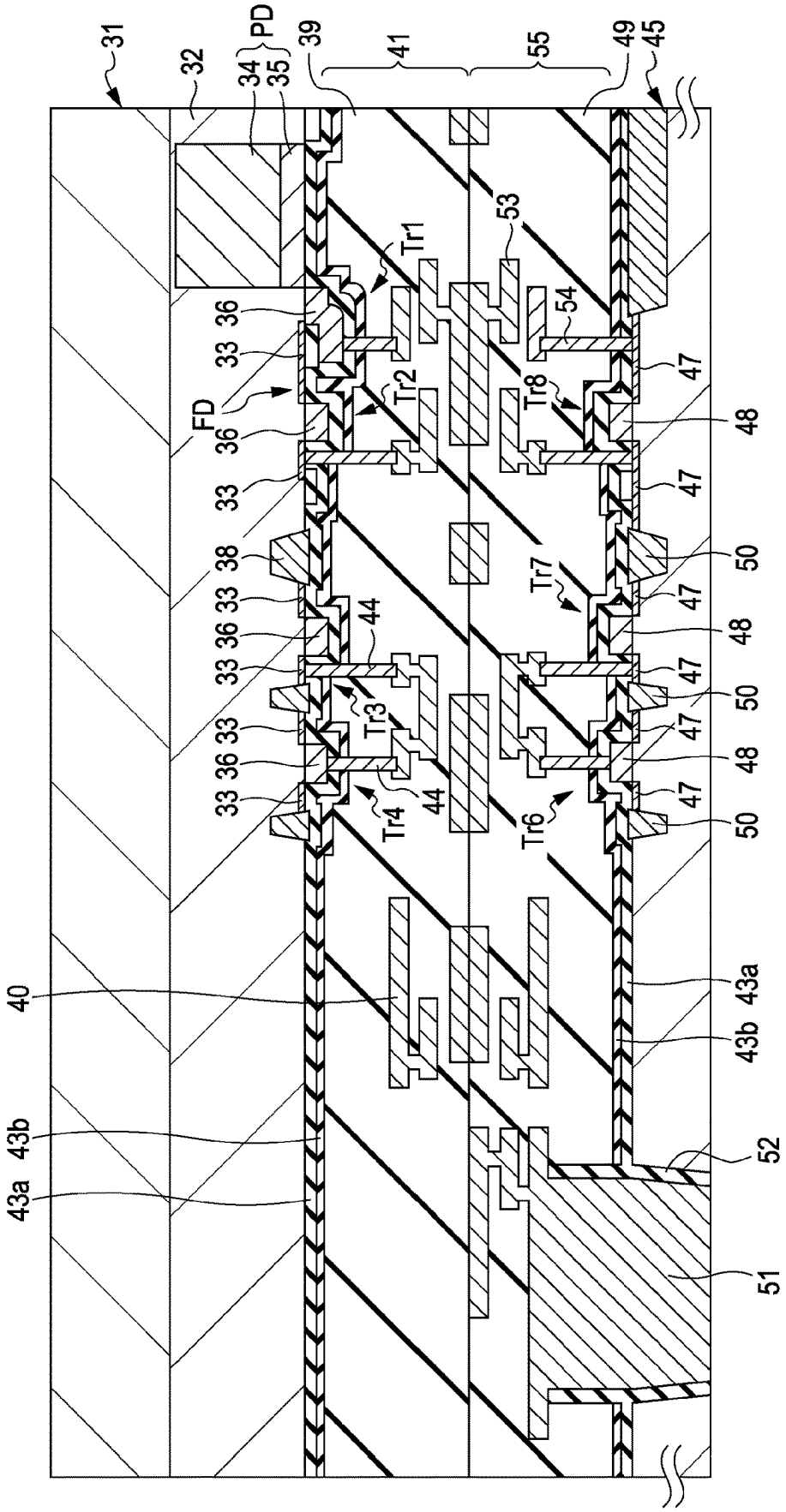

31
32
34
35
PD
39
41
55
49
45
53
Tr1
54
36
33
FD
Tr2
Tr8
47
48
38
Tr7
50
44
Tr3
Tr4
Tr6
40
43a
43b
52
51

FIG. 20

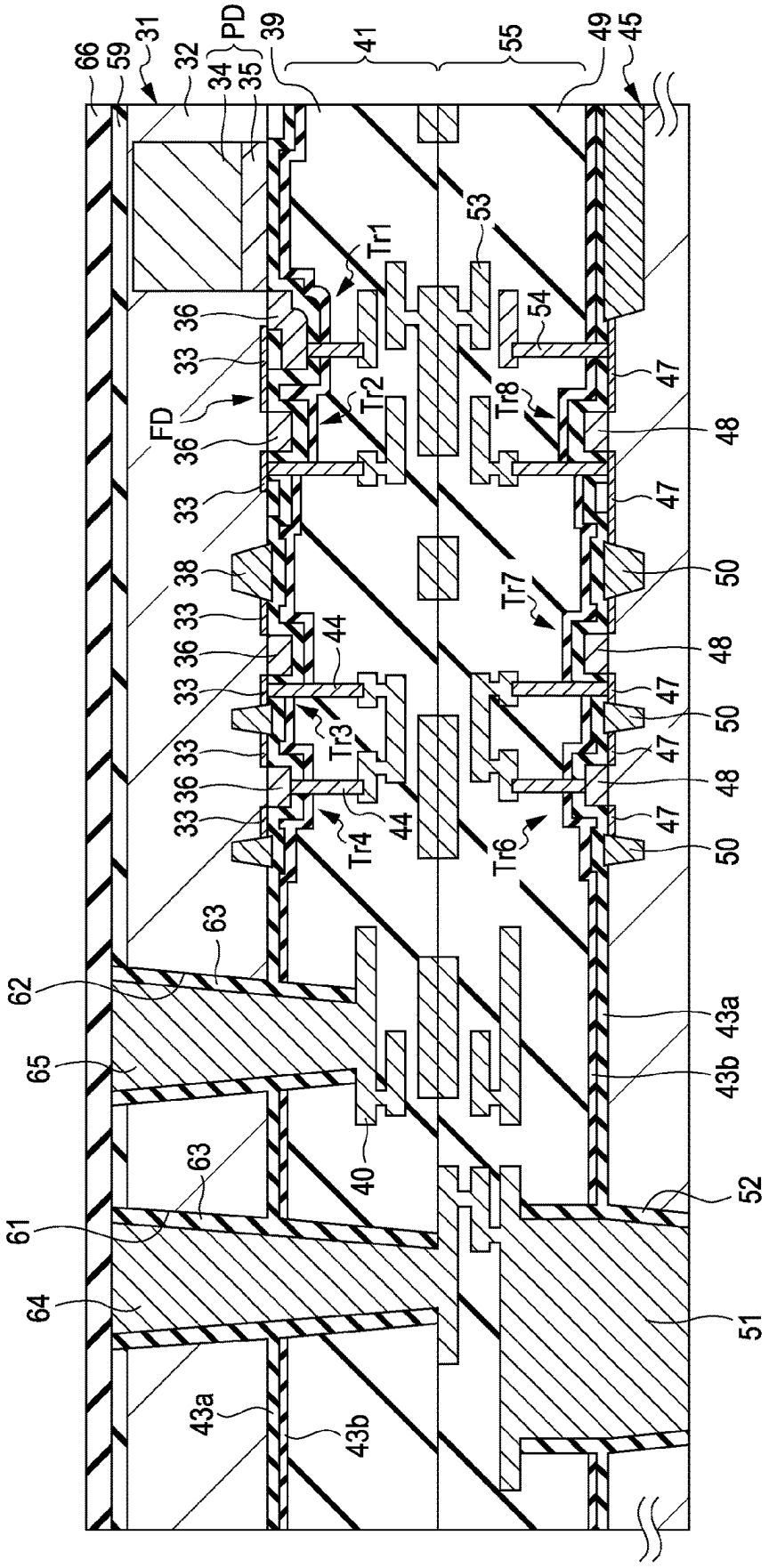
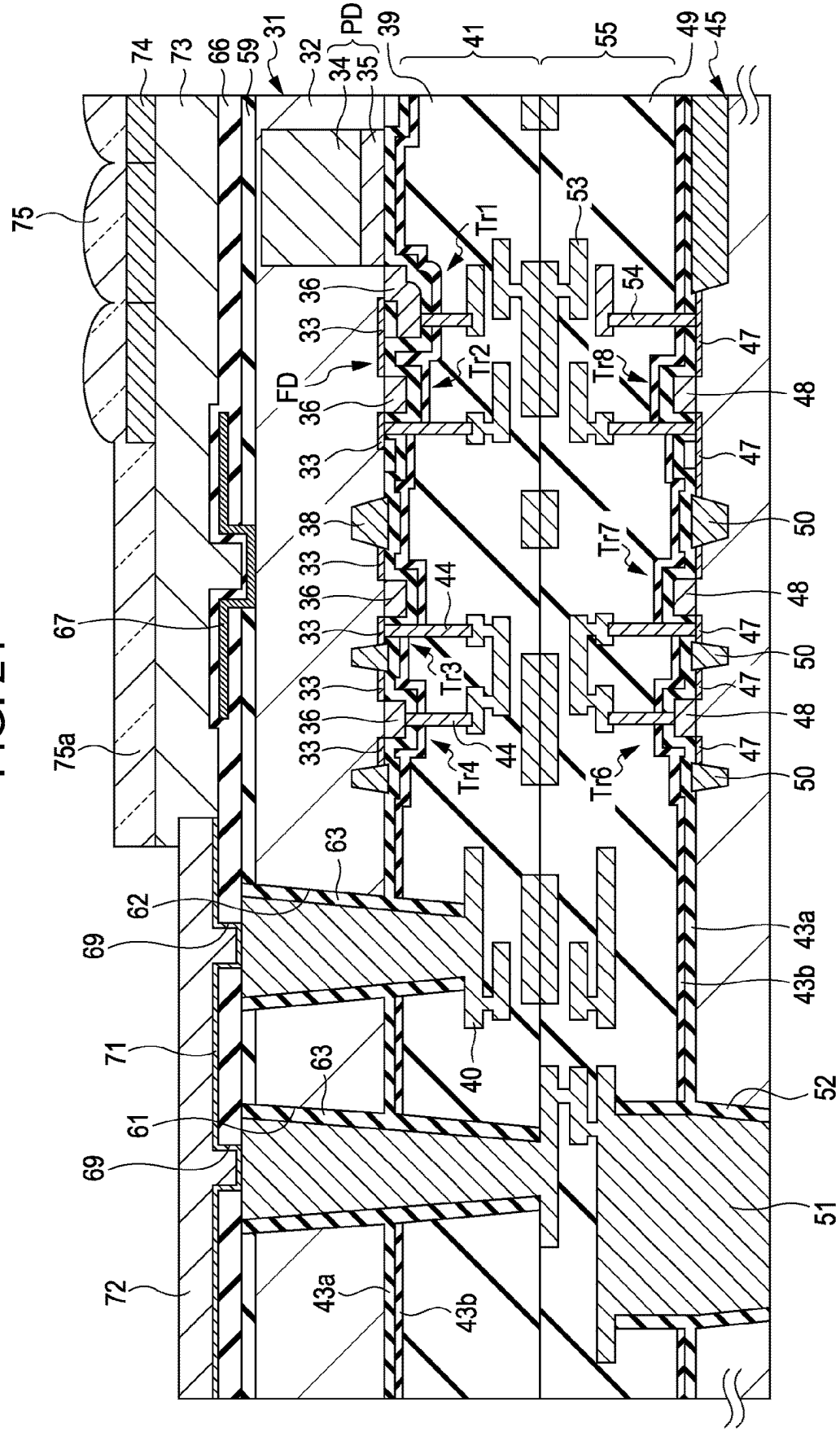

66
59
31
32
PD
34
35
39
41
55
49
45
53
Tr1
54
36
33
FD
Tr2
Tr8
47
48
38
Tr7
50
44
Tr3
Tr4
Tr6
63
62
65
43a
43b
40
52
61
64
51

FIG. 21


74
73
66
59
31
32
PD
34
35
39
41
55
49
45
75
53
Tr1
36
33
54
47
FD
Tr2
Tr8
48
38
Tr7
50
44
67
Tr3
75a
Tr4
Tr6
63
62
69
43a
43b
71
40
52
61
51
72

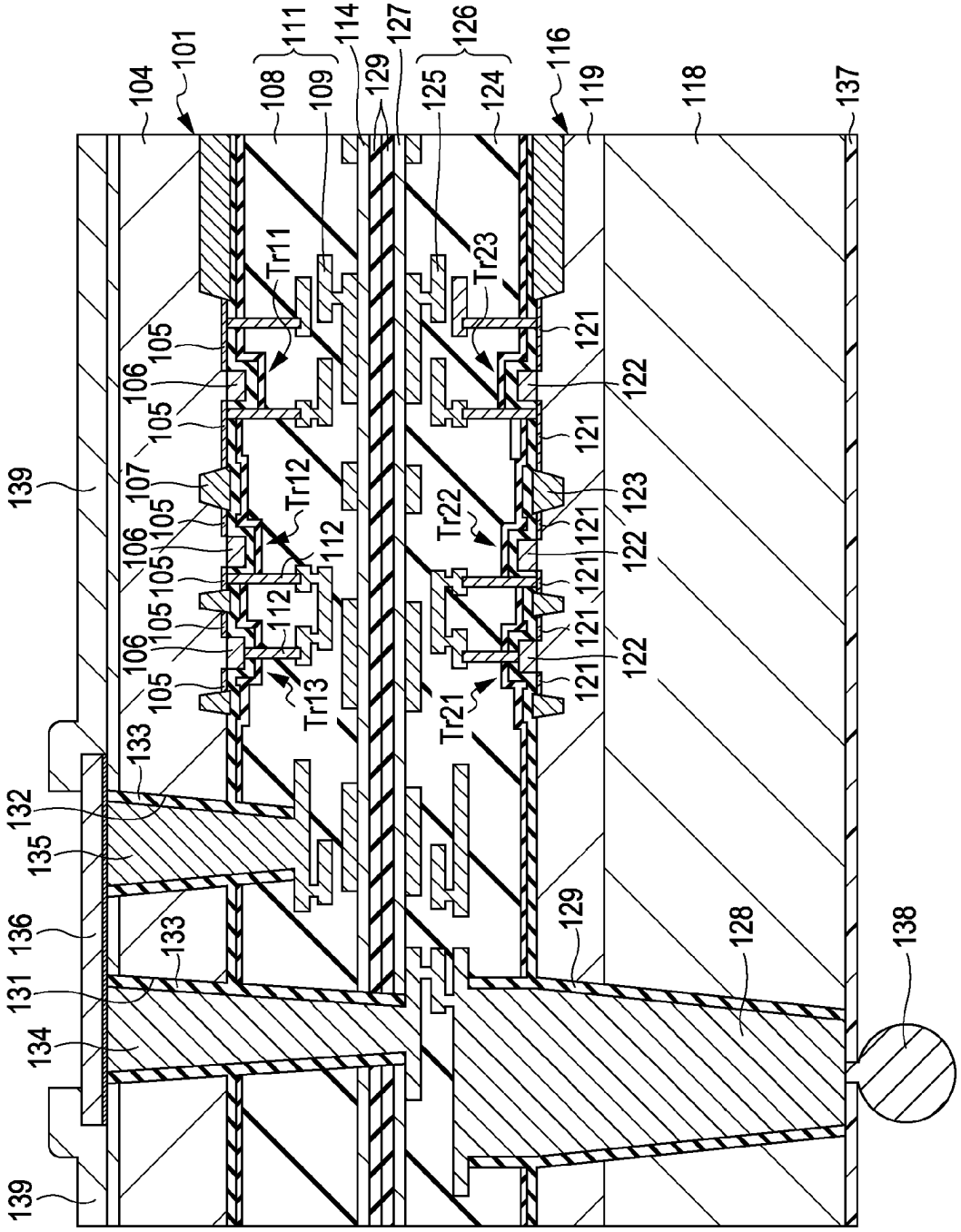

104
101
111
108
109
114
129
127
126
125
124
116
119
118
137
Tr11
Tr23
105
106
107
Tr12
112
Tr22
121
122
123
Tr13
Tr21
139
133
132
135
136
131
134
128
138

FIG. 22

140

FIG. 23

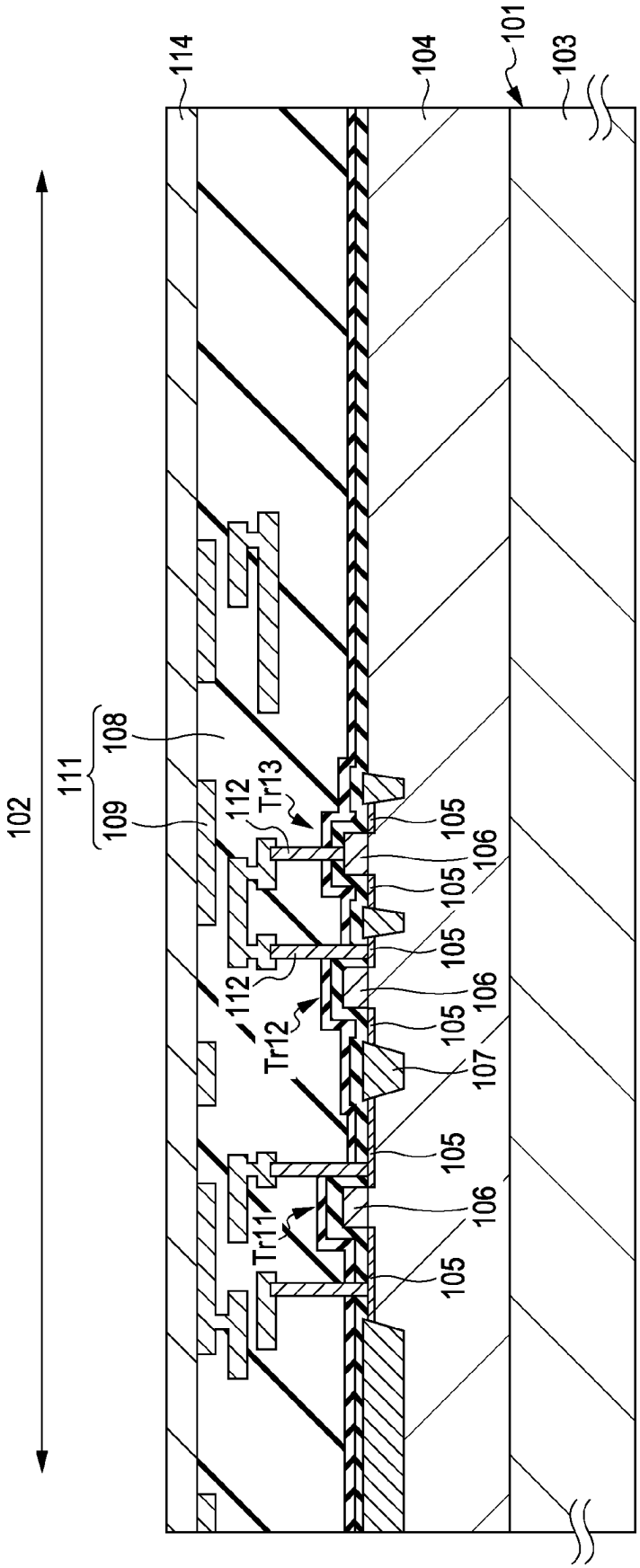

114
104
101
103
102
111
108
109
112
Tr13
105
106
105
105
112
106
Tr12
105
107
105
106
Tr11
105

FIG. 24

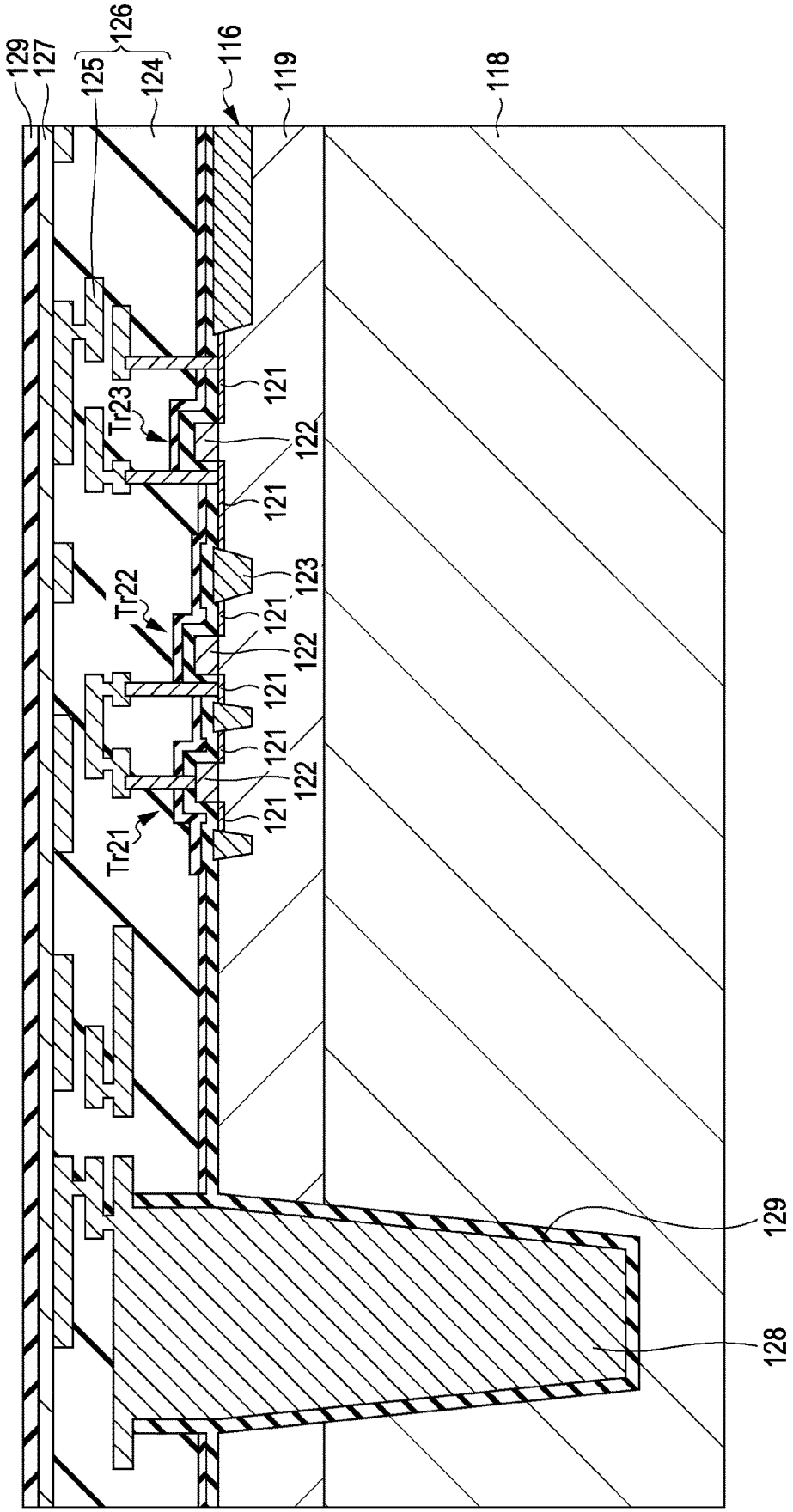

129
127
125
126
124
116
119
118
121
Tr23
122
121
123
Tr22
121
122
121
121
122
121
Tr21
129
128

FIG. 25

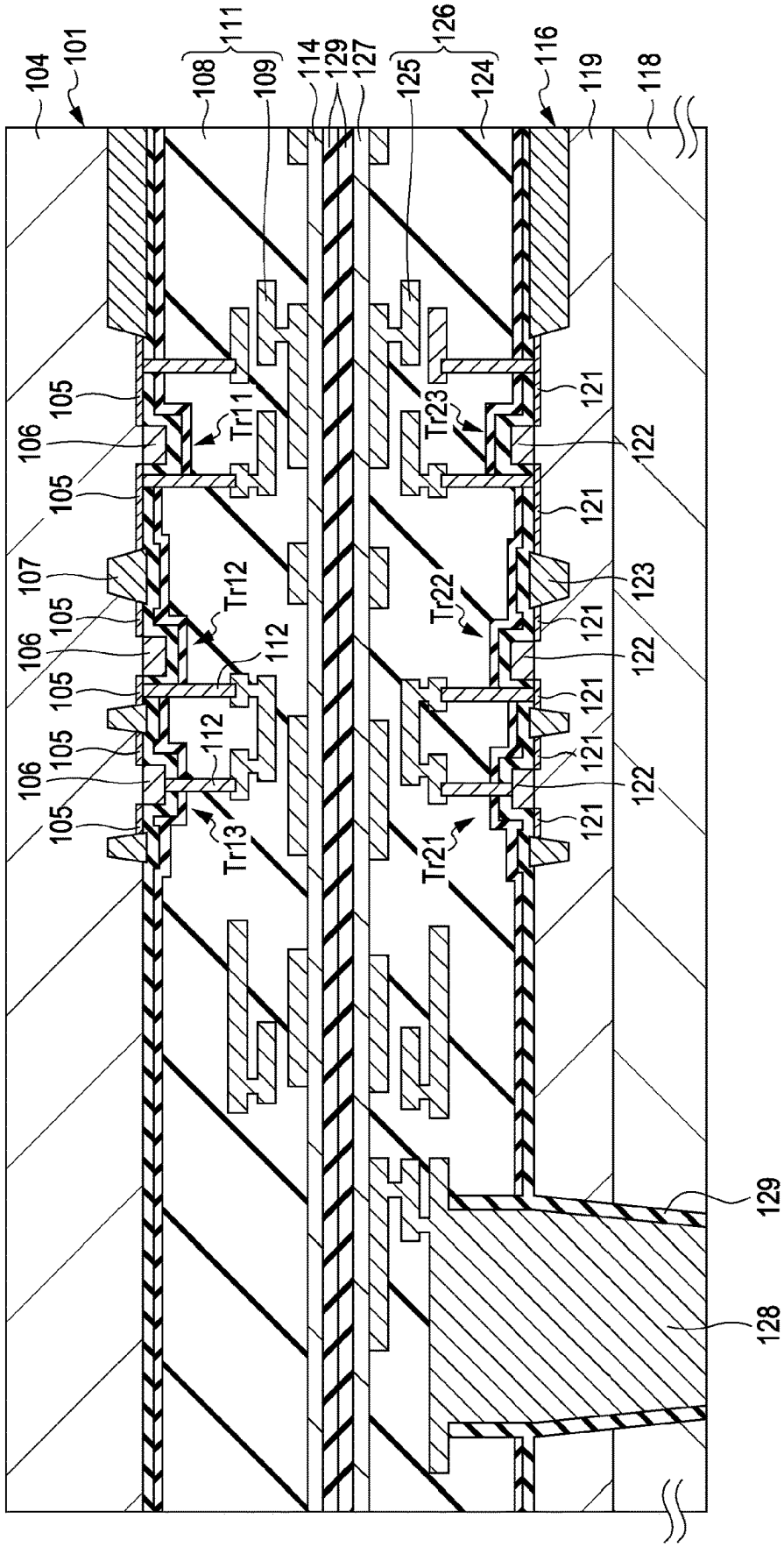

104
101
108
111
109
114
129
127
125
126
124
116
119
118
105
106
107
Tr11
Tr12
Tr13
Tr21
Tr22
Tr23
112
121
122
123
128
129

FIG. 26

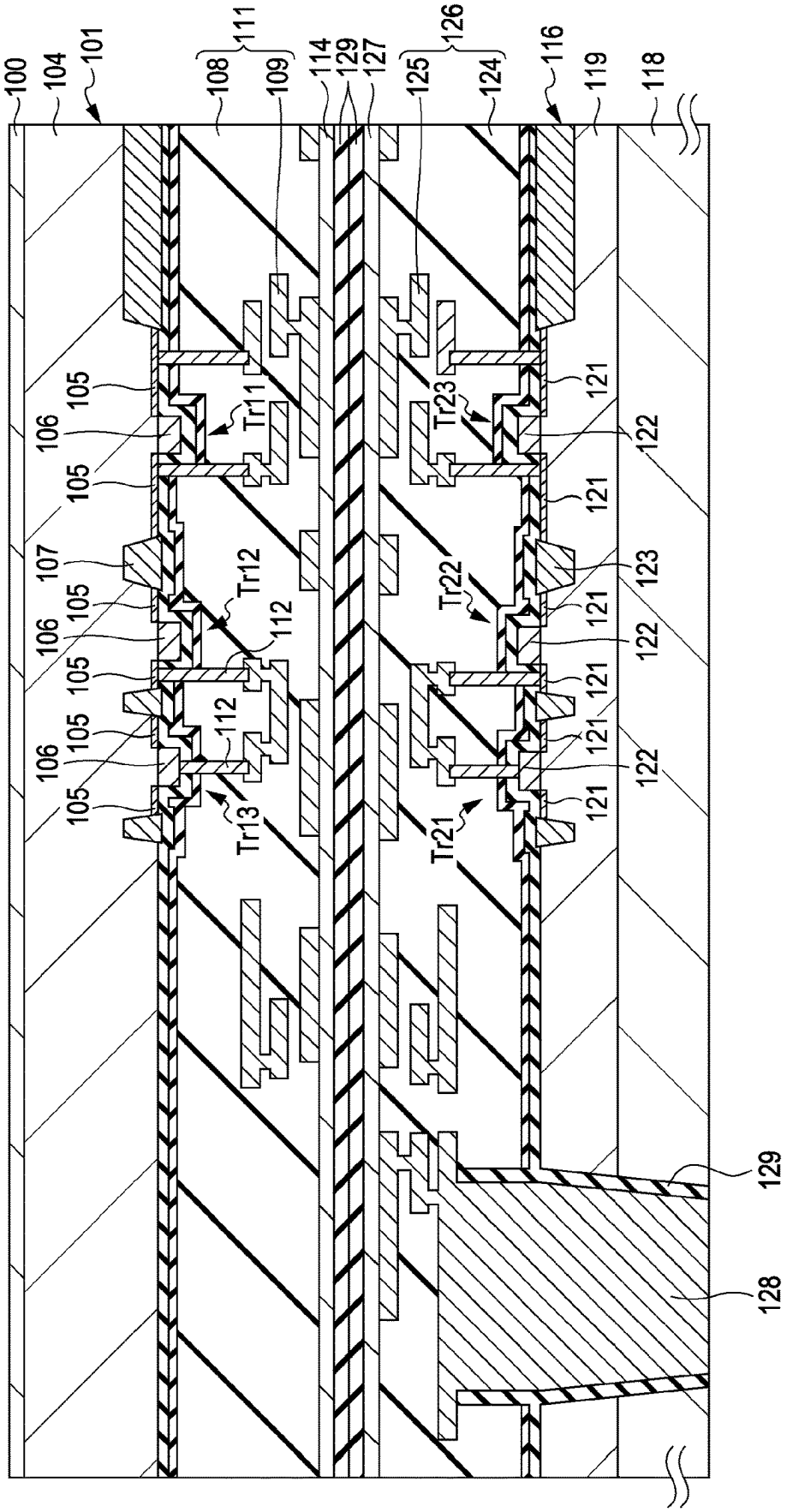

100
104
101
108
111
109
114
129
127
125
126
124
116
119
118
105
106
107
Tr11
Tr12
Tr13
Tr21
Tr22
Tr23
112
121
122
123
128

FIG. 27

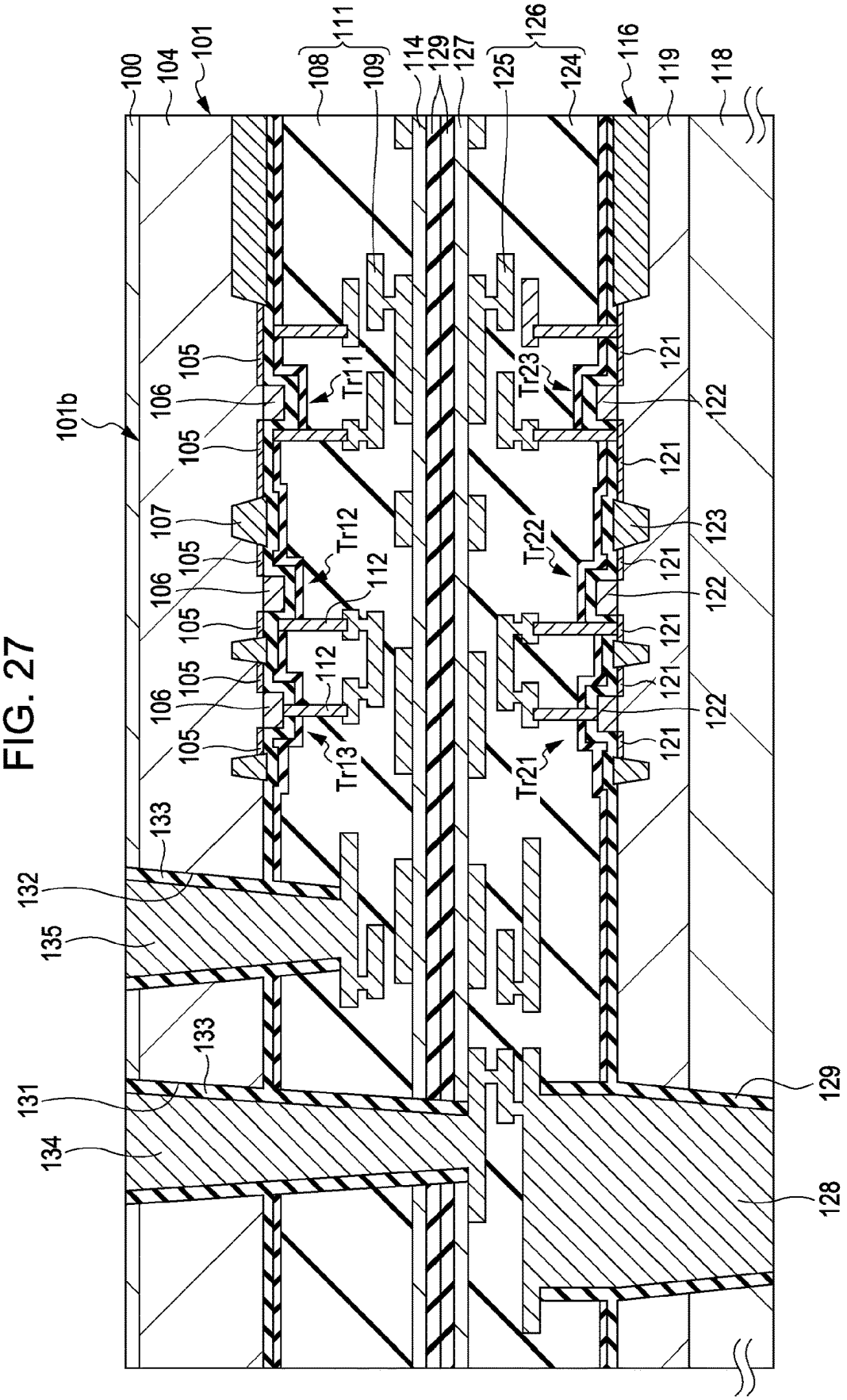

100
104
101
108
111
109
114
129
127
125
126
124
116
119
118
101b
105
106
107
Tr11
Tr12
Tr13
Tr21
Tr22
Tr23
112
121
122
123
133
132
135
131
134
128

FIG. 28

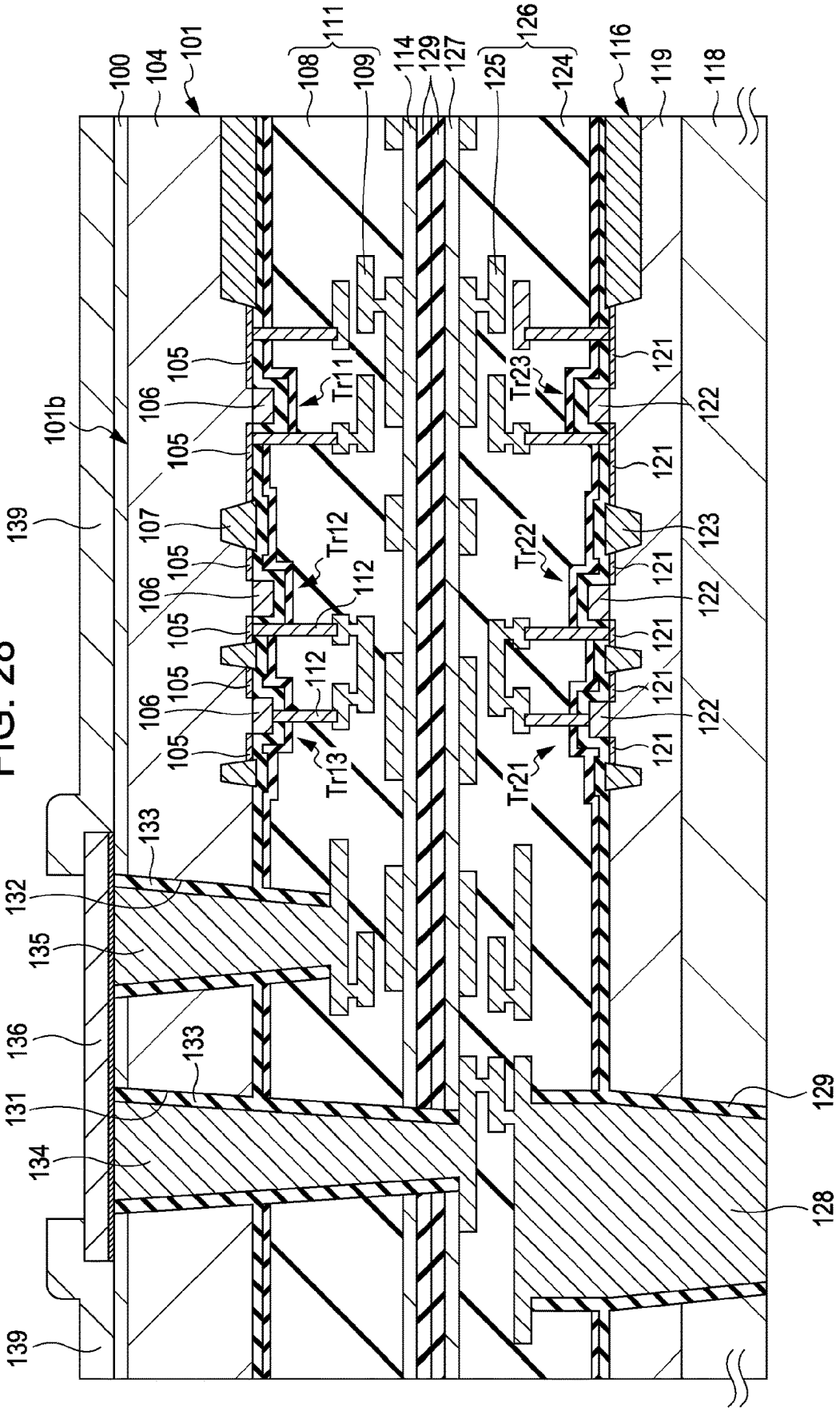
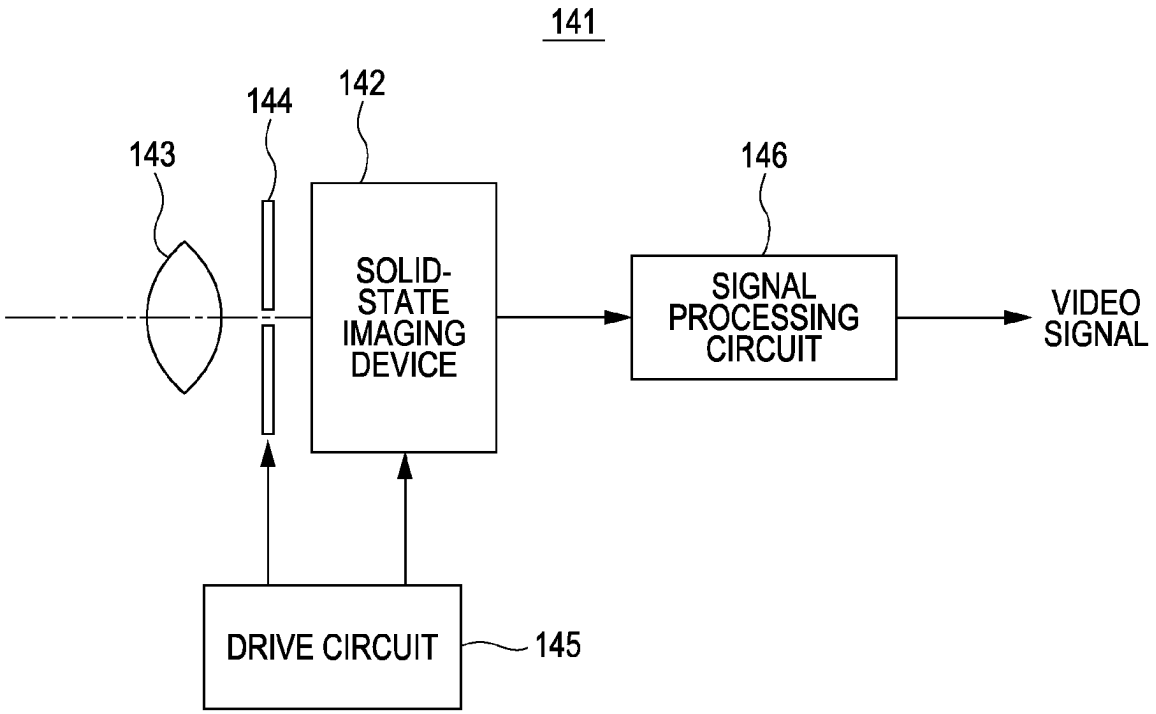

100
104
101
108
111
109
114
129
127
125
126
124
116
119
118
105
106
Tr11
Tr23
121
122
101b
139
107
Tr12
112
Tr22
123
Tr13
Tr21
133
132
135
136
131
134
128

FIG. 29


141
142
144
143
146
SOLID-STATE IMAGING DEVICE
SIGNAL PROCESSING CIRCUIT
VIDEO SIGNAL
DRIVE CIRCUIT
145

SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME, AND ELECTRONIC APPARATUS

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation of U.S. patent application Ser. No. 18/321,439, filed May 22, 2023, which is a continuation of U.S. patent application Ser. No. 17/110,145, filed Dec. 2, 2020, now U.S. Pat. No. 11,764,243, which is a continuation of U.S. patent application Ser. No. 16/913,075, filed Jun. 26, 2020, now U.S. Pat. No. 10,950,647, which is a continuation of U.S. patent application Ser. No. 16/358,348, filed Mar. 19, 2019, now U.S. Pat. No. 10,916,577, which is a continuation of U.S. patent application Ser. No. 15/814,177, filed Nov. 15, 2017, now U.S. Pat. No. 10,403,670, which is a continuation of U.S. patent application Ser. No. 15/713,226, filed Sep. 22, 2017, now U.S. Pat. No. 10,141,361, which is a continuation of U.S. patent application Ser. No. 15/374,864, filed Dec. 9, 2016, now U.S. Pat. No. 9,799,695, which is a continuation of U.S. patent application Ser. No. 15/087,695, filed Mar. 31, 2016, now U.S. Pat. No. 9,530,812, which is a continuation of U.S. patent application Ser. No. 14/834,010, filed Aug. 24, 2015, now U.S. Pat. No. 9,319,569, which is a continuation of U.S. patent application Ser. No. 12/722,069, filed Mar. 11, 2010, now U.S. Pat. No. 9,451,131, which claims priority to Japanese Patent Application Nos. JP 2009-068582 and JP 2010-012586, filed in the Japan Patent Office on Mar. 19, 2009 and Jan. 22, 2010, respectively, the entire disclosures of which are hereby incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor device, such as a solid-state imaging device, and a method of manufacturing such a semiconductor device. The present invention also relates to an electronic apparatus, such as a camera, equipped with the semiconductor device.

2. Description of the Related Art

Solid-state imaging devices, which have been commonly used, include amplification-type solid-state imaging devices as typified by MOS image sensors such as complementary metal oxide semiconductors (CMOSs) and charge-transfer solid-state imaging devices as typified by charge coupled device (CCD) image sensors. These solid-state imaging devices have been widely used for digital still cameras, digital video cameras, and so on. Furthermore, in recent years, MOS image sensors have been used for most of solid-state imaging devices mounted on mobile devices such as camera cell-phones and PDAs (Personal Digital Assistants) because of their low power voltages, low consumption powers, and so on.

The MOS solid-state imaging device includes a pixel array (pixel region) where a plurality of unit pixels are arranged in a two-dimensional array, and a peripheral circuit region. The unit pixel is formed of a photodiode and a plurality of pixel transistors, serving as a photoelectric conversion part. The pixel transistors may be three MOS transistors: a transfer transistor, a reset transistor, and an amplification transistor, or may be four in which a selection transistor is further included.

Some of the MOS solid-state imaging devices are those in which a semiconductor chip with a pixel region on which a plurality of pixel is arranged is electrically connected to a semiconductor chip in which a logic circuit for signal processing is formed to form a single device. Various kinds of such a device have been proposed. For example, Japanese Unexamined Patent Application Publication No. 2006-49361 discloses a semiconductor module where a back-illuminated image sensor chip having a micro-pad for each pixel cell and a signal processing chip, on which a signal processing circuit is formed, having a micro-pad are connected to each other via a micro-bump. Japanese Unexamined Patent Application Publication No. 2007-13089 discloses a device on which a sensor chip and a signal processing chip are mounted on an interposer (intermediate substrate). The sensor chip is a back-illuminated MOS solid-state imaging device with an imaging pixel section and the signal processing chip is provided with a peripheral circuit performing signal processing. In Japanese Unexamined Patent Application Publication No. 2008-130603, an imaging device includes an image sensor chip, a thin-layer circuit board, and a logic circuit chip for signal processing. In addition, it also discloses the configuration of the device in which the thin-layer circuit board and the logic circuit chip are electrically connected to each other. In this case, the thin-layer circuit board is electrically connected from the backside of the image sensor chip through a through-hole-via.

In addition, Japanese Patent No. 4000507 discloses a solid-state imaging device provided with a penetration electrode on a solid-state imaging element supported on a transparent substrate, where the solid-state imaging element is electrically connected to a flexible circuit substrate. Furthermore, Japanese Unexamined Patent Application Publication No. 2003-31785 discloses a back-illuminated solid-state imaging device provided with an electrode passing through a supporting substrate.

As described in Japanese Unexamined Patent Application Publication Nos. 2006-49361, 2007-13089, and 2008-130603, various technologies for combining an image sensor chip with different circuit chips such as logic circuit have been proposed. In these technologies, any of functional chips is almost completely built up in advance and then mounted on a substrate while being allowed to make a connection between the chips by the formation of a connection through hole.

SUMMARY OF THE INVENTION

As is evident from any of the above solid-state imaging devices, there is an idea of constructing a semiconductor device by making a connection between different microchips using a connection conductor passing through a substrate. However, a connection hole has to be formed deeply in a substrate while being insulated. Thus, it is practically difficult from the viewpoints of the processing of a connection hole and the cost effectiveness of a process for embedding a connection conductor.

On the other hand, the formation of a contact hole with a small diameter of about 1 micrometer uses the thinning of an upper chip to the minimum. In this case, however, some complicated steps, such as one for bonding the upper chip on a supporting substrate, may be desired, which causes an increase in cost. In order to embed the connection conductor in the connection hole with a high aspect ratio, the connection conductor materials are limited because it is necessary

to use a CVD film with good coatability, such as tungsten (W), as a connection conductor.

In order to have economical efficiency simply applicable by mass production, it is desirable to choose such art that the aspect ratio of this connecting hole is lowered dramatically so as to form the hole easily and the hole is processed within a related-art wafer manufacturing process without using special connecting hole processing.

Furthermore, it is desirable to provide the solid-state imaging device with a high performance by designing both an imaging region and a logic circuit for signal processing to sufficiently exert their respective performances.

In addition to the solid-state imaging device, it is also desirable to provide any of other semiconductor devices having semiconductor integrated circuits with high performance by designing the circuits to sufficiently exert their respective performances.

The present invention has been made in consideration of the aforementioned desires and intends to provide a solid-state imaging device that allows its circuits to sufficiently exert their respective capabilities to attain mass productivity and cost reduction.

Also, the present invention intends to provide an electronic apparatus, such as a camera, equipped with the above solid-state imaging device.

According to an embodiment of the present invention, a semiconductor device is a back-illuminated solid-state imaging device that includes microchips prepared by bonding a first semiconductor wafer having a pixel array in a half-finished product state (hereinafter, also referred to as a half-finished pixel array) and a second semiconductor wafer having a logic circuit in a half-finished product state (hereinafter, also referred to as a half-finished logic circuit) together and then completing the circuits to make them into microchips. The bonding may include bonding the semiconductor wafers together, thinning the first semiconductor wafer, and making an electric connection between the pixel array and the logic circuit.

In the semiconductor device according to the embodiment of the present invention, a pixel array is formed on a microchip part made of a first semiconductor wafer and a logic circuit is formed on a microchip part of a second semiconductor wafer. Thus, the pixel array and the logic circuit are formed under optimal conditions. Under the optimal process technology, the pixel array and the logic circuit that exert sufficient performance capabilities can be formed.

The second semiconductor wafer with the half-finished logic circuit can also serve as a substrate supporting the first semiconductor wafer to be thinned. Subsequently, the first semiconductor wafer with the half-finished pixel array and the second semiconductor wafer with the half-finished logic circuit are bonded together. Finally, the pixel array in a finished product state and the logic circuit in a finished product state are formed. Therefore, the back-illuminated solid-state imaging device suitable for mass production and cost reduction can be obtained.

A method of manufacturing a semiconductor device according to an embodiment of the present invention prepares a first semiconductor wafer with a half-finished pixel array and a second semiconductor wafer with a half-finished logic circuit. The method includes steps of bonding the first semiconductor wafer and the second semiconductor wafer together, thinning the first semiconductor wafer, and electrically connecting the pixel array and the logic circuit together. The method further includes steps of completing the first semiconductor wafer and the second semiconductor wafer which are bonded together and cutting them into pieces for the respective microchips. Consequently, the back-illuminated solid-state imaging device can be produced.

In the method of manufacturing the semiconductor device according to the embodiment of the present invention, the pixel array is formed on the microchip part of the first semiconductor wafer and the logic circuit is formed on the microchip part of the second semiconductor wafer. Both the pixel array and the logic circuit can be formed under optimum conditions. In other words, under the optimal process technology, the pixel array and the logic circuit that exert sufficient performance capabilities can be formed. In addition, the second semiconductor wafer with the half-finished logic circuit can also serve as a substrate supporting the first semiconductor wafer to be thinned.

Subsequently, the first semiconductor wafer with the half-finished pixel array and the second semiconductor wafer with the half-finished logic circuit are bonded together, and then subjected to the thinning and the electric connection, followed by completing the wafers and dividing them into the respective microchips. Consequently, it becomes possible to mass-produce the back-illuminated solid-state imaging device. Thus, the sold-state imaging device can be produced at low cost.

An electronic apparatus according to an embodiment of the present invention includes a solid-state imaging device, an optical system that introduces incident light into a photodiode in the solid-state imaging device, and a signal-processing circuit that processes an output signal from the solid-state imaging device. In the electronic apparatus, the solid-state imaging device is a back-illuminated solid-state imaging device that includes microchips prepared by bonding a first semiconductor wafer having a half-finished pixel array and a second semiconductor wafer having a half-finished logic circuit together and then completing the circuits to make them into microchips. The bonding may include bonding the semiconductor wafers together, thinning the first semiconductor wafer, and making an electric connection between the pixel array and the logic circuit. As the electronic apparatus of the present invention includes the solid-state imaging device of the embodiment of the present invention, the pixel array and the logic circuit that exert sufficient performance capabilities for the solid-state imaging device can be formed. In addition, the solid-state imaging device can be produced at low cost. Thus, the electronic apparatus can be produced at low cost.

According to an embodiment of the present invention, a semiconductor device includes microchips prepared by bonding a first semiconductor wafer having a half-finished first semiconductor integrated circuit and a second semiconductor wafer having a half-finished second semiconductor integrated circuit together and then completing the circuits to make them into microchips. The bonding may include bonding the semiconductor wafers together, thinning the first semiconductor wafer, and making an electric connection between the first semiconductor integrated circuit and the second semiconductor integrated circuit.

In the semiconductor device according to the embodiment of the present invention, a first semiconductor integrated circuit is formed on a microchip part made of a first semiconductor wafer and a second semiconductor integrated circuit is formed on a microchip part of a second semiconductor wafer. Thus, the first semiconductor integrated circuit and the second semiconductor integrated circuit are formed under optimal conditions. Under the optimal process technology, the first semiconductor integrated circuit and the

second semiconductor integrated circuit that exert sufficient performance capabilities can be formed.

The second semiconductor wafer with the second semiconductor integrated circuit can also serve as a substrate supporting the first semiconductor wafer to be thinned.

Subsequently, the first semiconductor wafer with the half-finished first semiconductor integrated circuit and the second semiconductor wafer with the half-finished second semiconductor integrated circuit are bonded together to finally complete the semiconductor integrated circuits. Therefore, the semiconductor device suitable for mass production and cost reduction can be obtained.

A method of manufacturing a semiconductor device according to an embodiment of the present invention prepares a first semiconductor wafer with a half-finished first semiconductor integrated circuit and a second semiconductor wafer with a half-finished second semiconductor integrated circuit. The method includes steps of bonding the first semiconductor wafer and the second semiconductor wafer together, thinning the first semiconductor wafer, and electrically connecting the first semiconductor integrated circuit and the second semiconductor integrated circuit together. The method further includes steps of completing the first semiconductor wafer and the second semiconductor wafer which are bonded together and cutting them into pieces for the respective microchips.

In the method of producing the semiconductor device according to the embodiment of the present invention, a first semiconductor integrated circuit is formed on a microchip part made of a first semiconductor wafer and a second semiconductor integrated circuit is formed on a microchip part of a second semiconductor wafer. Thus, the first semiconductor integrated circuit and the second semiconductor integrated circuit are formed under optimal conditions. Under the optimal process technology, the first semiconductor integrated circuit and the second semiconductor integrated circuit that exert sufficient performance capabilities can be formed.

In addition, the second semiconductor wafer with the half-finished second semiconductor integrated circuit can also serve as a substrate supporting the first semiconductor to be thinned. Subsequently, the first semiconductor wafer with the half-finished first semiconductor integrated circuit and the second semiconductor wafer with the half-finished second semiconductor integrated circuit are bonded together, and then subjected to the thinning and the electric connection, followed by completing the wafers and dividing them into the respective microchips. Consequently, it becomes possible to mass-produce the semiconductor device. Thus, the semiconductor device can be produced at low cost.

In the semiconductor device according to any of the embodiments of the present invention, the pixel array and the logic circuit that exert their respective sufficient performance capabilities are formed in each microchip part. Thus, a high-performance semiconductor device, or a back-illuminated solid-state imaging device, can be provided. In addition, the high-performance back-illuminated solid-state imaging device with excellent mass productivity and cost effectiveness can be provided.

In the semiconductor device according to any of the embodiments of the present invention, furthermore, the first semiconductor integrated circuit and the second semiconductor integrated circuit that exert their respective sufficient performance capabilities are formed in each microchip part. Therefore, a high-performance semiconductor device can be provided. In addition, the high-performance semiconductor device with excellent mass productivity and cost effectiveness can be provided.

In the method of manufacturing the semiconductor device according to any of the embodiments of the present invention, under the optimal process technology, a high-performance semiconductor device, or a high-performance back-illuminated solid-state imaging device, provided with the pixel array and the logic circuit that exert sufficient performance capabilities can be manufactured. In addition, the high-performance back-illuminated solid-state imaging device with excellent mass productivity and cost effectiveness can be provided.

In the method of manufacturing the semiconductor device according to any of the embodiments of the present invention, under the optimal process technology, a high-performance semiconductor provided with the first semiconductor integrated circuit and the second semiconductor integrated circuit that exert sufficient performance capabilities can be manufactured. In addition, the high-performance semiconductor device with excellent mass productivity and cost effectiveness can be produced.

The electronic apparatus according to the embodiment of the present invention includes a high-performance solid-state imaging device with a lower production cost. Therefore, an inexpensive and reliable electronic apparatus can be provided.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a schematic diagram illustrating the configuration of a MOS solid-state imaging device according to an embodiment of the present invention;

FIGS. **2**A to **2**C are schematic diagrams illustrating the solid-state imaging device according to the embodiment of the present invention;

FIG. **3** is a schematic diagram illustrating a main part of the solid-state imaging device according to a first embodiment of the present invention;

FIG. **4** is a diagram (first) illustrating an example of a method of manufacturing the solid-state imaging device according to the first embodiment of the present invention;

FIG. **5** is a diagram (second) illustrating the example of the method of manufacturing the solid-state imaging device according to the first embodiment of the present invention;

FIG. **6** is a diagram (third) illustrating the example of the method of manufacturing the solid-state imaging device according to the first embodiment of the present invention;

FIG. **7** is a diagram (fourth) illustrating the example of the method of manufacturing the solid-state imaging device according to the first embodiment of the present invention;

FIG. **8** is a diagram (fifth) illustrating the example of the method of manufacturing the solid-state imaging device according to the first embodiment of the present invention;

FIG. **9** is a diagram (sixth) illustrating the example of the method of manufacturing the solid-state imaging device according to the first embodiment of the present invention;

FIG. **10** is a diagram (seventh) illustrating the example of the method of manufacturing the solid-state imaging device according to the first embodiment of the present invention;

FIG. **11** is a diagram (eighth) illustrating the example of the method of manufacturing the solid-state imaging device according to the first embodiment of the present invention;

FIG. **12** is a diagram (ninth) illustrating the example of the method of manufacturing the solid-state imaging device according to the first embodiment of the present invention;

FIG. **13** is a diagram (tenth) illustrating the example of the method of manufacturing the solid-state imaging device according to the first embodiment of the present invention;

FIG. **14** is a diagram illustrating a solid-state imaging device according to a second embodiment of the present invention;

FIG. **15** is a diagram illustrating a solid-state imaging device according to a third embodiment of the present invention;

FIG. **16** is a schematic diagram illustrating a main part of a solid-state imaging device according to a fourth embodiment of the present invention;

FIG. **17** is a diagram (first) illustrating the example of the method of manufacturing the solid-state imaging device according to the fourth embodiment of the present invention;

FIG. **18** is a diagram (second) illustrating the example of the method of manufacturing the solid-state imaging device according to the fourth embodiment of the present invention;

FIG. **19** is a diagram (third) illustrating the example of the method of manufacturing the solid-state imaging device according to the fourth embodiment of the present invention;

FIG. **20** is a diagram (fourth) illustrating the example of the method of manufacturing the solid-state imaging device according to the fourth embodiment of the present invention;

FIG. **21** is a diagram (fifth) illustrating the example of the method of manufacturing the solid-state imaging device according to the fourth embodiment of the present invention;

FIG. **22** is a schematic diagram illustrating a main part of a semiconductor device according to a fifth embodiment of the present invention;

FIG. **23** is a diagram (first) illustrating the example of the method of manufacturing the semiconductor device according to the fifth embodiment of the present invention;

FIG. **24** is a diagram (second) illustrating the example of the method of manufacturing the semiconductor device according to the fifth embodiment of the present invention;

FIG. **25** is a diagram (third) illustrating the example of the method of manufacturing the semiconductor device according to the fifth embodiment of the present invention;

FIG. **26** is a diagram (fourth) illustrating the example of the method of manufacturing the semiconductor device according to the fifth embodiment of the present invention;

FIG. **27** is a diagram (fifth) illustrating the example of the method of manufacturing the semiconductor device according to the fifth embodiment of the present invention;

FIG. **28** is a diagram (sixth) illustrating the example of the method of manufacturing the semiconductor device according to the fifth embodiment of the present invention; and

FIG. **29** is a schematic diagram illustrating the configuration of an electronic apparatus according to a sixth embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereinafter, the best mode for carrying out the present invention will be described as embodiments thereof. The embodiments will be described in the following order:

1. Example of the schematic configuration of MOS solid-state imaging device;
2. First embodiment (an example of the configuration of a solid-state imaging device and the method of manufacturing the solid-state imaging device);
3. Second embodiment (an example of the configuration of a solid-state imaging device);
4. Third embodiment (an example of the configuration of a solid-state imaging device);
5. Fourth embodiment (an example of the configuration of a solid-state imaging apparatus and the method of manufacturing the solid-state imaging device);
6. Fifth embodiment (an example of the configuration of a semiconductor device and the method of manufacturing the solid-state imaging device); and
7. Sixth embodiment (an example of an electronic apparatus).

1. Example of the Schematic Configuration of MOS Solid-State Imaging Device

FIG. **1** is a schematic diagram illustrating an exemplary configuration of a MOS solid-state imaging device, which can be applied to a semiconductor device of any embodiment of the present invention. The configuration of the MOS solid-state imaging device illustrated in FIG. **1** is also applied to a solid-state imaging device according to each embodiment of the present invention. As shown in FIG. **1**, the solid-state imaging device **1** includes a semiconductor substrate **11**; a pixel section (so-called pixel array) **3**, where a plurality of pixels **2** with photoelectric conversion parts are regularly placed on the silicon substrate **11**, and a peripheral circuit section. Each pixel (i.e., unit pixel) **2** includes a photoelectric conversion part such as a photodiode and a plurality of pixel transistors (so-called MOS transistors). The plurality of pixel transistors may include, for example, three transistors: a transfer transistor, a reset transistor, and an amplification transistor. Alternatively, the plurality of pixel transistors may further include a selection transistor, thus including four transistors. The equivalent circuits of the unit pixel is the same as one typically used, so that the details thereof will be omitted in the following description. The pixel **2** may be one unit pixel. Alternatively, the pixel **2** may have a shared pixel structure. The shared pixel structure includes a plurality of photodiodes, a plurality of transfer transistors, one shared floating diffusion, and each of shared other pixel transistors. In other words, the shared pixel structure includes photodiodes and transfer transistors, which constitute the plurality of unit pixels, and each of other shred pixel transistors.

The peripheral circuit section includes a vertical drive circuit **4**, a column signal processing circuit **5**, a horizontal drive circuit **6**, an output circuit **7**, a control circuit **8**, and so on.

The control circuit **8** receives an input clock and data for the instruction of an operation mode and so on and outputs information such as the internal information of the solid-state imaging device. In other words, the control circuit **8** generates signals, such as a clock signal and a control signal to be referenced for driving the vertical drive circuit **4**, the column signal processing circuit **5**, the horizontal drive circuit **6**, and so on. Then, the control unit **8** inputs these signals to the vertical drive circuit **4**, the column signal processing circuit **5**, the horizontal drive circuit **6**, and so on.

The vertical drive circuit **4** includes a shift register or the like and drives pixels on a line by selecting a pixel-driving line and supplying a pulse for driving pixels to a selected pixel line-at-a-time. In other words, the vertical drive circuit **4** sequentially performs selective scanning of pixels **2** of the pixel region **3** line-at-a-time in the vertical direction. Then, the vertical drive circuit **4** supplies a pixel signal to the column signal processing circuit **5**. Here, the pixel signal is based on a signal electric charge generated according to the amount of light received on the photoelectric transducer (e.g., photodiode) of each pixel **2** through a vertical signal line **9**.

In this embodiment, for example, the column signal processing circuit **5** may be provided for each column of the pixels **2** and carries out signal processing, such as noise removal, of a signal output from each of the pixels **2** on one line. In other words, the column signal processing circuit **5** performs CDS (correlated double sampling) for removal of a fixed pattern noise specific to the pixel **2** and signal processing such as signal amplification and AD (analogue-to-digital) conversion. The output stage of the column signal processing circuit **5** is connected to a horizontal selection switch (not shown) which is located between the output stage and a horizontal signal line **10**.

The horizontal drive circuit **6**, which is constructed of a shift resister or the like, sequentially outputs horizontal scanning pulses, selecting the respective column signal processing circuits **5** in order to output pixel signals thereof to the horizontal signal line **10**.

The output circuit **7** carries out signal processing of signals sequentially supplied from the respective column signal processing circuits **5** through the horizontal signal line **10** and then outputs the processed signals.

Specifically, for example, the output circuit **7** may only perform buffering or may perform black level adjustment, column variation compensation, various digital signal processing, and so on. An input/output terminal **12** carries out an exchange of signals between the device and the outside.

FIGS. **2**A to **2**C are schematic diagrams illustrating a fundamental configuration of a MOS solid-state imaging device according to an embodiment of the present invention. First, a typical MOS solid-state imaging device **151** will be described with reference to FIG. **2**A. The typical MOS solid-state imaging device **151** includes a pixel region **153**, a control circuit **154**, and a logic circuit **155** for signal processing, which are mounted on a single semiconductor chip **152**. In general, an image sensor **156** includes the pixel region **153** and the control circuit **154**. As shown in FIG. **2**B, on the other hand, a MOS solid-state imaging device **21** according to the embodiment of the present invention includes a pixel region **23** and a control circuit (control region) **124** mounted on a first semiconductor chip section **22** and a logic circuit **25** including a signal processing circuit for signal processing mounted on a second semiconductor chip section **26**. The first semiconductor chip section **22** and the second semiconductor chip section **26** are electrically connected to each other to form a single semiconductor chip to provide the MOS solid-state imaging device **21**. As shown in FIG. **2**C, in a MOS solid-state imaging device **27** according to another embodiment of the present invention, a pixel region **23** is mounted on a first semiconductor chip section **22**. Also, a control circuit **24** and a logic circuit **25** including signal processing circuit are mounted on a second semiconductor chip section **26**. The first semiconductor chip section **22** and the second semiconductor chip section **26** are electrically connected to each other to form a single semiconductor chip to provide the MOS solid-state imaging device **27**.

The features of the MOS solid-state imaging devices according to the above embodiments are found in their manufacturing methods and their configurations based on such methods as described later.

2. First Embodiment

Example of Configuration of Solid-State Imaging Device and Example of Method of Manufacturing the Solid-State Imaging Device

Referring now to FIG. **3** and FIGS. **4** to **13**, a semiconductor device (i.e., a MOS solid-state imaging device) and a method of manufacturing the solid-state imaging device will be described.

In the first embodiment, first, as shown in FIG. **4**, a half-finished image sensor, or an pixel array (hereinafter, also referred to as a pixel region) **23**, and a control circuit (control region) **24** are formed on a region to be provided as each microchip part of a first semiconductor wafer (hereinafter, also referred to as a semiconductor substrate) **31**. In other words, a photodiode (PD), which acts as a photoelectric conversion part of each pixel, is formed on a region to be formed as each microchip part of the semiconductor substrate (for example, a silicon substrate) **31**. Then, a source/drain region **33** of each pixel transistor is formed on a semiconductor well region **32** in the semiconductor substrate **31**. The semiconductor well region **32** is formed by introduction of first-conductivity type (e.g., p-type) impurities and the source/drain region **33** is formed by introduction of second-conductivity type (e.g., n-type) impurities. The photodiode (PD) and the source/drain region **33** of each pixel transistor are formed by ion implantation from the surface of the substrate **31**.

The photodiode (PD) includes an n-type semiconductor region **34** and a p-type semiconductor region **35**. Here, the p-type semiconductor region **35** is on the surface side of the substrate **31**. On the surface of the substrate **31** forming the pixel, a gate electrode **36** is formed on a gate insulating layer. Pixel transistors Tr**1** and Tr**2** are formed by the gate electrode **36** and the paired source/drain regions **33**. In FIG. **4**, for simplifying the explanation, two pixel transistors Tr**1** and Tr**2** are illustrated on behalf of a plurality of pixel transistors. The pixel transistor Tr**1** adjacent to the photodiode (PD) is equivalent to a transfer transistor and the source/drain region thereof is equivalent to a floating diffusion (FD). The unit pixels **30** are separated from one another by isolation regions **38** respectively. The isolation regions **38** are formed by LOCOS (Local Oxidation of Silicon), STI (Shallow Trench Isolation), or using an impurity diffusion layer having a conductivity type different from that of a diffusion layer formed as a node. LOCOS is a process where the semiconductor substrate **31** is oxidized to form a silicon oxide layer. STI is a process of providing trenches in the semiconductor substrate **31** and filling the trenches with a silicon oxide layer.

On the other hand, on the control circuit (control region) **24**, MOS transistors that constitute a control circuit are formed on the semiconductor substrate **31**. FIG. **4** illustrates the MOS transistors that constitute the control circuit (control region) **24**, as represented by MOS transistors Tr**3** and Tr**4**. Each of the MOS transistors Tr**3** and Tr**4** includes an n-type source/drain region **33** and a gate electrode **36** on a gate insulating layer.

Subsequently, a first insulating interlayer **39** is formed on the surface of the semiconductor substrate **31** and connection holes are then formed in the insulating interlayer **39**, followed by the formation of connection conductors **44** connecting to the desired transistors through the connection holes. The formation of the connection conductors **44** with different heights may be performed by stacking a first insulation thin layer **43***a*, such as a silicon dioxide film, and a second insulation thin layer **43***b*, such as a silicon nitride film, on the entire surface of the semiconductor substrate **31** including the upper surfaces of the respective transistors. Here, the second insulation thin layer **43***b* acts as an etching stopper in an etching process for providing a contact hole connected to the gate electrode **36** and source/drain region

33 and afterward filled with a connection conductor **44**. The first insulating interlayer **39** is formed on the second insulation thin layer **43***b*. Then, the connection holes with different depths are selectively formed in the first insulating interlayer **39**, reaching to the second insulation thin layer **43***b* provided as the etching stopper. Subsequently, additional connection holes are formed in the respective portions of the first and second insulation thin layers **43***a* and **43***b* having the same film thickness by selective etching so that these additional connection holes can be communicated with the forgoing connection holes, respectively. After that, the connection conductor **44** is embedded in each of the resulting connection holes. In the case where the contact hole is provided without using the etching stopper, the second insulation thin layer **43***b* may not be formed.

Next, a plurality of layers is formed in the insulating interlayer **39** so that the layers can be connected to the respective connection conductors **44**. In this example, but not limited to, a multi-wiring layer **41** is formed by the formation of three metal wiring layers **40**. The metal wiring layer **40** is formed of a copper (CU) wiring line. In general, each copper wiring line is covered with a barrier metal layer that prevents Cu from dispersing. Thus, a cap layer, a so-called protective layer **42**, of the copper wiring line **40** is formed on the multi-wiring layer **41**. In the aforementioned steps, the first semiconductor substrate **31** having the half-finished pixel region **23** and control circuit **24** is formed.

On the other hand, as shown in FIG. **5**, a half-finished logic circuit **25** including a signal processing circuit for signal processing is formed on a region to be provided as each of microchip parts on a second semiconductor substrate (semiconductor wafer) **45**. Furthermore, on a p-type semiconductor well region **46** on the surface side of the second semiconductor substrate (for example, the silicon wafer) **45**, a plurality of MOS transistors, which forms a logic circuit, is formed so that the MOS transistors can be separated from each other by isolation regions **50**, respectively. Here, the plurality of the MOS transistors is represented by MOS transistors Tr**6**, Tr**7**, and Tr**8**. Each of the MOS transistors Tr**6**, Tr**7**, and Tr**8** is formed using a pair of n-type source/drain regions **47** and a gate electrode **48** formed on a gate insulation layer. The logic circuit **25** can be constructed of CMOS transistors.

Subsequently, a first insulating interlayer **49** is formed on the surface of the semiconductor substrate **45** and connection holes are then formed in the insulating interlayer **49**, followed by the formation of connection conductors **54** connecting to the desired transistors through the respective connection holes. The formation of the connection conductors **54** with different heights may be performed by stacking a first insulation thin layer **43***a*, such as a silicon dioxide film, and a second insulation thin layer **43***b*, such as a silicon nitride film, are stacked on the entire surface of the semiconductor substrate **45** including the upper surfaces of the respective transistors. Here, the second insulation thin layer **43***b* acts as an etching stopper.

The first insulating interlayer **49** is formed on the second insulation thin layer **43***b*. Then, the connection holes with different depths are selectively formed in the first insulating interlayer **49**, reaching to the second insulation thin layer **43***b* provided as an etching stopper. Subsequently, additional connection holes are formed in the respective portions of the first and second insulation thin layers **43***a* and **43***b* having the same film thickness by selective etching so that these additional connection holes can be communicated with the forgoing connection holes, respectively. After that, a connection conductor **44** is embedded in each of the resulting connection holes.

On the other hand, at a desired position on the area to be provided as each of microchip parts, a connection hole is formed from the surface of the first insulating interlayer **49** to a predetermined depth position in the semiconductor substrate **45**. Then, a connection conductor **51** for extraction electrode is embedded in the resulting connection hole. The connection conductor **51** may be made of copper (Cu), tungsten (W), polysilicon, or the like. Before embedding the connection conductor **51**, an insulation layer **52** is formed on the inner wall surface of the connection hole to insulate the connection conductor **51** from the semiconductor substrate **45**.

Next, a plurality of layers is formed through the insulating interlayer **49** so that they can be connected to the respective connection conductors **54** and the extraction connection conductor **51**. In this example, but not limited to, a multi-wiring layer **55** is formed by the formation of three metal wiring layers **53**. The metal wiring layer **53** is formed of a copper (CU) wiring line. In a manner similar to one described above, a cap layer, a so-called protective layer **56**, of the copper wiring line **53** is formed on the multi-wiring layer **49**. In the aforementioned steps, the first semiconductor substrate **45** having the half-finished logic circuit **25** is formed.

Next, as shown in FIG. **6**, the first semiconductor substrate **31** and the second semiconductor substrate **45** are bonded together so that their respective multi-wiring layers **41** and **55** can be faced with each other. The bonding may be performed using plasma bonding, an adhesive agent, or the like. In the case of the plasma bonding, as shown in FIG. **7**, a layer **57**, such as a plasma TEOS film, a plasma SiN film, a SiON film (block film), or a SiC film, is formed on the bonding surface of each of the first and second semiconductor wafers **31** and **45**. The bonding surfaces with the layers **57** are subjected to a plasma treatment and then placed over one another, followed by being bonded by an annealing treatment. Such bonding processing is preferably performed using a low-temperature process at 400° C. or less. Such a range of the temperature will not affect on the bonding processing, wiring, or the like. In the case of the adhesive agent, as shown in FIG. **8**, an adhesive layer **58** is formed on one of the bonding surfaces of the first and second semiconductor wafers **31** and **45** and both the wafers are then placed over one another through the adhesive layer **58**. In this example, the bonding is performed using the plasma bonding.

Next, as shown in FIG. **9**, grinding and polishing are performed from the back side **31***b* of the first semiconductor substrate **31** to make the first semiconductor substrate **31** into a thin film. The thin-film processing is performed to close in the photodiode (PD). After the thin-film processing, a p-type semiconductor layer for dark current control is formed on the back side of the photodiode (PD).

For example, the semiconductor substrate **31** with a thickness of about 600 μm may be thinned to about 1 to 10 μm, preferably about 1 to 5 μm. The thin-film processing has been commonly performed using a separately prepared supporting substrate for bonding them together. In the embodiment, however, the second semiconductor substrate **45** on which the logic circuit **25** is formed is also used as a supporting substrate to make the first semiconductor substrate **31** into a thin film. After the thin-film processing, an insulating interlayer **59**, such as a silicon dioxide film, is formed on the backside of the substrate **31**. In the back-

illuminated solid-state imaging device, the back side **31***b* of the first semiconductor substrate **31** serves as a light-incident surface.

Next, as shown in FIG. **10**, a connection through-hole **61** is formed in the thin-filmed first semiconductor substrate **31** at a desired position of a region to be provided as each microchip part. The connection through-hole **61** extends from the back side **31***b* to the uppermost layer of the wiring **53** of the second semiconductor substrate **45** through the first semiconductor substrate **31**. Simultaneously, a connection hole **62** is formed near the connection through-hole **61** in the first semiconductor substrate **31**, extending from the back side **31***b* to the first layer wiring **40** on the first semiconductor substrate **31**. Each of the connection through-hole **61** and connection hole **62** may have a contact area of 1 to 5 μm in diameter. Since the connection through-hole **61** and the connection hole **62** are formed after making the first semiconductor substrate **31** into a thin film, these holes **61** and **62** can be formed as micropores with a smaller aspect ratio. For example, each of the connection through-hole **61** and the connection hole **62** may have a contact depth of about 5 to 15 μm. Subsequently, an insulating layer **63** for electric insulation with the semiconductor substrate **31** is formed on the inner wall surface of each of the connection through-hole **61** and the connection hole **62**.

At this time, the process for manufacturing a pixel array is incomplete because the steps of forming an on-chip color filter and an on-chip microlens are still untouched. In addition, both the connection holes **61** and **62** may be processed and formed in the extension of the typical wafer process. In the case of the logic circuit, the process up to the uppermost layer wiring **53** suitable for a circuit technology has been completed, but the whole manufacturing process has not been completed. Therefore, a decrease in manufacturing cost can be attained.

Next, as shown in FIG. **11**, a through-connection conductor **64** and a connection conductor **65** are embedded in the connection through-hole **61** and the connection hole **62**, respectively. Each of the through-connection conductor **64** and the connection conductor **65** may be made of a metal, such as copper (Cu) or tungsten (W). After that, an insulating protective layer **66** is formed on the entire back side of the first semiconductor substrate **31**. The insulating protective layer **66** may be made of, for example, a SiCN film, a plasma silicon nitride film, or a SiC film.

Next, as shown in FIG. **12**, a light-shielding layer **67** is formed on a region to be shielded from light. In this figure, the light-shielding layer **67** is formed above the control circuit **24**. Alternatively, it may be also formed above other pixel transistors. The light-shielding layer **67** may be a metal layer such as a tungsten film. The light-shielding layer **67** is electrically connected to the semiconductor well region **32** having a ground potential and prevented from being in an electrically floating state. In addition, since the light-shielding layer **67** electrically connected to the semiconductor well region **32** is provided with the ground potential, the semiconductor well region **32** is prevented from being in an electrically floating state. A passivation layer **68** is formed on the whole surface of the light-shielding layer **67** so that it entirely covers the light-shielding layer **67**. The passivation layer **68** may be, for example, a plasma silicon nitride film or a CVD-SiV film. Subsequently, connection holes **69** are formed in the portions of the passivation layer **68** and the insulating protective layer **66**, which correspond to the through-connection conductor **64** and the connection conductor **65**, respectively. Then, connection wiring **72**, an aluminum film, is formed on a barrier metal layer **71** on the connection hole **69**. The barrier metal layer **71** is formed, for example, by a stacked film of Ti (downside)/TiN (upside). The connection wiring **72** is connected to both the through-connection conductor **64** and the connection conductor **65** through the barrier metal layer **71**. The connection wiring **72** is used for connecting the pixel region **23** and the control circuit **24** to the logic circuit **25** and serves as an extraction electrode from the upper side, or serves as a so-called electrode pad. Hereinafter, the connection wiring **72** is also referred to as an electrode pad.

Therefore, an image sensor constructed of the image region **23** and the control circuit **24** formed on the first semiconductor substrate **31** is electrically connected to the logic circuit **25** formed on the second semiconductor substrate **45** through the connection conductor **65**, the electrode pad **72**, and the through-connection conductor **64**.

After that, a planarizing layer **73** is formed on these structural components.

Next, as shown in FIG. **13**, red (R), green (G), and blue (B) on-chip color filters **74** are formed on the planarizing layer **73**, corresponding to the respective pixels, and on-chip microlenses **75** are then formed on the respective color filters **74**. In other words, both the on-chip color filters **74** and the on-chip microlenses **75** are formed so that each of them corresponds to each unit pixel of the pixel array.

Here, to facilitate understanding of the embodiments of the present invention, FIG. **12** is an enlarged cross-sectional diagram illustrating the configuration of the substrate, but the on-chip color filters **74** and on-chip microlenses **75** are not shown in the figure. Thus, the pitch sizes of the on-chip color filters **74** and the on-chip microlenses **75** are reduced with reference to the pitch size of the unit pixels.

Next, although not illustrated in FIG. **13**, the electrode pad **72** is exposed by selectively removing a lens material layer **75***a* and the planarizing layer **73**. On the other hand, on the side of the second semiconductor substrate **45**, the surface of the substrate **45** is ground and polished to expose the surface of the connection conductor **51** that serves as an extraction electrode. After forming a passivation layer **76** on the exposed surface of the connection conductor **51** of the second semiconductor substrate **45**, an opening **77** corresponding to the connection conductor **51** is formed in the passivation layer **76**. A spherical electrode bump **78** is formed so that it can be electrically connected to the connection conductor **51** through the opening **77** (see FIG. **3**). In the first semiconductor substrate **31**, therefore, both the pixel region **23** and the control circuit **24** are brought into a finished product state. In the second semiconductor substrate **45**, the logic circuit **25** is brought into a finished product state.

Subsequently, the resulting product is divided into the respective microchips, thereby obtaining a desired back-illuminated solid-state imaging device **79** as shown in FIG. **3**.

In the solid-state imaging device **79** of the first embodiment, if the electrode pad **72** is used, the device **79** can be electrically connected to external wiring by wire bonding to the electrode pad **72**. If the electrode bump **78** is used, the device **78** can be electrically connected to external wiring by face-down bonding. The user may choose one of the electrode pad **72** and the electrode bump **78** according to user's wishes.

In the first embodiment, the sold-state imaging device can be inspected using the electrode pad **72** with respect to the semiconductor wafers. In addition, the inspection includes two inspection steps, one in the state of wafer and the other in the final module state after cutting into chips.

According to the solid-state imaging device **79** and the manufacturing method thereof according to the first embodiment of the present invention, both the pixel region **23** and the control circuit **24** are formed on the microchip part from the first semiconductor substrate **31**. In addition, the logic circuit **25** for signal processing is formed on the microchip part from the second semiconductor substrate **45**.

In this way, the functions of the pixel array and the functions of the logic circuit are assigned on different microchip parts, so that suitable processing technologies can be individually applied to the pixel array and the logic circuit. Therefore, the performances of the pixel array and the logic circuit can be efficiently exerted. Thus, a high-performance solid-state imaging device can be provided.

In the case of the configuration of the device shown in FIG. **2**C, only the pixel region **23** for receiving incident light may be formed on the side of the semiconductor chip section **22**. Thus, the control circuit **24** and the logic circuit **25** can be separately formed on the semiconductor chip section **26**. Therefore, processing technologies suitable for the respective functional microchips can be independently selected while the surface area of the product module can be also reduced.

Since the pixel array and the logic circuit can be mounted in combination using the typical wafer-processing technology, the production of the device can be also facilitated.

The first semiconductor substrate **31** having the pixel region **23** and the control circuit **24** in a half-finished state and the second semiconductor substrate **45** having the logic circuit **25** in a half-finished state are attached together, followed by making the first semiconductor substrate **31** into a thin film. In other words, the second semiconductor substrate **45** may be used as a supporting substrate for making the first semiconductor substrate **31** into a thin film. Therefore, it becomes possible to reduce the number of structural members and reduce the number of manufacturing steps. Furthermore, since the connection through-hole is formed during the thin-film formation, the aspect ratio of the hole can be reduced and the formation of connection holes can be performed with high accuracy. Furthermore, the through-connection conductor **61** and the connection conductor **62** are embedded into the connection through-hole and the connection hole of small aspect ratios. Therefore, the metal materials which can be used may include those with low coatability, such as copper (Cu), as well as those with high coatability, such as tungsten (W). In other words, the connection conductor materials hardly impose restrictions on the device. Thus, the pixel region and the control circuit can be electrically connected to the logic circuit with high precision. Therefore, it becomes possible to manufacture a high performance solid-state imaging device with high mass productivity while keeping production costs down.

3. Second Embodiment

Example of Configuration of Solid-State Imaging Device

Referring now to FIG. **14**, a solid-state imaging device (i.e., a MOS solid-state imaging device) according to a second embodiment of the present invention will be described. The solid-state imaging device **81** according to the second embodiment of the present invention is constructed in a manner similar to that of the first embodiment, except for the followings: In this embodiment, only the electrode pad **72** on the side of the first semiconductor substrate **31** is formed, while the connection conductor **51**, the insulating layer **52**, and the electrode bump **78** on the side of the second semiconductor substrate **45** are omitted. In addition, a passivation layer **76** is formed on the back side of the second semiconductor substrate **45**. Other structural components are the same as those described in the first embodiment. Therefore, the corresponding structural components are designated by the same reference numerals as those in FIG. **3** to omit the duplicated explanations thereof. In addition, the manufacture of the solid-stage imaging device **81** is performed by the same method as that of the first embodiment shown in FIG. **4** to FIG. **13**, except for the followings: The method of the present embodiment does not include the steps of forming the connection conductor **51**, the insulating layer **52**, and the electrode bump **78** as well as the formation of the connection hole desired for forming the connection conductor **51**.

The solid-state imaging device of the second embodiment exerts the same advantageous effects as those of the first embodiment because of having the similar configuration to that of the first embodiment except for the electrode bump **78**. In the second embodiment, the connection hole, the insulating layer **62**, and the connection conductor **61** are not formed on the side of the logic circuit in advance. Thus, lower costs can be expected.

4. Third Embodiment

Example of Configuration of Solid-State Imaging Device

Referring now to FIG. **15**, a semiconductor device (i.e., a MOS solid-state imaging device) according to a third embodiment of the present invention will be described.

In the solid-state imaging device **83** of the third embodiment, the pixel region **23** and the control circuit **24** formed on the side of the first semiconductor substrate **31** are electrically connected to the logic circuit **25** on the side of the second semiconductor substrate **45** through one through-connection conductor **84** formed in the first semiconductor substrate **31**.

In other words, a connection through-hole **85** is formed such that it extends from the back side **31***b* of the first semiconductor substrate to the uppermost layer of the wiring **53** of the second semiconductor substrate **45** through the first semiconductor substrate **31**. In addition, part of the connection through-hole **85** reaches to the uppermost layer of the wiring **40** of the first semiconductor substrate **31**. After the formation of the insulating layer **63** on the inner wall surface of the connection through-hole **85**, the through-connection conductor **84** is embedded in the connection through-hole **85** to connect the wiring **40** on the side of the pixel region **23** and the control circuit **24** to the wiring **53** on the side of the logic circuit **25**. In the above first embodiment, the connection conductor **65** is connected to the first layer of the wiring **40** while the connection conductor **65** serves as a connection end. However, in the second embodiment, the through-connection conductor **84** is connected to the uppermost layer of the wiring **40**. The respective layers of the wiring **40** are connected to one another so that the uppermost layer thereof connected to the through-connection conductor **84** will serve as a connection end.

In the present embodiment, the pixel region **23** and the control circuit **24** are connected to the logic circuit **25** through one through-connection conductor **84**. Thus, an electrode pad **72** that serves as the uppermost layer of the connection wiring as described in the first embodiment is not formed.

Other structural components are the same as those described in the first embodiment. Therefore, the corresponding structural components are designated by the same reference numerals as those in FIG. **3** to omit the duplicated

explanations thereof. In addition, the manufacture of the solid-stage imaging device **83** is performed by the same method as that of the first embodiment shown in FIG. **4** to FIG. **13**, except for the steps of forming the connection conductor **65** and the electric pad **72** and the steps of selectively etching the lens material layer **75***a* and the planarizing layer **73**.

In the third embodiment, the sold-state imaging device can be inspected using the electrode pump from the connection conductor **51**.

According to the solid-state imaging device **83** of the third embodiment, the pixel region **23** and the control circuit **24** are electrically connected to the logic circuit **25** through one through-connection conductor **84**. In addition, the electrode pad **72** is omitted. Thus, the configuration of the device is simplified compared with that of the first embodiment. Furthermore, the number of the manufacturing steps can be reduced. Therefore, a further reduction in manufacturing costs can be attained. In addition, the same effects as those described in the first embodiment can be exerted.

5. Fourth Embodiment

Example of Configuration of Solid-State Imaging Device and Example of Manufacturing Method Thereof

Referring now to FIG. **16** and FIGS. **17** to **21**, a semiconductor device (i.e., a MOS solid-state imaging device) according to a fourth embodiment of the present invention and a manufacturing method thereof will be described.

In the fourth embodiment, first, as shown in FIG. **17**, a half-finished image sensor, or a pixel region **23**, and a control circuit **24** are formed on a region to be provided as each microchip part of a first semiconductor substrate **31**. The manufacturing steps in the present embodiment are the same as those illustrated in FIG. **4** of the aforementioned first embodiment. The same reference numerals as in FIG. **4** are used to denote the corresponding or similar portions. Thus, redundant descriptions will be omitted. However, in the present embodiment, the multi-wiring layer **41** is formed on the first semiconductor substrate **31**. However, the process is completed at the time of forming the uppermost layer of the wiring **40**. In other words, the process is completed when the uppermost layer of the wiring **40** is exposed. The protective layer **42** shown in FIG. **4** is not formed on the exposed layer.

On the other hand, as shown in FIG. **18**, a half-finished logic circuit **25** for signal processing circuit is formed on a region to be provided as each of microchip parts on a second semiconductor substrate **45**. The manufacturing steps in the present embodiment are the same as those illustrated in FIG. **5** of the aforementioned first embodiment. The same reference numerals as in FIG. **5** are used to denote the corresponding structural components. Thus, redundant descriptions will be omitted. However, in the present embodiment, the multi-wiring layer **55** is formed on the second semiconductor substrate **45** and the process is completed at the time of forming the uppermost layer of the wiring **53**. In other words, the process is completed when the uppermost layer of the wiring **53** is exposed. The protective layer **56** shown in FIG. **5** is not formed on the exposed layer.

Next, as shown in FIG. **19**, the first semiconductor substrate **31** and the second semiconductor substrate **45** are bonded together so that their respective multi-wiring layers **41** and **55** can be faced with each other, while their wiring **40** and **53** are connected to each other and their insulating interlayers **39** and **49** are connected to each other.

In this bonding process, the wiring **40** and **53** are copper (Cu) wiring and the insulating interlayers **39** and **40** are silicon dioxide films. Furthermore, both the semiconductor substrates **31** and **45** are placed over one another and heated while receiving a predetermined load while their respective Cu wirings **40** and **50** are directly touched with each other. Simultaneously, the insulating interlayers **39** and **49** may be connected with each other. The heating temperature at this time is, for example, about 300° C., which prevents Cu wiring from being deteriorated.

Next, as shown in FIG. **20**, grinding and polishing are performed from the back side **31***b* of the first semiconductor substrate **31** to thin the first semiconductor substrate **31**. The thin-film processing is performed to close in the photodiode (PD). After the thin-film formation, an insulating interlayer **59**, such as a silicon dioxide film, is formed on the backside of the substrate **31**. Subsequently, a connection hole **88** is formed in the thin-filmed first semiconductor substrate **31**. The connection hole **88** is located at a desired position in a region to be provided as each microchip part and extends from the back side **31***b* of the substrate **31** to the first layer of the wiring **40**. An insulating layer **63** is formed on the inner wall surface of the connection hole **88**. Then, the connection hole **62** and the connection through-hole **61** are formed. The connection trough-hole **61** reaches to the uppermost layer of the wiring **53** on the side of the second semiconductor substrate **45**. Next, a through-connection conductor **64** and a connection conductor **65** are embedded in the connection through-hole **61** and the connection hole **62**, respectively. After that, an insulating protective layer **66** is formed on the entire surface on the back side **31***b* of the first semiconductor substrate **31**. The manufacturing steps illustrated in FIG. **20** are the same as those illustrated in FIGS. **9** to **11**. The same reference numerals as in FIGS. **9** to **11** are used to denote the corresponding structural components. Thus, redundant descriptions will be omitted.

Next, as shown in FIG. **21**, an electronic pad **72** and a light-shielding layer **67** are formed on the side of the first semiconductor substrate **31**. Here, the electric pad **72** is connected to the connection conductor **62** and the through-connection conductor **61**. Furthermore, a planarizing layer **73**, an on-chip color filter **74**, and an on-chip microlens **74** are formed on the same side. On the other hand, on the side of the second semiconductor substrate **45**, the back side of the substrate is ground and polished to expose the connection conductor **51**. A passivation layer **76** is formed and an electrode bump **78** is then formed on the connection conductor **51** (see FIG. **16**). The manufacturing steps illustrated in FIG. **21** are the same as those illustrated in FIG. **13** as described above. The same reference numerals as in FIG. **13** are used to denote the corresponding structural components. Thus, redundant descriptions will be omitted.

Subsequently, the resulting product is divided into the respective microchips, thereby obtaining a desired back-illuminated solid-state imaging device **91** as shown in FIG. **16**. In this embodiment, the configuration of the device illustrated in FIG. **2**B is employed. Alternatively, the configuration of the device illustrated in FIG. **2**C may be employed.

According to the solid-state imaging device **91** and the manufacturing method thereof according to the fourth embodiment of the present invention, in the step of combining the first semiconductor substrate **31** and the second semiconductor substrate **45**, simultaneously, the wiring **40** and the wiring **53** are directly connected to each other. Thus, the pixel region **23** and the control circuit **24** are electrically connected to the logic circuit **25**, completing their electrical

connection. Therefore, the number of the manufacturing steps can be further reduced and a further reduction in manufacturing costs can be also attained. In addition, the device of the present embodiment exerts the same advantageous effects as those described in the first embodiment.

6. Fifth Embodiment

Example of Configuration of Semiconductor Device and Example of Manufacturing Method Thereof

Referring now to FIG. **22** and FIGS. **23** to **28**, a semiconductor device and a manufacturing method thereof in accordance with the fifth embodiment of the present invention will be described. The semiconductor device of the present embodiment is a semiconductor device on which a first semiconductor integrated circuit and a second semiconductor integrated circuit are mounted in combination.

In the fifth embodiment, first, as shown in FIG. **23**,

a half-finished first semiconductor integrated circuit (logic circuit **102** in this example) is formed on a region to be provided as each of microchip parts on a first semiconductor substrate (semiconductor wafer) **101**. In other words, on the region to be provided as each of microchip parts on the semiconductor well region **104** formed in the semiconductor substrate (e.g., silicon substrate) **103**, a plurality of MOS transistors Tr**11**, Tr**12**, and Tr**13** are formed. Each of the MOS transistors Tr**11** to Tr**13** includes a pair of source/drain regions **105** and a gate electrode **106** with a gate insulating layer placed therebetween. The MOS transistors Tr**11** to Tr**13** are separated from one another by the presence of isolation regions **107**, respectively. Here, but not limited to, the MOS transistors are represented by MOS transistors Tr**11** to Tr**13**. The logic circuit **102** includes CMOS transistors. Therefore, these MOS transistors may be n-channel MOS transistors or p-channel MOS transistors. Thus, when the n-channel MOS transistor is formed, an n-type source/drain region is formed on a p-type semiconductor well region. When a p-channel MOS transistor is formed, a p-type source/drain region is formed in an n-type semiconductor well region.

Furthermore, for example, the first semiconductor integrated circuit may be a semiconductor memory circuit instead of the logic circuit **102**. In this case, the logic circuit to be used as a second semiconductor integrated circuit is subjected to the signal processing of the semiconductor memory circuit.

Next, a plurality of layers are formed on the conductive substrate **103** through an interlayer insulating layer **108**. In this example, a multi-wiring layer **111** is formed by laminated three metal wiring layers **109**. For example, the metal wiring **109** may be made of copper, or Cu wiring. In addition, the respective MOS transistors Tr**11** to Tr**13** are connected to one another through the desired first layer of the wiring **109** and a connection conductor **112**. Furthermore, three layers of the wiring **109** are connected to one another through the connection conductor. A cap layer, a so-called protective layer **114** which prevents the copper wiring **109** from being dispersed, is formed on the multi-wiring layer **113**.

On the other hand, as shown in FIG. **24**, a half-finished second semiconductor integrated circuit, a logic circuit **117** is formed in a region to be provided as each microchip part of the second semiconductor substrate (semiconductor wafer) **116**. In other words, as shown in FIG. **20**, on the region to be provided as each of microchip parts on the semiconductor well region **119** formed in the semiconductor substrate (e.g., silicon substrate) **118**, a plurality of n-channel MOS transistors Tr**21**, Tr**22**, and Tr**23** are formed. Each of the MOS transistors Tr**21** to Tr**23** includes a pair of source/drain regions **121** and a gate electrode **122** with a gate insulating layer placed therebetween. The MOS transistors Tr**21** to Tr**23** are separated from one another by the presence of isolation regions **123**, respectively. Here, but not limited to, the MOS transistors are represented by MOS transistors Tr**21** to Tr**23**. The logic circuit **117** includes CMOS transistors. Therefore, these MOS transistors may be n-channel MOS transistors or p-channel MOS transistors. Thus, when the re-channel MOS transistor is formed, an n-type source/drain region is formed on a p-type semiconductor well region. When a p-channel MOS transistor is formed, a p-type source/drain region is formed in an n-type semiconductor well region.

Next, a plurality of layers is formed on the conductive substrate **118** through an interlayer insulating layer **124**. In this example, a multi-wiring layer **126** is formed by laminated three metal wiring layers **125**. For example, the metal wiring **125** may be made of copper, or Cu wiring. In addition, the respective MOS transistors Tr**21** to Tr**23** are connected to one another through the desired first layer of the wiring **125** and a connection conductor **112**. Furthermore, three layers of the wiring **125** are connected to one another through the connection conductor.

On the semiconductor substrate **118**, furthermore, at a desired position on the area to be provided as each of microchip parts, a connection hole is formed from the surface of the first insulating interlayer **124** to a predetermined depth position in the semiconductor substrate **118**. Then, a connection conductor **128** for extraction electrode is embedded in the resulting connection hole. The connection conductor **128** may be made of copper (Cu), tungsten (W), polysilicon, or the like. Before embedding the connection conductor **128**, an insulation layer **129** is formed on the inner wall surface of the connection hole to insulate the connection conductor **128** from the semiconductor substrate **118**. Then, a cap layer, a so-called protective layer **127** which prevent the copper wiring **125** from being dispersed, is formed on the multi-wiring layer **126**.

Next, as shown in FIG. **25**, the first semiconductor substrate **101** and the second semiconductor substrate **116** are bonded together so that their respective multi-wiring layers **111** and **126** can be faced with each other. Just as in the case with the aforementioned embodiment, the bonding may be performed using plasma bonding, an adhesive agent, or the like. In this example, on the bonding surface of each of the first and second semiconductor wafers **101** and **116**, a layer **129**, such as a plasma TEOS film, a plasma SiN film, a SiON film (block film), or a SiC film, is formed and bonded together by plasma bonding.

Next, as shown in FIG. **26**, grinding and polishing are performed from the back side of the first semiconductor substrate **101** to thin the first semiconductor substrate **101**. For example, the semiconductor substrate **101** with a thickness of 600 μm may be thinned to about 5 to 10 μm.

Next, as shown in FIG. **27**, a connection through-hole **131** is formed in the thin-filmed first semiconductor substrate **101** at a desired position of a region to be provided as each microchip part. The connection through-hole **131** extends from the back side **101***b* to the uppermost layer of the wiring **125** of the second semiconductor substrate **116** through the first semiconductor substrate **101**. Simultaneously, a connection hole **132** is formed near the connection through-hole **131** in the first semiconductor substrate **101**, extending from the back side **101***b* to a first layer portion of wiring **109** on

the first semiconductor substrate **101**. Since the connection through-hole **131** and the connection hole **132** are formed after making the first semiconductor substrate **101** into a thin film, these holes **131** and **132** can be formed as micropores with a smaller aspect ratio. Subsequently, an insulating layer **133** for electric insulation with the semiconductor substrate **101** is formed on the inner wall surface of each of the connection through-hole **131** and the connection hole **132**.

Next, a through-connection conductor **134** and a connection conductor **135** are embedded in the connection through-hole **131** and the connection hole **132**, respectively. Each of the through-connection conductor **134** and the connection conductor **135** may be made of a metal, such as copper (Cu) or tungsten (W).

Next, as shown in FIG. **28**, connection wiring **136** is formed on the back side of the first semiconductor substrate **101** to make a connection between the through-connection conductor **134** and the connection conductor **135**. The first semiconductor integrated circuit **102** is electrically connected to the second semiconductor integrated circuit **117** through the connection conductor **135**, the through-connection conductor **134**, and the connection wiring **136**. The connection wiring **136** serves as an electrode pad used as an extraction electrode. An insulating layer is applied to the surface except for the connection wiring **136** to form an overcoat layer **139**. The overcoat layer **139** may be, for example, a plasma silicon nitride film. On the other hand, on the side of the second semiconductor substrate **116**, the surface of the substrate **116** is ground to expose the surface of the connection conductor **128** that serves as an extraction electrode. After forming a passivation layer **137** on the exposed surface of the connection conductor **128** of the second semiconductor substrate **116**, a spherical electrode bump **138** is formed so that it can be electrically connected to the connection conductor **128** (see FIG. **22**).

Subsequently, the resultant is divided into each chip and semiconductor device **140** to be shown in FIG. **22** is obtained.

According to the semiconductor device **140** and the manufacturing method thereof according to the fifth embodiment of the present invention, just as in the case with the aforementioned embodiments, the first semiconductor integrated circuit and the second semiconductor integrated circuit can be independently formed on different microchip parts by their optimal process technologies, respectively. Therefore, a high-performance semiconductor integrated circuit can be provided. In addition, a reduction in manufacturing costs can be attained by bonding and thinning the first and second semiconductor wafers together in a half-finished product state, electrically connecting the first and second integrated circuits to each other, and dividing the resulting combination in a completed product state into microchips.

In the fifth embodiment, just as in the case with the fourth embodiment, the first and second semiconductor substrates may be bonded together to directly connect the wiring layers of multi-layered wiring to each other. Such a configuration of the device can lead to a decrease in number of manufacturing steps and a further reduction in manufacturing costs.

Although the solid-state imaging device according to any of the above embodiments uses electrons as signal electric charges, a p-type as a first-conductivity type, and an n-type as a second-conductivity type, it may be also applied to one using electron holes as signal electronic charges. In this case, the conductivity types of the semiconductor substrates, semiconductor well regions, or semiconductor regions are reversed. Thus, the n-type is provided as the first-conductivity type and the p-type is provided as the second-conductivity type.

In the solid-state imaging device according to any of the above embodiments, the first semiconductor chip section **22** may have a thickness smaller than the thickness of the second semiconductor chip section **26**.

7. Sixth Embodiment

Example of Configuration of Electronic Apparatus

The solid-state imaging devices according to the embodiments of the present invention can be applied to electronic apparatuses including camera systems such as digital cameras and video cameras, cellular phones with imaging functions, other apparatuses with imaging functions, and so on.

FIG. **29** illustrates the configuration of a camera as an exemplary electronic apparatus according to the sixth embodiment of the present invention. An example of the camera according to the present embodiment is a video camera which can shoot a still picture or video. The camera **141** of the present embodiment includes a solid-state imaging device **142**, an optical system **143** that introduces incident light into a photoreceptor of the solid-state imaging device **142**, and a shutter device **144**. Furthermore, the camera **141** includes a drive circuit **145** for driving the solid-state imaging device **142** and a signal processing circuit **146** for processing an output signal from the solid-state imaging device **142**.

The solid-state imaging device **142** is any of the solid-state imaging devices of the aforementioned embodiments. The optical system (optical lens) **143** carries out image formation of image light (incident light) from a photographic subject onto an imaging surface of the solid-state imaging device **142**. Therefore, signal electric charges are accumulated in the solid-state imaging device **142** for a given period of time. The optical system **143** may be an optical lens system constructed of a plurality of optical lenses. The shutter device **144** controls a period of light irradiation on the solid-state imaging device **142** and a period of light shielding.

The drive circuit **145** supplies drive signals for controlling the transfer operation of the solid-state imaging device **142** and the shutter operation of the shutter device **144**. The driving signals (timing signals) supplied from the drive circuit **145** allow the solid-state imaging device **142** to transmit signals. The signal-processing circuit **146** performs various kinds of signal processing. Video signals subjected to the signal processing are stored in a storage medium such as a memory or outputted to a monitor.

The electronic apparatus, such as a camera, according to the sixth embodiment of the present invention includes a high-performance solid-state imaging device **142** with a lower production cost. Therefore, an inexpensive and reliable electronic apparatus can be provided.

It should be understood by those skilled in the art that various modifications, combinations, sub-combinations and alterations may occur depending on design requirements and other factors insofar as they are within the scope of the appended claims or the equivalents thereof.

What is claimed is:

1. An image sensor, comprising:

a first semiconductor section including a first semiconductor substrate and a first wiring layer, the first semiconductor substrate including a photodiode, and the first wiring layer including a first insulating interlayer and first and second wirings; and

a second semiconductor section including a second semiconductor substrate and a second wiring layer, the second semiconductor section including a transistor, and the second wiring layer including a second insulating interlayer and third and fourth wirings,

wherein the first semiconductor section and the second semiconductor section are bonded together such that the first wiring layer and the third wiring layer face each other,

wherein the first wiring of the first wiring layer directly contacts the third wiring of the second wiring layer in a pixel region including the photodiode, and

wherein the second wiring of the first wiring layer directly contacts the fourth wiring of the second wiring layer in a peripheral region other than the pixel region.

2. The image sensor according to claim **1**, wherein a part of the first insulating interlayer and a part of the second insulating interlayer are in contact with each other.

3. The image sensor according to claim **1**, further comprising an isolation region separating unit pixels of the pixel region from one another.

4. The image sensor according to claim **1**, wherein the second semiconductor section further includes a fifth wiring.

5. The image sensor according to claim **1**, wherein the third wiring is electrically connected to the transistor via a fifth wiring.

6. The image sensor according to claim **1**, further comprising a through connection conductor that penetrates the second semiconductor substrate, and that is electrically connected to a fifth wiring.

7. The image sensor according to claim **1**, further comprising a light-shielding layer formed at a light incident side of the first semiconductor section in the peripheral region.

8. The image sensor according to claim **7**, wherein the light-shielding layer overlaps at least a part of the second wiring of the first wiring layer and the fourth wiring of the second wiring layer.

9. The image sensor according to claim **7**, wherein the light-shielding layer includes metal.

10. The image sensor according to claim **9**, wherein the metal is tungsten.

11. The image sensor according to claim **7**, wherein the light-shielding layer is electrically connected to the first semiconductor substrate.

12. The image sensor according to claim **11**, wherein the light-shielding layer is provided with a ground potential from the first semiconductor substrate.

13. The image sensor according to claim **11**, wherein a contact area where the light-shielding layer contacts the first semiconductor substrate overlaps a contact area where a portion of the second wiring of the first wiring layer contacts a portion of the fourth wiring of the second wiring layer in the peripheral region.

14. The image sensor according to claim **1**, wherein the first and the second wiring layers include copper (Cu).

15. An image sensing method, comprising:

providing a first semiconductor section including a first semiconductor substrate and a first wiring layer, the first semiconductor substrate including a photodiode, and the first wiring layer including a first insulating interlayer and first and second wirings;

providing a second semiconductor section including a second semiconductor substrate and a second wiring layer, the second semiconductor section including a transistor, and the second wiring layer including a second insulating interlayer and third and fourth wirings; and

bonding the first semiconductor section and the second semiconductor section together such that the first wiring layer and the third wiring layer face each other,

wherein the first wiring of the first wiring layer directly contacts the third wiring of the second wiring layer in a pixel region including the photodiode, and

wherein the second wiring of the first wiring layer directly contacts the fourth wiring of the second wiring layer in a peripheral region other than the pixel region.

16. The method according to claim **15**, wherein a part of the first insulating interlayer and a part of the second insulating interlayer are in contact with each other.

17. The method according to claim **15**, further comprising providing an isolation region separating unit pixels of the pixel region from one another.

18. The method according to claim **15**, wherein the second semiconductor section further includes a fifth wiring.

19. The method according to claim **15**, wherein the third wiring is electrically connected to the transistor via a fifth wiring.

20. The method according to claim **15**, further comprising providing a through connection conductor that penetrates the second semiconductor substrate, and that is electrically connected to a fifth wiring.

* * * * *