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(54) **MULTILAYER CERAMIC ELECTRONIC COMPONENT**

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(57) **ABSTRACT**

A multilayer ceramic capacitor includes a multilayer body and external electrodes at both end portions of the multilayer body. The external electrodes include main surface-side external electrodes. In a cross-sectional view along a lamination direction and a length direction, main surface-side external electrodes include a recess recessed towards a side of the multilayer body, a first bulge on a central side of the multilayer body in the length direction, and a second bulge at an end portion side of the multilayer body in the length direction, between which the recess is interposed. A distance between a vertex of the first bulge and a vertex of the second bulge in the length direction is longer than a distance between an inner end portion of the main surface-side external electrode and the vertex of the first bulge in the length direction.

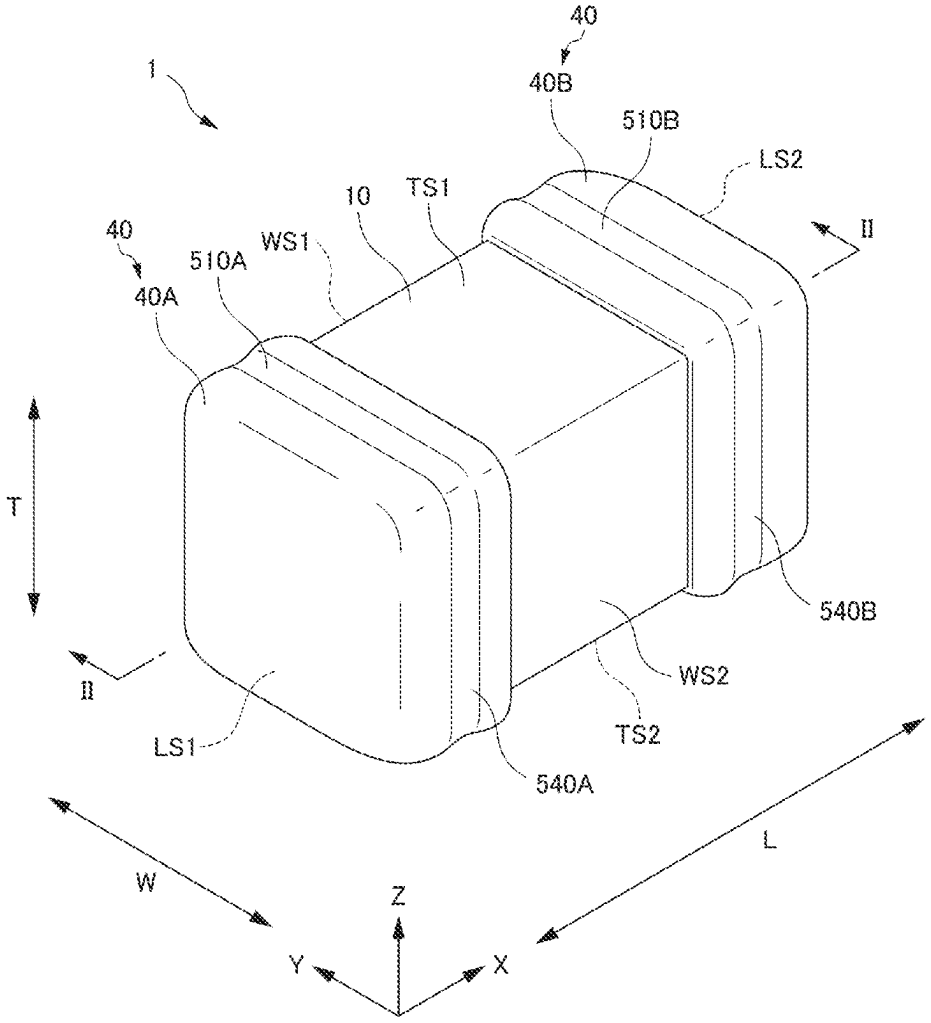
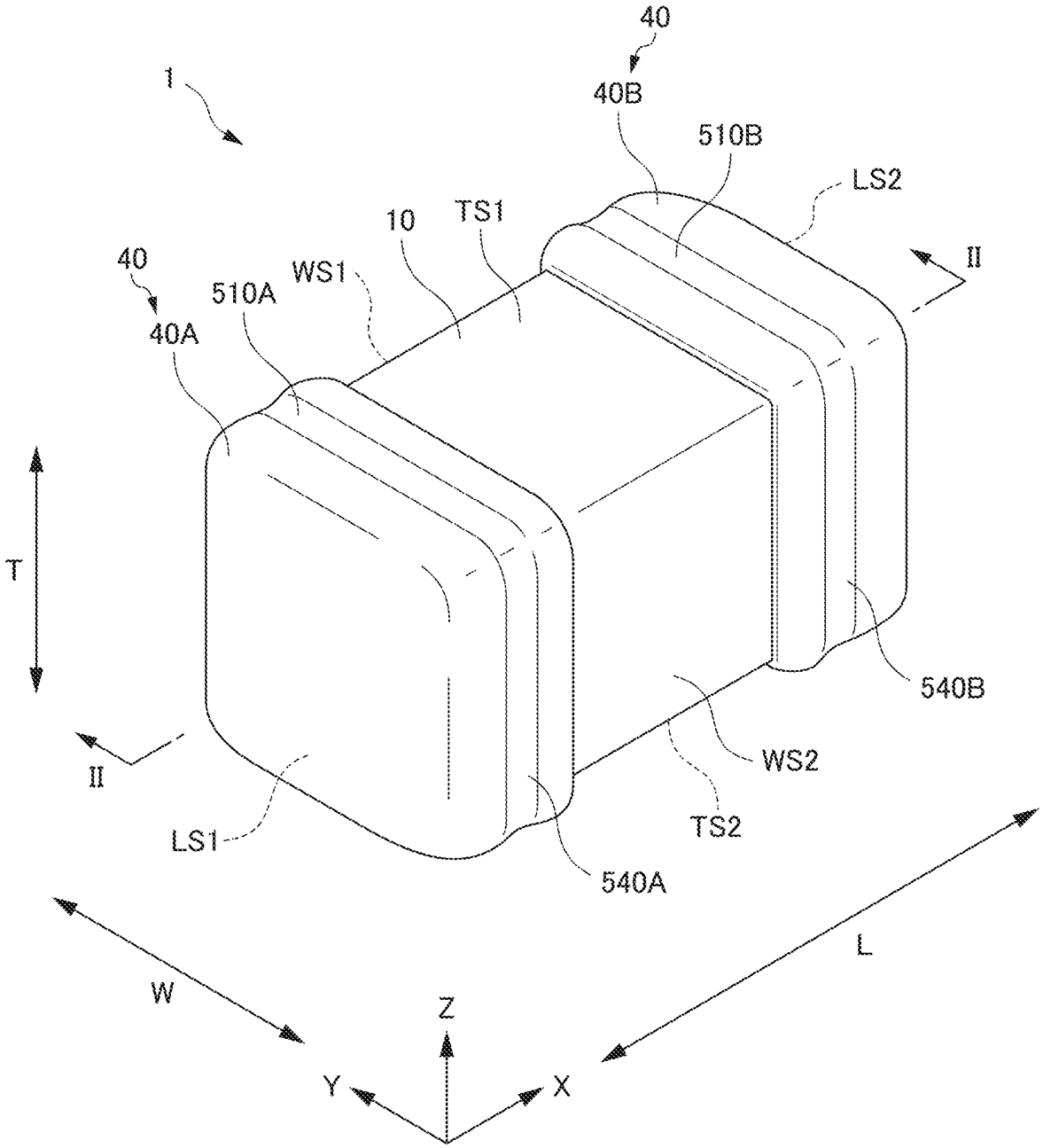


FIG. 1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LS2
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TS1
II
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WS1
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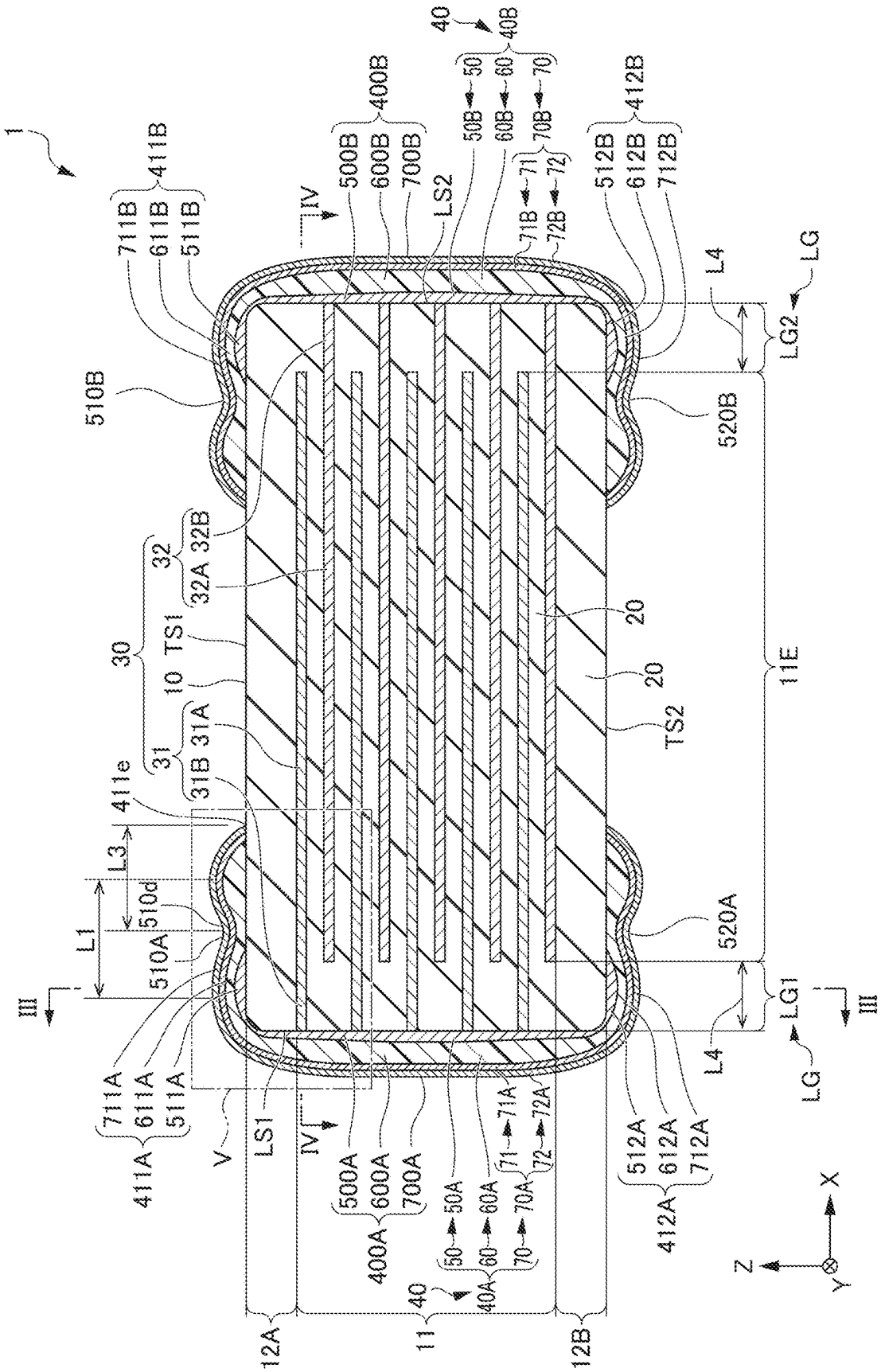
T
540B
II
WS2
LS1
TS2
540A
L
W
Z
Y
X

FIG. 2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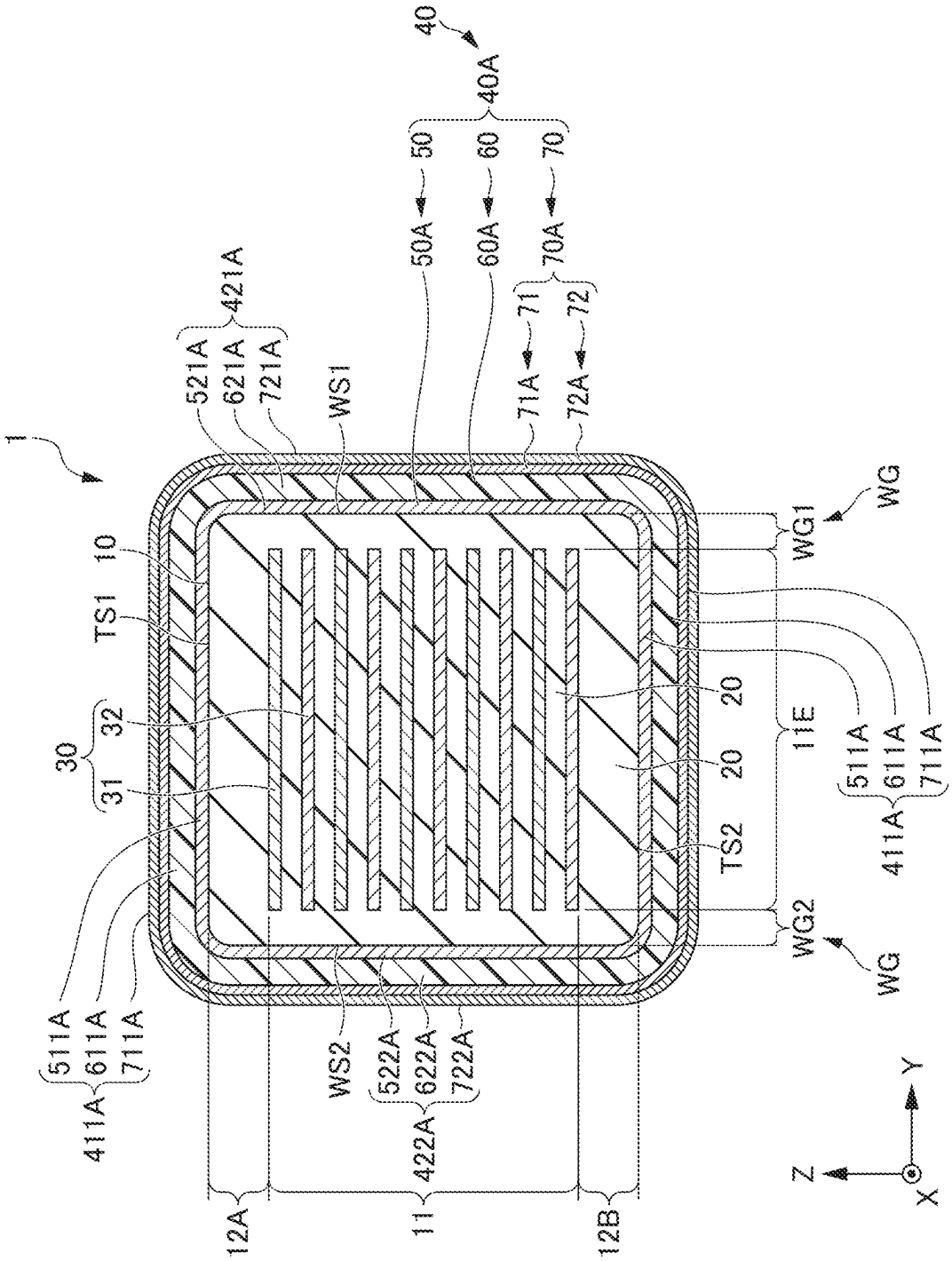
612B
712B
411B
711B
611B
511B
IV
LS2
L4
LG
LG2
510B
520B
32
32A
32B
30
TS1
10
20
11E
TS2
31
31A
31B
411e
L3
510d
L1
510A
520A
LG1
III
711A
611A
511A
411A
V
LS1
500A
600A
700A
50A
60A
70A
71A
72A
512A
612A
712A
412A
12A
11
12B
X
Y
Z

FIG. 3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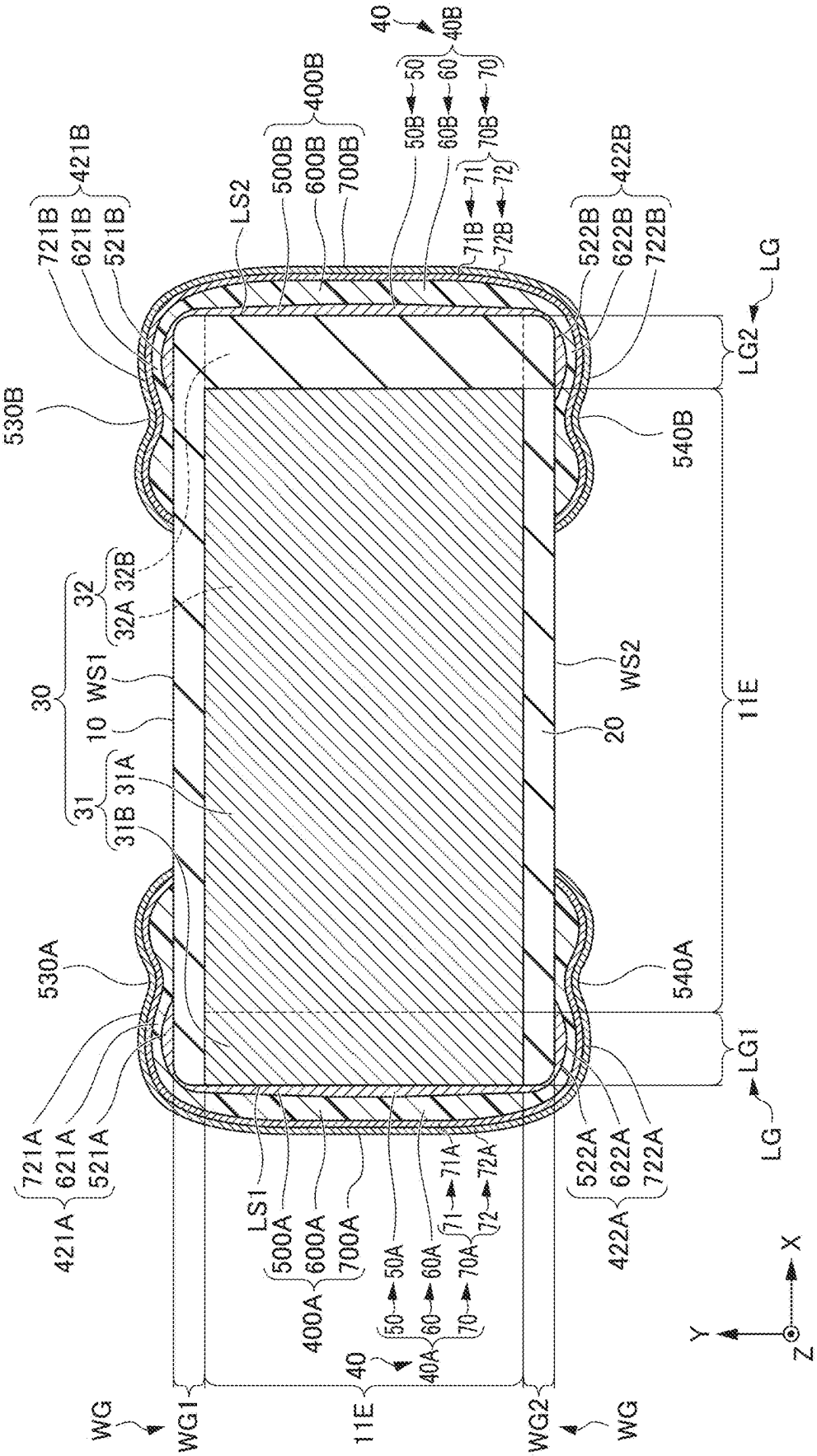
TS1
30
31
32
511A
611A
711A
411A
521A
621A
721A
421A
WS1
WS2
522A
622A
722A
422A
50
50A
60
60A
70
70A
71
71A
72
72A
40
40A
20
20
TS2
11E
WG1
WG2
WG
12A
11
12B
Z
Y
X

FIG. 4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421B
721B
621B
521B
422B
522B
622B
722B
LG
LG2
530B
540B
32
32A
32B
30
WS1
10
WS2
20
11E
31
31A
31B
530A
540A
LG1
721A
621A
521A
421A
LS1
500A
600A
700A
400A
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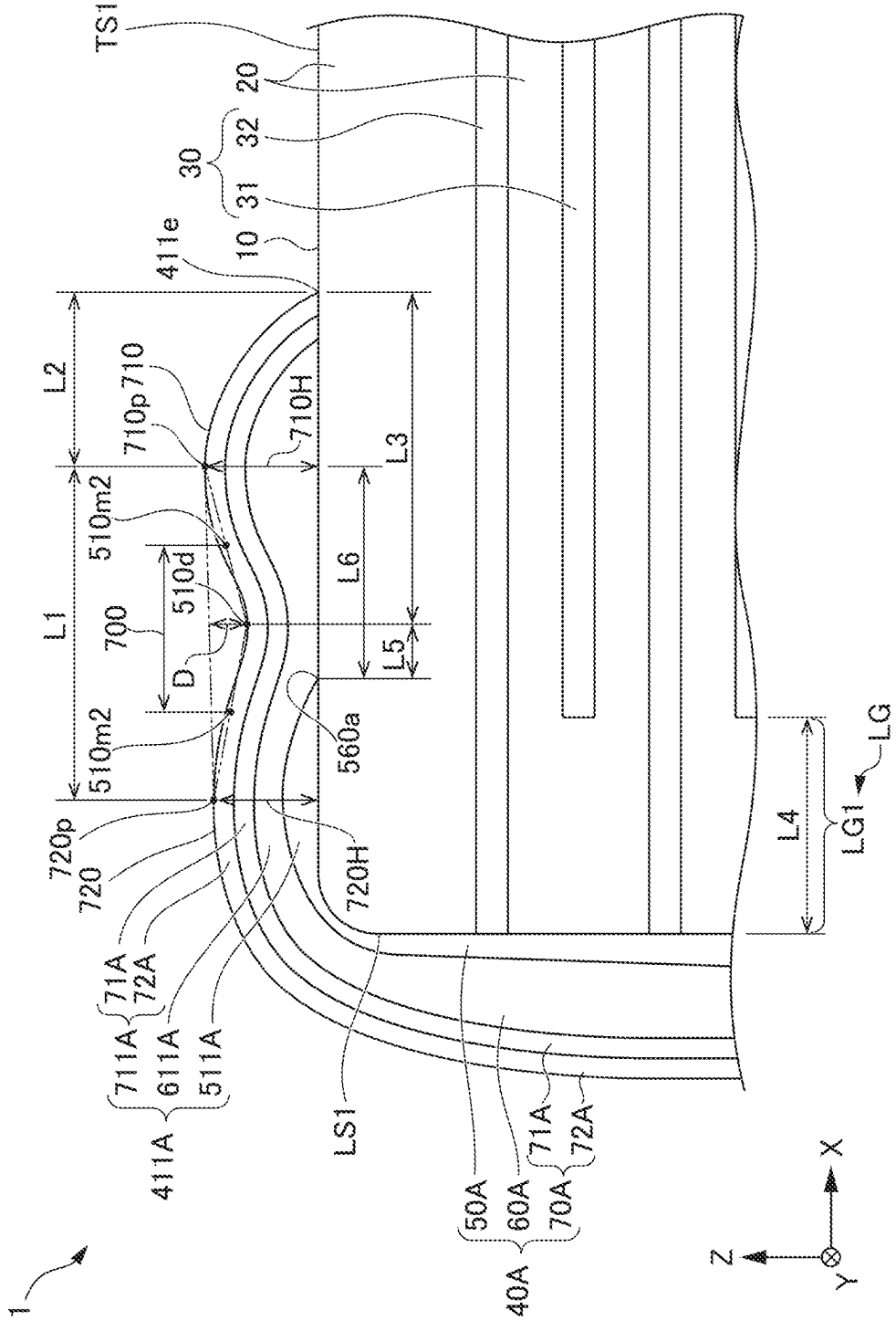
522A
622A
722A
422A
40A
WG
WG1
WG2
X
Y
Z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20
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32
31
10
411e
L2
710p
710
710H
L3
510m2
510d
L6
L1
700
D
L5
560a
510m2
720p
720
720H
LG
L4
LG1
71A
72A
711A
611A
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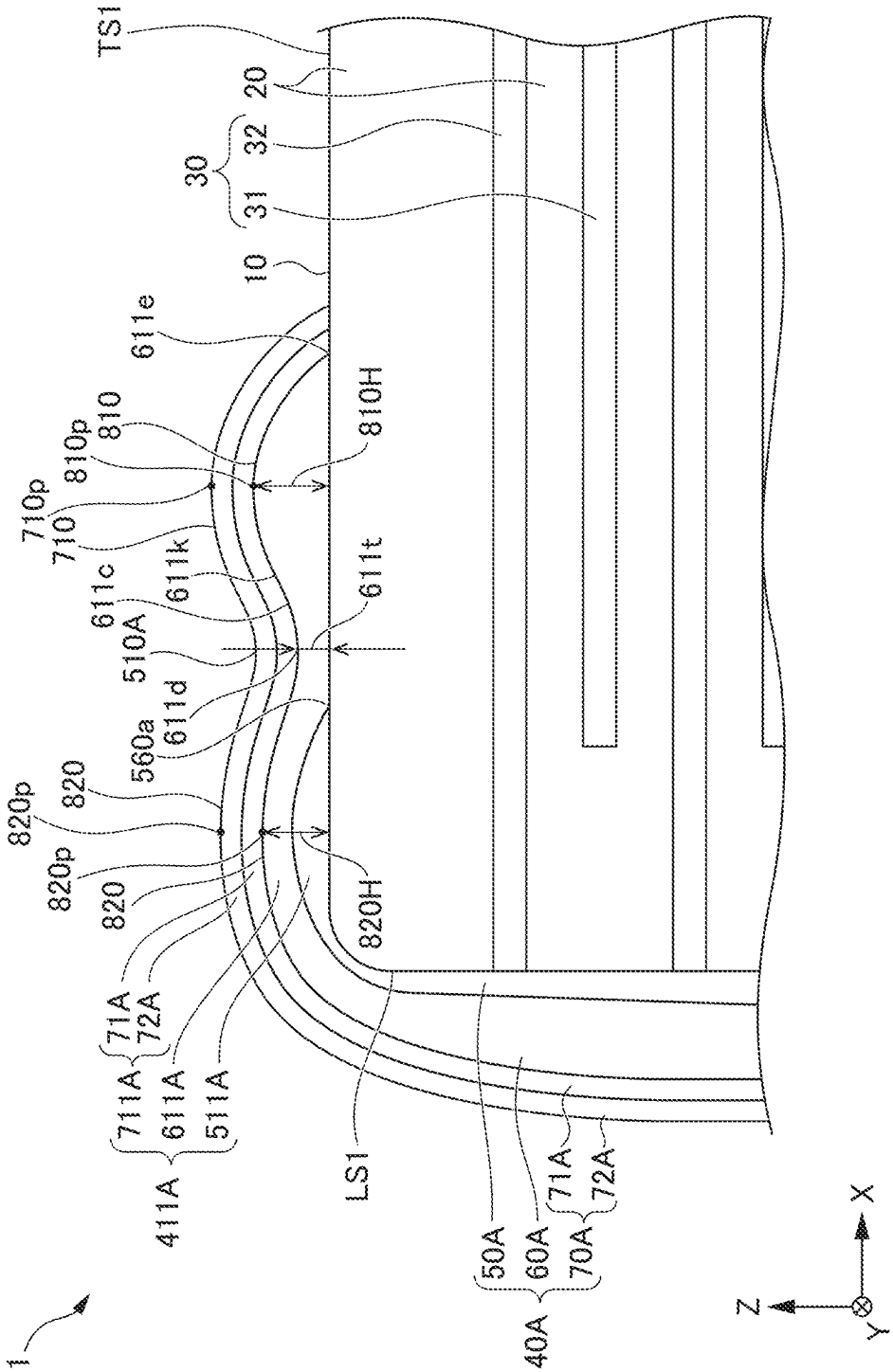
411A
LS1
50A
60A
70A
40A
71A
72A
1
Z
Y
X

FIG. 5A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32
31
10
611e
810
810p
810H
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611c
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611t
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820p
820p
820
820H
71A
72A
711A
611A
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LS1
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40A
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X
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Z

FIG. 5B

FIG. 6A

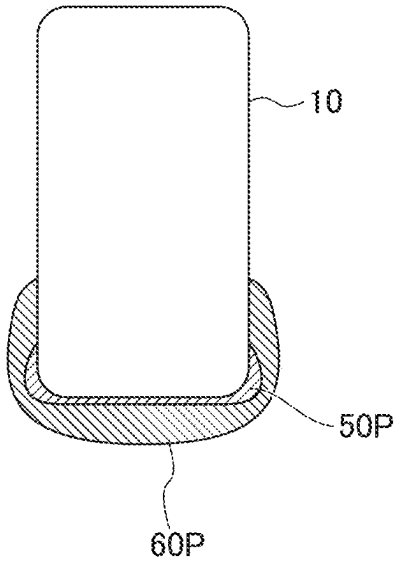


FIG. 6B

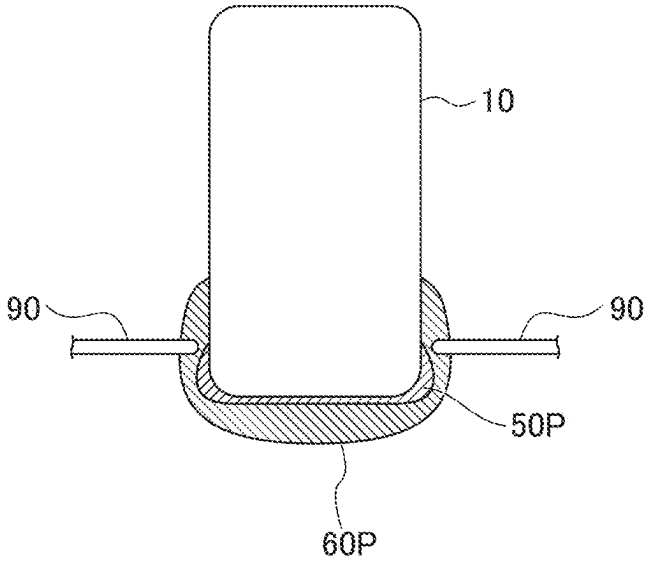


FIG. 6C

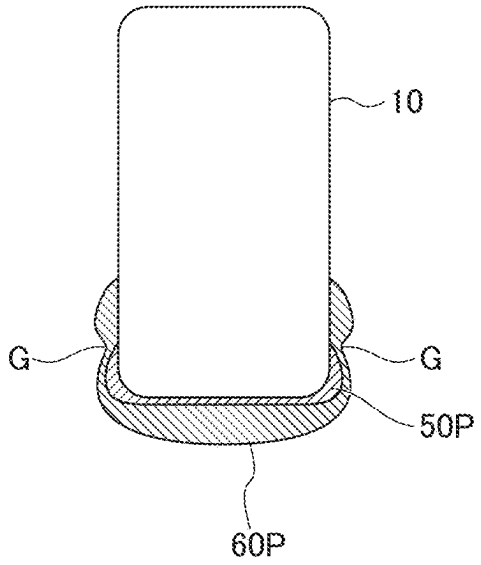


FIG. 7A

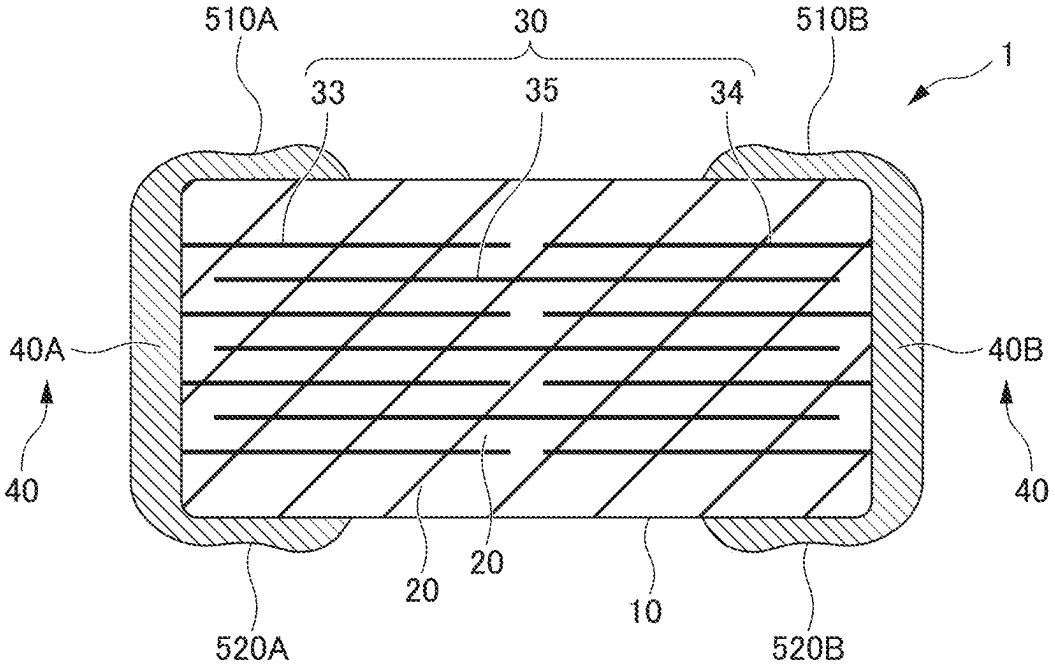


FIG. 7B

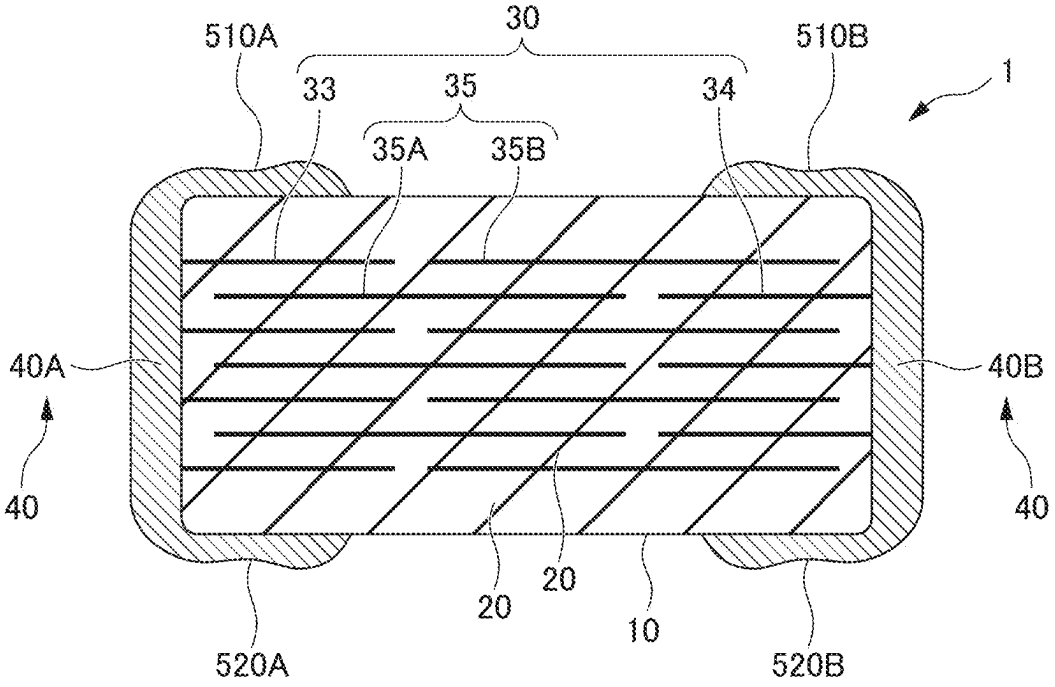
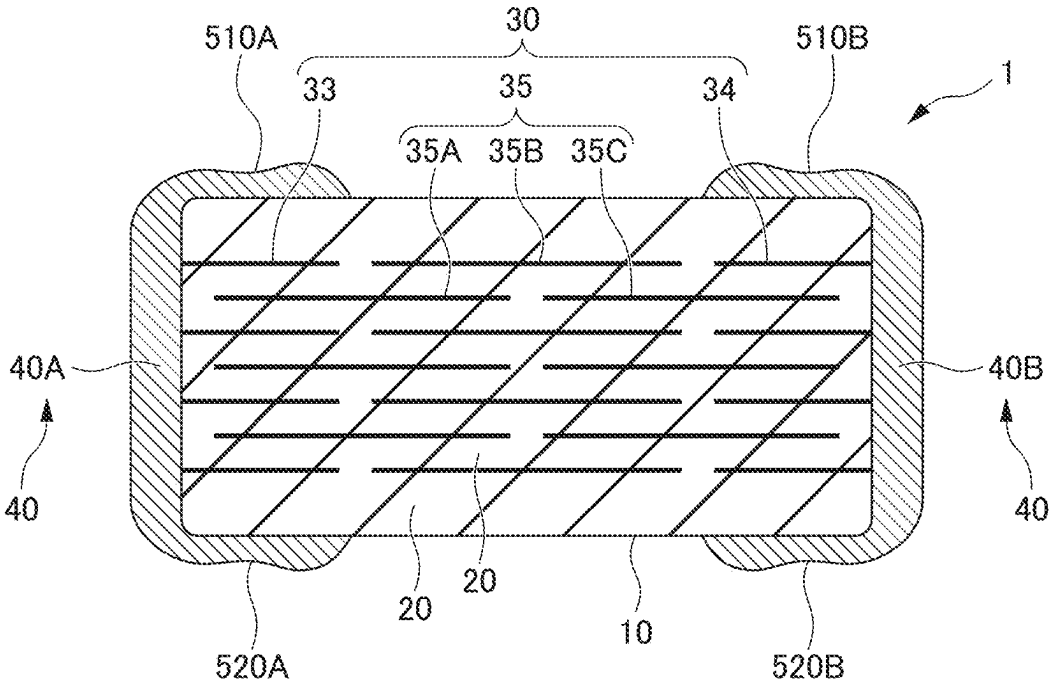


FIG. 7C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520B

MULTILAYER CERAMIC ELECTRONIC COMPONENT

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is based on and claims the benefit of priority from Japanese Patent Application No. 2024-032039, filed on Mar. 4, 2024, the contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0002] The present invention relates to multilayer ceramic electronic components.

2. Description of the Related Art

[0003] Conventionally, multilayer ceramic capacitors as a type of multilayer ceramic electronic component are known. In general, a multilayer ceramic capacitor includes a rectangular multilayer body in which a plurality of dielectric layers and a plurality of internal electrode layers are alternately stacked, and external electrodes on both end surfaces of the multilayer body. For example, Japanese Unexamined Patent Application Publication No. 2003-243249 discloses a multilayer ceramic capacitor with the abovementioned structure, in which the external electrodes include a base electrode layer formed by firing.

[0004] Typically, the external electrode of the multilayer ceramic capacitor is also provided on the main surface side, which is the widest plane of the rectangular multilayer body. The shape of the surface of the external electrode on the main surface side is rounded as a whole. In this case, when mounting the multilayer ceramic capacitor on a board, the ground contact area between the external electrodes and the board may be reduced, potentially leading to instability during the mounting process.

SUMMARY OF THE INVENTION

[0005] Example embodiments of the present invention provide multilayer ceramic capacitors that each facilitate stability during a mounting process.

[0006] A multilayer ceramic capacitor according to an example embodiment of the present invention includes a multilayer body that includes a plurality of ceramic layers and a plurality of inner conductive layers stacked alternately in a height direction, a first main surface and a second main surface on opposite sides in the height direction, a first end surface and a second end surface on opposite sides in a length direction orthogonal or substantially orthogonal to the height direction, a first lateral surface and a second lateral surface on opposite sides in a width direction orthogonal or substantially orthogonal to both of the height direction and the length direction, and a pair of external electrodes spaced apart from each other at both end portions of the multilayer body in the length direction. The inner conductive layers include a first inner conductive layer extending to the first end surface and a second inner conductive layer extending to the second end surface. The external electrodes include a main surface-side external electrode on at least one of the first main surface or the second main surface. In a cross-sectional view along the height and the length directions, the main surface-side external electrode includes, on a surface thereof, a recess recessed towards a side of the multilayer body, a first bulge on a central side of the multilayer body in the length direction, and a second bulge at an end portion side of the multilayer body in the length direction, between which a conductive resin layer recess is interposed. A distance between a vertex of the first bulge and a vertex of the second bulge in the length direction is longer than a distance between an inner end portion of the main surface-side external electrode and a vertex of the first bulge in the length direction.

[0007] Example embodiments of the present invention are each able to provide a multilayer ceramic capacitor that facilitates stability during a mounting process.

[0008] The above and other elements, features, steps, characteristics and advantages of the present invention will become more apparent from the following detailed description of the example embodiments with reference to the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] FIG. **1** is a perspective view of a multilayer ceramic capacitor according to an example embodiment of the present invention.

[0010] FIG. **2** is a cross-sectional view taken along the line II-II of FIG. **1**.

[0011] FIG. **3** is a cross-sectional view taken along the line III-III of FIG. **2**.

[0012] FIG. **4** is a cross-sectional view taken along the line IV-IV of FIG. **2**.

[0013] FIG. **5**A is an enlarged view of the portion indicated by V in FIG. **2**, illustrating a cross section of the first main surface-side external electrode.

[0014] FIG. **5**B is an enlarged view of the portion indicated by V in FIG. **2**, illustrating a cross section of the first main surface-side external electrode.

[0015] FIG. **6**A is a diagram illustrating a method of manufacturing the multilayer ceramic capacitor according to an example embodiment of the present invention, illustrating a first step of forming an external electrode on a multilayer body.

[0016] FIG. **6**B is a diagram illustrating a method of manufacturing the multilayer ceramic capacitor according to an example embodiment of the present invention, illustrating a second step of forming the external electrode on the multilayer body.

[0017] FIG. **6**C is a diagram illustrating a method of manufacturing the multilayer ceramic capacitor according to an example embodiment of the present invention, illustrating a third step of forming the external electrode on the multilayer body.

[0018] FIG. **7**A is a diagram illustrating a two-portion-structured multilayer ceramic capacitor according to an example embodiment of the present invention.

[0019] FIG. **7**B is a diagram illustrating a three-portion-structured multilayer ceramic capacitor according to an example embodiment of the present invention.

[0020] FIG. **7**C is a diagram illustrating a four-portion-structured multilayer ceramic capacitor according to an example embodiment of the present invention.

DETAILED DESCRIPTION OF THE EXAMPLE EMBODIMENTS

[0021] Example embodiments of the present invention will be described in detail below with reference to the drawings.

[0022] Hereinafter, a multilayer ceramic capacitor **1** as a multilayer ceramic electronic component according to an example embodiment of the present invention will be described with reference to FIGS. **1** to **4**. FIG. **1** is a perspective view of the multilayer ceramic capacitor **1** according to the present example embodiment. FIG. **2** is a cross-sectional view taken along the line II-II of the multilayer ceramic capacitor **1** in FIG. **1**. FIG. **3** is a cross-sectional view taken along the line III-III of the multilayer ceramic capacitor **1** in FIG. **2**. FIG. **4** is a cross-sectional view taken along the line IV-IV of the multilayer ceramic capacitor **1** in FIG. **2**.

[0023] The multilayer ceramic capacitor **1** includes a multilayer body **10** and external electrodes **40**.

[0024] FIGS. **1** to **4** illustrate an XYZ orthogonal coordinate system. The length direction L of the multilayer ceramic capacitor **1** and the multilayer body **10** corresponds to the X direction. The width direction W of the multilayer ceramic capacitor **1** and the multilayer body **10** corresponds to the Y direction. The lamination direction T as a height direction of the multilayer ceramic capacitor **1** and the multilayer body **10** corresponds to the Z direction. The cross section illustrated in FIG. **2** is also referred to as an LT cross section. The cross section illustrated in FIG. **3** is also referred to as a WT cross section. The cross section illustrated in FIG. **4** is also referred to as an LW cross section.

[0025] As illustrated in FIGS. **1** to **4**, the multilayer body **10** includes a first main surface TS**1** and a second main surface TS**2** on opposite sides in the lamination direction T, a first lateral surface WS**1** and a second lateral surface WS**2** on opposite sides in the width direction W orthogonal or substantially orthogonal to the lamination direction T, and a first end surface LS**1** and a second end surface LS**2** on opposite sides in the length direction L orthogonal or substantially orthogonal to both the lamination direction T and the width direction W.

[0026] As illustrated in FIG. **1**, the multilayer body **10** has a rectangular or substantially rectangular parallelepiped shape. The dimension in the length direction L of the multilayer body **10** is not necessarily longer than the dimension in the width direction W. The corners and edges of the multilayer body **10** are preferably rounded. The corners are where three faces of the multilayer body intersect, and the edges are where two faces of the multilayer body intersect. The surfaces of the multilayer body **10** may include irregularities in whole or in part.

[0027] The dimensions of the multilayer body **10** are not particularly limited. However, the dimension of the multilayer body **10** in the length direction L, denoted as the L dimension, is preferably, for example, between about 0.2 mm and about **10** mm inclusive. The dimension of the multilayer body **10** in the lamination direction T, denoted as the T dimension, is preferably, for example, between about 0.1 mm and about 10 mm inclusive. The dimension of the multilayer body **10** in the width direction W, denoted as the W dimension, is preferably, for example, between about 0.1 mm and about 10 mm inclusive.

[0028] As illustrated in FIGS. **2** and **3**, the multilayer body **10** includes an inner layer portion **11**, and a first main surface-side outer layer portion **12**A and a second main surface-side outer layer portion **12**B, with the inner layer portion **11** being interposed between the first main surface-side outer layer portion **12**A and the second main surface-side outer layer portion **12**B in the lamination direction T.

[0029] The inner layer portion **11** includes a plurality of dielectric layers **20** as a plurality of ceramic layers, and a plurality of internal electrode layers **30** as a plurality of inner conductive layers. The internal electrode layers **30** included in the inner layer portion **11** range from an internal electrode layer **30** closest to the first main surface TS**1** to another internal electrode layer **30** closest to the second main surface TS**2**, in the lamination direction T. In the inner layer portion **11**, the plurality of internal electrode layers **30** face each other via the dielectric layers **20**. The inner layer portion **11** generates capacitance, and essentially defines and functions as a capacitor.

[0030] The dielectric layers **20** are made of dielectric materials. The dielectric materials may be dielectric ceramics including components such as, for example, $BaTiO_3$, $CaTiO_3$, $SrTiO_3$, or $CaZrO_3$. In addition to these main components, the dielectric materials may include accessory components such as, for example, Mn compounds, Fe compounds, Cr compounds, Co compounds, or Ni compounds.

[0031] The thickness of the dielectric layers **20** is preferably,

[0032] for example, between about 0.5 μm and about 30 μm inclusive. The number of dielectric layers **20** to be stacked (laminated) is preferably, for example, between 10 and 1500 inclusive. The number of dielectric layers **20** is the total of the number of dielectric layers in the inner layer portion **11**, and the number of the dielectric layers in the first main surface-side outer layer portion **12**A and the second main surface-side outer layer portion **12**B.

[0033] The plurality of internal electrode layers **30** include first internal electrode layers **31** as a plurality of first inner conductive layers, and second internal electrode layers **32** as a plurality of second inner conductive layers. The plurality of first internal electrode layers **31** are provided on the plurality of dielectric layers **20**. The plurality of second internal electrode layers **32** are provided on the plurality of dielectric layers **20**. The plurality of first internal electrode layers **31** and the plurality of second internal electrode layers **32** are alternately provided in the lamination direction T of the multilayer body **10**, with the dielectric layers **20** being interposed therebetween. Each of the first internal electrode layers **31** and each of the second internal electrode layers **32** are provided such that a dielectric layer **20** of the dielectric layers **20** is interposed therebetween. Hereinafter, unless necessary to distinguish, the first internal electrode layers **31** and the second internal electrode layers **32** may collectively be referred to as the internal electrode layers **30**.

[0034] The first internal electrode layer **31** includes a first counter portion **31**A facing the second internal electrode layer **32**, and a first extension portion **31**B extending from the first counter portion **31**A to the first end surface LS**1**. The first extension portion **31**B is exposed at the first end surface LS**1**.

[0035] The second internal electrode layer **32** includes a second counter portion **32**A facing the first internal electrode layer **31**, and a second extension portion **32**B extending from the second counter portion **32**A to the second end surface LS**2**. The second extension portion **32**B is exposed at the second end surface LS**2**.

[0036] In the present example embodiment, the first counter portion **31**A and the second counter portion **32**A face each other, with the dielectric layer **20** being interposed therebetween, thus generating capacitance and providing the characteristics of the capacitor.

[0037] The shapes of the first counter portion **31**A and the second counter portion **32**A are not particularly limited but are preferably rectangular or substantially rectangular. However, the corners of the rectangular-shaped portions may be rounded or formed diagonally. The shapes of the first extension portion **31**B and the second extension portion **32**B are not particularly limited but are preferably rectangular or substantially rectangular. However, the corners of the rectangular-shaped portions may be rounded or formed diagonally.

[0038] Both of the dimensions of the first counter portion **31**A and the first extension portion **31**B in the width direction W may be the same, or one of the dimensions may be smaller. Both of the dimensions of the second counter portion **32**A and the second extension portion **32**B in the width direction W may be the same, or one of the dimensions may be smaller.

[0039] The first internal electrode layers **31** and the second internal electrode layers **32** include appropriate conductive materials such as, for example, Ni, Cu, Ag, Pd, Au, or alloys including at least one of these metals. When using an alloy, for example, the first internal electrode layers **31** and the second internal electrode layers **32** may include, for example, Ag—Pd alloy.

[0040] The thickness of the first internal electrode layers **31** and the second internal electrode layers **32** is preferably, for example, between about 0.2 μm and about 2.0 μm inclusive. The total number of the first internal electrode layers **31** and the second internal electrode layers **32** is, for example, preferably between 10 and 1500 inclusive.

[0041] The first main surface-side outer layer portion **12**A is provided on the first main surface TS**1** side of the multilayer body **10**. The first main surface-side outer layer portion **12**A is a collective portion including the plurality of dielectric layers **20** between the first main surface TS**1** and the internal electrode layer **30** closest to the first main surface TS**1**. The dielectric layers **20** used in the first main surface-side outer layer portion **12**A may be the same as the dielectric layers **20** used in the inner layer portion **11**, or may be dielectric layers including different materials.

[0042] The second main surface-side outer layer portion **12**B is provided on the second main surface TS**2** side of the multilayer body **10**. The second main surface-side outer layer portion **12**B is a collective portion including the plurality of dielectric layers **20** between the second main surface TS**2** and the internal electrode layer **30** closest to the second main surface TS**2**. The dielectric layers **20** used in the second main surface-side outer layer portion **12**B may be the same as the dielectric layers **20** used in the inner layer portion **11**, or may be dielectric layers include different materials.

[0043] The multilayer body **10** includes a counter electrode portion **11**E. The counter electrode portion **11**E is a portion where the first counter portion **31**A of the first internal electrode layer **31** faces the second counter portion **32**A of the second internal electrode layer **32**. The counter electrode portion **11**E includes a portion of the inner layer portion **11**. FIG. **4** illustrates the range of the counter electrode portion **11**E in the width direction W and the length direction L. The counter electrode portion **11**E is also referred to as the capacitor active portion.

[0044] The multilayer body **10** includes lateral surface-side outer layer portions WG. The lateral surface-side outer layer portions WG include a first lateral surface-side outer layer portion WG**1** and a second lateral surface-side outer layer portion WG**2**. The first lateral surface-side outer layer portion WG**1** is a portion including the dielectric layers **20** between the counter electrode portion **11**E and the first lateral surface WS**1**. The second lateral surface-side outer layer portion WG**2** is a portion including the dielectric layers **20** between the counter electrode portion **11**E and the second lateral surface WS**2**. FIGS. **3** and **4** illustrate the range of the first lateral surface-side outer layer portion WG**1** and the second lateral surface-side outer layer portion WG**2** in the width direction W. The lateral surface-side outer layer portions are also referred to as W gaps or side gaps.

[0045] The multilayer body **10** includes end surface-side outer layer portions LG. The end surface-side outer layer portions LG include a first end surface-side outer layer portion LG**1** and a second end surface-side outer layer portion LG**2**. The first end surface-side outer layer portion LG**1** is a portion including the dielectric layers **20** between the counter electrode portion **11**E and the first end surface LS**1**. The second end surface-side outer layer portion LG**2** is a portion including the dielectric layers **20** between the counter electrode portion **11**E and the second end surface LS**2**. FIGS. **2** and **4** illustrate the range of the first end surface-side outer layer portion LG**1** and the second end surface-side outer layer portion LG**2** in the length direction L. The end surface-side outer layer portions are also referred to as L gaps or end gaps.

[0046] The external electrodes **40** include a first external electrode **40**A on the first end surface LS**1** side, and a second external electrode **40**B on the second end surface LS**2** side.

[0047] The first external electrode **40**A is provided on the first end surface LS**1**. The first external electrode **40**A is connected to the first internal electrode layer **31**. The first external electrode **40**A is provided on a portion of the first main surface TS**1** and a portion of the second main surface TS**2**. In the example embodiment, the first external electrode **40**A extends from the first end surface LS**1** to a portion of the first main surface TS**1** and a portion of the second main surface TS**2**, a portion of the first lateral surface WS**1**, and a portion of the second lateral surface WS**2**.

[0048] The second external electrode **40**B is provided on the second end surface LS**2**. The second external electrode **40**B is connected to the second internal electrode layer **32**. The second external electrode **40**B is provided on a portion of the first main surface TS**1** and a portion of the second main surface TS**2**. In the present example embodiment, the second external electrode **40**B extends from the second end surface LS**2** to a portion of the first main surface TS**1** and a portion of the second main surface TS**2**, a portion of the first lateral surface WS**1**, and a portion of the second lateral surface WS**2**.

[0049] As described above, within the multilayer body **10**, the first counter portion **31**A of the first internal electrode layer **31** faces the second counter portion **32**A of the second internal electrode layer **32**, with the dielectric layer **20** being interposed therebetween, thereby generating the capacitance. Therefore, capacitor characteristics are generated between the first external electrode **40**A connected to the

first internal electrode layer **31**, and the second external electrode **40**B connected to the second internal electrode layer **32**.

[0050] The first external electrode **40**A includes a first base electrode layer **50**A including metal components, a first conductive resin layer **60**A on the first base electrode layer **50**A, and a first plated layer **70**A on the first conductive resin layer **60**A. The first plated layer **70**A includes a first Ni plated layer **71**A as the lower plated layer and a first Sn plated layer **72**A as the upper plated layer.

[0051] The second external electrode **40**B includes a second base electrode layer **50**B including metal components, a second conductive resin layer **60**B on the second base electrode layer **50**B, and a second plated layer **70**B on the second conductive resin layer **60**B. The second plated layer **70**B includes a second Ni plated layer **71**B as the lower plated layer and a second Sn plated layer **72**B as the upper plated layer.

[0052] Here, the basic configuration of the first external electrode **40**A and the second external electrode **40**B is the same or substantially the same. The first external electrode **40**A and the second external electrode **40**B are plane-symmetrical or substantially plane-symmetrical with respect to the LW cross section at the center of the multilayer ceramic capacitor **1** in the length direction L. Therefore, unless necessary to distinguish, the first external electrode **40**A and the second external electrode **40**B may be collectively referred to as the external electrodes **40**. Similarly, unless necessary to distinguish, the first base electrode layer **50**A and the second base electrode layer **50**B may be collectively referred to as the base electrode layers **50**. Unless necessary to distinguish, the first conductive resin layer **60**A and the second conductive resin layer **60**B may be collectively referred to as the conductive resin layers **60**. Unless necessary to distinguish, the first plated layer **70**A and the second plated layer **70**B may be collectively referred to as the plated layers **70**. Unless necessary to distinguish, the first Ni plated layer **71**A and the second Ni plated layer **71**B may be collectively referred to as the Ni plated layers **71**. Unless necessary to distinguish, the first Sn plated layer **72**A and the second Sn plated layer **72**B may be collectively referred to as the Sn plated layers **72**.

[0053] The base electrode layer **50** includes the first base electrode layer **50**A and the second base electrode layer **50**B.

[0054] The first base electrode layer **50**A is provided on the first end surface LS**1**. The first base electrode layer **50**A is connected to the first internal electrode layers **31**. In the present example embodiment, the first base electrode layer **50**A extends from the first end surface LS**1** to a portion of the first main surface TS**1**, a portion of the second main surface TS**2**, a portion of the first lateral surface WS**1**, and a portion of the second lateral surface WS**2**.

[0055] The second base electrode layer **50**B is provided on the second end surface LS**2**. The second base electrode layer **50**B is in contact with the second internal electrode layers **32**. In the present example embodiment, the second base electrode layer **50**B extends from the second end surface LS**2** to a portion of the first main surface TS**1**, a portion of the second main surface TS**2**, a portion of the first lateral surface WS**1**, and a portion of the second lateral surface WS**2**.

[0056] The first base electrode layer **50**A and the second base electrode layer **50**B of the present example embodiment are fired layers. The fired layer preferably includes, for example, a metal component and either a glass component or a ceramic component, or both. This can improve the adhesion between the multilayer body **10** and the base electrode layers. The metal component may include, for example, at least one of Cu, Ni, Ag, Pd, Ag—Pd alloy, or Au. The glass component may include, for example, at least one of B, Si, Ba, Mg, Al, or Li. The glass component being present can aid and promote sintering of the metal components within the base electrode layer. The ceramic component may use the same ceramic material as the dielectric layer **20** or a different type of ceramic material. Examples of the ceramic component include at least one of $BaTiO_3$, $CaTiO_3$, $(Ba,Ca)TiO_3$, $SrTiO_3$, or $CaZrO_3$.

[0057] The fired layer, for example, is prepared by applying a conductive paste including glass and metal to the multilayer body, followed by firing. The fired layer may be prepared by simultaneously firing the multilayer chips including internal electrodes and dielectric layers, and the conductive paste applied to the multilayer chips, or may be prepared by obtaining the multilayer body by firing the multilayer chips including internal electrodes and dielectric layers, and then applying the conductive paste to the multilayer body, followed by firing. In the case of simultaneously firing the multilayer chip including internal electrodes and dielectric layers, and the conductive paste applied to the multilayer chip, the fired layer is preferably formed by firing a mixture including ceramic material instead of a glass component. In this case, as the ceramic material to be added, using a ceramic material the same as or similar to the dielectric layer **20** is preferable. The fired layer may include a plurality of layers.

[0058] The thickness of the first base electrode layer **50**A on the first end surface LS**1** in the length direction L is, for example, preferably between about 2 μm and about 220 μm inclusive at the center of the first base electrode layer **50**A in the lamination direction T and the width direction W.

[0059] The thickness of the second base electrode layer **50**B on the second end surface LS**2** in the length direction L is, for example, preferably between about 2 μm and about 220 μm inclusive at the center of the second base electrode layer **50**B in the lamination direction T and the width direction W.

[0060] In cases where the first base electrode layer **50**A is also provided on a portion of at least one of the first main surface TS**1** or the second main surface TS**2**, the thickness of the first base electrode layer **50**A in this portion in the lamination direction T is, for example, preferably between about 3 μm and about 40 μm inclusive at the center of the first base electrode layer **50**A in this portion in the length direction L and the width direction W.

[0061] In cases where the first base electrode layer **50**A is also provided on a portion of at least one of the first lateral surface WS**1** or the second lateral surface WS**2**, the thickness of the first base electrode layer **50**A in this portion in the width direction W is, for example, preferably between about 3 μm and about 40 μm inclusive at the center of the first base electrode layer **50**A in this portion in the length direction L and the lamination direction T.

[0062] In cases where the second base electrode layer **50**B is also provided on a portion of at least one of the first main surface TS**1** or the second main surface TS**2**, the thickness of the second base electrode layer **50**B in this portion in the lamination direction T is, for example, preferably between about 3 μm and about 40 μm inclusive at the center of the

second base electrode layer **50**B in this portion in the length direction L and the width direction W.

[0063] In cases where the second base electrode layer **50**B is also provided on a portion of at least one of the first lateral surface WS**1** or the second lateral surface WS**2**, the thickness of the second base electrode layer **50**B in this portion in the width direction W is, for example, preferably between about 3 μm and about 40 μm inclusive at the center of the second base electrode layer **50**B in this portion in the length direction L and the lamination direction T.

[0064] The external electrode **40** includes the conductive resin layer **60**, which includes resin components and metal components, on the base electrode layer **50**.

[0065] The conductive resin layer **60** includes the first conductive resin layer **60**A and the second conductive resin layer **60**B.

[0066] The first conductive resin layer **60**A covers the first base electrode layer **50**A. In the present example embodiment, the first conductive resin layer **60**A extends from the first end surface LS**1** to a portion of the first main surface TS**1** and the second main surface TS**2**, and a portion of the first lateral surface WS**1** and the second lateral surface WS**2**. The second conductive resin layer **60**B covers the second base electrode layer **50**B. In the present example embodiment, the second conductive resin layer **60**B extends from the second end surface LS**2** to a portion of the first main surface TS**1** and the second main surface TS**2**, and a portion of the first lateral surface WS**1** and the second lateral surface WS**2**. The dimension of the first conductive resin layer **60**A on the first main surface TS**1** and the second main surface TS**2** in the length direction L is longer than the dimension of the first base electrode layer **50**A on the first main surface TS**1** and the second main surface TS**2** in the length direction L. The dimension of the second conductive resin layer **60**B on the first main surface TS**1** and the second main surface TS**2** in the length direction L is longer than the dimension of the second base electrode layer **50**B on the first main surface TS**1** and the second main surface TS**2** in the length direction L.

[0067] The thickness of the first conductive resin layer **60**A on the first end surface LS**1** side in the length direction L is, for example, preferably between about 5 μm and about 200 μm inclusive at the central portion of the first conductive resin layer **60**A in the lamination direction T and width direction W.

[0068] The thickness of the second conductive resin layer **60**B on the second end surface LS**2** side in the length direction L is, for example, preferably between about 5 μm and about 200 μm inclusive at the central portion of the second conductive resin layer **60**B in the lamination direction T and width direction W.

[0069] In the case where the first conductive resin layer **60**A is also provided on a portion of the first main surface TS**1** side and part of the second main surface TS**2** side, the thickness of the first conductive resin layer **60**A in this portion in the lamination direction T is, for example, preferably between about 5 μm and about 200 μm inclusive at the central portion of the first conductive resin layer **60**A in the length direction L and width direction W.

[0070] In the case where the first conductive resin layer **60**A is also provided on a portion of the first lateral surface WS**1** side and part of the second lateral surface WS**2** side, the thickness of the first conductive resin layer **60**A in this portion in the width direction is, for example, preferably between about 5 μm and about 200 μm inclusive at the central portion of the first conductive resin layer **60**A in the length direction L and lamination direction T.

[0071] In the case where the second conductive resin layer **60**B is also provided on a portion of the first main surface TS**1** side and part of the second main surface TS**2** side, the thickness of the second conductive resin layer **60**B in this portion in the lamination direction T is, for example, preferably between about 5 μm and about 200 μm inclusive at the central portion of the second conductive resin layer **60**B in the length direction L and width direction W.

[0072] In the case where the second conductive resin layer **60**B is also provided on a portion of the first lateral surface WS**1** side and part of the second lateral surface WS**2** side, the thickness of the second conductive resin layer **60**B in this portion in the width direction is, for example, preferably between about 5 μm and about 200 μm inclusive, at the central portion of the second conductive resin layer **60**B in the length direction L and lamination direction T.

[0073] The conductive resin layer **60** is provided on the base electrode layer **50**. The plated layer **70** covers the conductive resin layer **60**. The plated layer **70** includes, for example, the Ni plated layer **71** and the Sn plated layer **72**.

[0074] The conductive resin layer **60** includes a resin portion as resin components, and conductive fillers as filler particles dispersed within the resin portion.

[0075] The resin portion of the conductive resin layer **60** may include at least one of various known thermosetting resins such as epoxy resin, phenoxy resin, phenol resin, urethane resin, silicone resin, polyimide resin, etc. Among these, epoxy resin, which has excellent heat resistance, moisture resistance, and adhesiveness, is a suitable resin. The resin portion of the conductive resin layer **60** preferably includes a curing agent, along with the thermosetting resin. In the case of using epoxy resin as the base resin, the curing agent for the epoxy resin may be various known compounds such as, for example, phenolic, amine, anhydride, imidazole, active ester, and amide-imide compounds.

[0076] The conductive resin layer **60**, including such a resin portion, is more flexible than the base electrode layer **50** made of a plating film or a fired material of metal components and glass components. Therefore, the conductive resin layer **60** defines and functions as a buffering layer even when the multilayer ceramic capacitor **1** is subjected to physical shock or thermal-cycling shock. Thus, the conductive resin layer **60** reduces or prevents the occurrence of cracks in the multilayer ceramic capacitor **1**.

[0077] The conductive fillers are dispersed uniformly or substantially uniformly within the resin portion. The conductive fillers primarily ensure the conductivity of the conductive resin layer **60**. Specifically, contact between a plurality of conductive fillers provides conductive pathways within the conductive resin layer **60**, ensuring electrical conductivity between the base electrode layer **50** and the plated layer **70**.

[0078] The metal of the conductive filler may be, for example, pure Ag, an alloy including Ag, or metal powders coated with Ag on their surface. Ag, the resistivity of which is the lowest among metals, is suitable as an electrode material. Being a noble metal, Ag is less prone to oxidation and exhibits high weather resistance. Therefore, Ag metal powders are suitable as conductive fillers. When using metal powders coated with Ag on their surface, it is preferable to use, for example, Cu, Ni, Sn, Bi, or alloy powders thereof.

[0079] The conductive fillers may be, for example, Cu or Ni subjected to an antioxidation treatment. The conductive fillers may also be metal powders coated with, for example, Sn, Ni, Cu on their surface. When using metal powders coated with Sn, Ni, Cu on their surface, the metal powders are preferably, for example, Ag, Cu, Ni, Sn, Bi, or alloys thereof. The conductive fillers preferably include, for example, a core of Cu particles. At least a portion of the surface of the Cu particles is preferably coated with, for example, a Cu-Ag alloy of Cu and Ag. At least a portion of the surface of the Cu particles may be coated with Ag. This improves the affinity with Ni plating and enhances electrical properties.

[0080] The shape of the conductive fillers is not particularly limited. The shape of the conductive fillers can be spherical, flat, etc. It is preferable to use a mixture of spherical and flat metal powders. In other words, the conductive fillers as filler powders include flat powders or spherical powders.

[0081] The average particle size of the conductive fillers may be, for example, between about 0.3 μm and about 10 μm inclusive.

[0082] A method of measuring the average particle size of the conductive fillers included in the conductive resin layer **60** is calculated using a laser diffraction particle size measurement method, based on ISO 13320, instead of the shape of the conductive fillers.

[0083] The plated layer **70** includes the first plated layer **70**A and the second plated layer **70**B.

[0084] The first plated layer **70**A covers the first conductive resin layer **60**A. In the present example embodiment, the first plated layer **70**A extends from the first end surface LS**1** to a portion of the first main surface TS**1** and the second main surface TS**2**, and a portion of the first lateral surface WS**1** and the second lateral surface WS**2**.

[0085] The second plated layer **70**B covers the second conductive resin layer **60**B. In the present example embodiment, the second plated layer **70**B extends from the first end surface LS**1** to a portion of the first main surface TS**1** and the second main surface

[0086] TS**2**, and a portion of the first lateral surface WS**1** and the second lateral surface WS**2**.

[0087] The plated layer **70** preferably includes a two-layer structure including, for example, the Ni plated layer **71** and the Sn plated layer **72**. The first Sn plated layer **72**A is preferably provided on the first Ni plated layer **71**A, and the second Sn plated layer **72**B is preferably provided on the second Ni plated layer **71**B. The Ni plated layer **71** prevents the base electrode layer **50** and the conductive resin layer **60** from being eroded by solder when mounting the multilayer ceramic capacitor **1**. The Sn plated layer **72** improves the solder wettability when mounting the multilayer ceramic capacitor **1**. This facilitates the mounting process of the multilayer ceramic capacitor **1**.

[0088] The thickness of the first Ni plated layer **71**A and the first Sn plated layer **72**A is, for example, preferably between about 1 μm and about 15 μm inclusive.

[0089] The thickness of the second Ni plated layer **71**B and the second Sn plated layer **72**B is, for example, preferably between about 1 μm and about 15 μm inclusive.

[0090] The basic configuration of the multilayer ceramic capacitor **1** according to the present example embodiment has been described above. The dimension of the multilayer ceramic capacitor **1** including the multilayer body **10** and the external electrodes **40** in the length direction L, denoted as the L dimension, is, for example, preferably between about 0.2 mm and about 10 mm inclusive. The dimension of the multilayer ceramic capacitor **1** in the lamination direction T, denoted as the T dimension, is, for example, preferably between about 0.05 mm and about 10 mm inclusive. The dimension of the multilayer ceramic capacitor **1** in the width direction W, denoted as the W dimension, is, for example, preferably between about 0.1 mm and about 10 mm inclusive.

[0091] The multilayer ceramic capacitor **1** of the present example embodiment including the basic configuration has the following characteristics in the external electrodes **40**, which is the first external electrode **40**A and the second external electrode **40**B.

[0092] The external electrodes **40** of the present example embodiment include the main surface-side external electrodes on at least one of the first main surface TS**1** or the second main surface TS**2**. Specifically, as described above, the first external electrode **40**A of the present example embodiment is provided on the first end surface LS**1** and extends from the first end surface LS**1** to a portion of the first main surface TS**1**, a portion of the second main surface TS**2**, a portion of the first lateral surface WS**1**, and a portion of the second lateral surface WS**2**. The first external electrode **40**A of the present example embodiment includes a first end surface-side external electrode **400**A as an end surface-side external electrode on the first end surface LS**1**, a first main surface-side external electrode **411**A as a main surface-side external electrode on the first main surface TS**1**, a second main surface-side external electrode **412**A as a main surface-side external electrode on the second main surface TS**2**, as illustrated in FIGS. **2** and **4**, a first lateral surface-side external electrode **421**A on the first lateral surface WS**1**, and a second lateral surface-side external electrode **422**A on the second lateral surface WS**2**, as illustrated in FIG. **4**.

[0093] As described earlier, the first external electrode **40**A includes the first base electrode layer **50**A, the first conductive resin layer **60**A on the first base electrode layer **50**A, and the first plated layer **70**A on the first conductive resin layer **60**A. In the present example embodiment, the first base electrode layer **50**A extends from the first end surface LS**1** to a portion of the first main surface TS**1** and the second main surface TS**2**, and a portion of the first lateral surface WS**1** and the second lateral surface WS**2**. The first conductive resin layer **60**A covers the first base electrode layer **50**A, and the first plated layer **70**A covers the first conductive resin layer **60**A.

[0094] In other words, as illustrated in FIGS. **2** and **4**, the first end surface-side external electrode **400**A of the present example embodiment includes the first end surface-side base electrode layer **500**A on the first end surface LS**1**, the first end surface-side conductive resin layer **600**A above the first end surface-side base electrode layer **500**A, and the first end surface-side plated layer **700**A above the first end surface-side conductive resin layer **600**A. The first end surface-side base electrode layer **500**A is a portion of the first base electrode layer **50**A. The first end surface-side conductive resin layer **600**A is a portion of the first conductive resin layer **60**A. The first end surface-side plated layer **700**A is a portion of the first plated layer **70**A, and includes the first Ni plated layer **71**A and the first Sn plated layer **72**A on the first Ni plated layer **71**A.

[0095] As illustrated in FIG. **2**, the first main surface-side external electrode **411**A of the present example embodiment includes the first main surface-side base electrode layer **511**A as the main surface-side base electrode layer on the first main surface TS**1**, the first main surface-side conductive resin layer **611**A as the main surface-side conductive resin layer above the first main surface-side base electrode layer **511**A, and the first main surface-side plated layer **711**A as the main surface-side plated layer above the first main surface-side conductive resin layer **611**A. The first main surface-side base electrode layer **511**A is a portion of the first base electrode layer **50**A. The first main surface-side conductive resin layer **611**A is a portion of the first conductive resin layer **60**A. The first main surface-side plated layer **711**A, a portion of the first plated layer **70**A, and includes the first Ni plated layer **71**A and the first Sn plated layer **72**A on the first Ni plated layer **71**A.

[0096] As illustrated in FIG. **2**, the second main surface-side external electrode **412**A of the present example embodiment includes the second main surface-side base electrode layer **512**A as the main surface-side base electrode layer on the second main surface TS**2**, the second main surface-side conductive resin layer **612**A as the main surface-side conductive resin layer above the second main surface-side base electrode layer **512**A, and the second main surface-side plated layer **712**A as the main surface-side plated layer above the second main surface-side conductive resin layer **612**A. The second main surface-side base electrode layer **512**A is a portion of the first base electrode layer **50**A. The second main surface-side conductive resin layer **612**A is a portion of the first conductive resin layer **60**A. The second main surface-side plated layer **712**A is a portion of the first plated layer **70**A, and includes the first Ni plated layer **71**A and the first Sn plated layer **72**A on the first Ni plated layer **71**A.

[0097] As illustrated in FIG. **4**, the first lateral surface-side external electrode **421**A of the present example embodiment includes the first lateral surface-side base electrode layer **521**A on the first lateral surface WS**1**, the first lateral surface-side conductive resin layer **621**A above the first lateral surface-side base electrode layer **521**A, and the first lateral surface-side plated layer **721**A above the first lateral surface-side conductive resin layer **621**A. The first lateral surface-side base electrode layer **521**A is part of the first base electrode layer **50**A. The first lateral surface-side conductive resin layer **621**A is a portion of the first conductive resin layer **60**A. The first lateral surface-side plated layer **721**A is a portion of the first plated layer **70**A, and includes the first Ni plated layer **71**A and the first Sn plated layer **72**A on the first Ni plated layer **71**A.

[0098] As illustrated in FIG. **4**, the second lateral surface-side external electrode **422**A of the present example embodiment includes the second lateral surface-side base electrode layer **522**A on the second lateral surface WS**2**, the second lateral surface-side conductive resin layer **622**A above the second lateral surface-side base electrode layer **522**A, and the second lateral surface-side plated layer **722**A above the second lateral surface-side conductive resin layer **622**A. The second lateral surface-side base electrode layer **522**A is a portion of the first base electrode layer **50**A. The second lateral surface-side conductive resin layer **622**A is a portion of the first conductive resin layer **60**A. The second lateral surface-side plated layer **722**A is a portion of the first plated layer **70**A, and includes the first Ni plated layer **71**A and the first Sn plated layer **72**A on the first Ni plated layer **71**A.

[0099] The thickness of the first main surface-side base electrode layer **511**A, the second main surface-side base electrode layer **512**A, the first lateral surface-side base electrode layer **521**A, and the second lateral surface-side base electrode layer **522**A is, for example, preferably between about 5 μm and about 10 μm inclusive.

[0100] The thickness of the first Ni plated layer **71**A and the first Sn plated layer **72**A, in the first main surface-side plated layer **711**A, the second main surface-side plated layer **712**A, the first lateral surface-side plated layer **721**A, and the second lateral surface-side plated layer **722**A, is, for example, preferably between about 1 μm and about 4 μm inclusive.

[0101] As described above, the second external electrode **40**B of the present example embodiment is provided on the second end surface LS**2** and extends from the second end surface LS**2** to a portion of the first main surface TS**1**, a portion of the second main surface TS**2**, a portion of the first lateral surface WS**1**, and a portion of the second lateral surface WS**2**. Specifically, the second external electrode **40**B of the present example embodiment includes a second end surface-side external electrode **400**B as an end surface-side external electrode on the second end surface LS**1**, a first main surface-side external electrode **411**B as a main surface-side external electrode on the first main surface TS**1**, a second main surface-side external electrode **412**B as a main surface-side external electrode on the second main surface TS**2**, as illustrated in FIG. **2**, a first lateral surface-side external electrode **421**B on the first lateral surface WS**1**, and a second lateral surface-side external electrode **422**B on the second lateral surface WS**2**, as illustrated in FIG. **4**.

[0102] As described earlier, the second external electrode **40**B includes the second base electrode layer **50**B, the second conductive resin layer **60**B on the second base electrode layer **50**B, and the second plated layer **70**B on the second conductive resin layer **60**B. In the present example embodiment, the second base electrode layer **50**B extends from the second end surface LS**2** to a portion of the first main surface TS**1** and the second main surface TS**2**, and a portion of the first lateral surface WS**1** and the second lateral surface WS**2**. The second conductive resin layer **60**B covers the second base electrode layer **50**B, and the second plated layer **70**B covers the second conductive resin layer **60**B.

[0103] In other words, as illustrated in FIGS. **2** and **4**, the second end surface-side external electrode **400**B of the present example embodiment includes the second end surface-side base electrode layer **500**B on the second end surface LS**2**, the second end surface-side conductive resin layer **600**B above the second end surface-side base electrode layer **500**B, and the second end surface-side plated layer **700**B above the second end surface-side conductive resin layer **600**B. The second end surface-side base electrode layer **500**B is a portion of the second base electrode layer **50**B. The second end surface-side conductive resin layer **600**B is a portion of the second conductive resin layer **60**B. The second end surface-side plated layer **700**B is a portion of the second plated layer **70**B, and includes the second Ni plated layer **71**B and the second Sn plated layer **72**B on the second Ni plated layer **71**B.

[0104] As illustrated in FIG. **2**, the first main surface-side external electrode **411**B of the present example embodiment includes the first main surface-side base electrode layer

511B as the main surface-side base electrode layer on the first main surface TS**1**, the first main surface-side conductive resin layer **611**B as the main surface-side conductive resin layer above the first main surface-side base electrode layer **511**B, and the first main surface-side plated layer **711**B as the main surface-side plated layer above the first main surface-side conductive resin layer **611**B. The first main surface-side base electrode layer **511**B is a portion of the second base electrode layer **50**B. The first main surface-side conductive resin layer **611**B is a portion of the second conductive resin layer **60**B. The first main surface-side plated layer **711**B is a portion of the second plated layer **70**B, and includes the second Ni plated layer **71**B and the second Sn plated layer **72**B on the second Ni plated layer **71**B.

[0105] As illustrated in FIG. **2**, the second main surface-side external electrode **412**B of the present example embodiment includes the second main surface-side base electrode layer **512**B as the main surface-side base electrode layer on the second main surface TS**2**, the second main surface-side conductive resin layer **612**B as the main surface-side conductive resin layer above the second main surface-side base electrode layer **512**B, and the second main surface-side plated layer **712**B as the main surface-side plated layer above the second main surface-side conductive resin layer **612**B. The second main surface-side base electrode layer **512**B is a portion of the second base electrode layer **50**B. The second main surface-side conductive resin layer **612**B is a portion of the second conductive resin layer **60**B. The second main surface-side plated layer **712**B is a portion of the second plated layer **70**B, and includes the second Ni plated layer **71**B and the second Sn plated layer **72**B on the second Ni plated layer **71**B.

[0106] As illustrated in FIG. **4**, the first lateral surface-side external electrode **421**B of the present example embodiment includes the first lateral surface-side base electrode layer **521**B on the first lateral surface WS**1**, the first lateral surface-side conductive resin layer **621**B above the first lateral surface-side base electrode layer **521**B, and the first lateral surface-side plated layer **721**B above the first lateral surface-side conductive resin layer **621**B. The first lateral surface-side base electrode layer **521**B is a portion of the second base electrode layer **50**B. The first lateral surface-side conductive resin layer **621**B is a portion of the second conductive resin layer **60**B. The first lateral surface-side plated layer **721**B is a portion of the second plated layer **70**B, and includes the second Ni plated layer **71**B and the second Sn plated layer **72**B on the second Ni plated layer **71**B.

[0107] As illustrated in FIG. **4**, the second lateral surface-side external electrode **422**B of the present example embodiment includes the second lateral surface-side base electrode layer **522**B on the second lateral surface WS**2**, the second lateral surface-side conductive resin layer **622**B above the second lateral surface-side base electrode layer **522**B, and the second lateral surface-side plated layer **722**B above the second lateral surface-side conductive resin layer **622**B. The second lateral surface-side base electrode layer **522**B is portion of the second base electrode layer **50**B.

[0108] The second lateral surface-side conductive resin layer **622**B is a portion of the second conductive resin layer **60**B. The second lateral surface-side plated layer **722**B is a portion of the second plated layer **70**B, and includes the second Ni plated layer **71**B and the second Sn plated layer **72**B on the second Ni plated layer **71**B.

[0109] The thickness of the first main surface-side base electrode layer **511**B, the second main surface-side base electrode layer **512**B, the first lateral surface-side base electrode layer **521**B, and the second lateral surface-side base electrode layer **522**B, is, for example, preferably between about 5 μm and about 10 μm inclusive.

[0110] The thickness of the second Ni plated layer **71**B and the second Sn plated layer **72**B of the first main surface-side plated layer **711**B, the second main surface-side plated layer **712**B, the first lateral surface-side plated layer **721**B, and the second lateral surface-side plated layer **722**B is preferably, for example, between about 1 μm and about 4 μm inclusive.

[0111] FIG. **2** illustrates the LT cross section of the multilayer ceramic capacitor **1** and the multilayer body **10** along the lamination direction T and the length direction L. In the LT cross-sectional view, the first main surface-side external electrode **411**A of the first external electrode **40**A includes a first main surface-side recess **510**A as a recess recessed towards the multilayer body **10** side. The first main surface-side recess **510**A is provided on the surface of the first main surface-side external electrode **411**A.

[0112] The shape of the first main surface-side recess **510**A is a groove extending in the width direction W orthogonal or substantially orthogonal to the LT cross section, i.e., in the direction perpendicular to the paper surface of FIG. **2**. The first main surface-side recess **510**A may be provided over the entire length of the first main surface-side external electrode **411**A along the width direction W. The first main surface-side recess **510**A is provided near the approximate center of the first main surface-side external electrode **411**A in the length direction L.

[0113] As illustrated in FIG. **2**, the second main surface-side external electrode **412**A of the first external electrode **40**A includes a second main surface-side recess **520**A as a recess recessed towards the multilayer body **10** side in the LT cross-sectional view. The second main surface-side recess **520**A is provided on the surface of the second main surface-side external electrode **412**A. The shape of the second main surface-side recess **520**A is a groove extending in the width direction W orthogonal or substantially orthogonal to the LT cross section, i.e., in the direction perpendicular to the paper surface of FIG. **2**. The second main surface-side recess **520**A may be provided over the entire length of the second main surface-side external electrode **412**A along the width direction W. The second main surface-side recess **520**A is provided near the approximate center of the second main surface-side external electrode **412**A in the length direction L.

[0114] As illustrated in FIG. **2**, the first main surface-side external electrode **411**B of the second external electrode **40**B includes a first main surface-side recess **510**B as a recess recessed towards the multilayer body **10** side in the LT cross-sectional view. The first main surface-side recess **510**B is provided on the surface of the first main surface-side external electrode **411**B. The shape of the first main surface-side recess **510**B is a groove extending in the width direction W orthogonal or substantially orthogonal to the LT cross section, i.e., in the direction perpendicular to the paper surface of FIG. **2**. The first main surface-side recess **510**B may be provided over the entire length of the first main surface-side external electrode **411**B along the width direction W. The first main surface-side recess **510**B is provided

near the approximate center of the first main surface-side external electrode **411**B in the length direction L.

[0115] As illustrated in FIG. **2**, the second main surface-side external electrode **412**B of the second external electrode **40**B includes a second main surface-side recess **520**B as a recess recessed towards the multilayer body **10** side in the LT cross-sectional view. The second main surface-side recess **520**B is provided on the surface of the second main surface-side external electrode **412**B. The shape of the second main surface-side recess **520**B is a groove extending in the width direction W orthogonal or substantially orthogonal to the LT cross section, i.e., in the direction perpendicular to the paper surface of FIG. **2**. The second main surface-side recess **520**B may be provided over the entire or substantially the entire length of the second main surface-side external electrode **412**B along the width direction W. The second main surface-side recess **520**B is provided near the approximate center of the second main surface-side external electrode **412**B in the length direction L.

[0116] FIG. **4** illustrates an LW cross section of the multilayer ceramic capacitor **1** and the multilayer body **10** along the length direction L and the width direction W. In the LW cross-sectional views, the first lateral surface-side external electrode **421**A of the first external electrode **40**A includes a first lateral surface-side recess **530**A as a recess recessed towards the multilayer body **10** side. The first lateral surface-side recess **530**A is provided on the surface of the first lateral surface-side external electrode **421**A. The shape of the first lateral surface-side recess **530**A is a groove extending in the lamination direction T orthogonal or substantially orthogonal to the LW cross section, i.e., in the direction perpendicular to the paper surface of FIG. **4**. The first lateral surface-side recess **530**A may be provided over the entire or substantially the entire length of the first lateral surface-side external electrode **421**A along the lamination direction T. The first lateral surface-side recess **530**A is provided near the approximate center of the first lateral surface-side external electrode **421**A in the length direction L. The first lateral surface-side recess **530**A may communicate with either or both of the first main surface-side recess **510**A and the second main surface-side recess **520**A, or may not communicate with both.

[0117] As illustrated in FIG. **4**, the second lateral surface-side external electrode **422**A of the first external electrode **40**A includes a second lateral surface-side recess **540**A as a recess recessed towards the multilayer body **10** side in the LW cross-sectional view. The second lateral surface-side recess **540**A is provided on the surface of the second lateral surface-side external electrode **422**A. The shape of the second lateral surface-side recess **540**A is a groove extending in the lamination direction T orthogonal or substantially orthogonal to the LW cross section, i.e., in the direction perpendicular to the paper surface of FIG. **4**. The second lateral surface-side recess **540**A may be provided over the entire or substantially the entire length of the second lateral surface-side external electrode **422**A along the lamination direction T. The second lateral surface-side recess **540**A is provided near the approximate center of the second lateral surface-side external electrode **422**A in the length direction L. The second lateral surface-side recess **540**A may communicate with either or both of the first main surface-side recess **510**A and the second main surface-side recess **520**A, or may not communicate with both.

[0118] As illustrated in FIG. **4**, the first lateral surface-side external electrode **421**B of the second external electrode **40**B includes a first lateral surface-side recess **530**B as a recess recessed towards the multilayer body **10** side in the LW cross-sectional view. The first lateral surface-side recess **530**B is provided on the surface of the first lateral surface-side external electrode **421**B. The shape of the first lateral surface-side recess **530**B is a groove extending in the lamination direction T orthogonal or substantially orthogonal to the LW cross section, i.e., in the direction perpendicular to the paper surface of FIG. **4**. The first lateral surface-side recess **530**B may be provided over the entire or substantially the entire length of the first lateral surface-side external electrode **421**B along the lamination direction T. The first lateral surface-side recess **530**B is provided near the approximate center of the first lateral surface-side external electrode **421**B in the length direction L. The first lateral surface-side recess **530**B may communicate with either or both of the first main surface-side recess **510**B and the second main surface-side recess **520**B, or may not communicate with both.

[0119] As illustrated in FIG. **4**, the second lateral surface-side external electrode **422**B of the second external electrode **40**B includes a second lateral surface-side recess **540**B as a recess recessed towards the multilayer body **10** side in the LW cross-sectional view. The second lateral surface-side recess **540**B is provided on the surface of the second lateral surface-side external electrode **422**B. The shape of the second lateral surface-side recess **540**B is a groove extending in the lamination direction T orthogonal or substantially orthogonal to the LW cross section, i.e., in the direction perpendicular or substantially perpendicular to the paper surface of FIG. **4**. The second lateral surface-side recess **540**B may be provided over the entire or substantially the entire length of the second lateral surface-side external electrode **422**B along the lamination direction T. The second lateral surface-side recess **540**B is provided near the approximate center of the second lateral surface-side external electrode **422**B in the length direction L. The second lateral surface-side recess **540**B may communicate with either or both of the first main surface-side recess **510**B and the second main surface-side recess **520**B, or may not communicate with both.

[0120] The first main surface-side external electrode **411**A and the second main surface-side external electrode **412**A of the first external electrode **40**A, as well as the first main surface-side external electrode **411**B and the second main surface-side external electrode **412**B of the second external electrode **40**B, share the same or substantially the same configuration. Similarly, the first lateral surface-side external electrode **421**A and the second lateral surface-side external electrode **422**A of the first external electrode **40**A, as well as the first lateral surface-side external electrode **421**B and the second lateral surface-side external electrode **422**B of the second external electrode **40**B, also share the same or substantially the same configuration as the four main surface-side external electrodes **411**A, **412**A, **411**B, and **412**B.

[0121] The first main surface-side recess **510**A and the second main surface-side recess **520**A of the first external electrode **40**A, as well as the first main surface-side recesses **510**B and the second main surface-side recesses **520**B of the second external electrode **40**B, share the same or substantially the same configuration. Similarly, the first lateral

surface-side recess **530**A and the second lateral surface-side recess **540**A of the first external electrode **40**A, as well as the first lateral surface-side recess **530**B and the second lateral surface-side recess **540**B of the second external electrode **40**B, also share the same or substantially the same configuration as the four main surface-side recesses **510**A, **520**A, **510**B, and **520**B.

[0122] Accordingly, the first main surface-side external electrode **411**A and the first main surface-side recess **510**A of the first external electrode **40**A will be described below, representatively describing the four main surface-side external electrodes, the four main surface-side recesses, the four lateral surface-side external electrodes, and the four lateral surface-side recesses.

[0123] The first main surface-side external electrode **411**A of the first external electrode **40**A corresponds to the second main surface-side external electrode **412**A, the first lateral surface-side external electrode **421**A, and the second lateral surface-side external electrode **422**A of the first external electrode **40**A, as well as the first main surface-side external electrode **411**B, the second main surface-side external electrode **412**B, the first lateral surface-side external electrode **421**B, and the second lateral surface-side external electrode **422**B of the second external electrode **40**B. The first main surface-side recess **510**A of the first external electrode **40**A corresponds to the second main surface-side recess **520**A, the first lateral surface-side recess **530**A, and the second lateral surface-side recess **540**A of the first external electrode **40**A, as well as the first main surface-side recesses **510**B, the second main surface-side recesses **520**B, the first lateral surface-side recess **530**B, and the second lateral surface-side recess **540**B of the second external electrode **40**B.

[0124] The first base electrode layer **50**A, the first conductive resin layer **60**A, and the first plated layer **70**A of the first external electrode **40**A correspond to the second base electrode layer **50**B, the second conductive resin layer **60**B, and the second plated layer **70**B of the second external electrode **40**B, respectively. The first Ni plated layer **71**A and the first Sn plated layer **72**A of the first plated layer **70**A of the first external electrode **40**A correspond to the second Ni plated layer **71**B and the second Sn plated layer **72**B of the second plated layer **70**B of the second external electrode **40**B, respectively.

[0125] FIGS. **5**A and **5**B are both enlarged views of the portion indicated by V in FIG. **2**, illustrating the LT cross-sectional view of the first main surface-side external electrode **411**A of the first external electrode **40**A. FIGS. **5**A and **5**B illustrate the XYZ orthogonal coordinate system similar to that in FIGS. **1** to **4**. In

[0126] FIGS. **5**A and **5**B, hatching is omitted to clearly illustrate symbols, leader lines, and dimension lines.

[0127] As illustrated in FIGS. **5**A and **5**B, the first main surface-side external electrode **411**A of the first external electrode **40**A includes the first main surface-side base electrode layer **511**A on the first main surface TS**1** and the first main surface-side conductive resin layer **611**A, and the first main surface-side plated layer **711**A including the first Ni plated layer **71**A and the first Sn plated layer **72**A. The first main surface-side recess **510**A is formed by the three layers being recessed towards the multilayer body **10** side in the lamination direction T (the Z direction in FIGS. **5**A and **5**B), in which the three layers include the outermost first Sn plated layer **72**A, the first Ni plated layer **71**A beneath the first Sn plated layer **72**A, and the first main surface-side conductive resin layer **611**A beneath the first Ni plated layer **71**A.

[0128] As illustrated in FIGS. **5**A and **5**B, the surface of the first main surface-side external electrode **411**A includes the first main surface-side recess **510**A, and also includes a first bulge **710** and a second bulge **720**. The first bulge **710** is provided on the inner side of the first main surface-side recess **510**A in the length direction L, i.e., on the central side of the multilayer body **10** in the length direction L (away from the first end surface LS**1** in the length direction L). The second bulge **720** is provided on the outer side of the first main surface-side recess **510**A in the length direction L, i.e., on the outer side of the multilayer body **10** in the length direction L (closer to the first end surface LS**1** in the length direction L). In other words, the first main surface-side external electrode **411**A includes the first main surface-side recess **510**A, as well as the first bulge **710** on the central side of the multilayer body **10** in the length direction L, and the second bulge **720** on the end portion side of the multilayer body **10** in the length direction L, between which the first main surface-side recess **510**A is interposed.

[0129] The reference number **700** in FIG. **5**A represents a region of the first main surface-side recess **510**A in the length direction L, in the example embodiment. The region **700** of the first main surface-side recess **510**A in the length direction L is based on the distance in the length direction L between a first midpoint **510***m***1**, which connects a deepest portion **510***d* of the first main surface-side recess **510**A to a vertex **710***p* of the first bulge **710**, and a second midpoint **510***m***2**, which connects the deepest portion **510***d* of the first main surface-side recess **510**A to a vertex **720***p* of the second bulge **720**. The deepest portion **510***d* of the first main surface-side recess **510**A refers to the portion closest to the first main surface TS**1** of the multilayer body **10** in the lamination direction T, in the first main surface-side recess **510**A. The vertex **710***p* of the first bulge **710** is the point farthest from the first main surface TS**1** of the multilayer body **10** in the lamination direction T, on the surface of the first bulge **710**. The vertex **720***p* of the second bulge **720** is the point farthest from the first main surface TS**1** of the multilayer body **10** in the lamination direction T, on the surface of the second bulge **720**.

[0130] The distance between the vertex **710***p* of the first bulge **710** and the first main surface TS**1** of the multilayer body **10** in the lamination direction T is the height **710**H of the first bulge **710**. The distance between the vertex **720***p* of the second bulge **720** and the first main surface TS**1** of the multilayer body **10** in the lamination direction T is the height **720**H of the second bulge **720**.

[0131] In the example embodiment, the height **710**H of the first bulge **710** is preferably higher than the height **720**H of the second bulge **720**. The height **710**H of the first bulge **710** and the height **720**H of the second bulge **720** may be the same or different. In the cases of being different, the height **710**H of the first bulge **710** may be higher or lower than the height **720**H of the second bulge **720**.

[0132] In the present example embodiment, the depth D of the first main surface-side recess **510**A refers to the shortest distance between the deepest portion **510***d* and the line connecting the vertex **710***p* of the first bulge **710** and the vertex **720***p* of the second bulge **720**.

[0133] In the present example embodiment, the depth D of the first main surface-side recess **510**A is, for example, preferably between about 3 μm and about 10 μm inclusive.

[0134] In the present example embodiment, the depth D of the first main surface-side recess **510**A is preferably greater than the thickness of the Ni plated layer **71**A in the lamination direction T, in the first main surface-side external electrode **411**A.

[0135] As illustrated in FIG. **5**A, in the present example embodiment, the distance L**1** between the vertex **710***p* of the first bulge **710** and the vertex **720***p* of the second bulge **720** in the length direction L is, for example, preferably between about 100 μm and about 400 μm inclusive.

[0136] As illustrated in FIG. **5**A, the distance L**1** is preferably longer than the distance L**2** between the inner end portion **411***e* of the first main surface-side external electrode **411**A in the length direction L and the vertex **710***p* of the first bulge **710** in the length direction L.

[0137] FIG. **2** illustrates the length L**4** of the end surface-side outer layer portion LG (first end surface-side outer layer portion LG**1**, second end surface-side outer layer portion LG**2**) of the multilayer body **10** in the length direction L. FIG. **5**A illustrates the length L**4** of the first end surface-side outer layer portion LG**1** in the length direction L. In the present example embodiment, the distance L**1** between the vertex **710***p* of the first bulge **710** and the vertex **720***p* of the second bulge **720** in the length direction L is preferably longer than the length L**4** of the first end surface-side outer layer portion LG**1** of the multilayer body **10** in the length direction L.

[0138] The distance L**1** is preferably greater than the maximum thickness of the first main surface-side external electrode **411**A in the lamination direction T. The distance L**1** is preferably greater than the maximum thickness of the first main surface-side conductive resin layer **611**A in the lamination direction T. The distance L**1** is preferably greater than the maximum thickness of the first main surface-side base electrode layer **511**A in the lamination direction T.

[0139] As illustrated in FIG. **5**A, the distance L**3** between the inner end portion **411***e* of the first main surface-side external electrode **411**A in the length direction L and the deepest portion **510***d* of the first main surface-side recess **510**A in the length direction L is preferably longer than the length L**4** of the end surface-side outer layer portion LG of the multilayer body **10** in the length direction L. The distance L**3** is, for example, preferably at least about 300 μm.

[0140] In the present example embodiment, the depth D of the first main surface-side recess **510**A is, for example, preferably between about 5% and about 15% inclusive, of the maximum thickness of the first main surface-side external electrode **411**A in the lamination direction T.

[0141] As illustrated in FIG. **5**A, in the present example embodiment, the distance L**5** between the inner end portion **560***a* of the first main surface-side base electrode layer **511**A and the deepest portion **510***d* of the first main surface-side recess **510**A in the length direction L is, for example, preferably between about 15 μm and about 150 μm inclusive.

[0142] As illustrated in FIG. **5**A, in the present example embodiment, the distance L**6** between the inner end portion **560***a* of the first main surface-side base electrode layer **511**A and the vertex **710***p* of the first bulge **710** in the length direction L is, for example, preferably between about 100 μm and about 300 μm inclusive.

[0143] The first main surface-side recess **510**A includes the three layers being recessed towards the multilayer body **10** side in the lamination direction T, in which the three layers include the outermost first Sn plated layer **72**A, the first Ni plated layer **71**A beneath the first Sn plated layer **72**A, and the first main surface-side conductive resin layer **611**A beneath the first Ni plated layer **71**A. That is, the first main surface-side base electrode layer **511**A does not include a recess recessed towards the multilayer body **10** side in the lamination direction T.

[0144] As illustrated in FIG. **5**B, in the LT cross-sectional view along the lamination direction T and the length direction L, the first main surface-side conductive resin layer **611**A includes a conductive resin layer recess **611***c* that is recessed towards the multilayer body **10** side at the boundary interface **611***k* with the first Ni plated layer **71**A of the first main surface-side plated layer **711**A. The conductive resin layer recess **611***c* is formed substantially at the same position as the first main surface-side recess **510**A in the length direction L, corresponding to the first main surface-side recess **510**A in the length direction L. The region of the conductive resin layer recess **611***c* in the length direction L corresponds to the region of the first main surface-side recess **510**A in the length direction L (indicated by the reference numeral **700** in FIG. **5**A).

[0145] As illustrated in FIG. **5**B, in the LT cross-sectional view, the deepest portion **611***d* of the conductive resin layer recess **611***c* is provided more inward than the inner end portion **560***a* of the first main surface-side base electrode layer **511**A, i.e., towards the central side of the multilayer body **10** in the length direction L. The deepest portion **611***d* of the conductive resin layer recess **611***c* refers to the portion closest to the first main surface TS**1** of the multilayer body **10** in the lamination direction T, within the conductive resin layer recess **611***c*.

[0146] The thickness **611***t* of the first main surface-side conductive resin layer **611**A at the deepest portion **611***d* of the conductive resin layer recess **611***c* is, for example, preferably between about 5 μm and about 20 μm inclusive. The thickness **611***t* is the distance between the deepest portion **611***d* and the first main surface TS**1** in the lamination direction T.

[0147] As illustrated in FIG. **5**B, in the LT cross-sectional view, the first main surface-side conductive resin layer **611**A includes the conductive resin layer recess **611***c*, as well as a first conductive resin layer bulge **810** and a second conductive resin layer bulge **820**. The first conductive resin layer bulge **810** is provided on the inner side of the conductive resin layer recess **611***c* in the length direction L. The second conductive resin layer bulge **820** is formed on the outer side of the conductive resin layer recess **611***c* in the length direction L. In other words, the first main surface-side conductive resin layer **611**A includes the conductive resin layer recess **611***c*, as well as the first conductive resin layer bulge **810** on the central side of the multilayer body **10** in the length direction L, and the second conductive resin layer bulge **820** on the end portion side of the multilayer body **10** in the length direction L, between which the conductive resin layer recess **611***c* is interposed.

[0148] The surface of multilayer body **10** closest to, i.e., at the shortest distance from, the vertexes **810***p* of the first conductive resin layer bulge **810** and the vertex **820***p* of the

second conductive resin layer bulge **820**, is the first main surface TS**1**. The distance between the vertex **810***p* of the first conductive resin layer bulge **810** and the first main surface TS**1** of multilayer body **10** in the lamination direction T is the height **810**H of the first conductive resin layer bulge **810**. Similarly, the distance between the vertex **820***p* of the second conductive resin layer bulge **820** and the first main surface TS**1** of multilayer body **10** in the lamination direction T is the height **820**H of the second conductive resin layer bulge **820**.

[0149] In the present example embodiment, the height **810**H of the first conductive resin layer bulge **810** is preferably higher than the height **820**H of the second conductive resin layer bulge **820**. The height **810**H of the first conductive resin layer bulge **810** and the height **820**H of the second conductive resin layer bulge **820** may be the same or different. In the cases of being different, as mentioned, the height **810**H of the first conductive resin layer bulge **810** may be higher or lower than the height **820**H of the second conductive resin layer bulge **820**.

[0150] In the present example embodiment, the height **810**H of the first conductive resin layer bulge **810** is, for example, preferably between about 15 μm and about 30 μm inclusive. On the other hand, the height **820**H of the second conductive resin layer bulge **820** is, for example, preferably between about 5 μm and about 20 μm inclusive.

[0151] The multilayer ceramic capacitor **1** of the present example embodiment is mounted on a board. Mounting to the board may involve, for example, soldering, where the external electrodes **40** are joined to terminals on the board. When the first main surface-side external electrode **411**A is joined to the board by soldering, the flexure stress generated in the first main surface-side external electrode **411**A concentrates particularly at the inner end portion **411***e* of the first main surface-side external electrode **411**A or the inner end portion **611***e* of the first main surface-side conductive resin layer **611**A as illustrated in FIG. **5**B, and transmits as tensile stress to the multilayer body **10**, potentially causing cracks or the like in the multilayer body **10**. In the example embodiment of the multilayer ceramic capacitor **1**, the first main surface-side external electrode **411**A includes the first main surface-side recess **510**A, and the first main surface-side conductive resin layer **611**A includes the conductive resin layer recess **611***c*, thereby dispersing the flexure stress to the first main surface-side recess **510**A and the conductive resin layer recess **611***c* or around these recesses. This advantageous effect mitigates the flexure stress, thus reducing or preventing the occurrence of cracks in the multilayer body **10**. As a result, durability under harsh conditions is improved.

[0152] When the first main surface-side external electrode **411**A of the multilayer ceramic capacitor **1** according to the present example embodiment is mounted to a board, namely, joined by soldering, the vertex **710***p* of the first bulge **710** and the vertex **720***p* of the second bulge **720**, which are separated in the length direction L, between which the first main surface-side recess **510**A is interposed, are placed on the surface of the terminals or the like of the board. In other words, the first main surface-side external electrode **411**A is joined to the board, in the state supported at two points. The solder enters inside the first main surface-side recess **510**A and contacts the inner surface of the first main surface-side recess **510**A. The distance L**1** between the vertex **710***p* of the first bulge **710** and the vertex **720***p* of the second bulge **720** in the length direction L is longer than the distance L**2** between the inner end portion **411***e* of the first main surface-side external electrode **411**A in the length direction L and the vertex **710***p* of the first bulge **710** in the length direction L. As a result, the inner surface area of the first main surface-side recess **510**A increases, enlarging the contact area for the solder. Consequently, even if the shape of the surface of the first main surface-side external electrode **411**A is rounded along the length direction L, the effective ground contact area with the board is increased in combination with the state supported at two points, thereby strengthening the bond between the board and the capacitor. In other words, the multilayer ceramic capacitor **1** of the present example embodiment facilitates stability during board mounting.

[0153] The dimensions such as the thickness of each layer of the first main surface-side external electrode **411**A, the depth of the first main surface-side recess **510**A, and the heights of the bulges are measured, for example, by the following example method. Namely, the multilayer ceramic capacitor **1** is polished from either the first lateral surface WS**1** or the second lateral surface WS**2** to approximately half of the width dimension W. This exposes the LT cross section at the middle position of the multilayer ceramic capacitor **1** in the width direction W. Next, the dimensions in the LT cross section exposed by polishing are measured using a digital microscope.

[0154] Next, an example of a method of manufacturing the multilayer ceramic capacitor **1** according to the present example embodiment will be described. The method of manufacturing the multilayer ceramic capacitor **1** according to the present example embodiment is not limited, as long as the requirements described above are satisfied. However, a preferable manufacturing method includes the following steps. The details of each step are described below.

[0155] A dielectric sheet for the dielectric layer **20** and a conductive paste for the internal electrode layer **30** are prepared. The dielectric sheet and the conductive paste for the internal electrode layer include binders and solvents. The binders and solvents may be any known ones.

[0156] The conductive paste for the internal electrode layer **30** is printed in a predetermined pattern on the dielectric sheet, for example, by screen printing or gravure printing. As a result, a dielectric sheet with a pattern of the first internal electrode layer **31** and a dielectric sheet with a pattern of the second internal electrode layer **32** are prepared.

[0157] A predetermined number of dielectric sheets without printed patterns of internal electrode layer are stacked, thus forming a portion that becomes the first main surface-side outer layer portion **12**A on the first main surface TS**1** side. On top of this, a dielectric sheet with printed patterns of the first internal electrode layer **31** and a dielectric sheet with printed patterns of the second internal electrode layer **32** are sequentially stacked, thus forming a portion that become the inner layer portion **11**. On top of the portion that become the inner layer portion **11**, a predetermined number of dielectric sheets without printed patterns of internal electrode layer are stacked, thus forming a portion that becomes the second main surface-side outer layer portion **12**B on the second main surface TS**2** side. Thus, a multilayer sheet is produced.

[0158] The multilayer sheet is pressed in the lamination direction using, for example, hydrostatic pressing, thus producing a multilayer block.

[0159] The multilayer block is cut into a predetermined size, thus producing multilayer chips. At this time, the corners and edges of the multilayer chips may be rounded by, for example, barrel polishing.

[0160] The multilayer chips are fired to produce the multilayer body **10**. The firing temperature is, for example, preferably between about 900° C. and about 1400° C. inclusive, depending on the materials of the dielectric layer **20** and the internal electrode layer **30**.

[0161] A conductive paste to become the base electrode layer **50** is applied to both end surfaces of the multilayer body **10**. In the present example embodiment, the base electrode layer **50** is a fired layer. The conductive paste containing glass components and metal components is applied to the multilayer body **10** by methods such as, for example, dipping. Subsequently, a firing process is performed, thus forming the base electrode layer **50**. The temperature during the firing process is, for example, preferably between about 700° C. and about 950° C. inclusive.

[0162] In the present example embodiment, dipping is conducted such that the first base electrode layer **50**A extends from the first end surface LS**1** to a portion of the first main surface TS**1** and the second main surface TS**2**. Similarly, dipping is conducted such that the second base electrode layer **50**B extends from the second end surface LS**2** to a portion of the first main surface TS**1** and the second main surface TS**2**. In this case, dipping is preferably conducted simultaneously such that the first base electrode layer **50**A extends to a portion of the first lateral surface WS**1** and the second lateral surface WS**2**. Similarly, dipping is preferably conducted such that the second base electrode layer **50**B extends to a portion of the first lateral surface WS**1** and the second lateral surface WS**2**.

[0163] The pre-firing multilayer chips and the conductive paste applied to the multilayer chips may be simultaneously fired. In this case, the fired layers are preferably formed by firing a material including a ceramic material instead of glass components. In this case, as the ceramic material to be added, a ceramic material of the same type as the dielectric layer **20** is particularly preferably used. In this case, a conductive paste is applied to the pre-firing multilayer chips, and the multilayer chips as well as the conductive paste applied to the multilayer chips are simultaneously fired, thus forming the multilayer body **10** with the fired layers.

[0164] Next, the conductive resin layer **60** is formed. In the present example embodiment, the conductive resin layer **60** is formed on the surface of the base electrode layer **50** and a portion of the surface of the multilayer body **10**.

[0165] First, a conductive resin paste is prepared, in which conductive fillers are dispersed within the thermosetting resin as the base resin that becomes the resin portion. The conductive resin paste is produced by stirring and mixing the thermosetting resin and the conductive fillers. Therefore, the conductive fillers are uniformly dispersed within the conductive resin paste. Here, the thermosetting resin is, for example, epoxy resin. The conductive filler is, for example, Ag metal powder.

[0166] Subsequently, the conductive resin paste is applied onto the base electrode layer **50** using, for example, a dipping method, and a thermal treatment is conducted, for example, at temperature between about 200° C. and about 550° C. inclusive. This process thermally cures the resin portion, thus forming the conductive resin layer **60**. The atmosphere during this heat treatment is, for example, preferably nitrogen (N_2). The oxygen concentration is preferably maintained at, for example, about 100 ppm or below to prevent the resin from scattering and the various metal components from oxidizing.

[0167] In the present example embodiment, dipping is conducted such that the first conductive resin layer **60**A extends from the first end surface LS**1** to a portion of the first main surface TS**1** and the second main surface TS**2**. Similarly, dipping is conducted such that the second conductive resin layer **60**B extends from the second end surface LS**2** to a portion of the first main surface TS**1** and the second main surface TS**2**. In this case, for example, dipping is preferably conducted simultaneously such that the first conductive resin layer **60**A extends to a portion of the first lateral surface WS**1** and the second lateral surface WS**2**. Similarly, for example, dipping is preferably conducted such that the second conductive resin layer **60**B extends to a portion of the first lateral surface WS**1** and the second lateral surface WS**2**.

[0168] Afterwards, the plated layer **70** is formed on the surface of the conductive resin layer **60**. In the present example embodiment, the Ni plated layer **71** and the Sn plated layer **72** are formed on the conductive resin layer **60**. The Ni plated layer **71** and the Sn plated layer **72** are sequentially formed using, for example, an electroplating method. Barrel plating, for example, is a preferred method of plating.

[0169] The following may be an example of a method of forming the groove-shaped recesses in the main surface-side external electrodes and the lateral surface-side external electrodes of the external electrodes **40** as in the present example embodiment.

[0170] FIGS. **6**A to **6**C schematically illustrate the steps of forming the base electrode layer **50** and the conductive resin layer **60** with this method. As illustrated in FIG. **6**A, the base electrode paste **50**P, which becomes the base electrode layer **50**, is applied by dipping to the end portions of the multilayer body **10** in the length direction L, then the conductive resin paste **60**P is applied by dipping, which becomes the conductive resin layer **60**. Next, as illustrated in FIG. **6**B, the multilayer body **10** is passed between a pair of rod-shaped tools **90** facing each other. The passage direction herein is the direction perpendicular or substantially perpendicular to the paper surface of FIG. **6**B. As a result, as illustrated in FIG. **6**C, groove-shaped recesses G are formed on both sides of the conductive resin paste **60**P that is the conductive resin layer **60**, at the tips of the pair of rod-shaped tools **90**. These recesses G become the first main surface-side recess **510**A, the second main surface-side recess **520**A, the first lateral surface-side recess **530**A, the second lateral surface-side recess **540**A, the first main surface-side recess **510**B, the second main surface-side recess **520**B, the first lateral surface-side recess **530**B, and the second lateral surface-side recess **540**B. Thereafter, the Ni plated layer **71** and the Sn plated layer **72** are formed on the conductive resin layer **60**.

[0171] The recesses can also be formed by appropriately adjusting the viscosity of the base electrode paste **50**P and the conductive resin paste **60**P, or by innovating the dipping method.

[0172] The multilayer ceramic capacitor is manufactured through the manufacturing steps described above.

[0173] The configurations of the multilayer ceramic capacitor **1** is not limited to those illustrated in FIGS. **1** to **4**B. For example, the multilayer ceramic capacitor **1** may

include a two-portion structure, a three-portion structure, or a four-portion structure as illustrated in FIGS. **7**A, **7**B, and **7**C.

[0174] The multilayer ceramic capacitor **1** illustrated in FIG. **7**A includes a two-portion structure, including a floating internal electrode layer **35** as a floating inner conductive layer that does not extend to either the first end surface LS**1** or the second end surface LS**2**, in addition to the first internal electrode layer **33** and the second internal electrode layer **34** as the internal electrode layer **30**.

[0175] The multilayer ceramic capacitor **1** illustrated in FIG. **7**B includes a three-portion structure, including a first floating internal electrode layer **35**A and a second floating internal electrode layer **35**B, as the floating internal electrode layer **35**.

[0176] The multilayer ceramic capacitor **1** illustrated in FIG. **7**C includes a four-portion structure, including the first floating internal electrode layer **35**A, the second floating internal electrode layer **35**B, and a third floating internal electrode layer **35**C, as the floating internal electrode layer **35**.

[0177] The multilayer ceramic capacitor **1** can be structured with a plurality of divided counter electrode portions by providing the floating internal electrode layers **35** as the internal electrode layer **30**. As a result, a plurality of capacitor components are formed between the counter internal electrode layers **30**, and the capacitor components are connected in series. Therefore, the voltage applied to each capacitor component is reduced, enabling the achievement of high withstand voltage of the multilayer ceramic capacitor **1**. The multilayer ceramic capacitor **1** in the present example embodiment may include a multi-portion structure including four or more portions.

[0178] In the multilayer ceramic capacitors **1** with the structures illustrated in FIGS. **7**A, **7**B, and **7**C, as in the case of the above-described example embodiments, both of the first external electrode **40**A and the second external electrode **40**B include the main surface-side external electrodes that include the main surface-side recesses. Although not illustrated, the conductive resin layers defining each main surface-side external electrode include the conductive resin layer recesses that are recessed towards the side of the multilayer body at the boundary interface with the main surface-side plated layer.

[0179] In the multilayer ceramic capacitors **1** with the structures illustrated in FIGS. **7**A, **7**B, and **7**C, as in the case of the above-described example embodiments, both of the first external electrode **40**A and the second external electrode **40**B include the lateral surface-side external electrodes that include the lateral surface-side recesses. Although not illustrated, the conductive resin layers defining each lateral surface-side external electrode include the conductive resin layer recesses that are recessed towards the side of the multilayer body at the boundary interface with the lateral surface-side plated layer.

[0180] In particular, the multilayer ceramic capacitors **1** with the structures such as the two-portion structure, three-portion structure, and four-portion structure including the floating internal electrode layer **35** illustrated in FIGS. **7**A to **7**C are effective to be used under high voltage. However, compressive stress is preferably applied to the multilayer body **10** as an electrostrictive countermeasure under high voltage, and in order to achieve this, the plating thickness of the external electrodes on the main surfaces and the lateral surfaces of the multilayer body **10** is increased. However, this can lead to a problem where the flexural resistance deteriorates due to increased tensile stress at the inner end portion **411***e* of the external electrode **40** and the inner end portion **611***e* of the conductive resin layer **60**A, as illustrated in FIG. **5**B. However, as in the present example embodiment, for example, the recesses (the first main surface-side recess and the second main surface-side recess) are provided in the main surface-side external electrodes, and the conductive resin layer recesses are provided, thereby allowing for improving the flexural resistance, thus reducing or preventing the occurrence of cracks in the multilayer body **10**.

[0181] The multilayer ceramic capacitor **1** according to the example embodiment can achieve the following effects.

[0182] When mounting the multilayer ceramic capacitor **1** on a board, the contact area for the solder entering the recesses increases, thereby enlarging the effective ground contact area with the board, and facilitating stability during board mounting.

[0183] In the multilayer ceramic capacitor **1** according to the present example embodiment, the multilayer body **10** includes the counter electrode portion **11**E, in which the first internal electrode layer **31** and the second internal electrode layer **32** face each other in the lamination direction T, and end surface-side outer layer portions LG between the counter electrode portion **11**E and the first end surface LS**1**, as well as between the counter electrode portion **11**E and the second end surface LS**2**, respectively. The distance L**1** is preferably longer than the length L**4** of the end surface-side outer layer portion LG in the length direction L.

[0184] This enables a sufficiently long distance L**1** between the vertex **710***p* of the first bulge **710** and the vertex **720***p* of the second bulge **720** in the length direction L. Thus, when mounting the multilayer ceramic capacitor **1** on a board, the ground contact area for the solder entering the recesses increases, thereby enlarging the effective grounding contact area with the board, and facilitating stability during board mounting.

[0185] In the multilayer ceramic capacitor **1** according to the present example embodiment, the distance L**1** is preferably greater than the maximum thickness of the main surface-side external electrode in the lamination direction T.

[0186] This enables a sufficiently long distance L**1** between the vertex **710***p* of the first bulge **710** and the vertex **720***p* of the second bulge **720** in the length direction L. Thus, when mounting the multilayer ceramic capacitor **1** on a board, the ground contact area for the solder entering the recesses increases, thus enlarging the effective grounding contact area with the board, and facilitating stability during board mounting.

[0187] In the multilayer ceramic capacitor **1** according to the present example embodiment, the distance L**3** between the inner end portion **441***e* of the main surface-side external electrode in the length direction and the deepest portion **510***d* of the main surface-side recess in the length direction is longer than the length L**4** of the end surface-side outer layer portion LG in the length direction.

[0188] This also enables a sufficiently long distance L**1** between the vertex **710***p* of the first bulge **710** and the vertex **720***p* of the second bulge **720** in the length direction L. Thus, when mounting the multilayer ceramic capacitor **1** on a board, the ground contact area for the solder entering the

recesses increases, thereby enlarging the effective grounding contact area with the board, and facilitating stability during board mounting.

[0189] In the multilayer ceramic capacitor **1** according to the present example embodiment, the height **710**H of the first bulge **710**, being the shortest distance from the surface of the multilayer body **10** to the vertex **710***p* of the first bulge **710** in the lamination direction T, is preferably higher than the height **720**H of the second bulge **720**, being the distance from the surface of the multilayer body **10** to the vertex **720***p* of the second bulge **720** in the lamination direction T.

[0190] When mounting the multilayer ceramic capacitor **1** on a board, this enables an increased amount of solder between the vertex **720***p* of the second bulge **720** and the surface of the board, thus improving the bonding strength.

[0191] In the multilayer ceramic capacitor **1** according to the present example embodiment, in a cross-sectional view along the lamination direction T and the length direction L, when the shortest distance between the line connecting the vertex **710***p* of the first bulge **710** and the vertex **720***p* of the second bulge **720** and the deepest portion **510***d* of the recess is defined as the depth D of the recess, the depth D is preferably between about 5% and about 15% inclusive of the maximum thickness of the main surface-side external electrode layer.

[0192] This enables for a relatively large depth of the recess, thus increasing the area within the recess and the contact area for the solder. Consequently, the effective ground contact area with the board increases, facilitating stability during board mounting.

[0193] In the multilayer ceramic capacitor **1** according to the present example embodiment, the internal electrode layer **30** includes the floating internal electrode layer **35** as a floating inner conductive layer, which does not extend to either the first end surface LS**1** or the second end surface LS**2**, and which faces at least one of the first internal electrode layer **31** or the second internal electrode layer **32**, in which a dielectric layer **20** of the dielectric layers **20** is interposed between the first internal electrode layer **31** and the second internal electrode layer **32**.

[0194] This enables for high withstand voltage of the multilayer ceramic capacitor **1**.

[0195] In the multilayer ceramic capacitor **1** according to the present example embodiment, the distance L**3** between the inner end portion **411***e* of the first main surface-side external electrode **411**A and the deepest portion **510***d* of the first main surface-side recess **510**A in the length direction L is longer than the length L**4** of the end surface-side outer layer portion LG of the multilayer body **10** in the length direction L, in which the distance L**3** is preferably at least about 300 μm.

[0196] As a result, the region with at least a certain thickness of the first main surface-side external electrode **411**A increases over the distance L**3**, thus improving the mechanical strength of the inner end portion **411***e*, and improving flexural resistance.

[0197] In an example embodiment of the multilayer ceramic capacitor **1**, each of the first external electrode **40**A and the second external electrode **40**B may include a lateral surface-side external electrode, which may also include a recess, as in the case of the main surface-side external electrodes.

[0198] Thus, the multilayer ceramic capacitor **1** according to present the example embodiment includes the multilayer body **10** that includes the dielectric layers **20** as the plurality of ceramic layers, and the internal electrode layers **30** as the plurality of inner conductive layers alternately stacked in the lamination direction T as the height direction. The multilayer body **10** also includes the first main surface TS**1** and the second main surface TS**2** on opposite sides in the lamination direction T, the first end surface LS**1** and the second end surface LS**2** on opposite sides in the length direction L orthogonal or substantially orthogonal to the lamination direction T, and the first lateral surface WS**1** and the second lateral surface WS**2** on opposite sides in the width direction W orthogonal or substantially orthogonal to both the lamination direction T and the length direction L. The multilayer body **10** also includes the pair of external electrodes **40** spaced apart from each other at the end portions of the multilayer body **10** in the length direction L. The internal electrode layers **30** include the first internal electrode layer **31** as the first inner conductive layer extending to the first end surface LS**1**, and the second internal electrode layer **32** as the second inner conductive layer extending to the second end surface LS**2**. The external electrodes **40** include a lateral surface-side external electrode on at least one of the first lateral surface or the second lateral surface. In a cross-sectional view along the height direction and the length direction, the lateral surface-side external electrode includes, on a surface thereof, a recess recessed towards the side of the multilayer body, and the first bulge on the central side of the multilayer body in the length direction and the second bulge at the end portion side of the multilayer body in the length direction. The distance L**1** between the vertex of the first bulge and the vertex of the second bulge in the length direction is longer than the distance L**2** between the inner end portion of the lateral surface-side external electrode and the vertex of the first bulge in the length direction.

[0199] The present invention is not limited to the configurations of the example embodiments and can be appropriately modified and applied within the scope that does not change the scope of the present invention. Combinations of two or more of any individual configurations described in the example embodiments are also included in example embodiments of the present invention.

[0200] For example, the multilayer ceramic capacitor **1** may be a two-terminal multilayer ceramic capacitor including two external electrodes or a multi-terminal multilayer ceramic capacitor including a plurality of external electrodes.

[0201] In example embodiment, the multilayer ceramic capacitor including dielectric ceramics has been described as examples of the multilayer ceramic electronic component. However, the multilayer ceramic electronic component disclosed herein is not limited to this, and various multilayer ceramic electronic components such as piezoelectric components using piezoelectric ceramics, thermistors using semiconductor ceramics, and inductors using magnetic ceramics can also be applied. Examples of piezoelectric ceramics may include PZT (lead zirconate titanate) ceramics, examples of semiconductor ceramics may include spinel ceramics, and examples of magnetic ceramics may include ferrites.

[0202] The external electrodes **40** in the example embodiments include the conductive resin layer **60**. However, the external electrodes **40** do not have to include the conductive resin layer **60**.

[0203] While example embodiments of the present invention have been described above, it is to be understood that variations and modifications will be apparent to those skilled in the art without departing from the scope and spirit of the present invention. The scope of the present invention, therefore, is to be determined solely by the following claims.

1. A multilayer ceramic electronic component comprising:

a multilayer body including a plurality of ceramic layers and a plurality of inner conductive layers stacked alternately in a height direction, a first main surface and a second main surface on opposite sides in the height direction, a first end surface and a second end surface on opposite sides in a length direction orthogonal or substantially orthogonal to the height direction, and a first lateral surface and a second lateral surface on opposite sides in a width direction orthogonal or substantially orthogonal to both the height direction and the length direction; and

a pair of external electrodes spaced apart from each other at both of the first and second end surfaces of the multilayer body in the length direction; wherein

the plurality of inner conductive layers include:

a first inner conductive layer extending to the first end surface; and

a second inner conductive layer extending to the second end surface;

the pair of external electrodes include a main surface-side external electrode on at least one of the first main surface or the second main surface;

in a cross-sectional view along the height direction and the length direction, the main surface-side external electrode includes, on a surface thereof, a recess recessed towards a side of the multilayer body;

a first bulge is provided on a central side of the multilayer body in the length direction, and a second bulge is provided at an end portion side of the multilayer body in the length direction, between which a conductive resin layer the recess is interposed; and

a distance L**1** between a vertex of the first bulge and a vertex of the second bulge in the length direction is longer than a distance L**2** between an inner end portion of the main surface-side external electrode and the vertex of the first bulge in the length direction.

2. The multilayer ceramic electronic component according to claim **1**, wherein

the multilayer body further includes:

a counter electrode portion in which the first inner conductive layer and the second inner conductive layer face each other in the height direction; and

an end surface-side outer layer portion between the counter electrode portion and the first end surface and between the counter electrode portion and the second end surface;

the distance L**1** is longer than a length L**4** of the end surface-side outer layer portion in the length direction.

3. The multilayer ceramic electronic component according to claim **1**, wherein the distance L**1** is greater than a maximum thickness of the main surface-side external electrode in the height direction.

4. The multilayer ceramic electronic component according to claim **1**, wherein a distance L**3** between the inner end portion of the main surface-side external electrode and a deepest portion of the recess in the length direction is longer than a length L**4** of the end surface-side outer layer portion in the length direction.

5. The multilayer ceramic electronic component according to claim **1**, wherein a height of the first bulge, being a shortest distance from a surface of the multilayer body to the vertex of the first bulge in the height direction, is higher than a height of the second bulge, being a distance from a surface of the multilayer body to the vertex of the second bulge in the height direction.

6. The multilayer ceramic electronic component according to claim **1**, wherein, in a cross-sectional view of the main surface-side external electrode along the height direction and the length direction, when a shortest distance between a line connecting the vertex of the first bulge and the vertex of the second bulge and a deepest portion of the recess is defined as a depth of the recess, the depth of the recess is between about 5% and about 15% inclusive of a maximum thickness of the main surface-side external electrode layer.

7. The multilayer ceramic electronic component according to claim **1**, wherein

the inner conductive layer includes a floating inner conductive layer that does not extend to either of the first end surface or the second end surface, the floating inner conductive layer facing at least one of the first inner conductive layer or the second inner conductive layer; and

a ceramic layer of the plurality of ceramic layers is interposed between the first inner conductive layer and the second inner conductive layer.

8. The multilayer ceramic electronic component according to claim **1**, wherein

a dimension of the multilayer body in the length direction is between about 0.2 mm and about 10 mm inclusive;

a dimension of the multilayer body in the height direction is between about 0.1 mm and about 10 mm inclusive; and

a dimension of the multilayer body in the width direction is between about 0.1 mm and about 10 mm inclusive.

9. The multilayer ceramic electronic component according to claim **1**, wherein each of the plurality of ceramic layers includes at least one of $BaTiO_3$, $CaTiO_3$, $SrTiO_3$, or $CaZrO_3$ as a main component.

10. The multilayer ceramic electronic component according to claim **9**, wherein each of the plurality of ceramic layers includes at least one of Mn compounds, Fe compounds, Cr compounds, Co compounds, or Ni compounds as an accessory component.

11. The multilayer ceramic electronic component according to claim **1**, wherein a thickness of each of the plurality of ceramic layers is between about 0.5 μm and about 30 μm inclusive.

12. The multilayer ceramic electronic component according to claim **1**, wherein a number of the plurality of ceramic layers is between 10 and 1500 inclusive.

13. The multilayer ceramic electronic component according to claim **1**, wherein each of the plurality of inner conductive layers includes at least one of Ni, Cu, Ag, Pd, or Au, or alloys including at least one of Ni, Cu, Ag, Pd, or Au.

14. The multilayer ceramic electronic component according to claim **1**, wherein a thickness of each of the plurality of inner conductive layers is between about 0.2 μm and about 2.0 μm inclusive.

15. The multilayer ceramic electronic component according to claim **1**, wherein a number of the plurality of inner conductive layers is between 10 and 1500 inclusive.

16. The multilayer ceramic electronic component according to claim **1**, wherein each of the pair of external electrodes includes a base electrode layer, a conductive resin layer, and a plated layer.

17. The multilayer ceramic electronic component according to claim **16**, wherein the plate layer includes a Ni plated layer and a Sn plated layer on the Ni plated layer.

18. The multilayer ceramic electronic component according to claim **16**, wherein the base electrode layer includes a metal component and at least one of a glass component or a ceramic component.

19. The multilayer ceramic electronic component according to claim **1**, wherein the metal component includes at least one of Cu, Ni, Ag, Pd, Ag—Pd alloy, or Au.

20. The multilayer ceramic electronic component according to claim **1**, wherein the glass component includes at least one of B, Si, Ba, Mg, Al, or Li.

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