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(54) **MULTI-TIER MEMORY ARRAY INCLUDING LATERALLY-STAGGERED STAIRCASES AND METHOD OF MAKING THE SAME**

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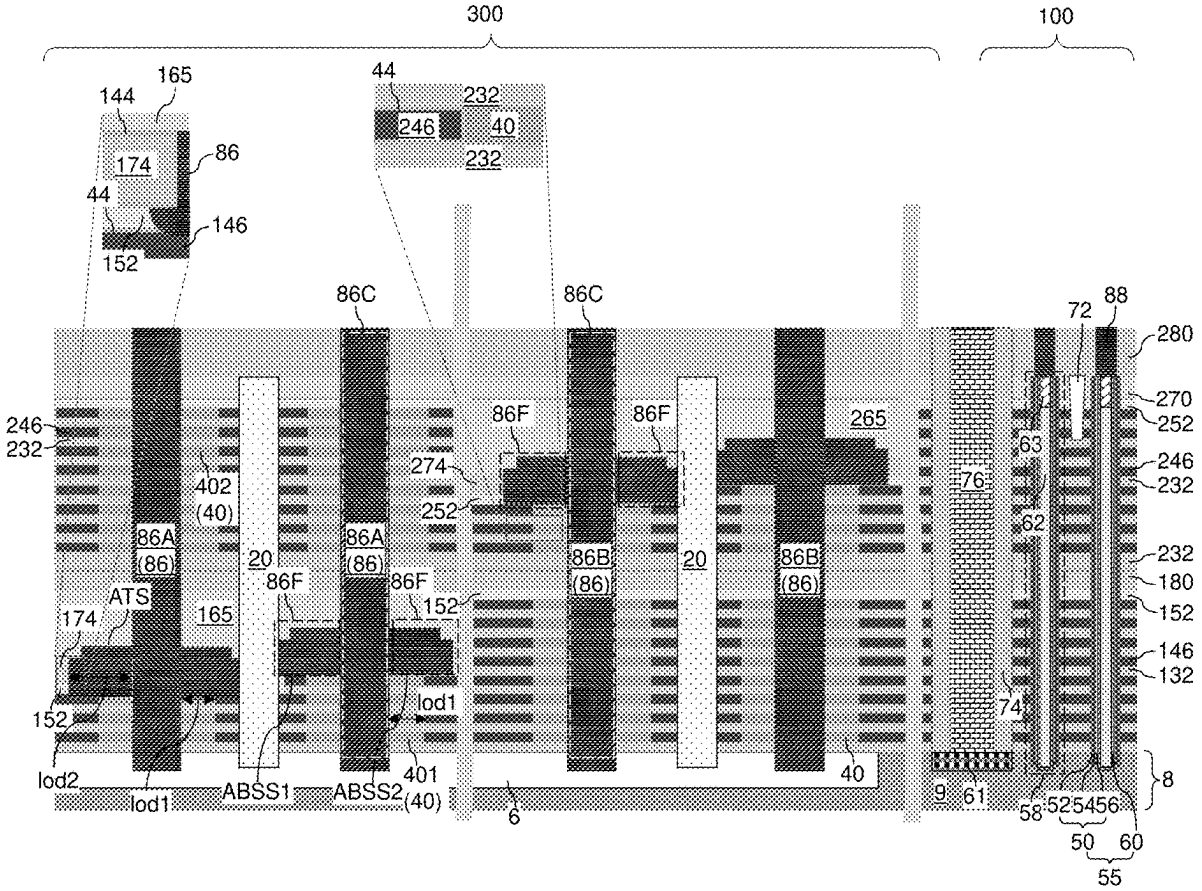
Publication Classification

(51) **Int. Cl.**
H10B 43/27 (2023.01)

(52) **U.S. Cl.**
CPC *H10B 43/27* (2023.02)

(57) **ABSTRACT**

A memory device includes a first-tier alternating stack of first insulating layers and first electrically conductive layers, where the first-tier alternating stack includes a first staircase region having first stepped surfaces, a first-tier retro-stepped dielectric material portion overlying the first stepped surfaces, a second-tier alternating stack of second insulating layers and second electrically conductive layers, where the second-tier alternating stack includes a second staircase region having second stepped surfaces, a second-tier retro-stepped dielectric material portion overlying the second stepped surfaces, memory stack structures vertically extending through each layer within the alternating stacks, and first-type layer contact via structures vertically extending through each layer within the second-tier alternating stack and through the first-tier retro-stepped dielectric material portion. Each of the first-type layer contact via structures contacts a respective one of the first electrically conductive layers.



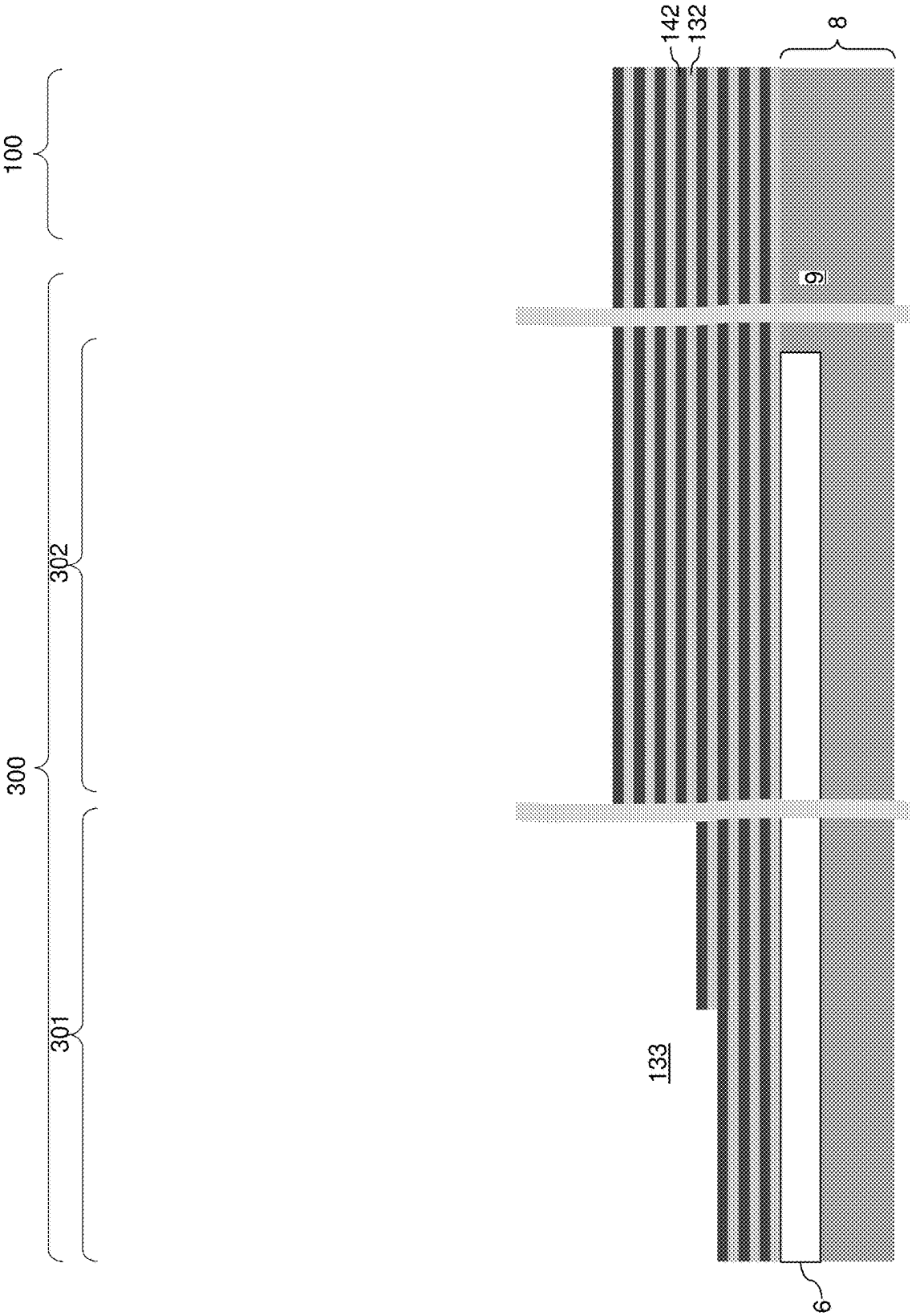


FIG. 1A

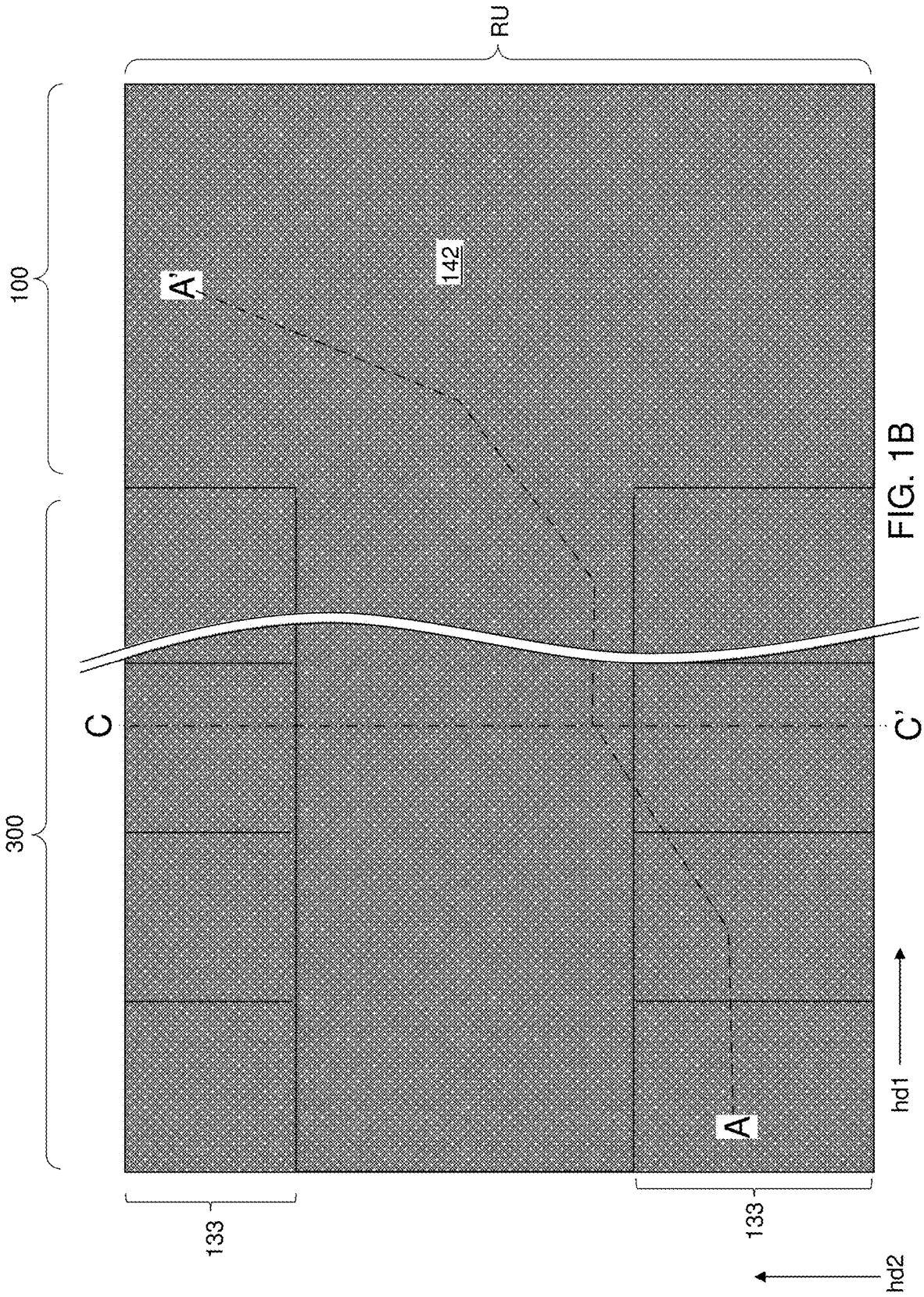


FIG. 1B

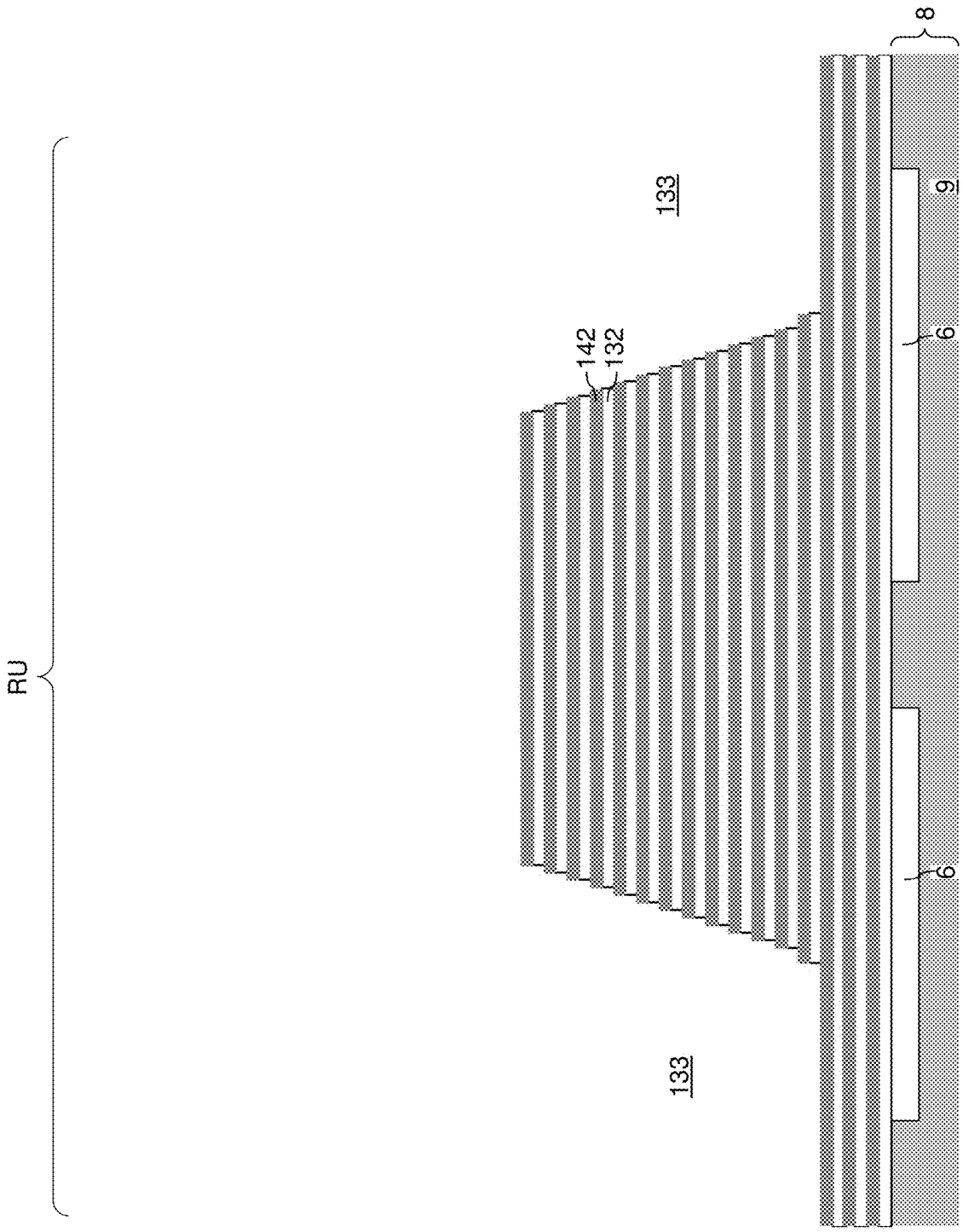


FIG. 1C

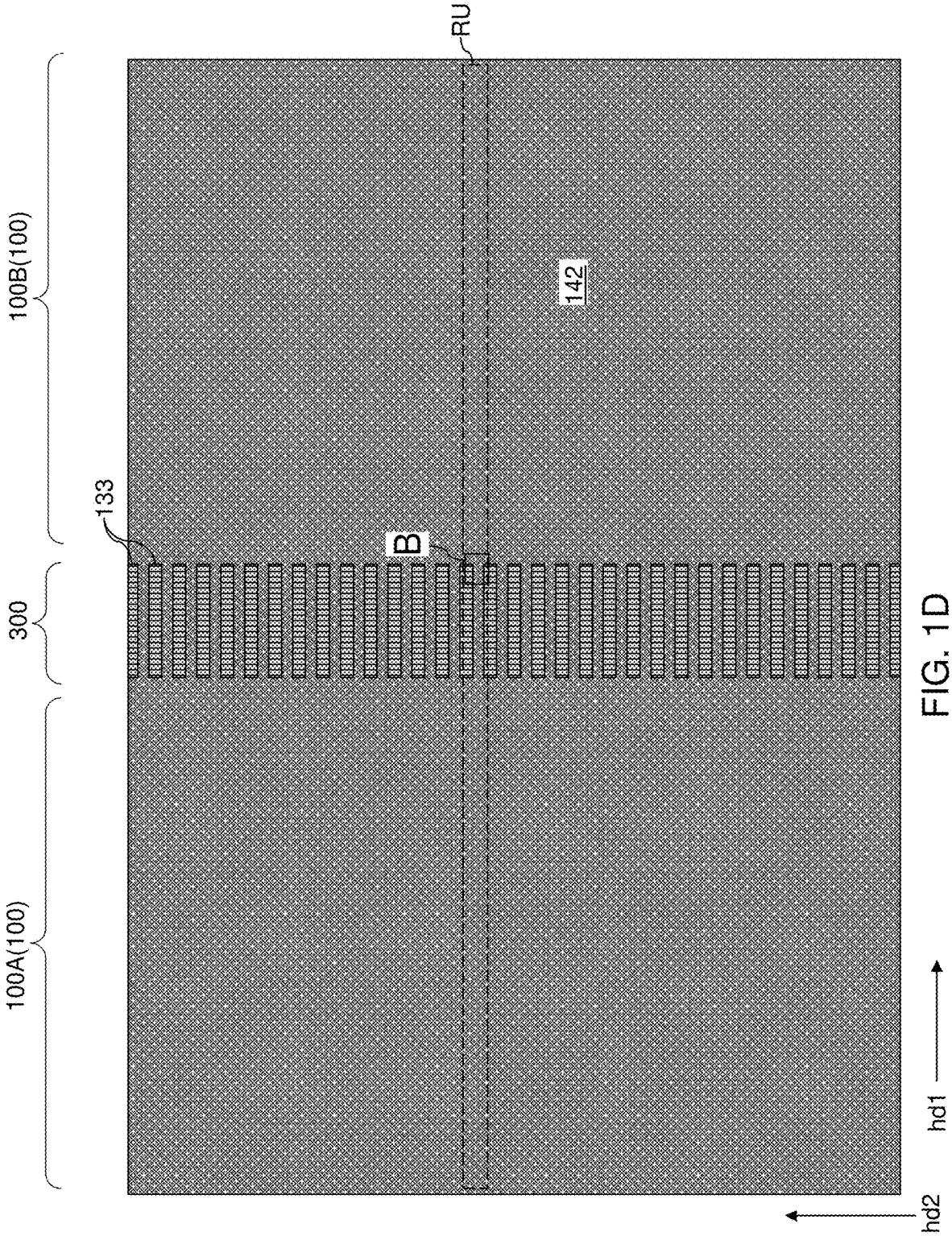


FIG. 1D

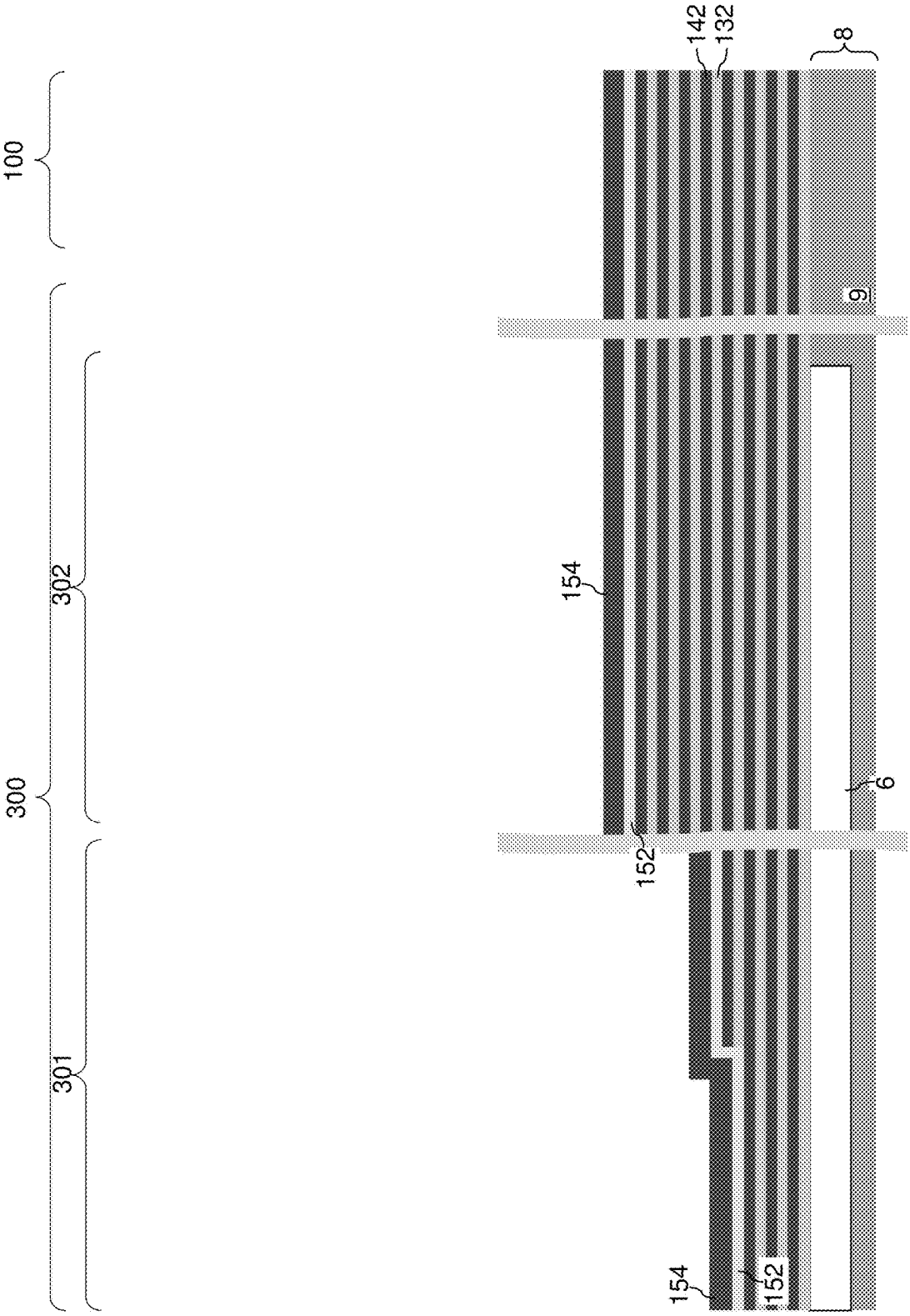


FIG. 2

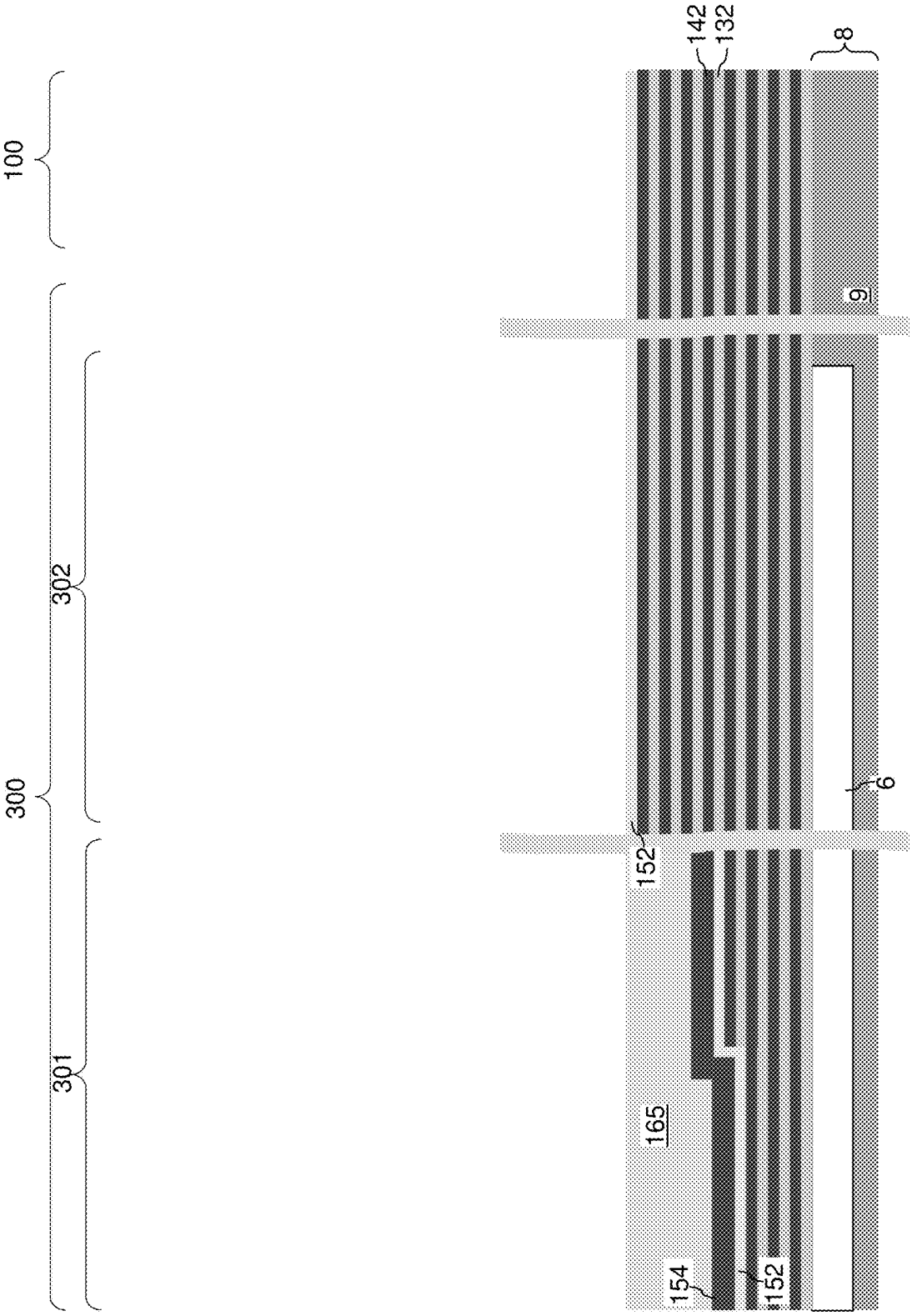


FIG. 3A

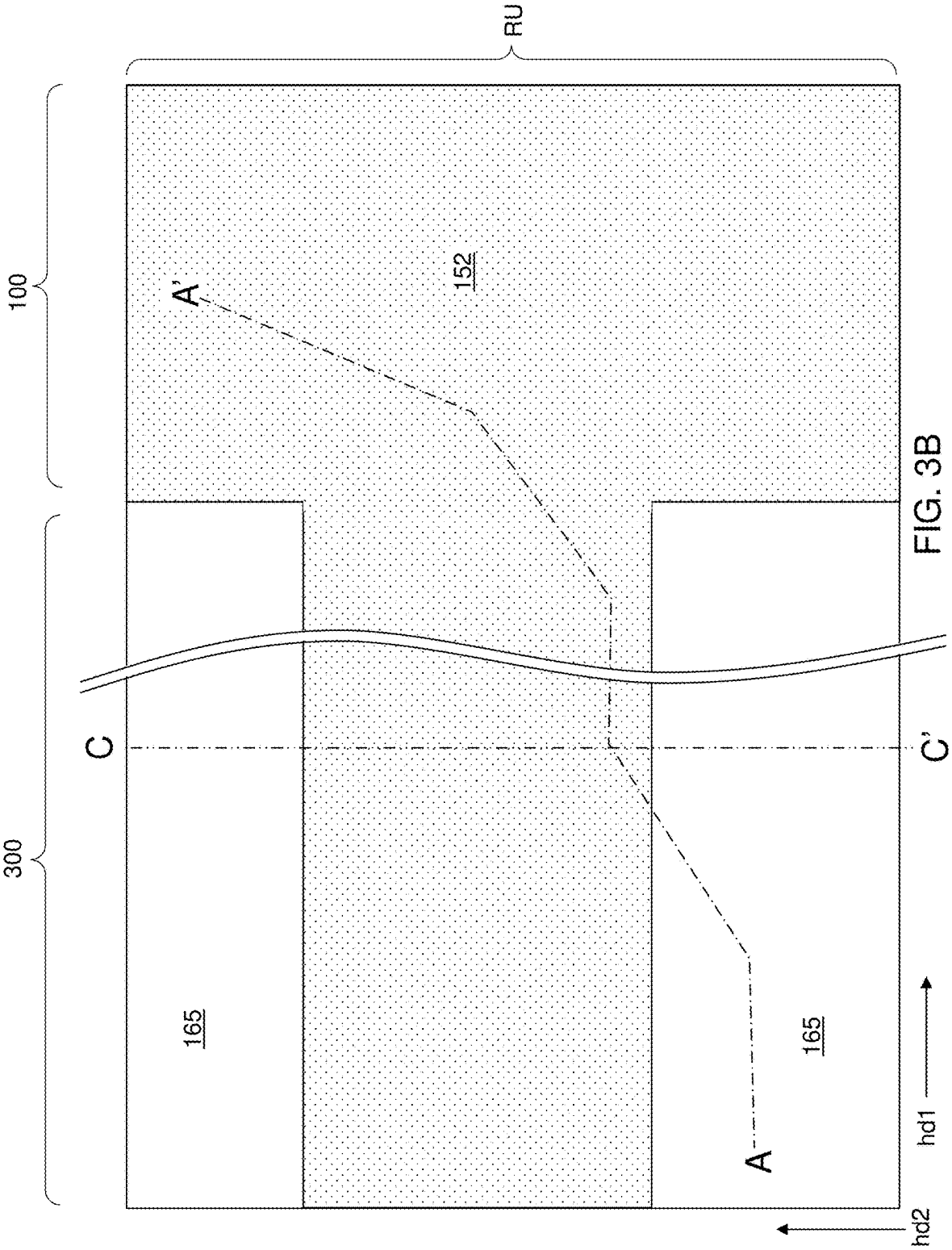


FIG. 3B

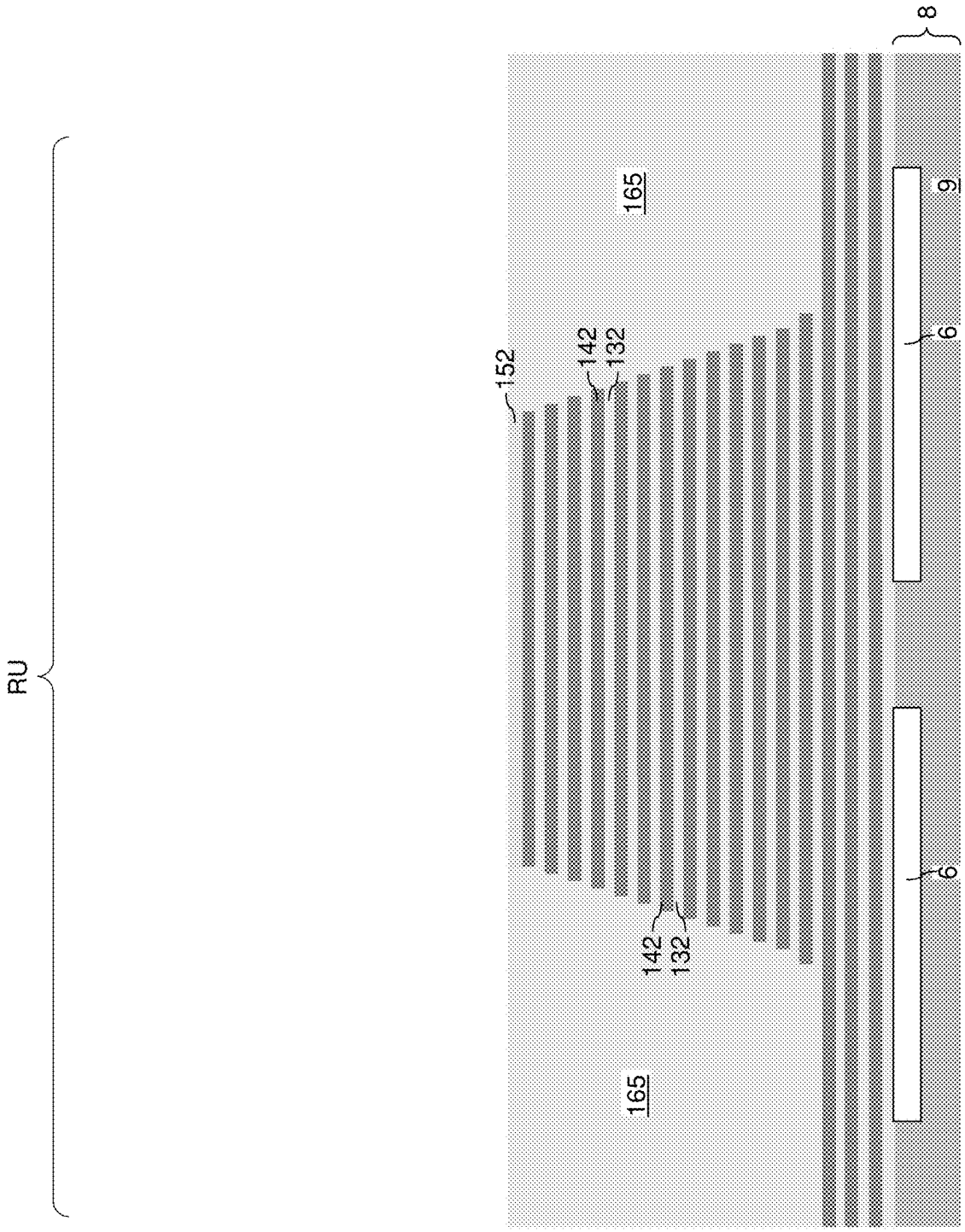


FIG. 3C

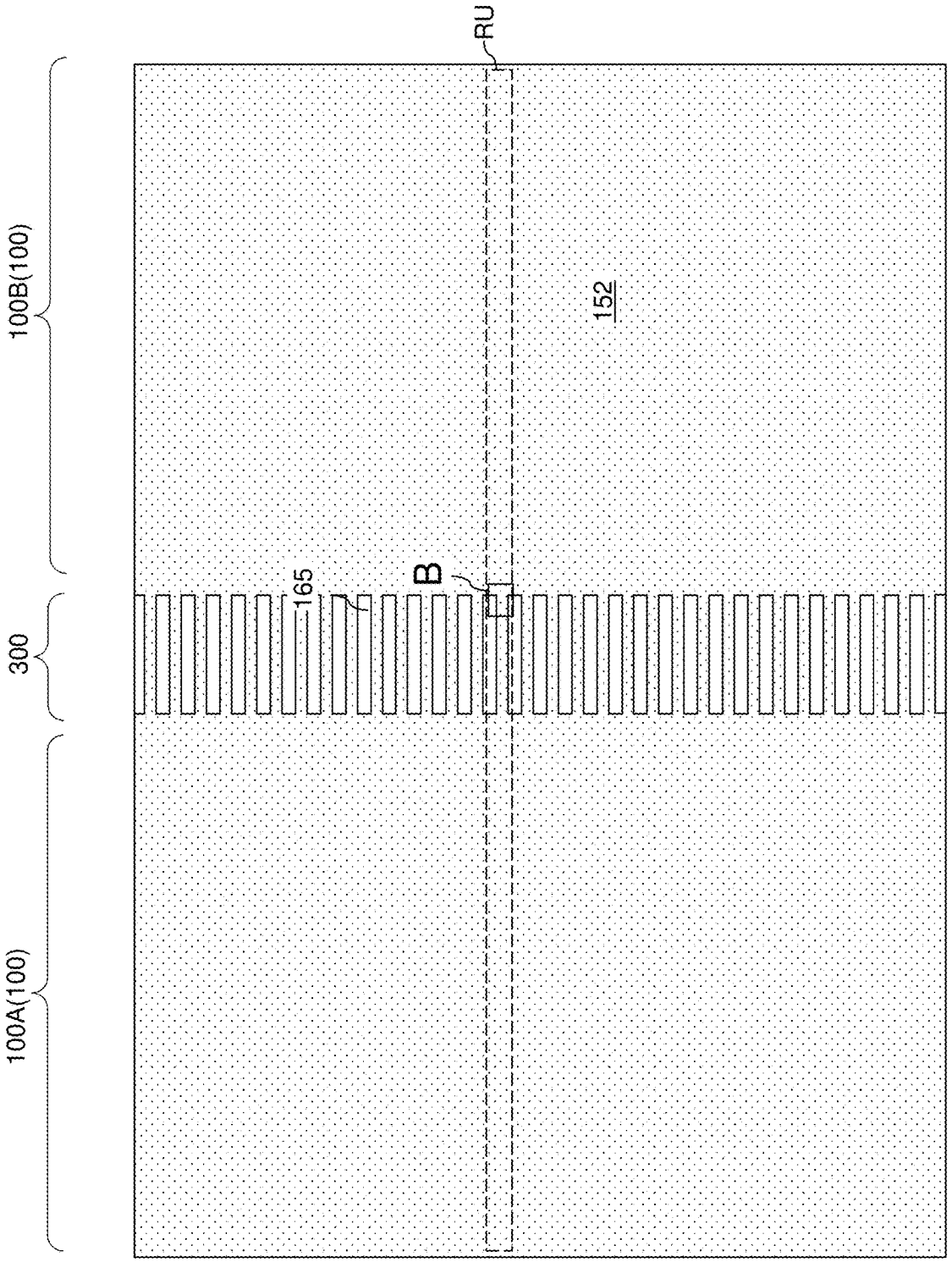


FIG. 3D

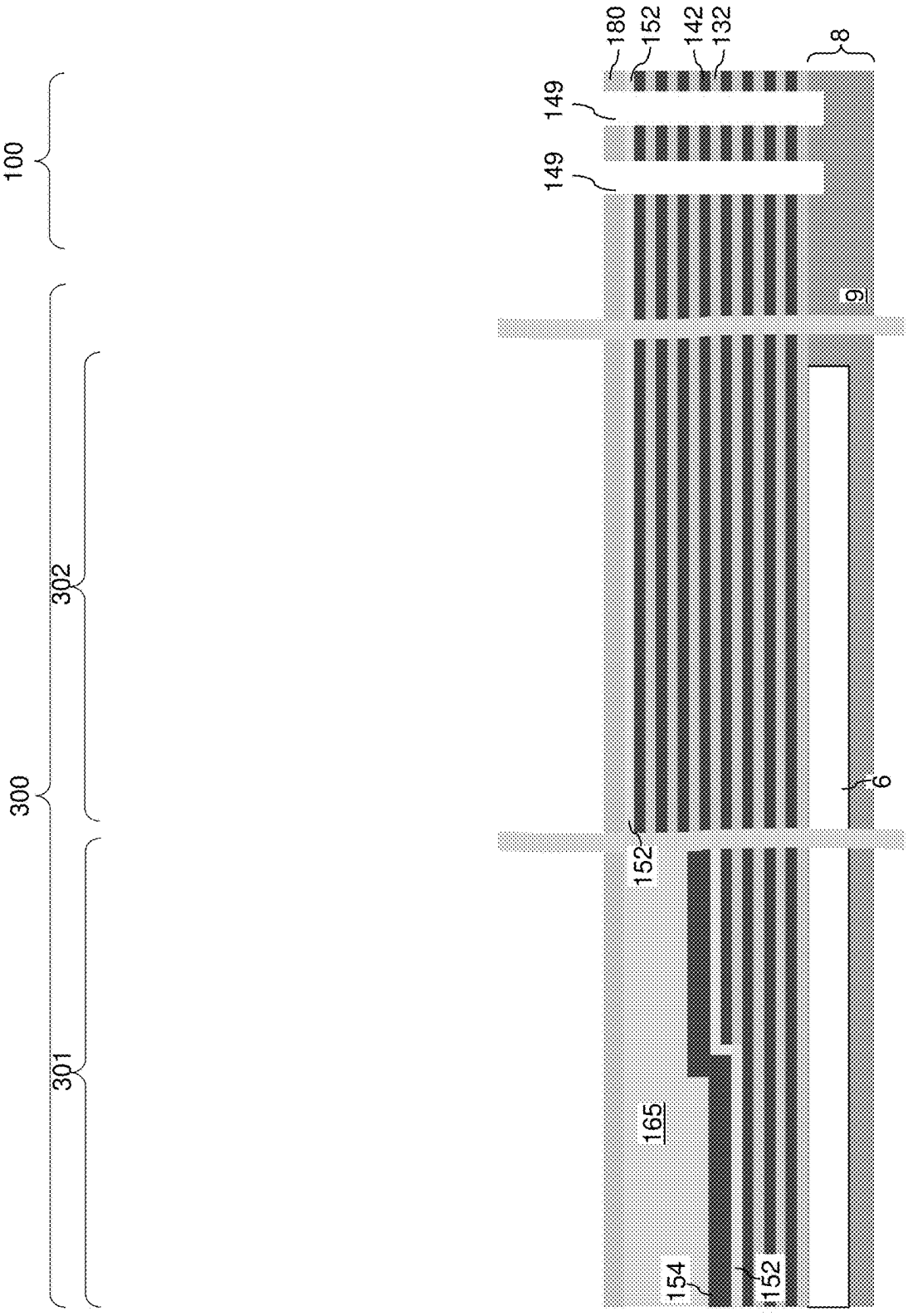


FIG. 4

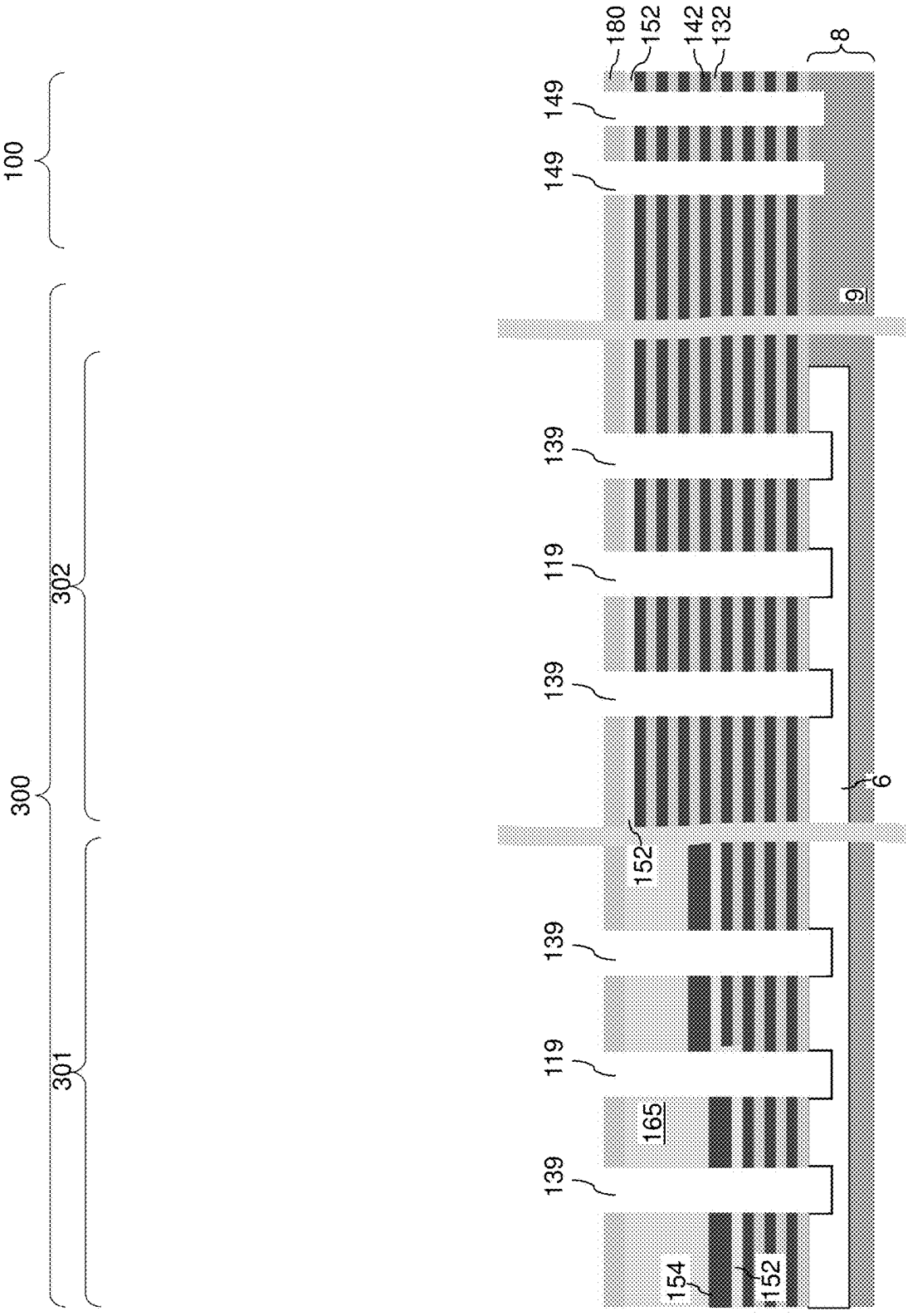

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FIG. 5A

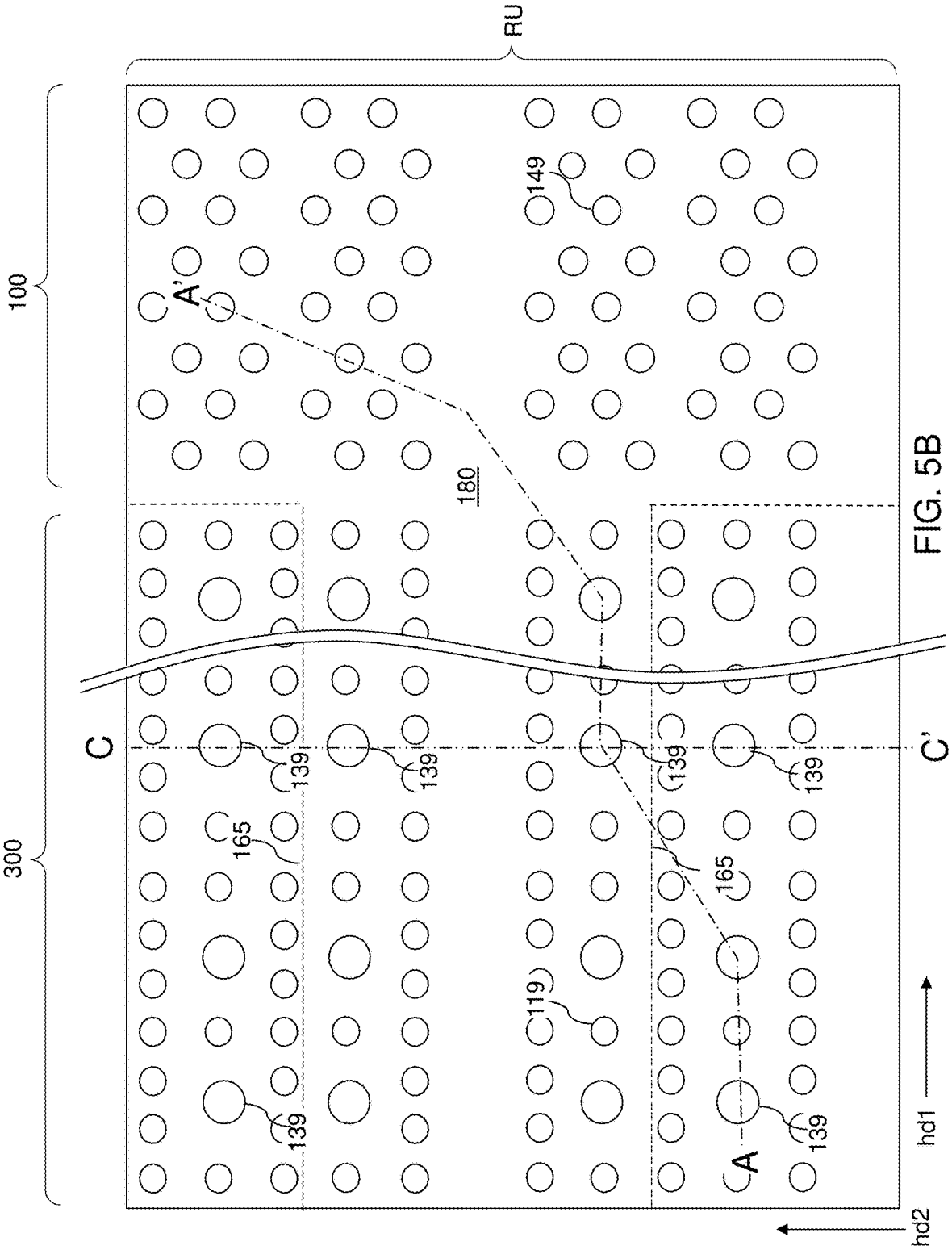

FIG. 5B

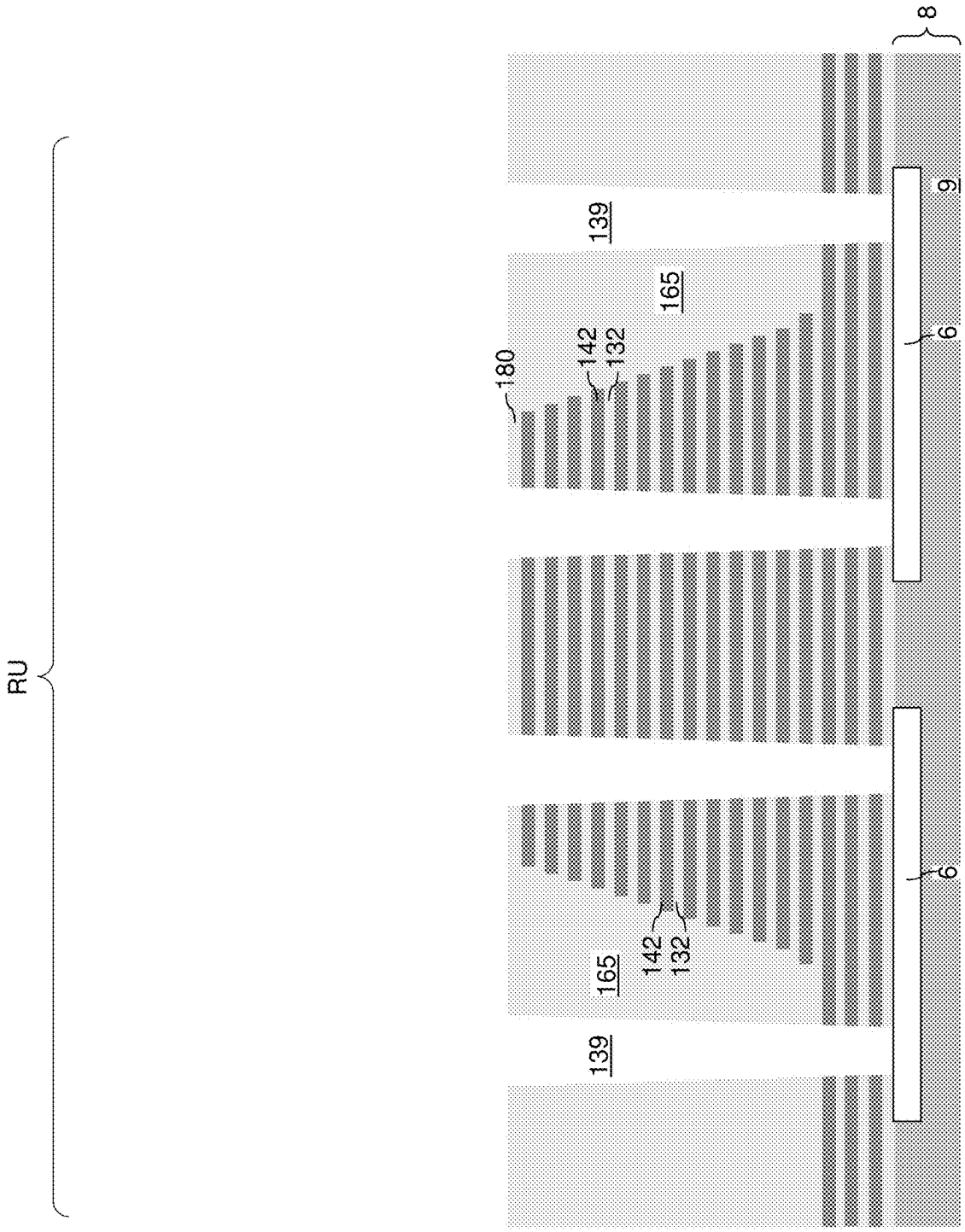

FIG. 5C

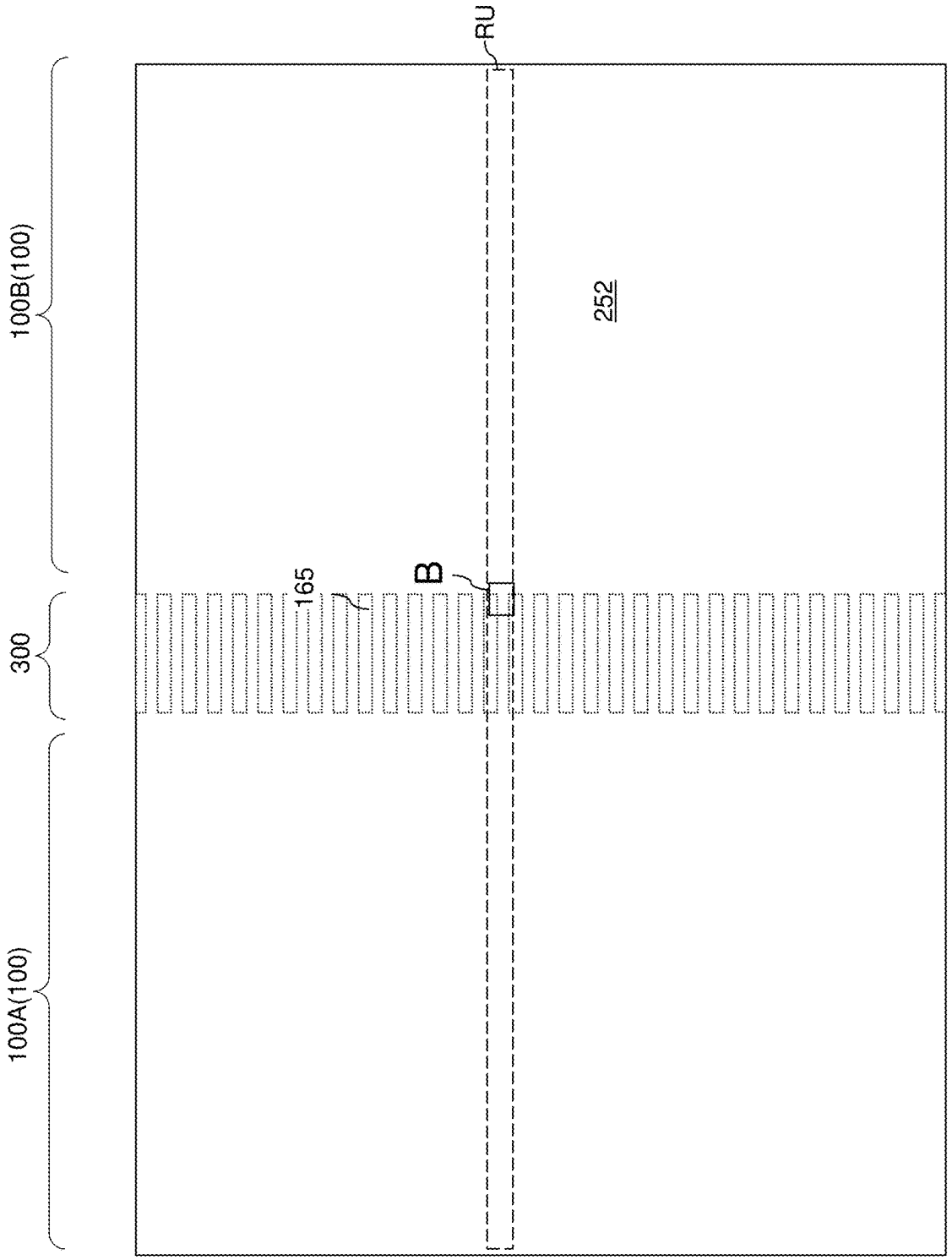

FIG. 5D

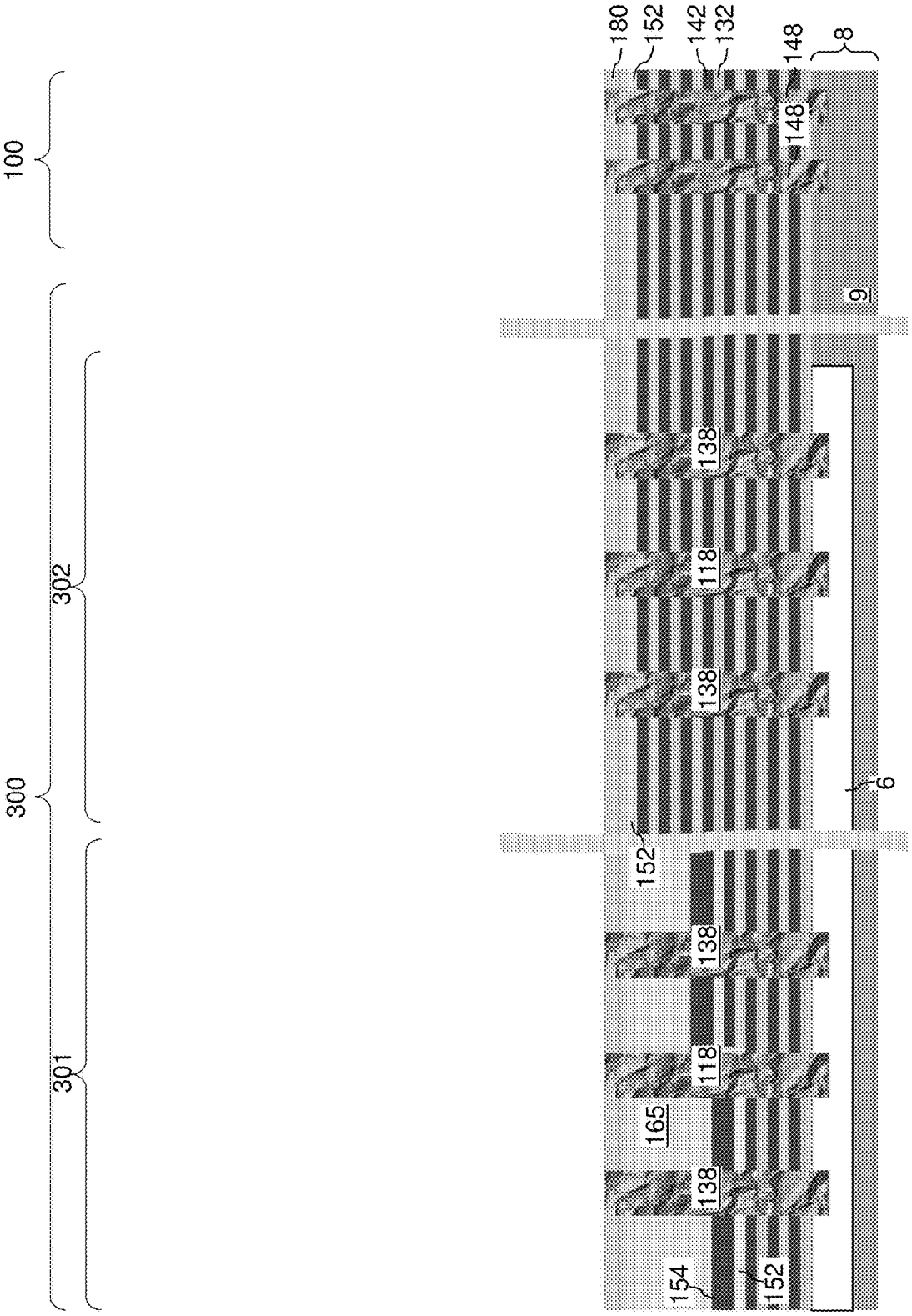
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FIG. 6

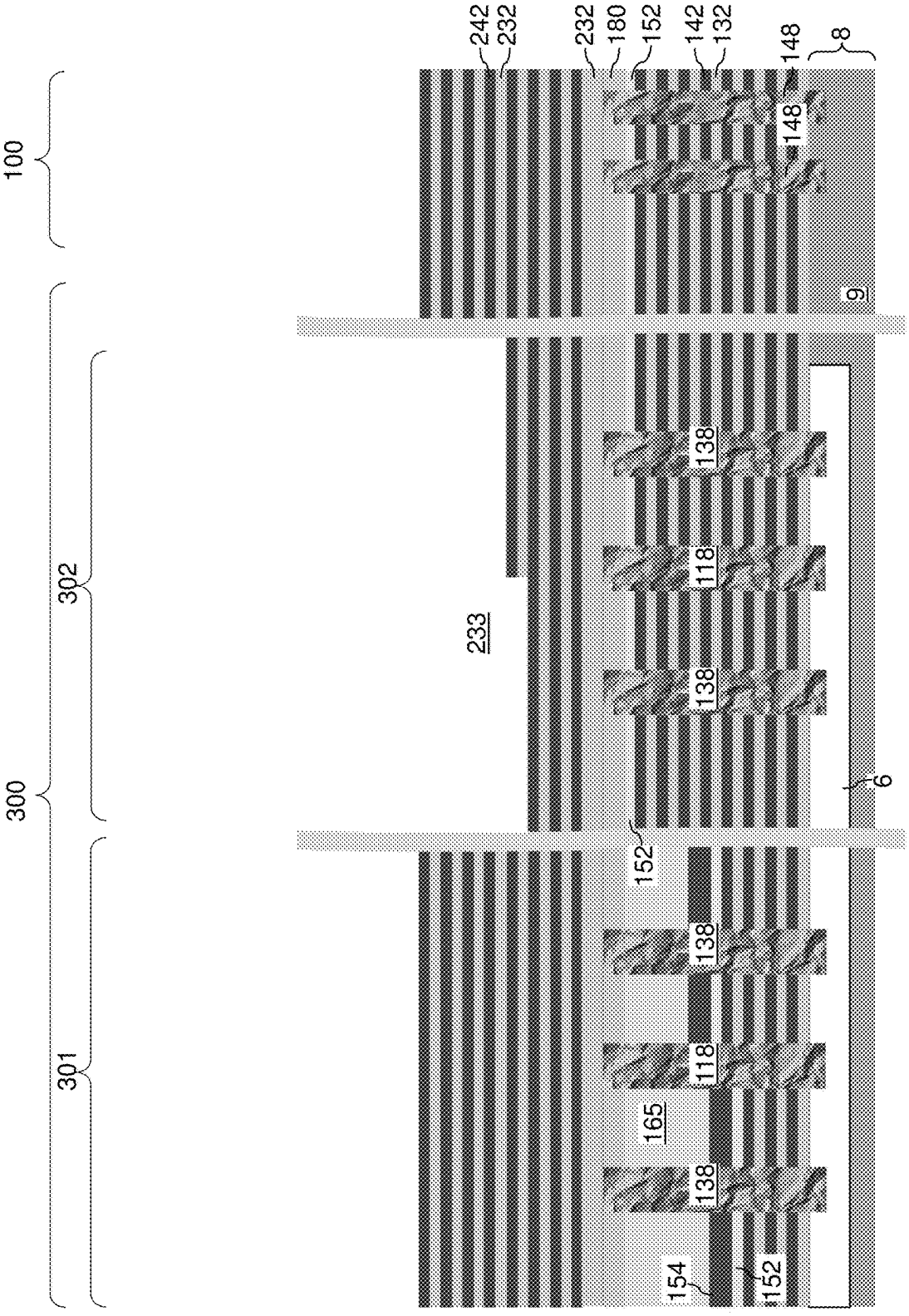
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FIG. 7

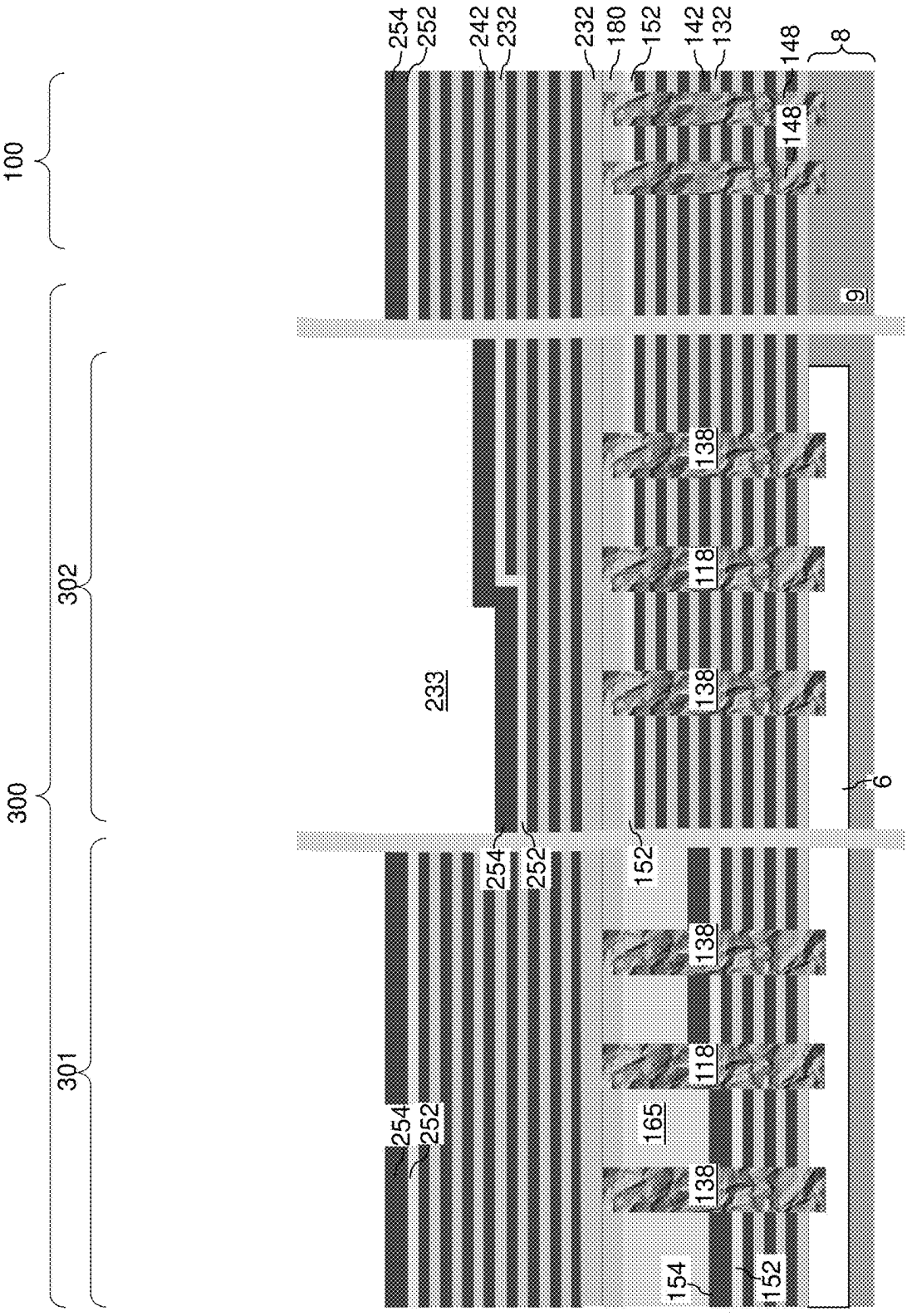
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FIG. 8

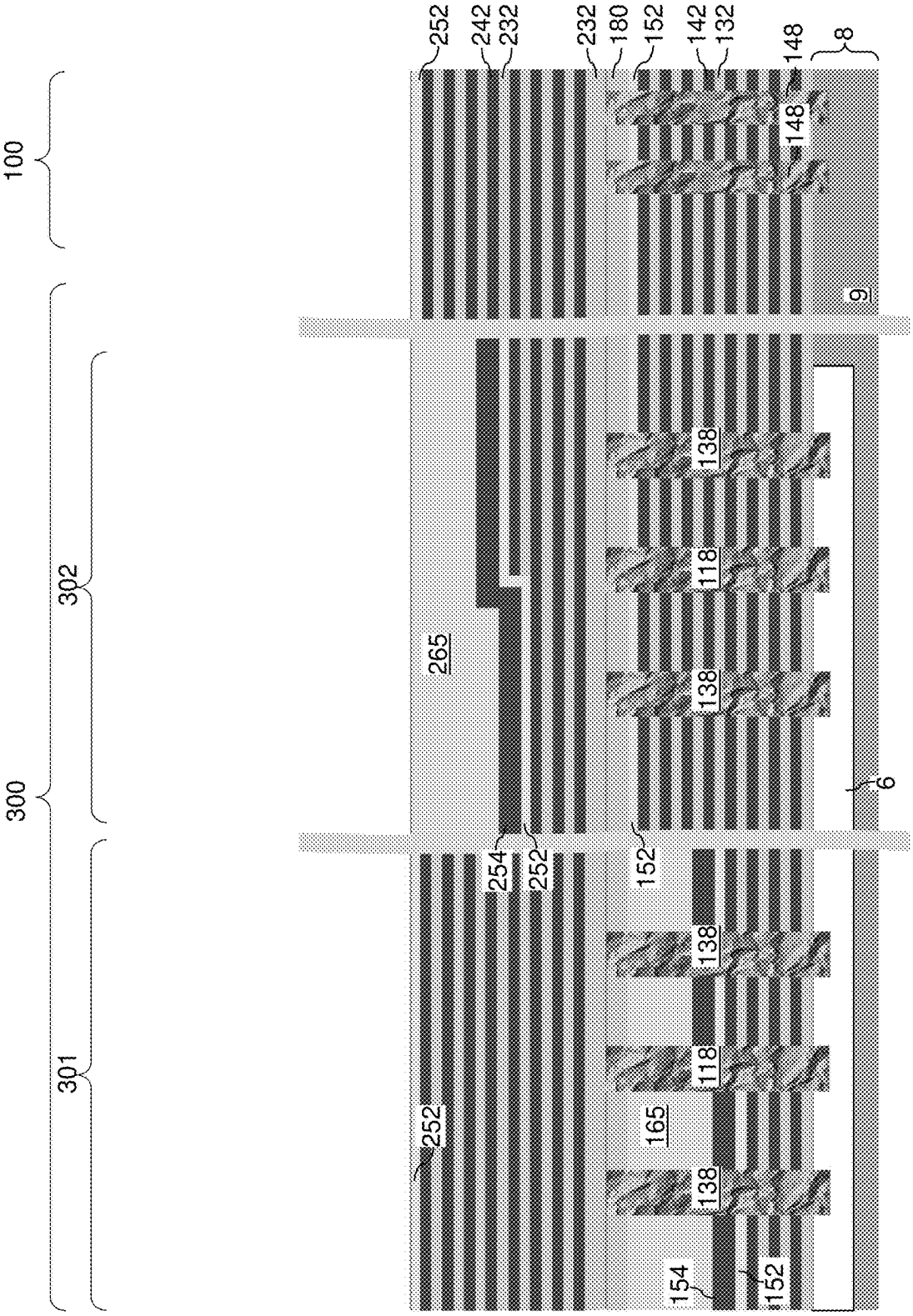
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FIG. 9A

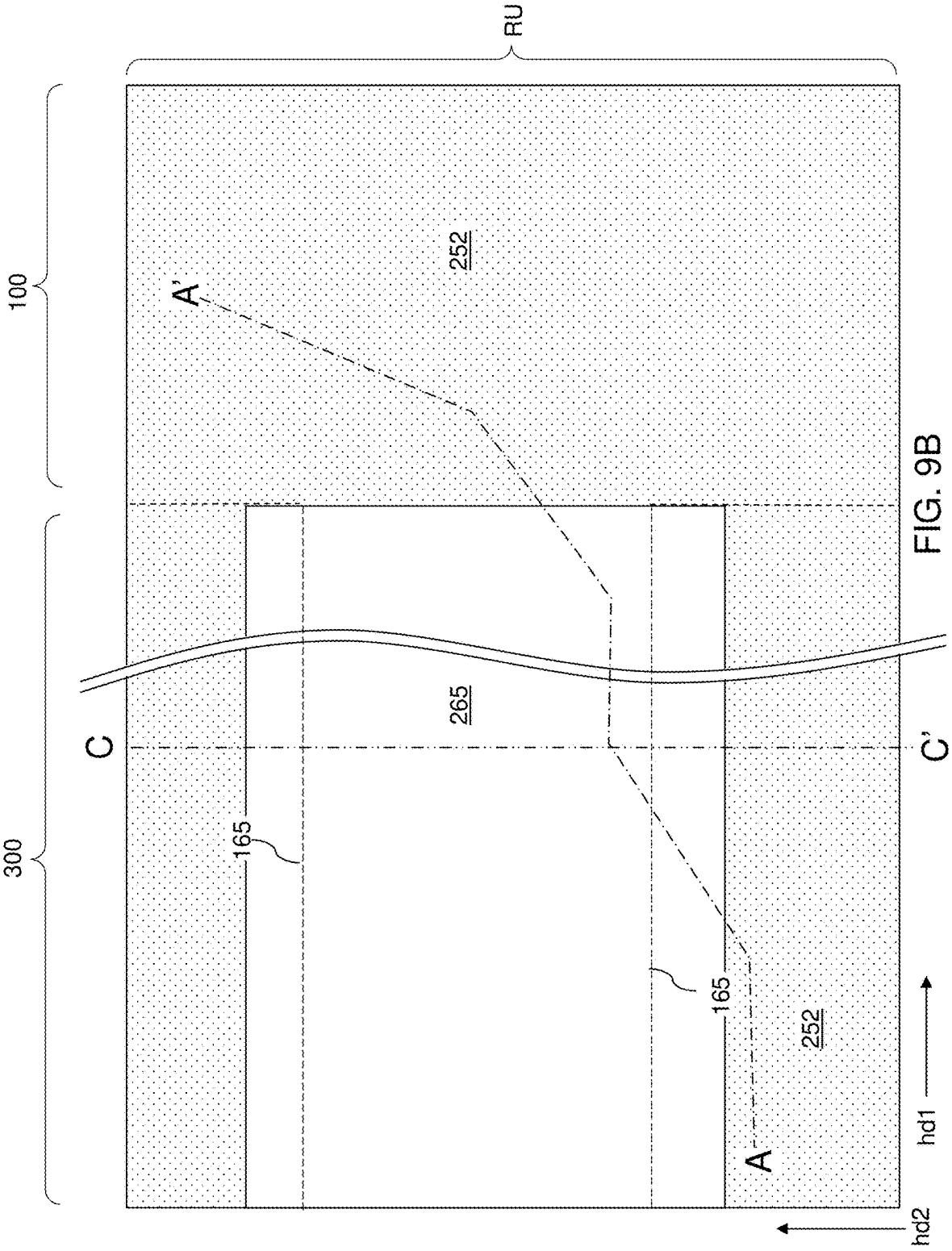

FIG. 9B

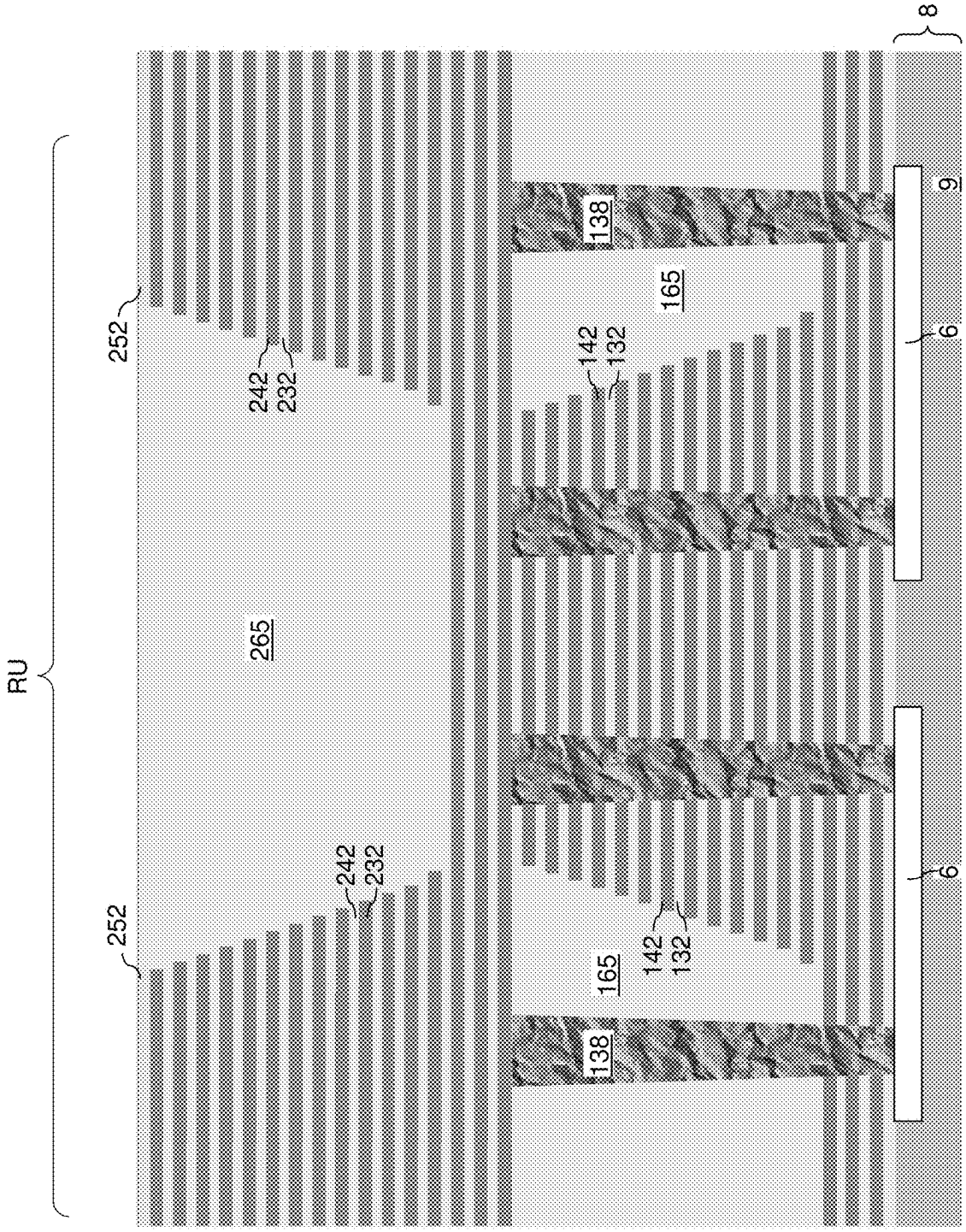
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FIG. 9C

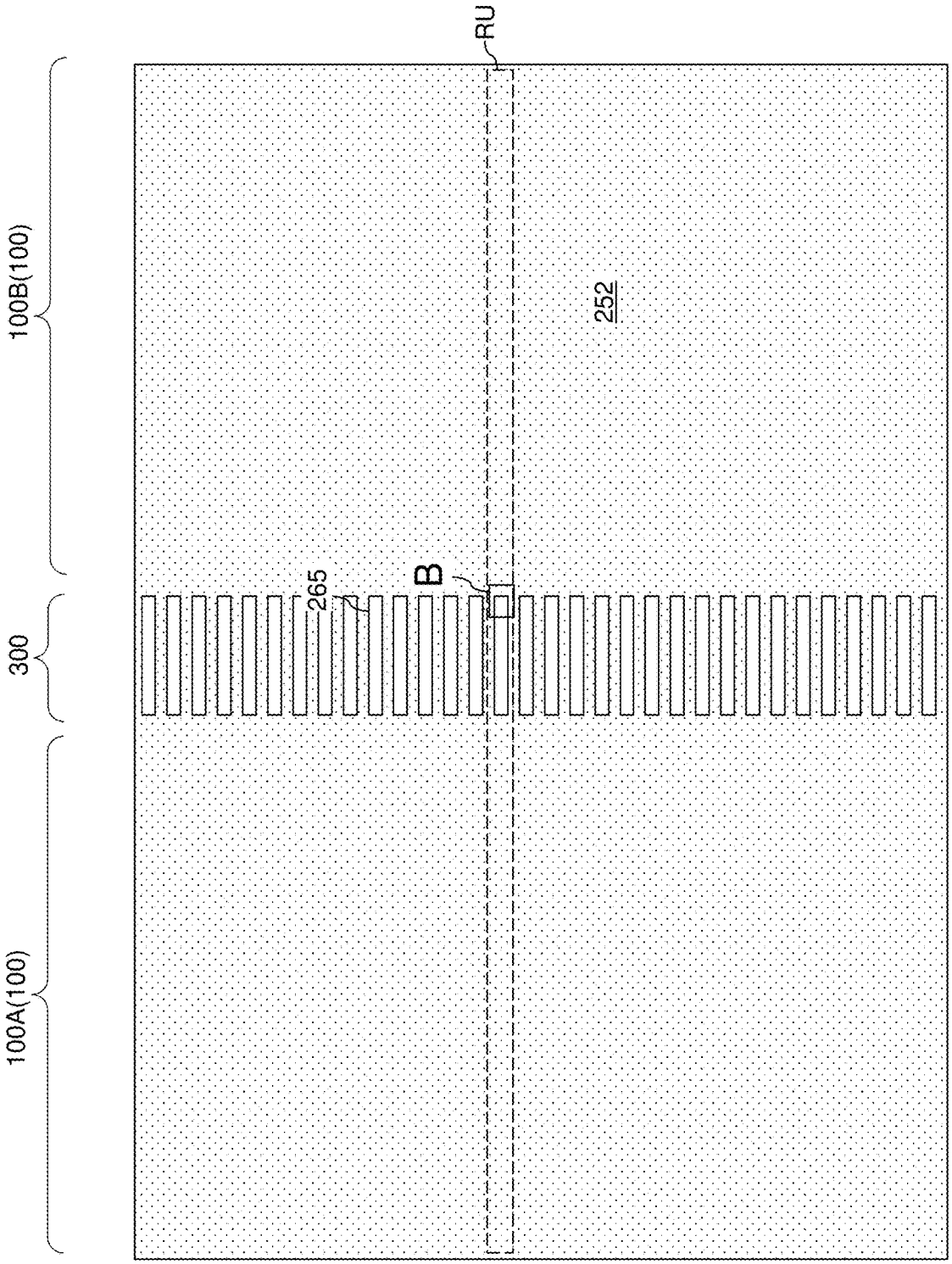

FIG. 9D

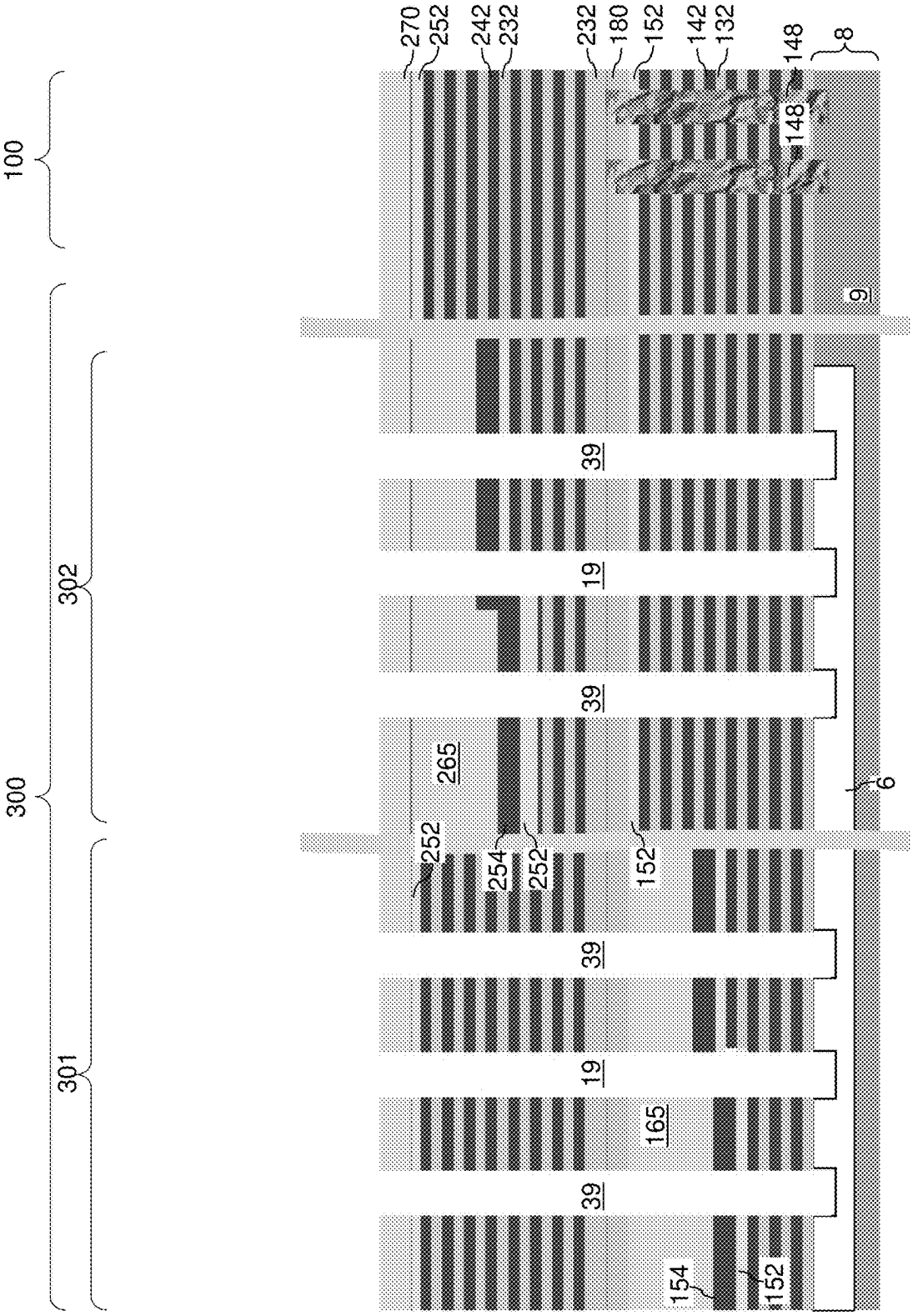
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FIG. 10A

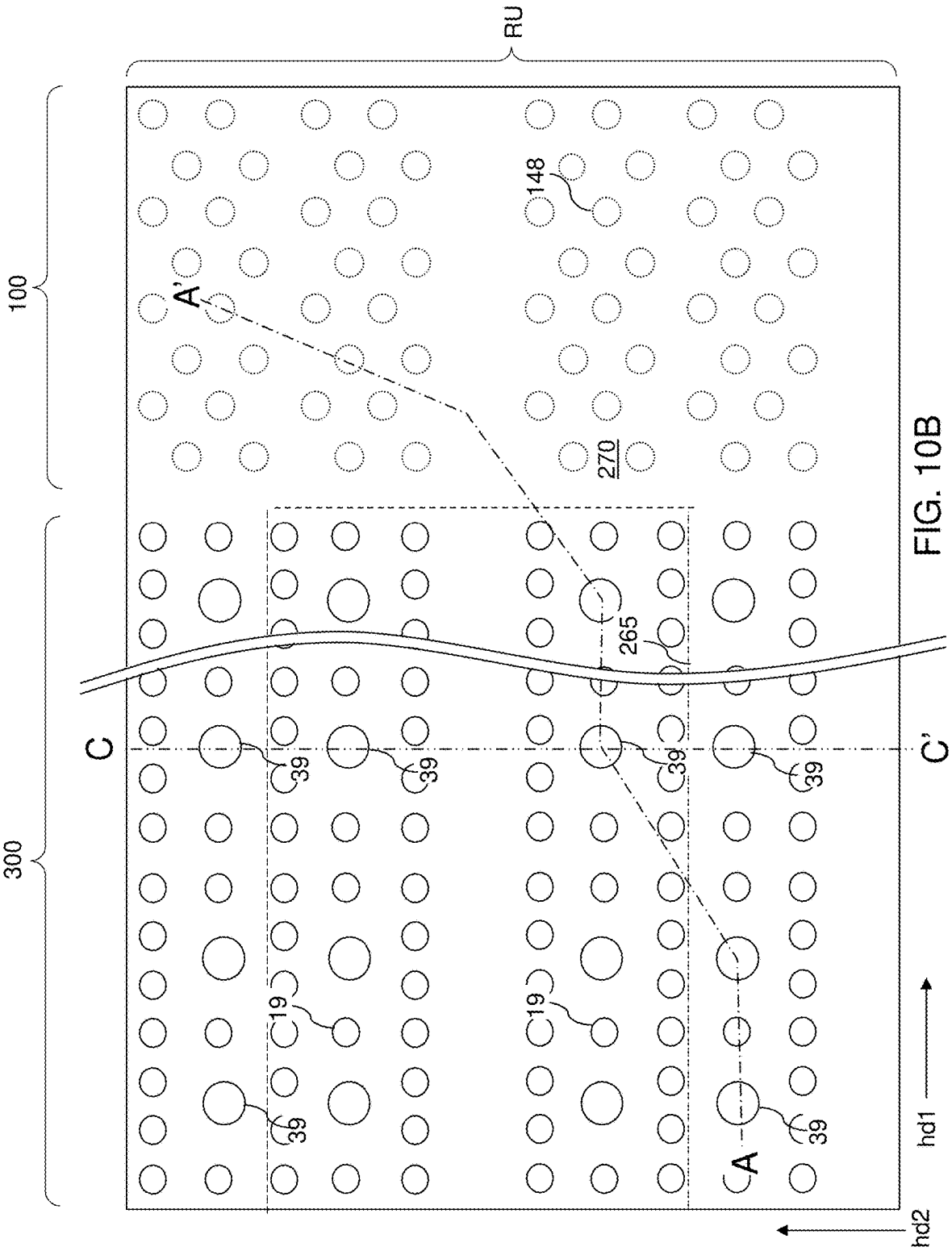

FIG. 10B

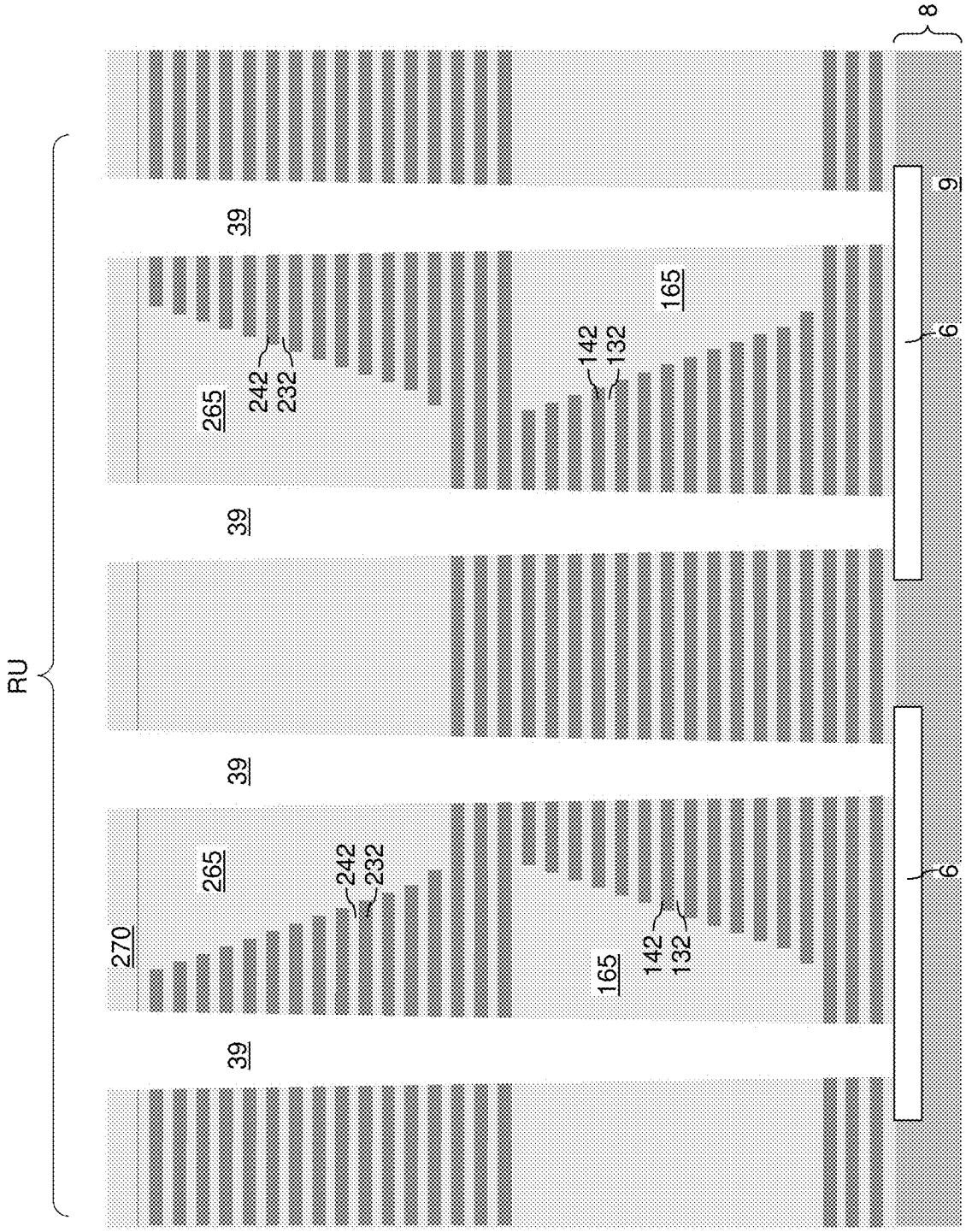
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FIG. 10C

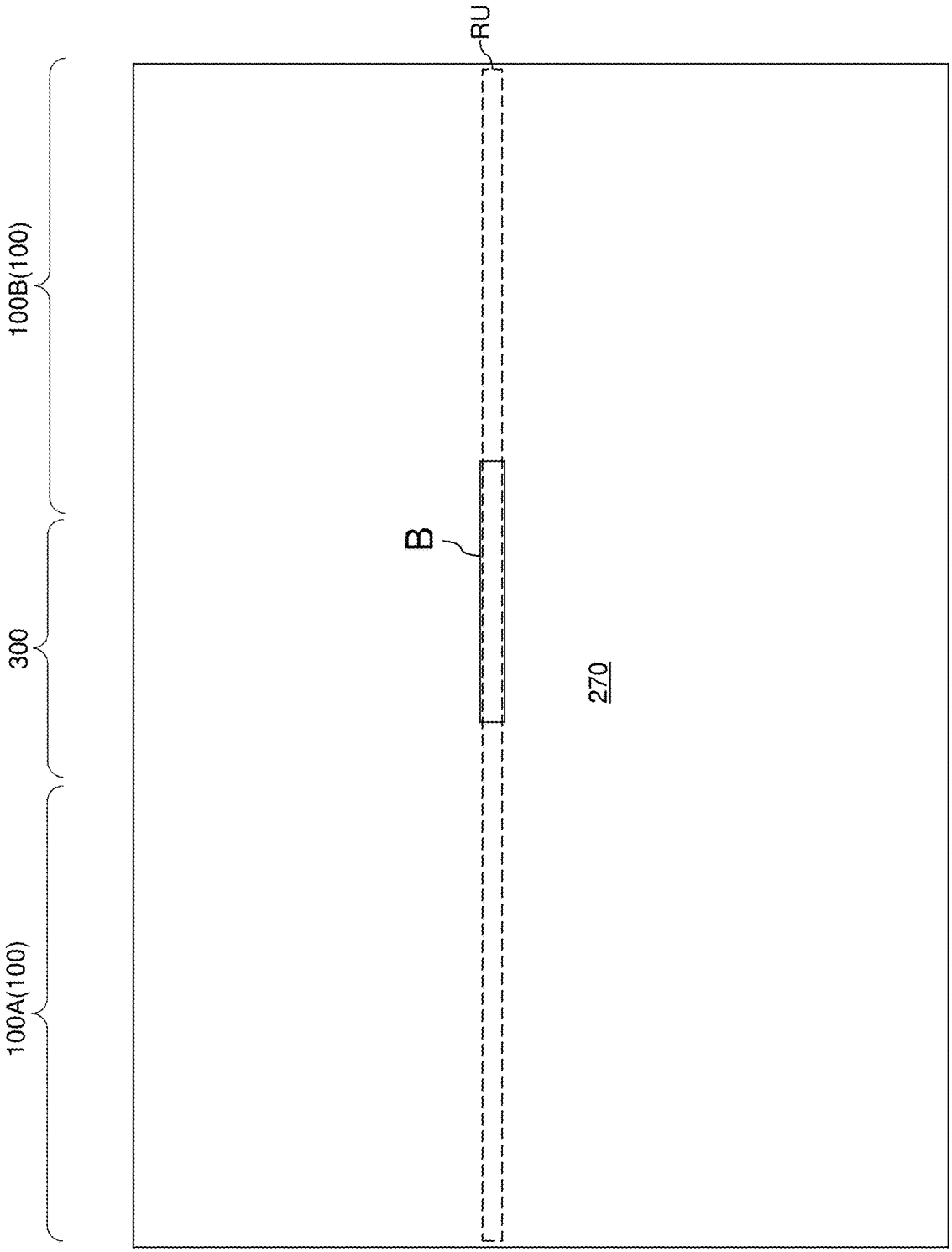

FIG. 10D

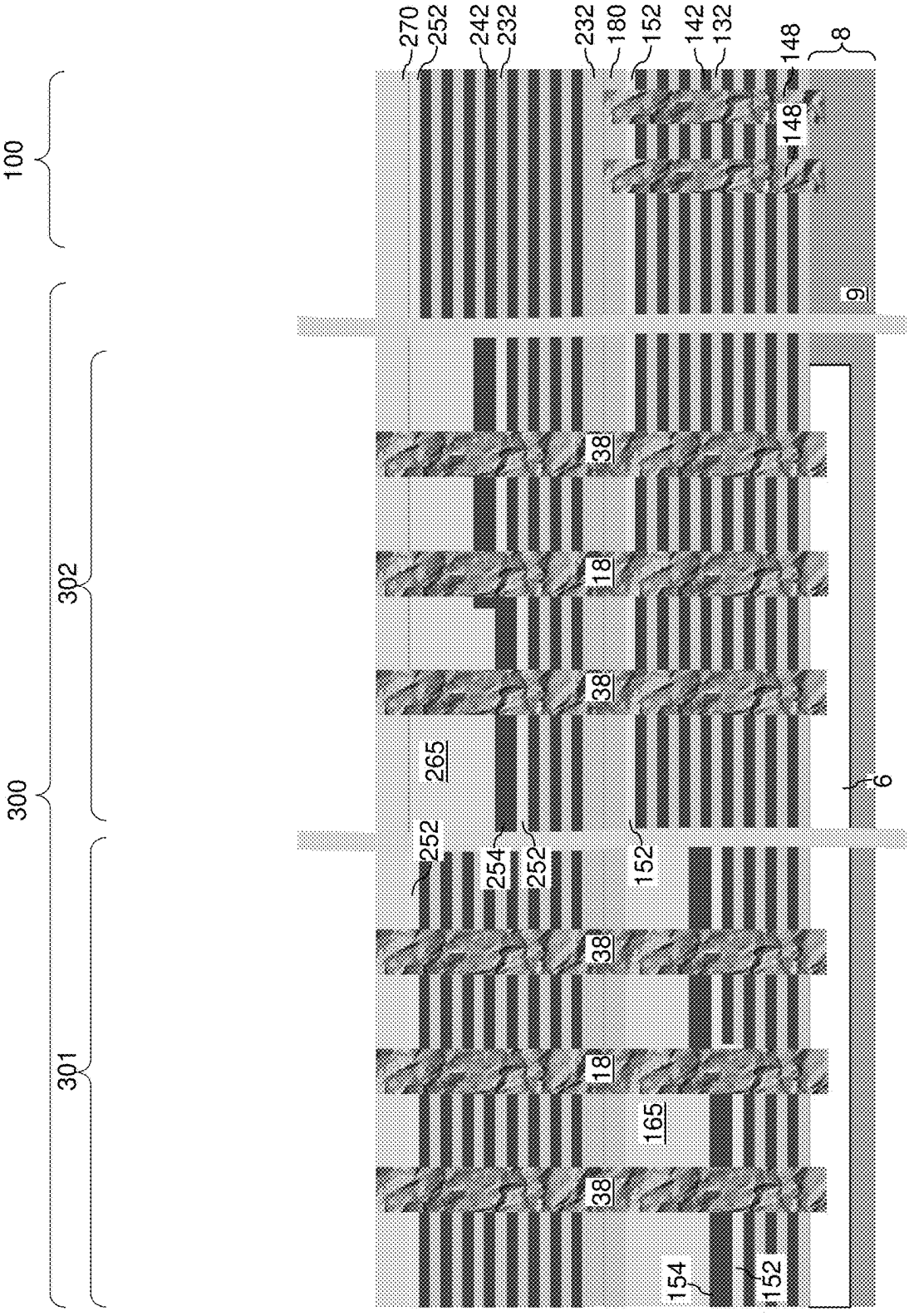
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FIG. 11

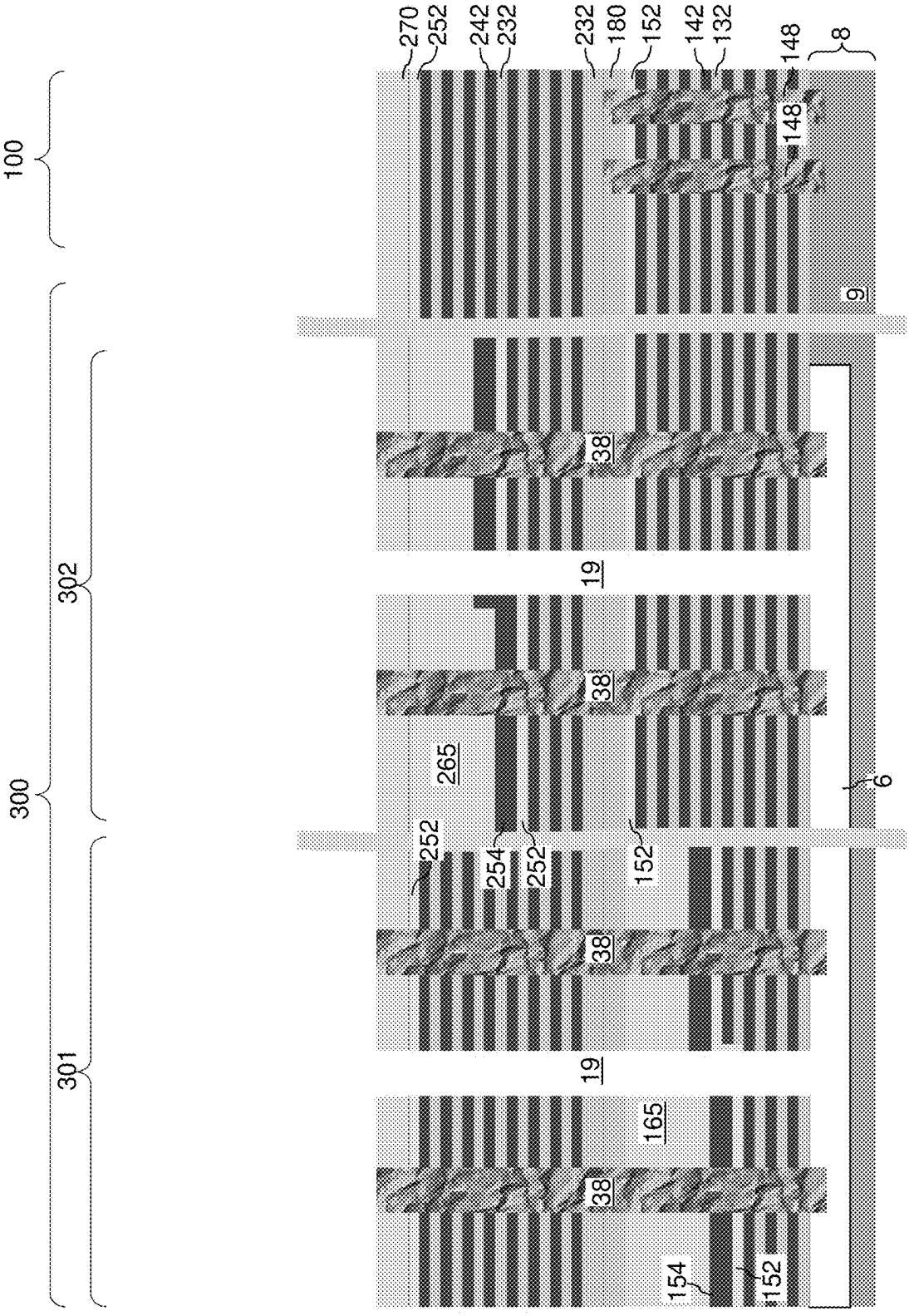
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FIG. 12

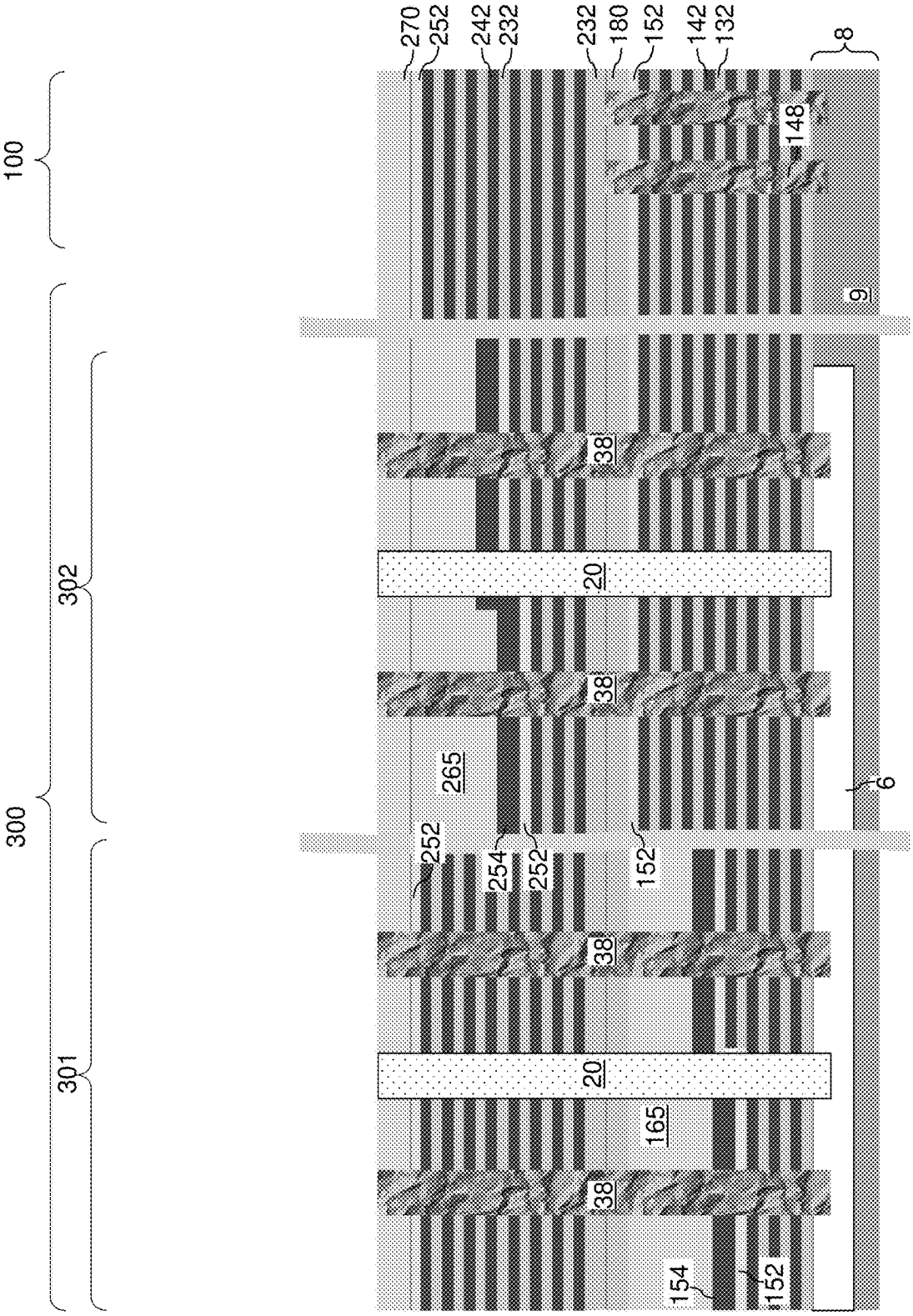
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FIG. 13

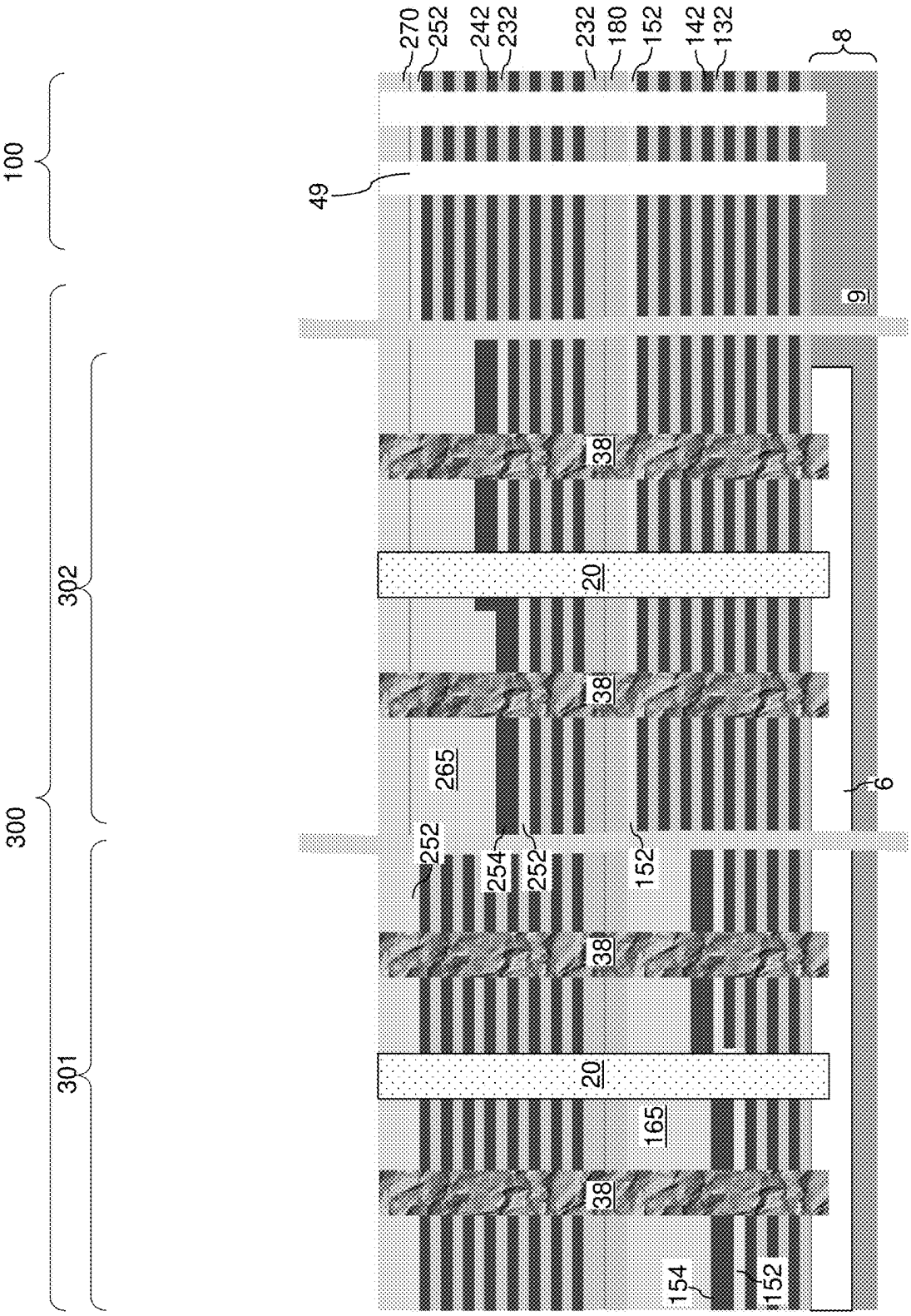
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FIG. 14

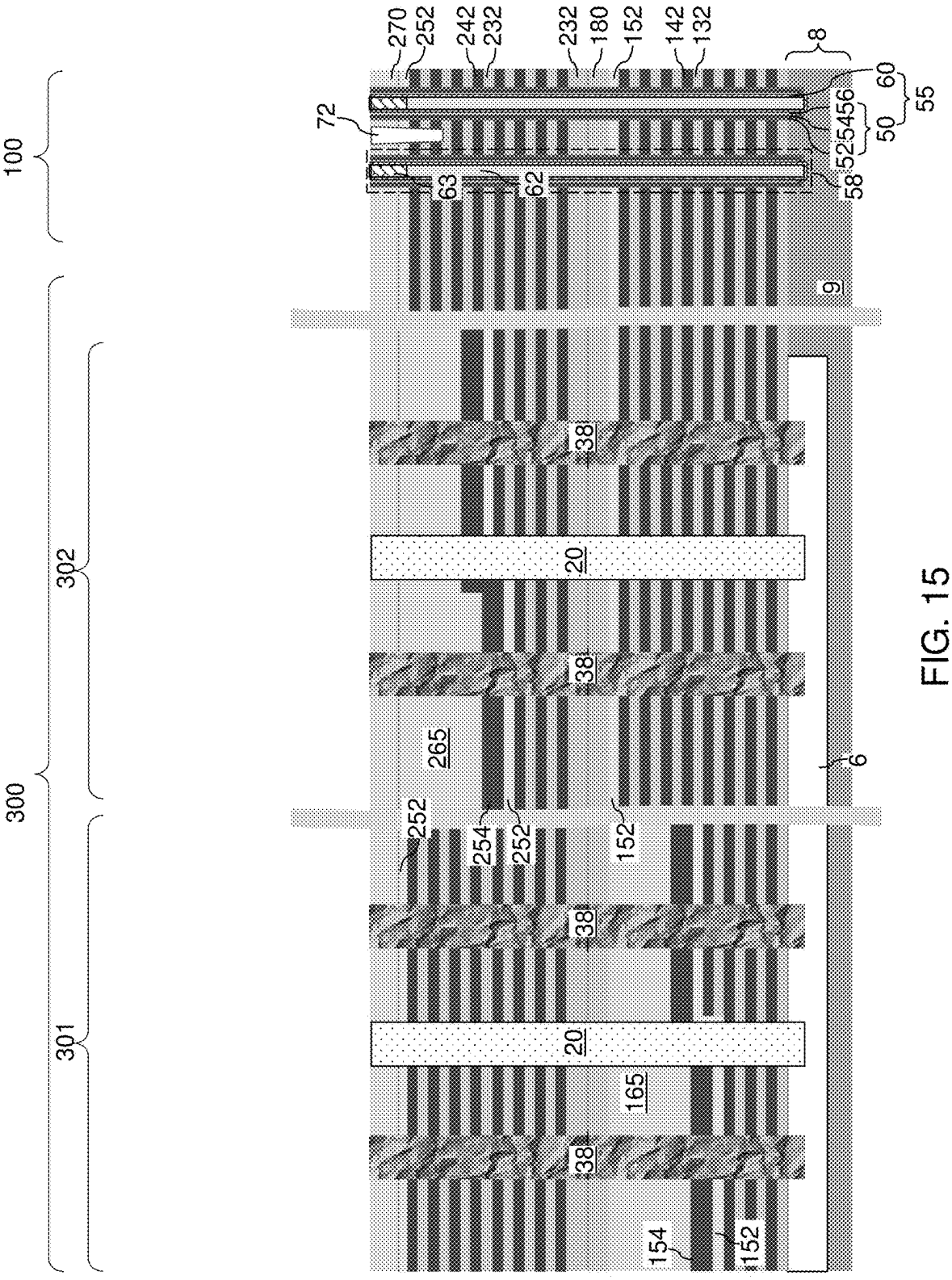
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FIG. 15

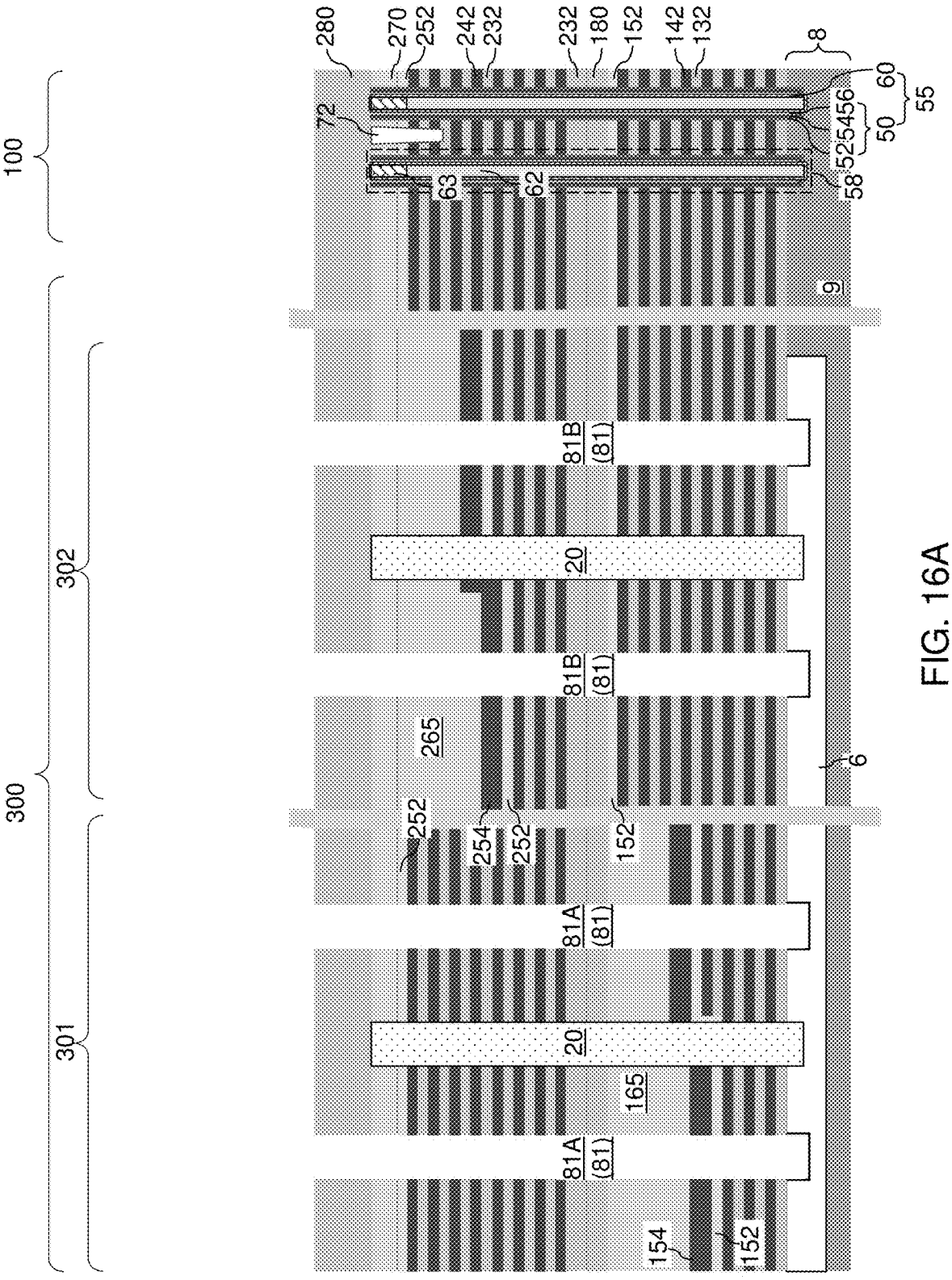
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FIG. 16A

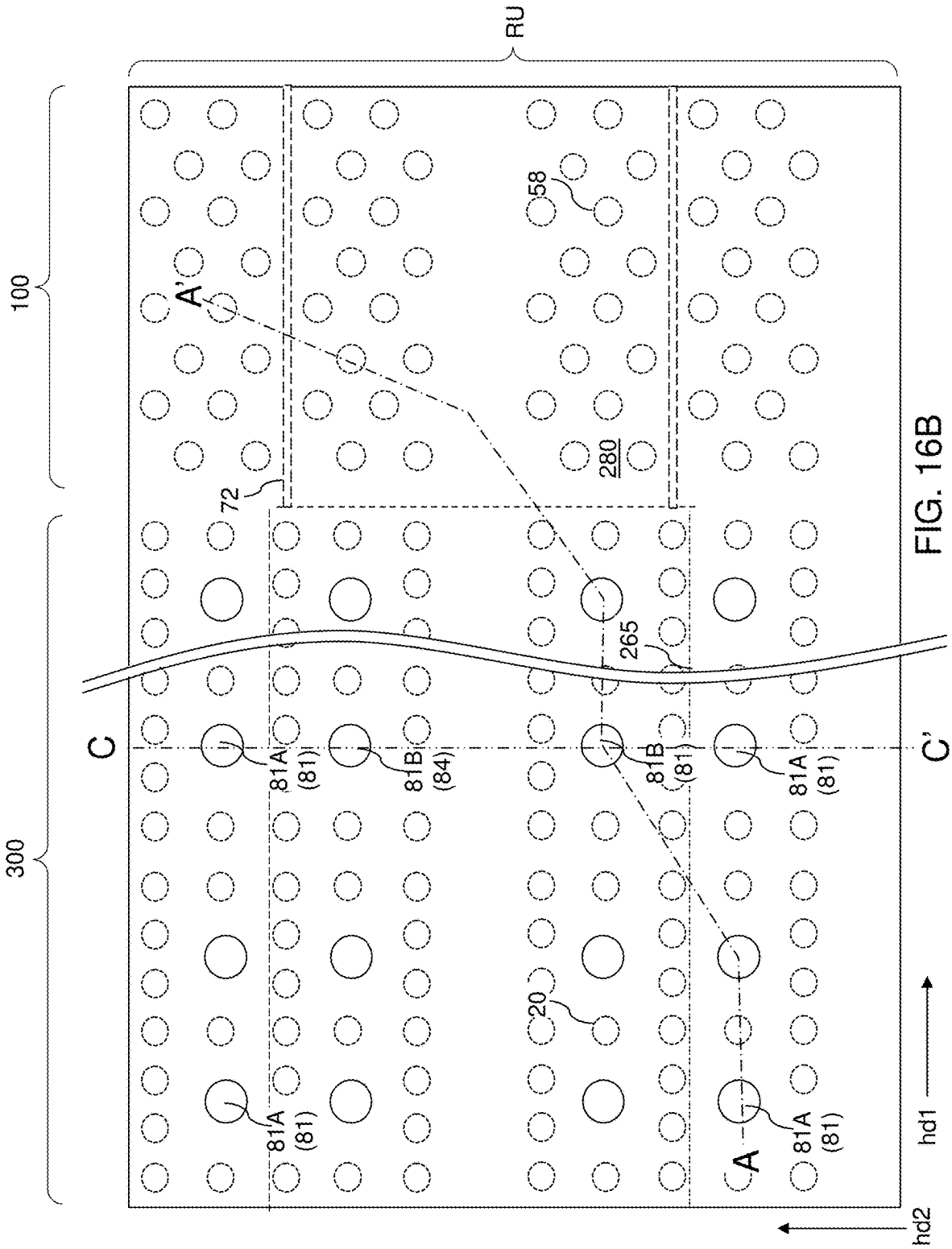

FIG. 16B

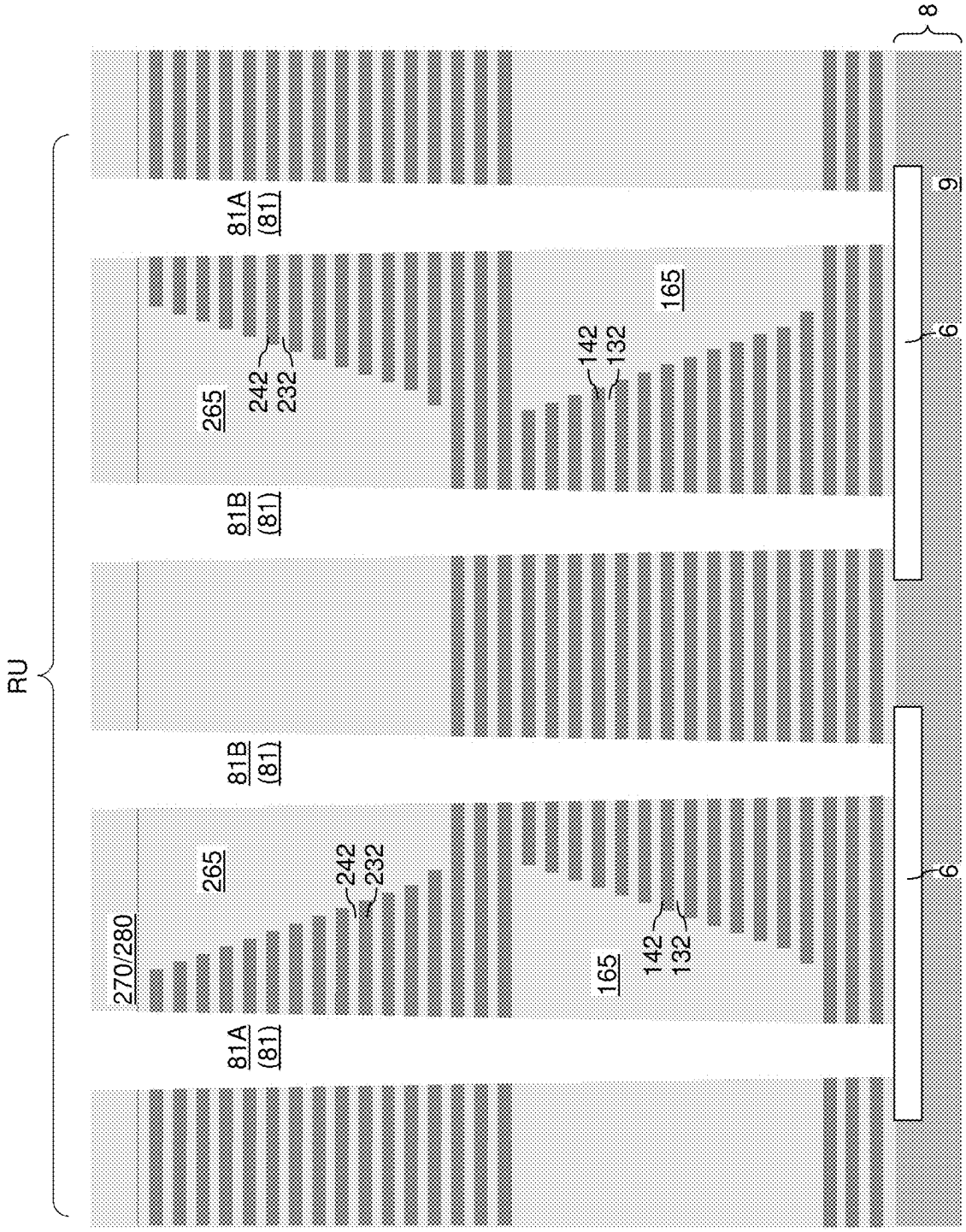

FIG. 16C

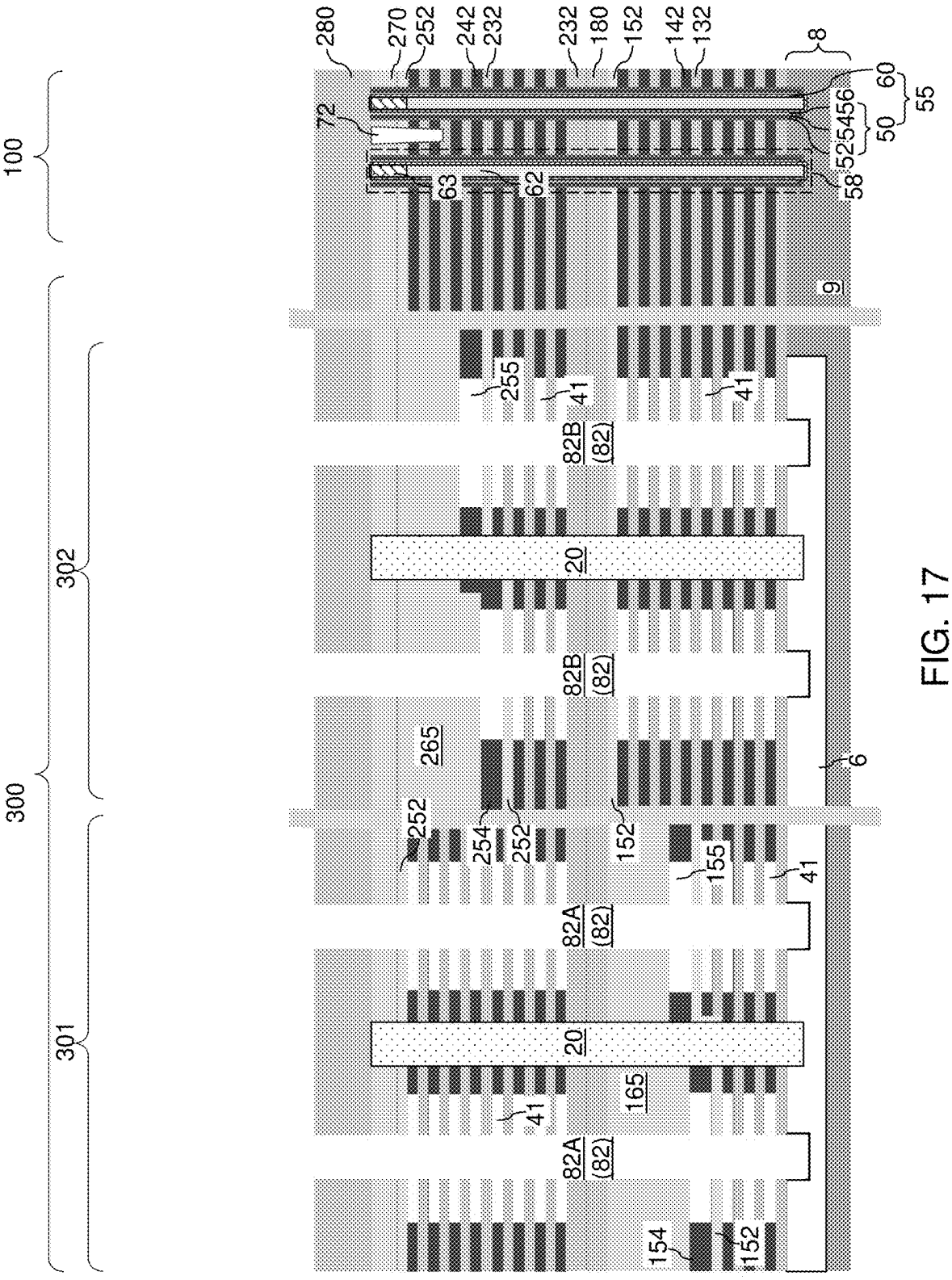
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FIG. 17

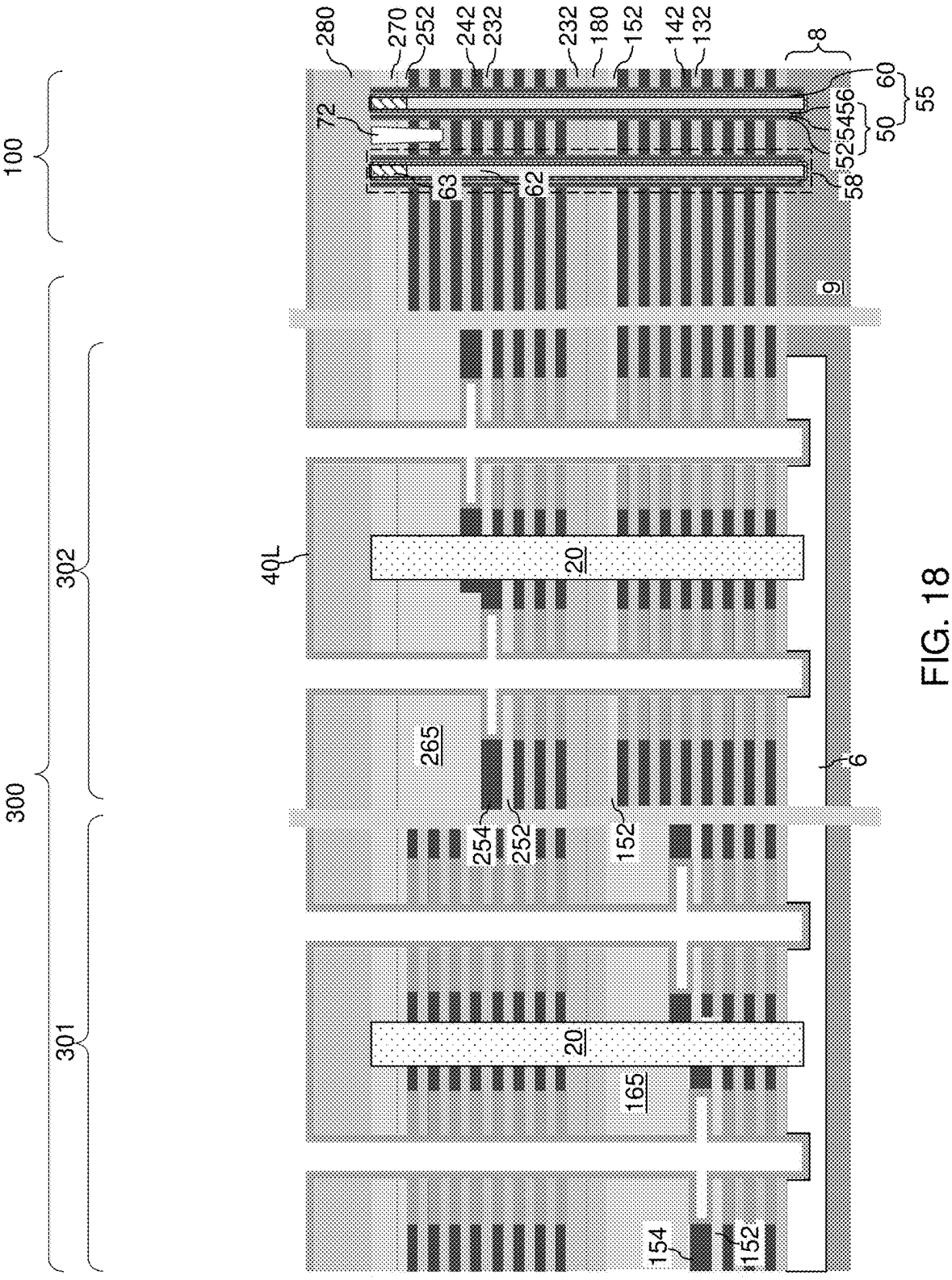
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FIG. 18

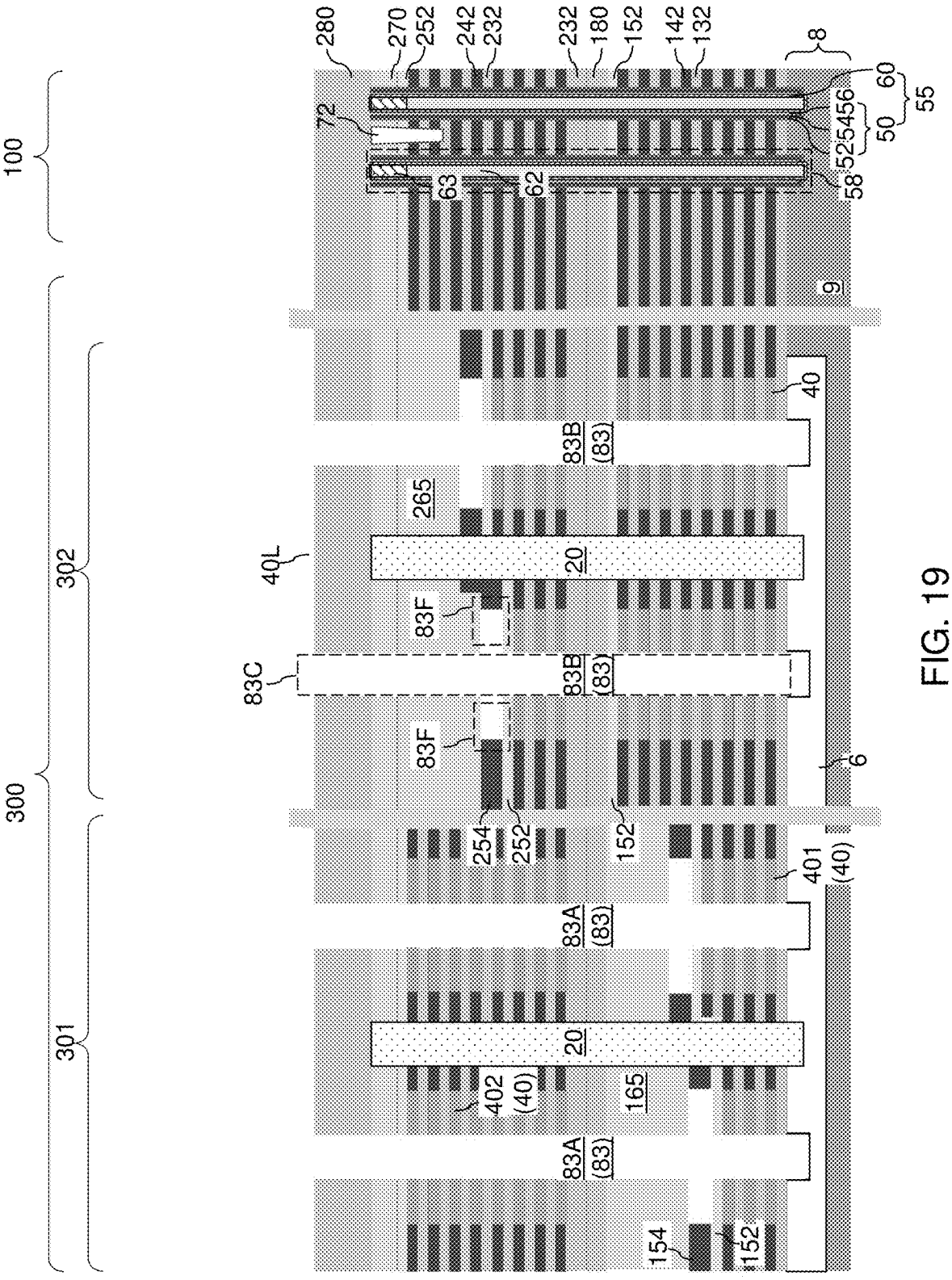
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FIG. 19

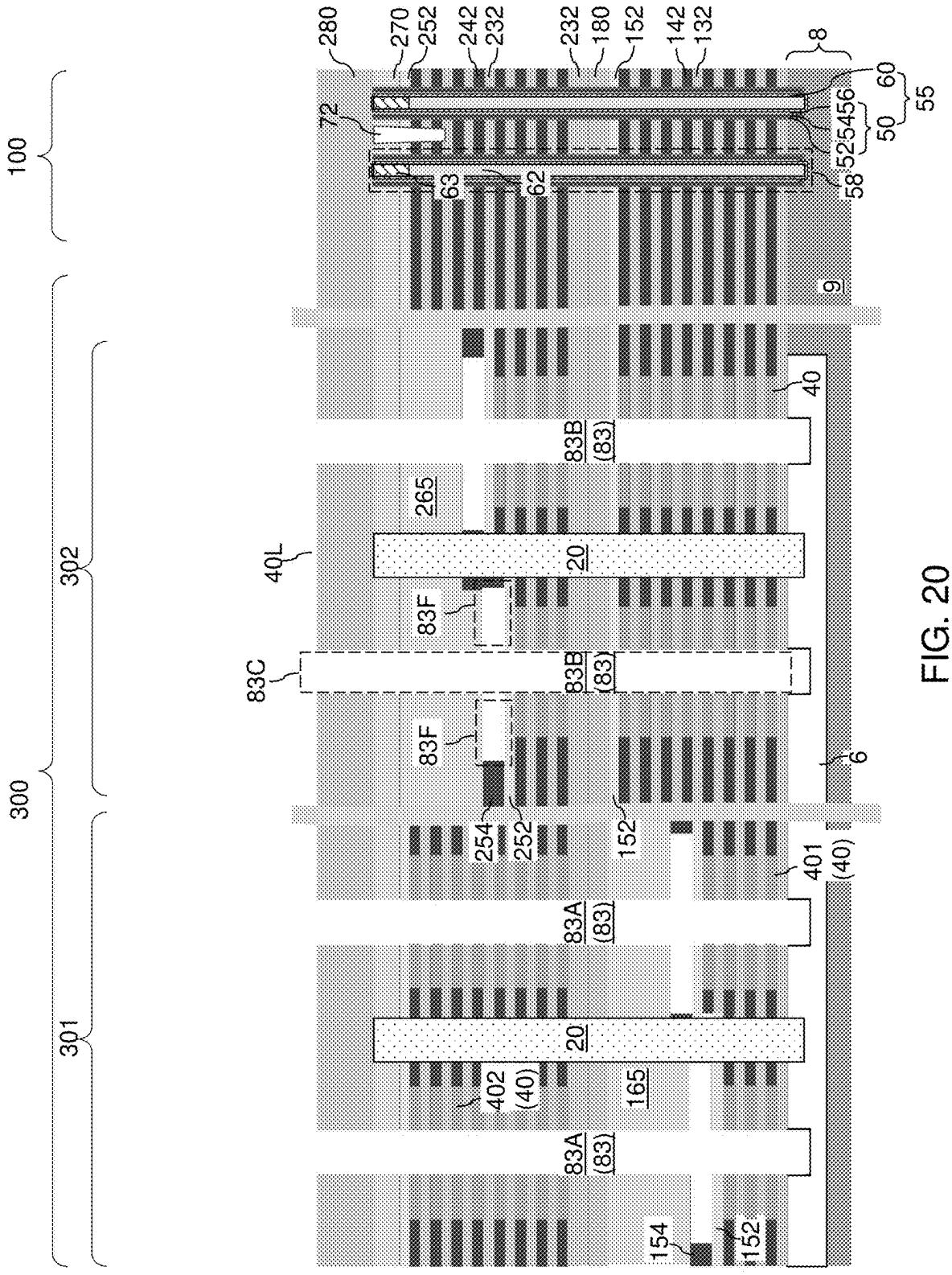
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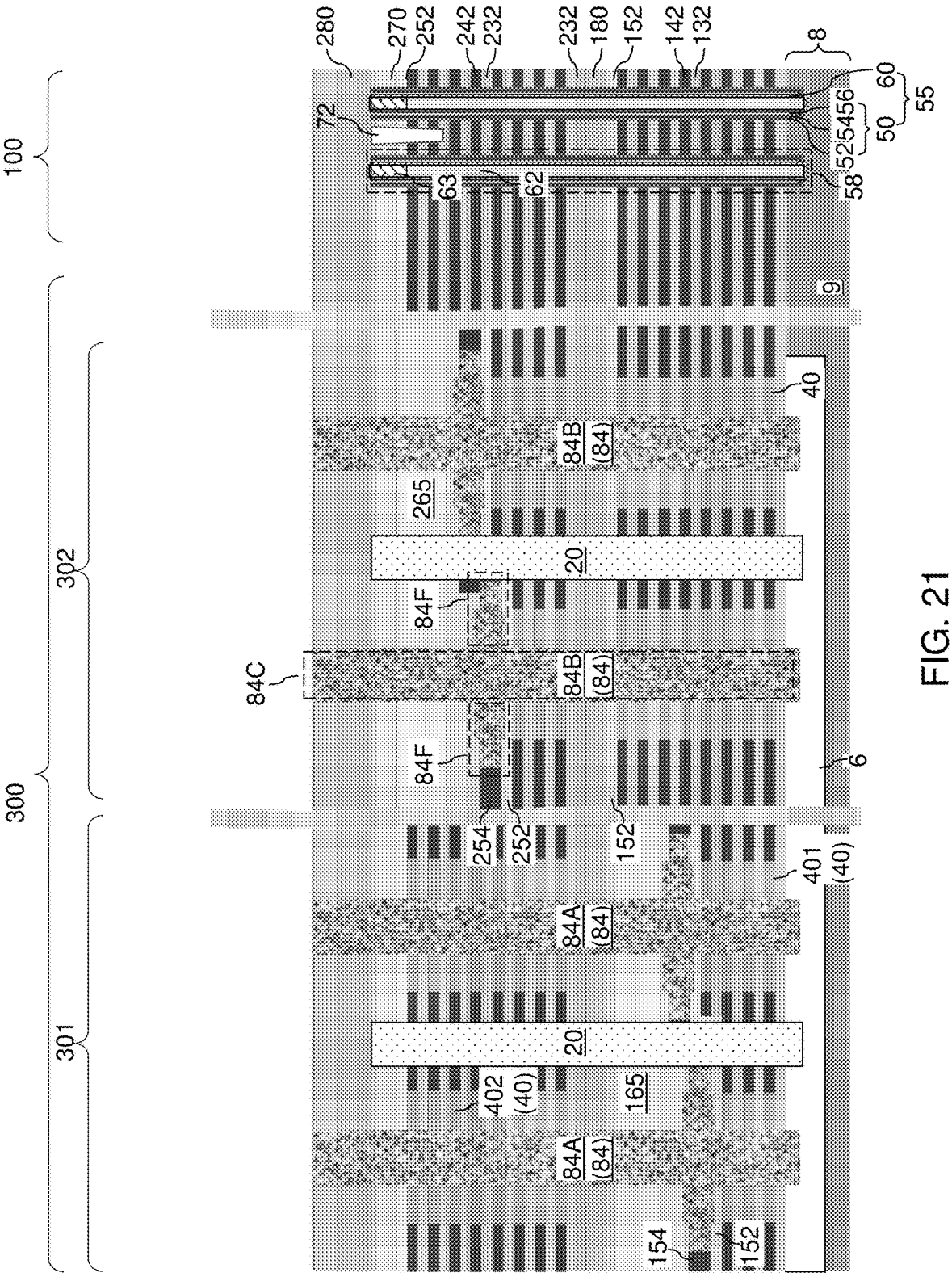
FIG. 20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84A
(84)
20
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(40)
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84A
(84)
154
152

FIG. 21

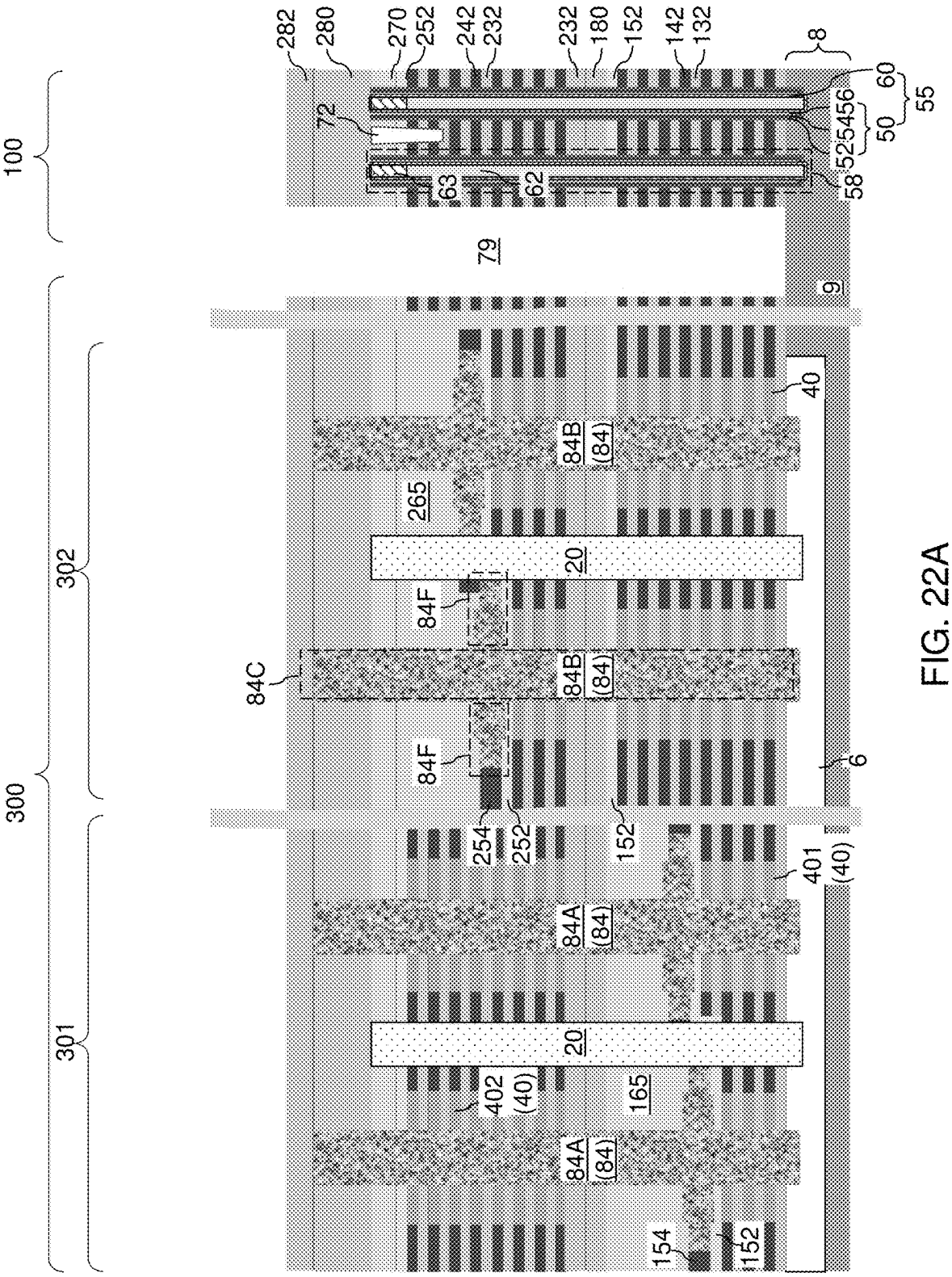
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FIG. 22A

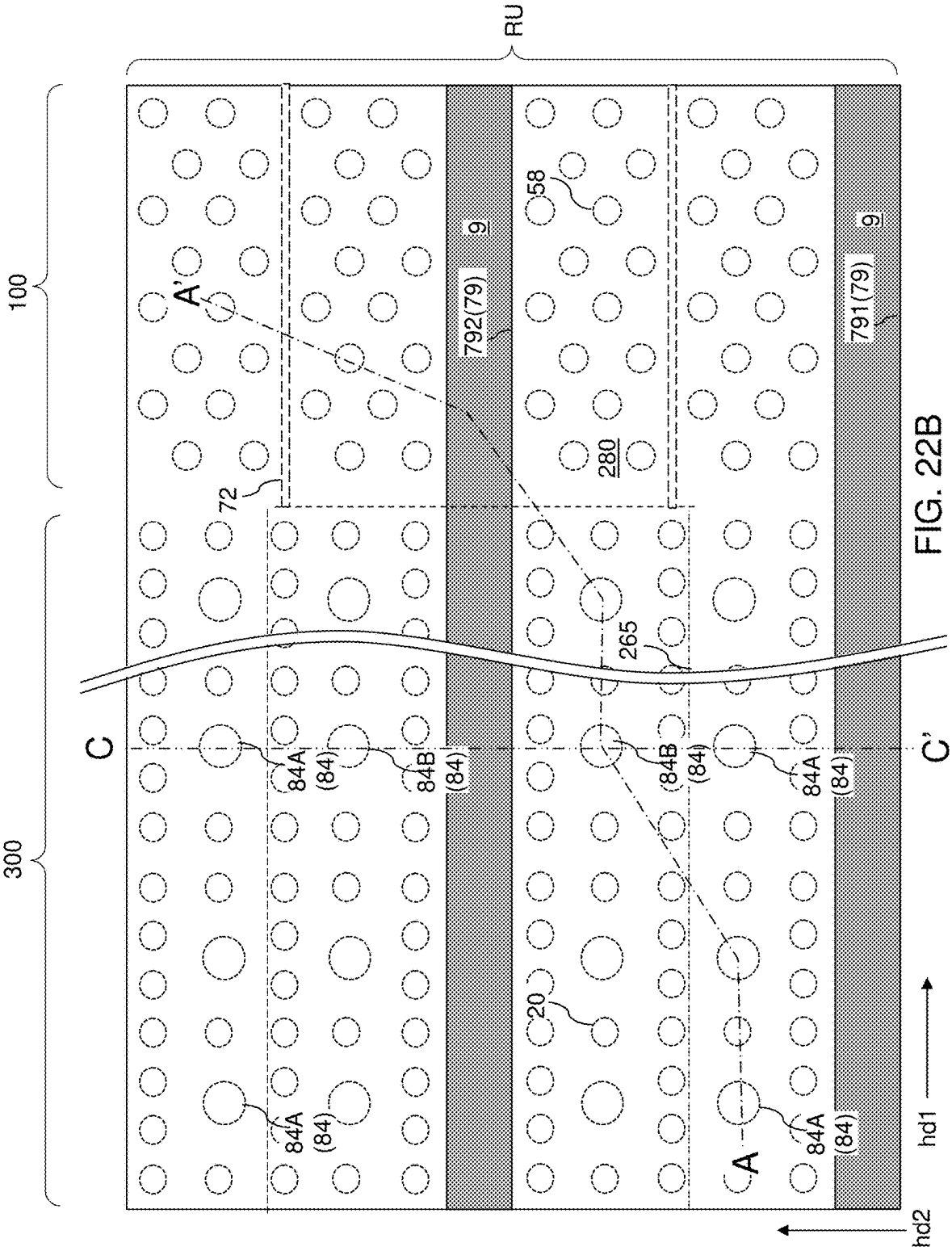
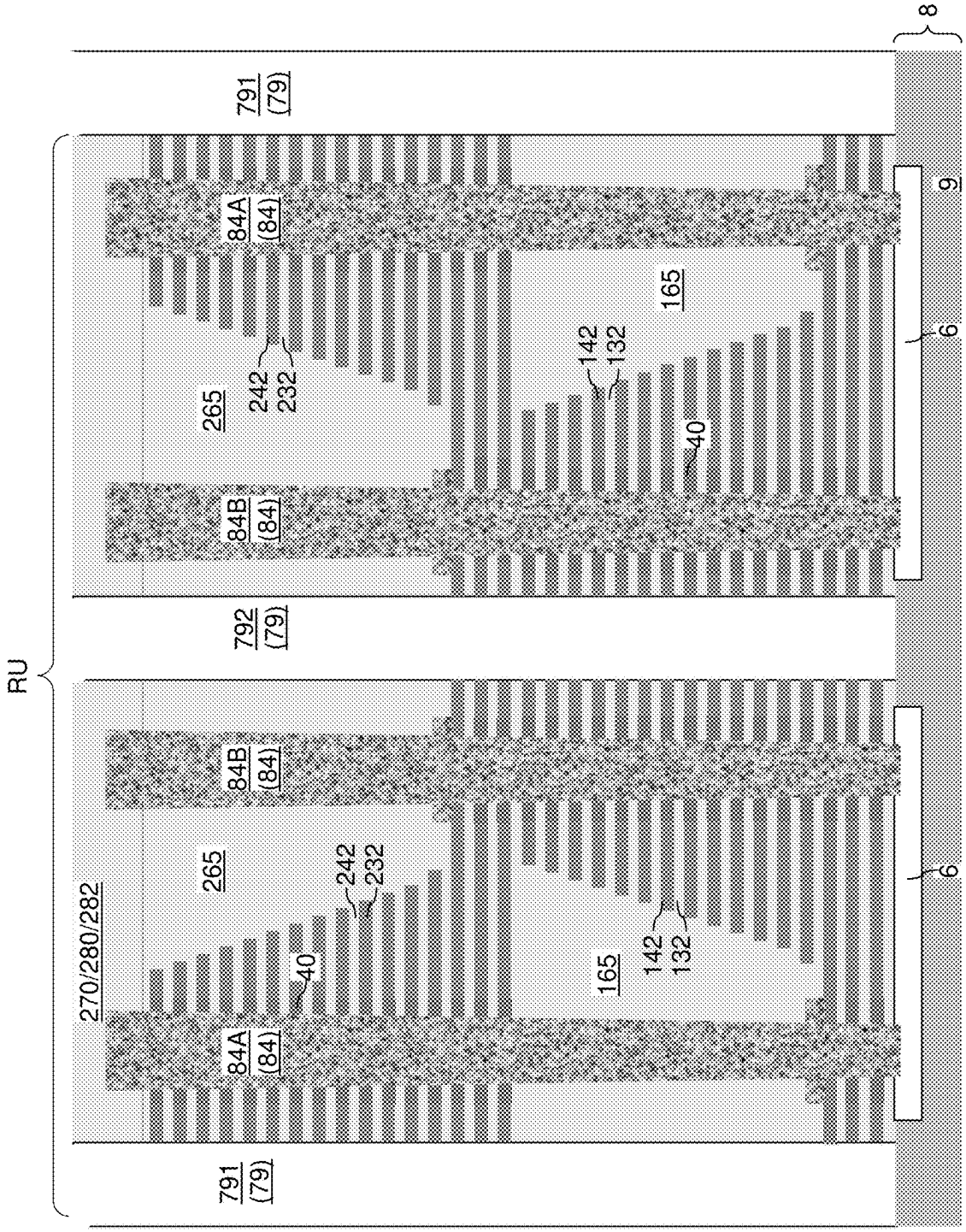


FIG. 22B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792
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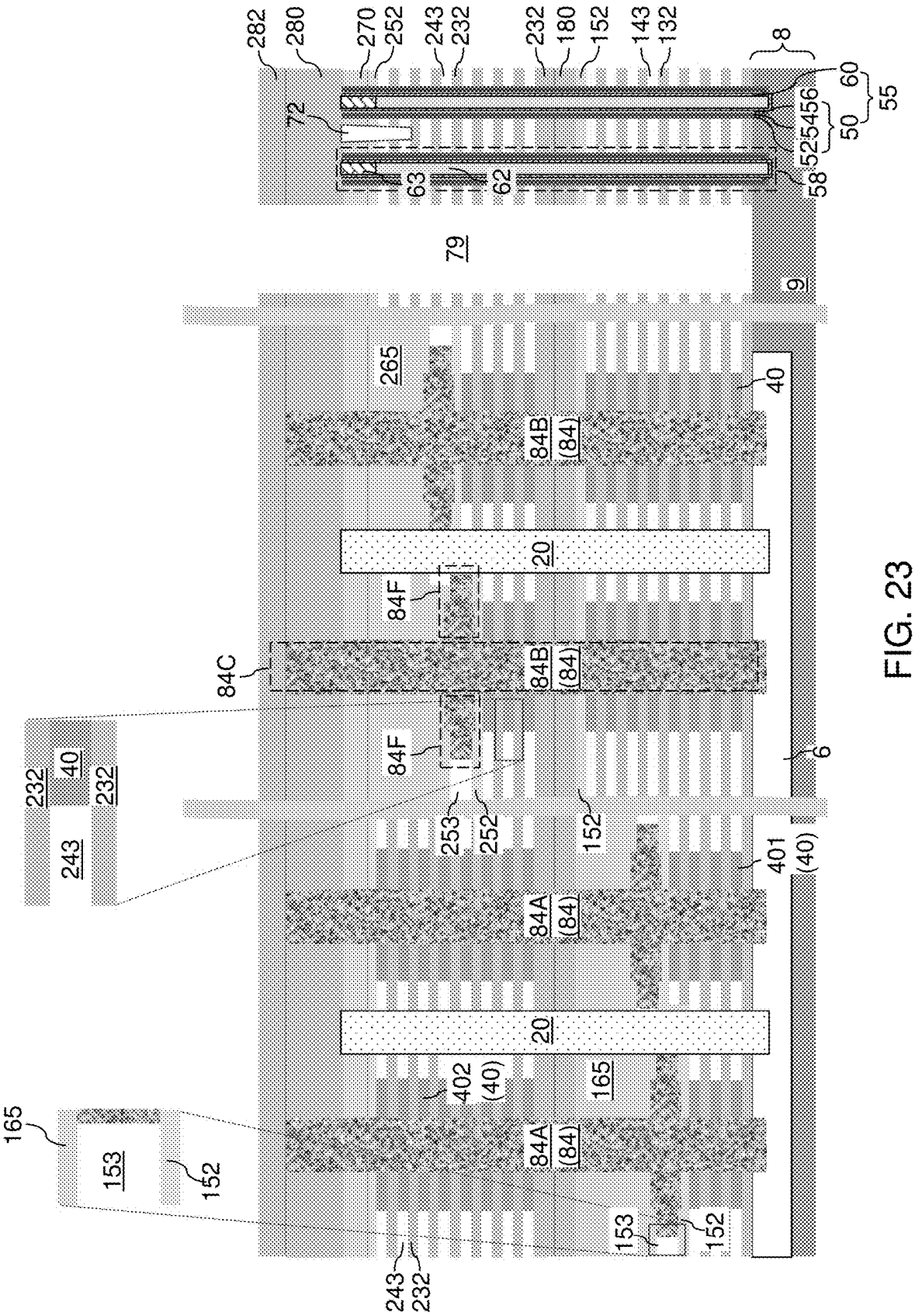
6
270/280/282

FIG. 22C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232
243
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252
152
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84A
(84)
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243
232

FIG. 23

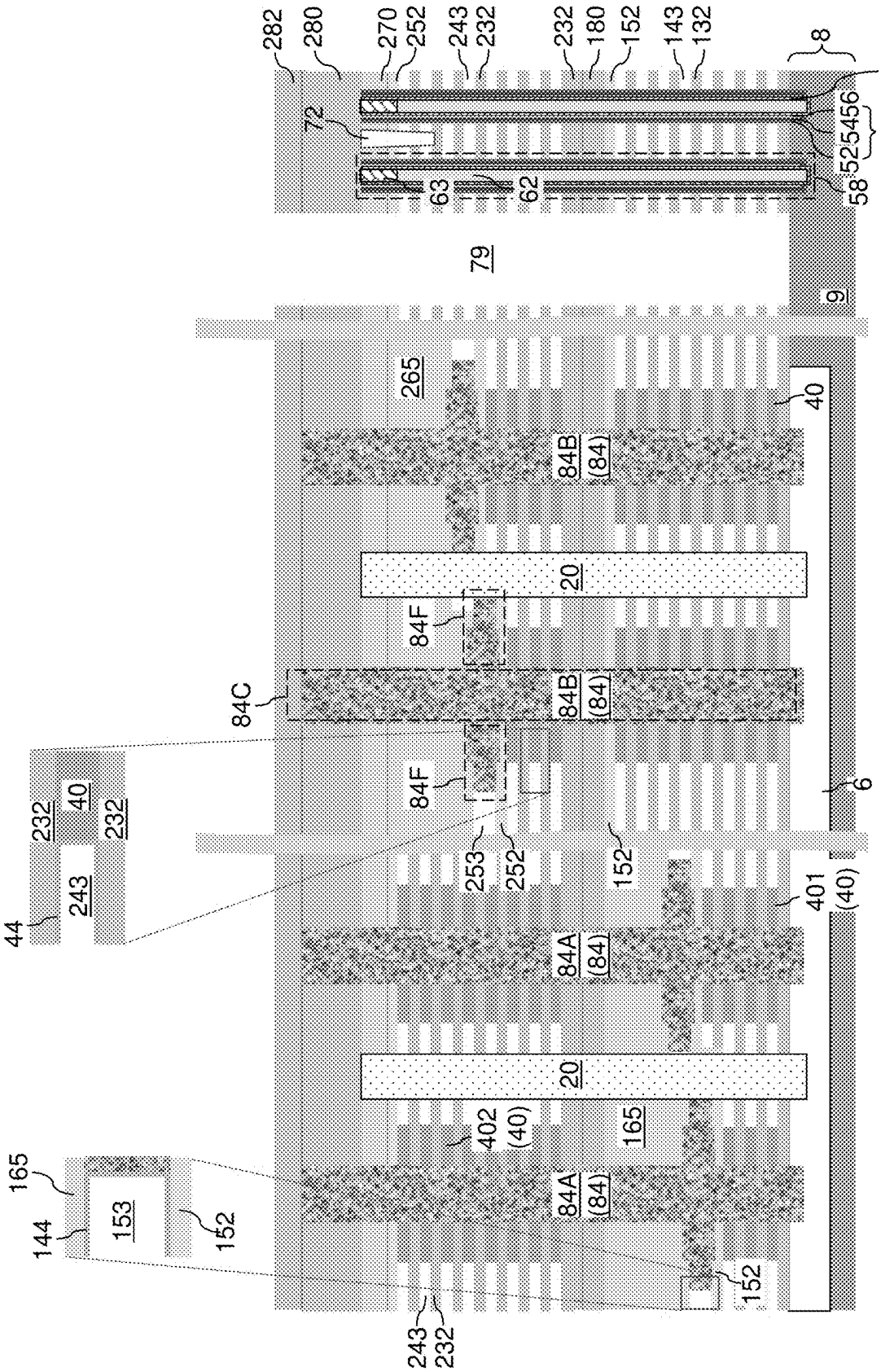
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FIG. 24

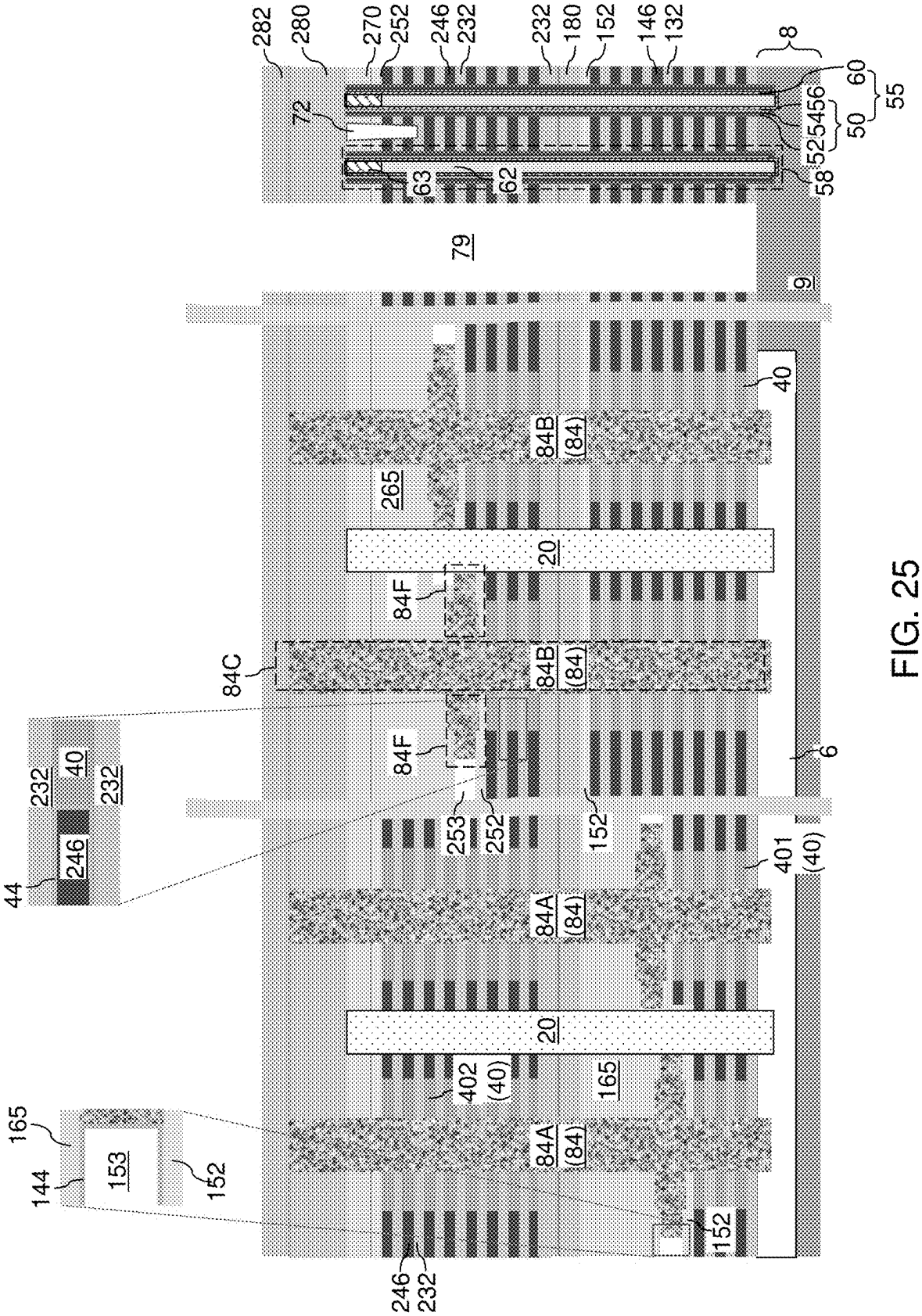
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FIG. 25

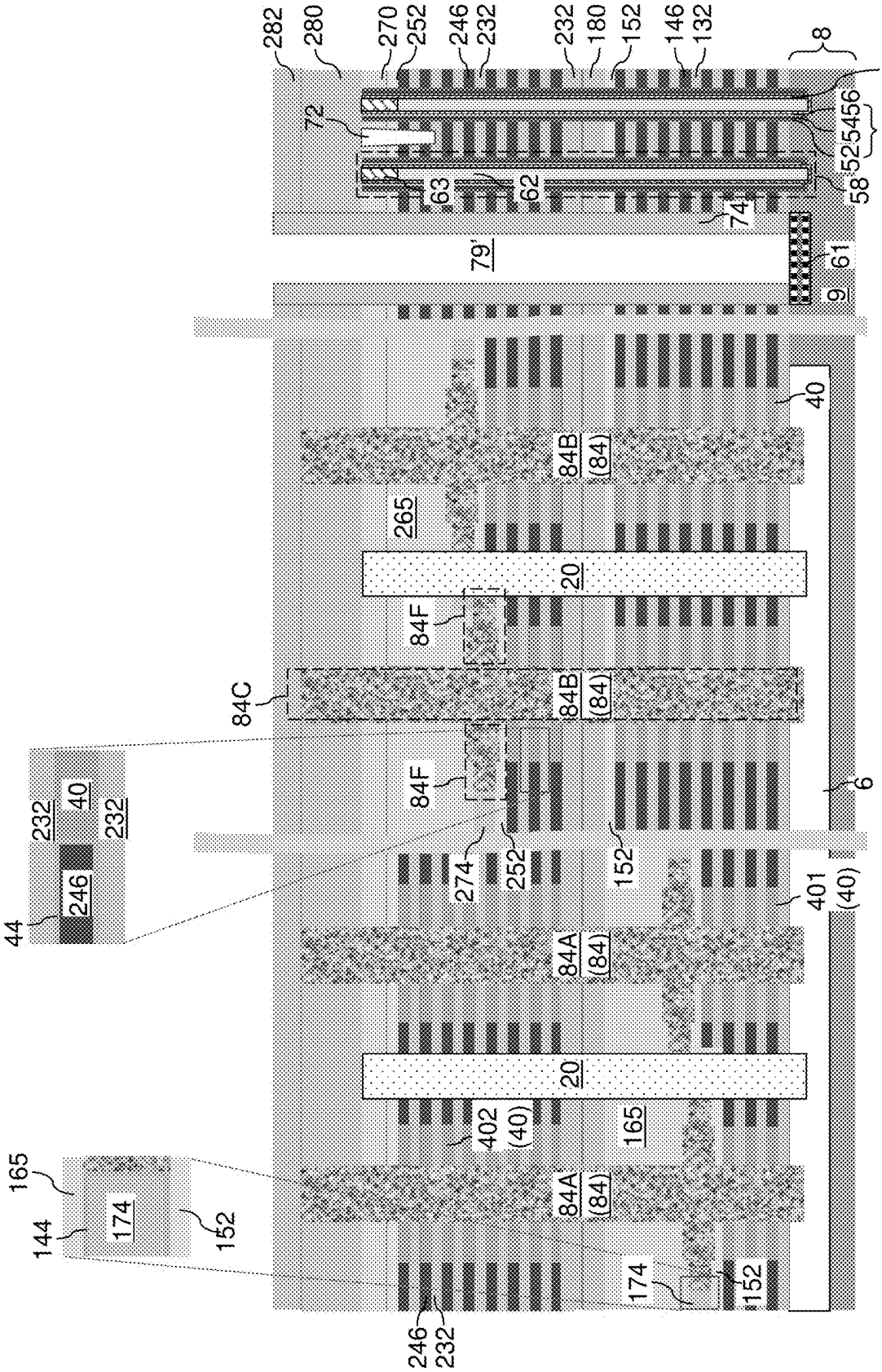
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FIG. 26

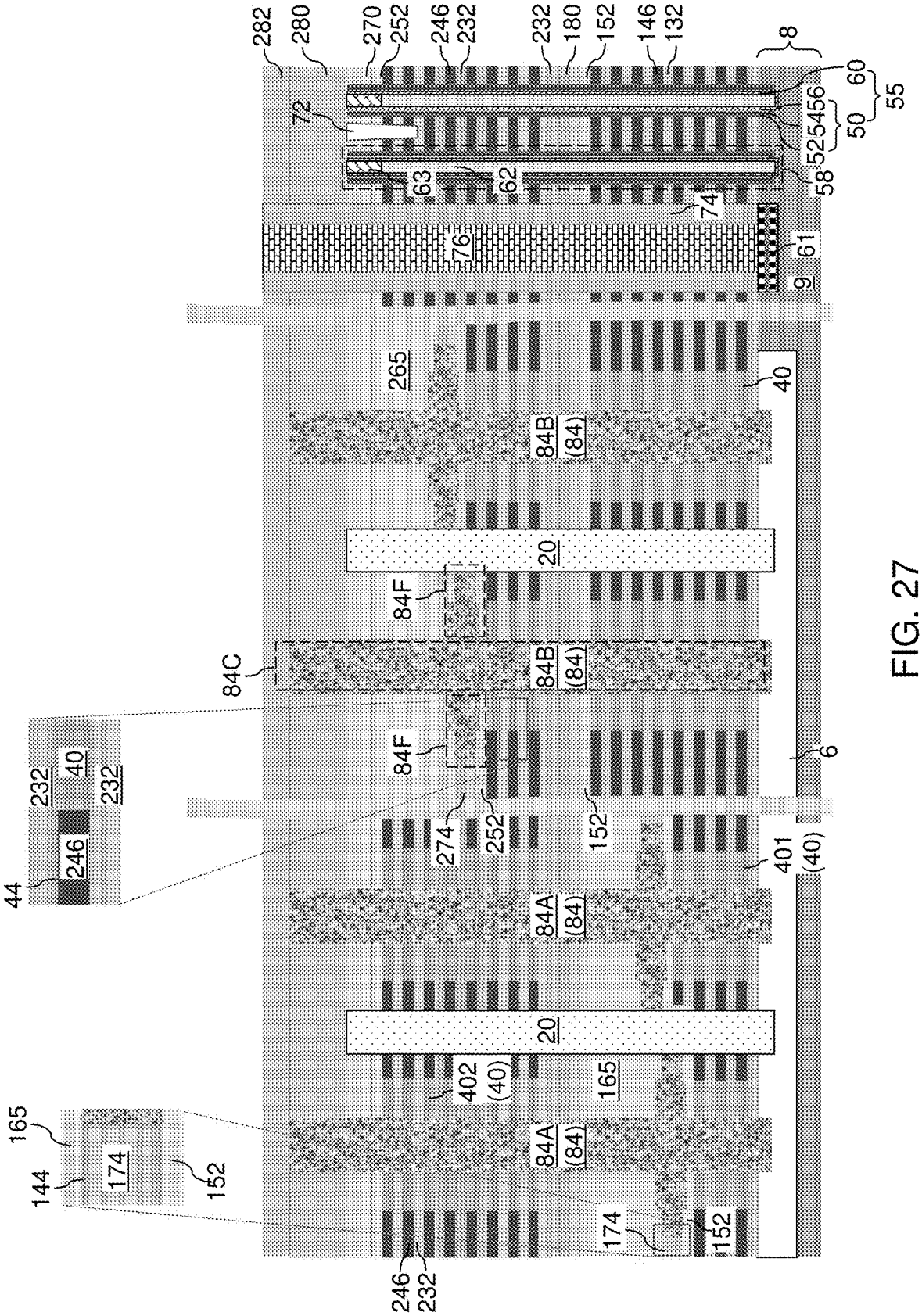
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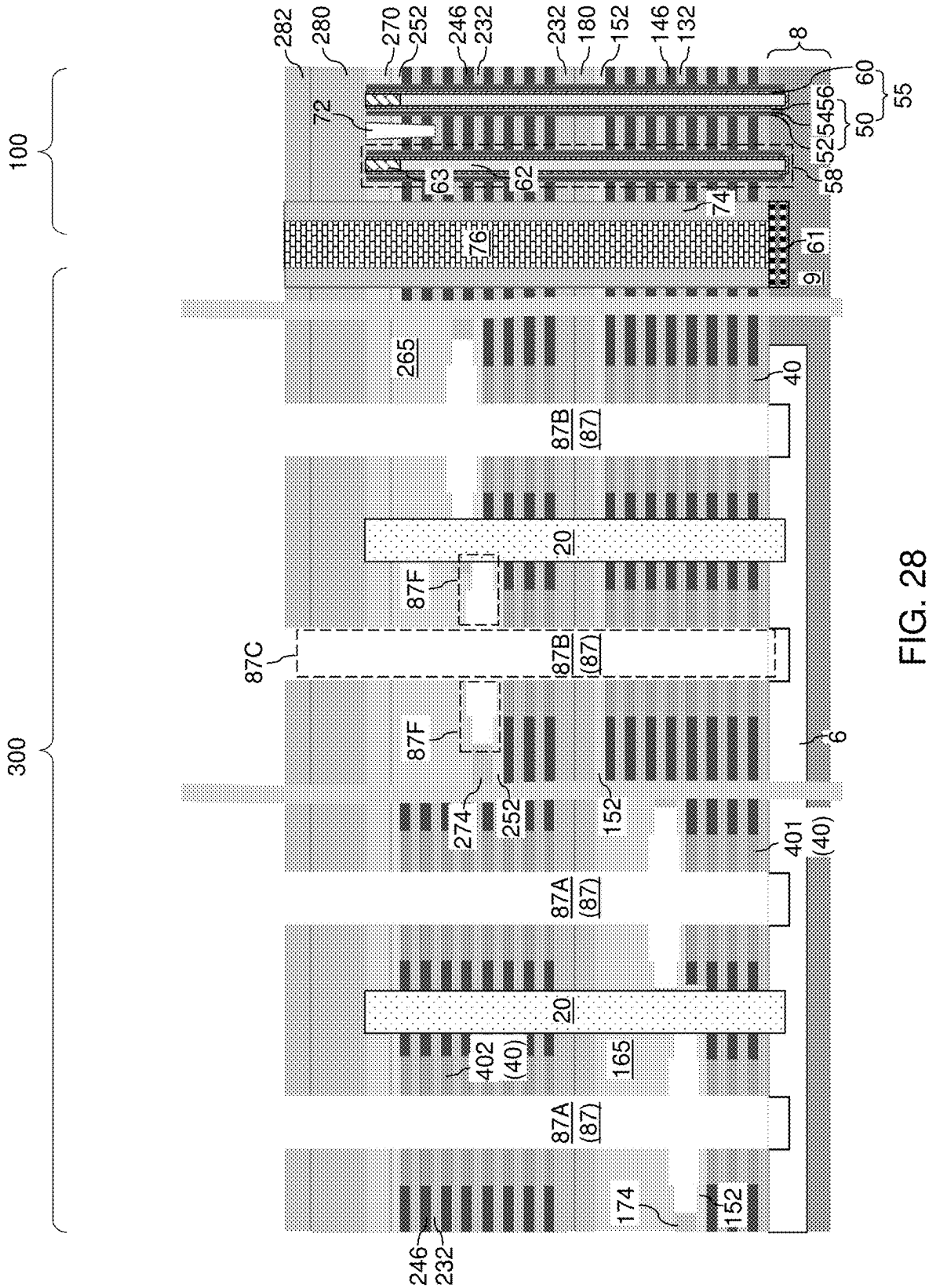
FIG. 27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246
232

FIG. 28

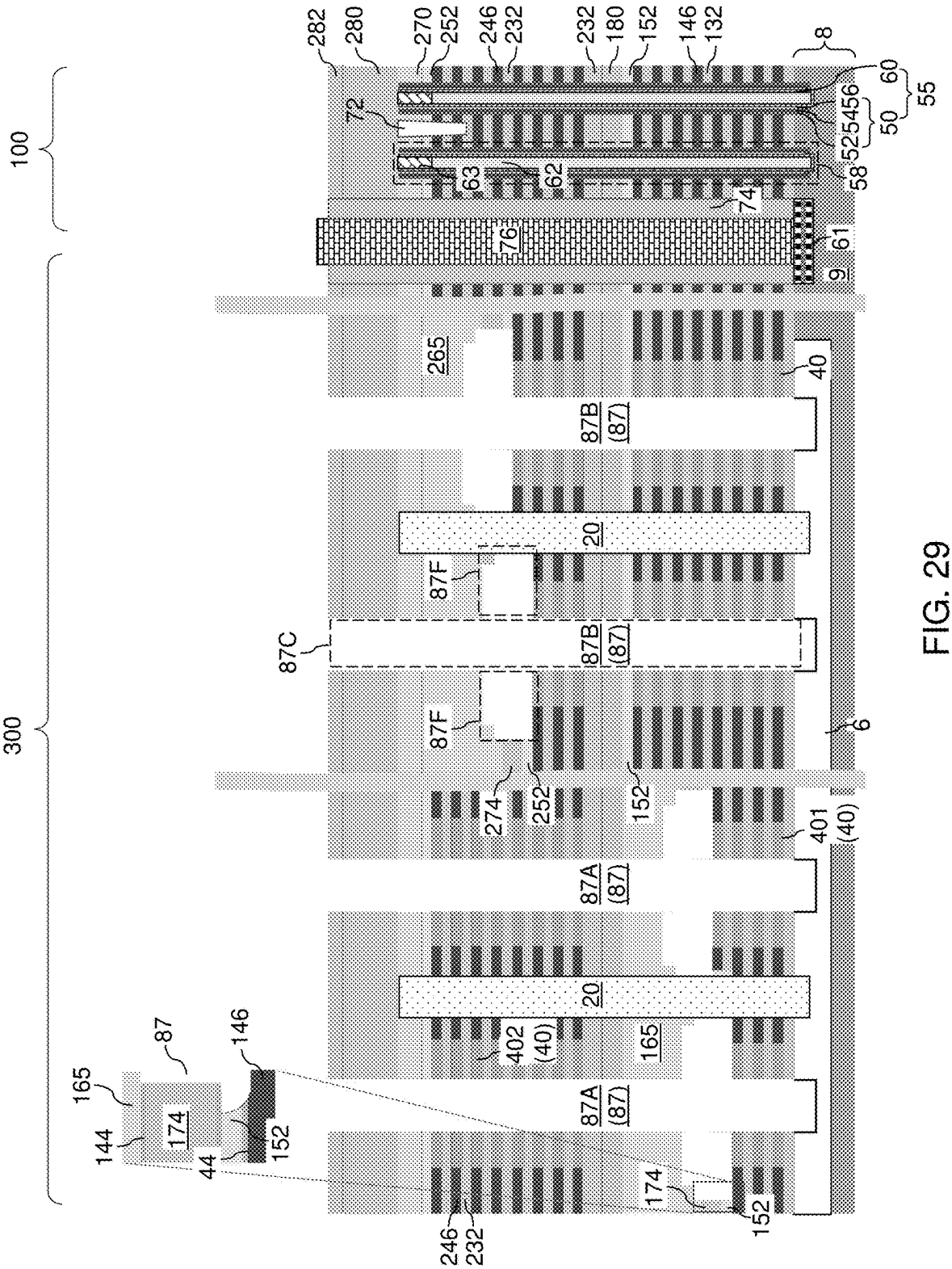
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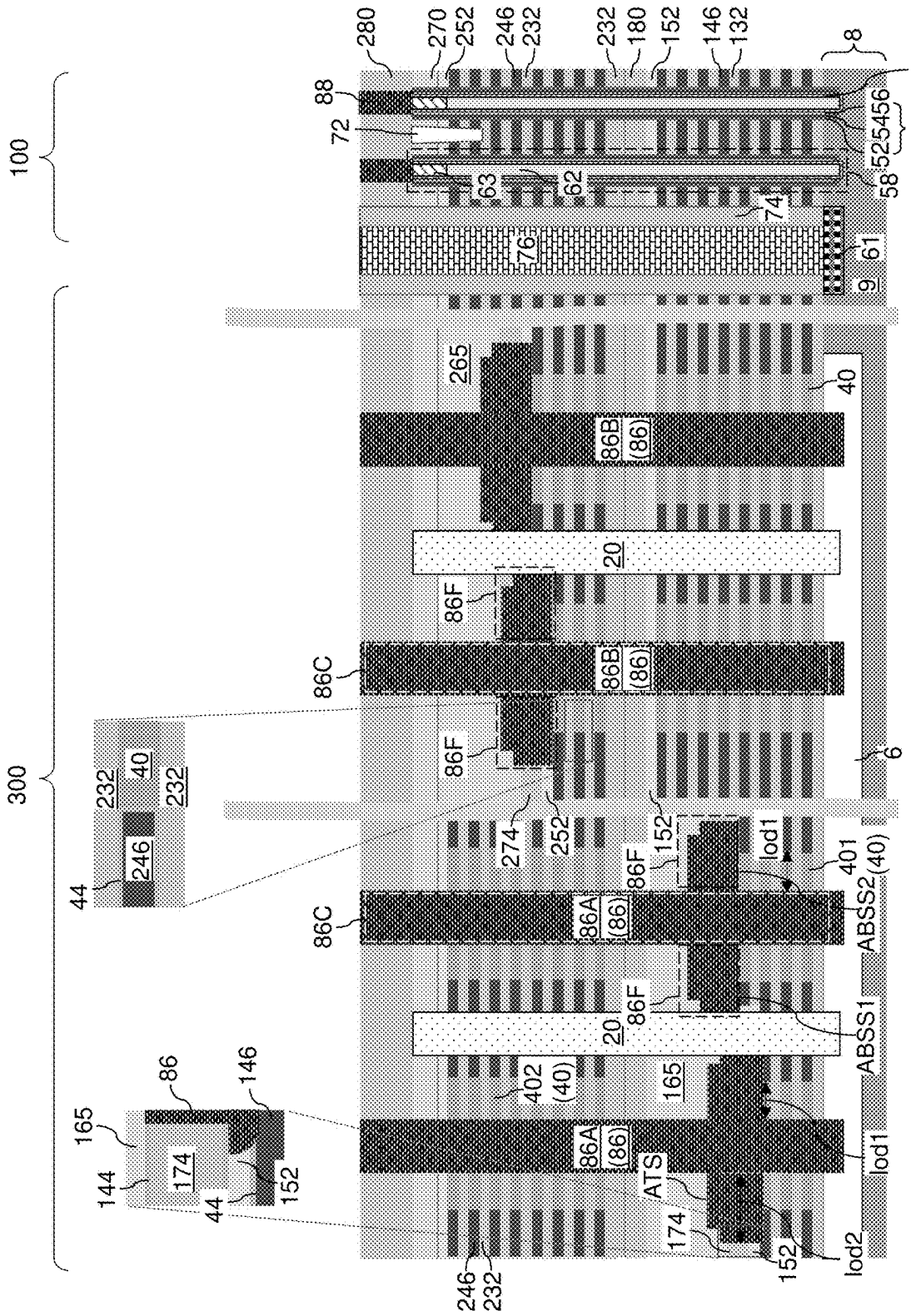
FIG. 29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401
86C
86A
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ABSS1
86
146
165
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lod1
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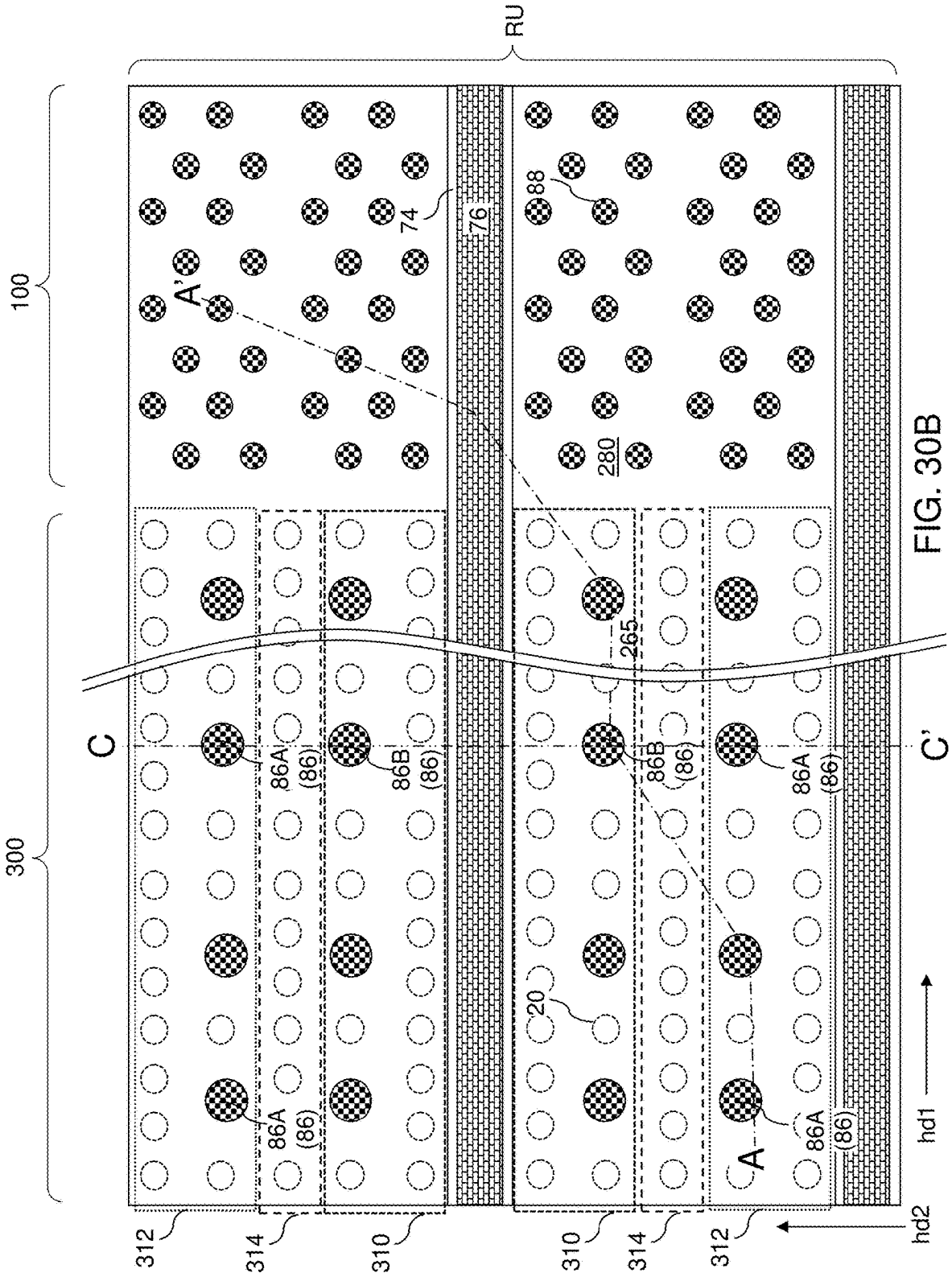
lod2
246
232

FIG. 30A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hd1
hd2

FIG. 30B

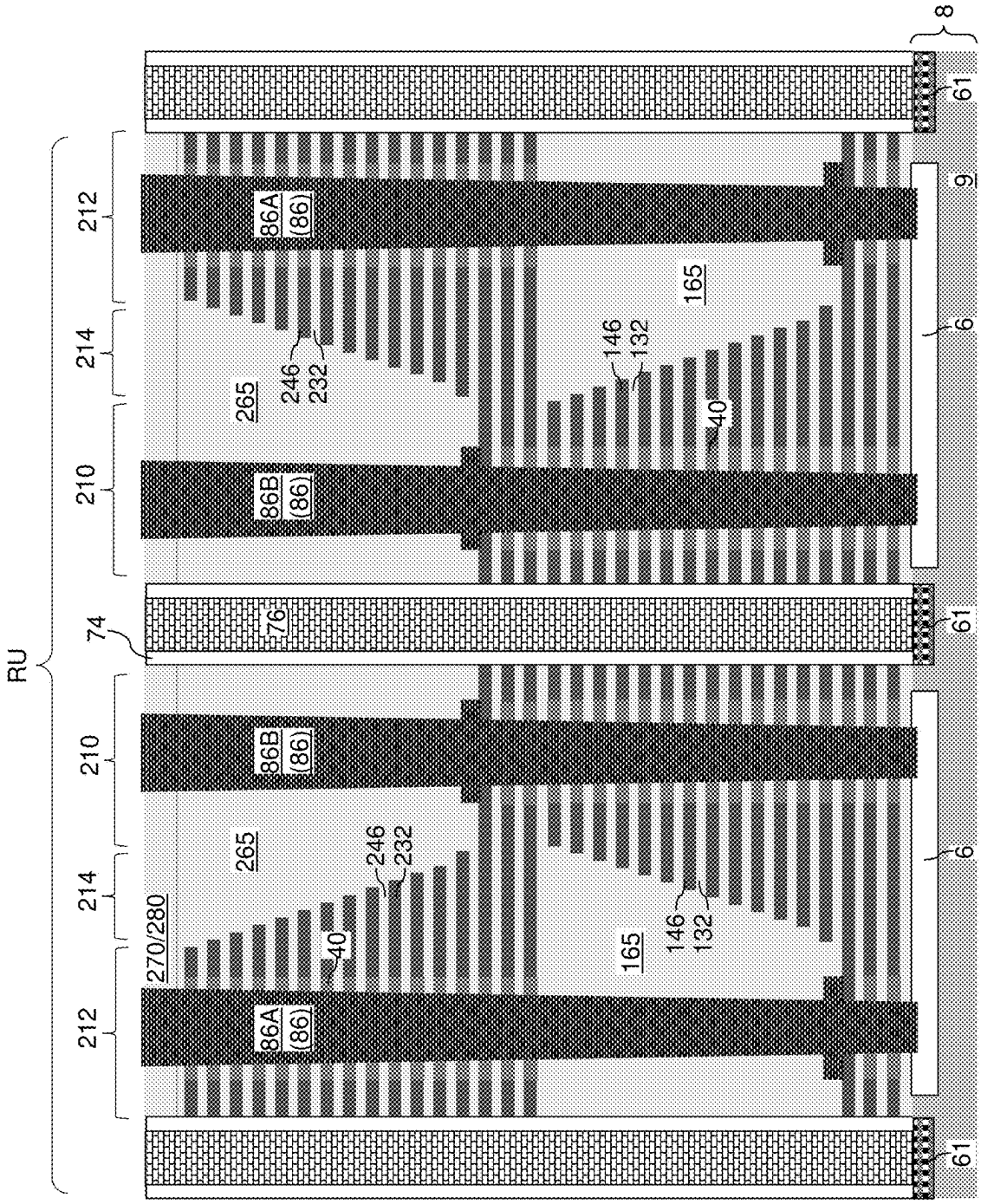
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FIG. 30C

MULTI-TIER MEMORY ARRAY INCLUDING LATERALLY-STAGGERED STAIRCASES AND METHOD OF MAKING THE SAME

FIELD

[0001] The present disclosure relates generally to the field of semiconductor devices, and particularly to a multi-tier memory array including laterally-staggered staircases and methods for manufacturing the same.

BACKGROUND

[0002] Three-dimensional vertical NAND strings having one bit per cell are disclosed in an article by T. Endoh et al., titled "Novel Ultra High Density Memory With A Stacked-Surrounding Gate Transistor (S-SGT) Structured Cell", IEDM Proc. (2001) 33-36.

SUMMARY

[0003] According to an aspect of the present disclosure, a memory device comprises: a first-tier alternating stack of first insulating layers and first electrically conductive layers, wherein the first-tier alternating stack comprises a first staircase region having first stepped surfaces; a first-tier retro-stepped dielectric material portion overlying the first stepped surfaces; a second-tier alternating stack of second insulating layers and second electrically conductive layers located over the first-tier alternating stack and the first-tier retro-stepped dielectric material portion, wherein the second-tier alternating stack comprises a second staircase region having second stepped surfaces; a second-tier retro-stepped dielectric material portion overlying the second stepped surfaces; memory stack structures vertically extending through each layer within the first-tier alternating stack and through each layer within the second-tier alternating stack in a memory array region; and first-type layer contact via structures vertically extending through each layer within the second-tier alternating stack and through the first-tier retro-stepped dielectric material portion, wherein each of the first-type layer contact via structures contacts a respective one of the first electrically conductive layers.

[0004] According to another aspect of the present disclosure, a method of forming a memory device is provided, which comprises: forming a first-tier alternating stack of first insulating layers and first sacrificial material layers over a substrate; forming first stepped surfaces in a first staircase region by patterning the first-tier alternating stack such that first vertical surface segments of the first stepped surfaces are laterally spaced apart along a first horizontal direction and are interconnected to each other by first horizontally-extending surface segments of the first stepped surfaces, wherein the first staircase region has a first area having a first width along a second horizontal direction that is perpendicular to the first horizontal direction in a plan view; forming a first-tier retro-stepped dielectric material portion over the first stepped surfaces; forming a second-tier alternating stack of second insulating layers and second sacrificial material layers over the first-tier alternating stack and the first-tier retro-stepped dielectric material portion; forming second stepped surfaces in a second staircase region by patterning the second-tier alternating stack such that second vertical surface segments of the second stepped surfaces are laterally spaced apart along the first horizontal direction and are interconnected to each other by second horizontally-extending surface segments of the second stepped surfaces, wherein the second staircase region has a second area having a second width along the second horizontal direction in the plan view, and the second area is laterally shifted relative to the first area along the second horizontal direction by a lateral offset distance that is greater than one half of the first width and is less than the first width so that a partial overlap between the second area and the first area is present in the plan view; forming memory stack structures through each layer within the first-tier alternating stack and with the second-tier alternating stack in at least one memory array region; forming first and second lateral isolation trenches, wherein the first lateral isolation trench cuts through the second-tier alternating stack, the first-tier alternating stack, and the first-tier retro-stepped dielectric material portion and does not contact the second-tier retro-stepped dielectric material portion, and the second lateral isolation trench cuts through the second-tier alternating stack, the second-tier retro-stepped dielectric material portion, and the first-tier alternating stack and does not contact the first-tier retro-stepped dielectric material portion; and replacing the first sacrificial material layers and the second sacrificial material layers with first electrically conductive layers and second electrically conductive layers, respectively, to form a replaced first-tier alternating stack and a replaced second-tier alternating stack.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] FIG. **1**A is a vertical cross-sectional view of an exemplary structure after formation of a dielectric isolation layer, a first-tier alternating stack of first insulating layers and first sacrificial material layers, and first stepped surfaces according to an embodiment of the present disclosure.

[0006] FIG. **1**B is a top-down view of the exemplary structure of FIG. **1**A. The hinged vertical plane A-A' is the cut plane of the vertical cross-sectional view of FIG. **1**A.

[0007] FIG. **1**C is a vertical cross-sectional view of the exemplary structure along the vertical plane C-C' of FIG. **1**B.

[0008] FIG. **1**D is a zoom-out top-down view of the exemplary structure of FIGS. **1**A-**1**C, which shows the area of a memory die, according to an embodiment of the present disclosure. Area B is the area of the top-down view of FIG. **1**B.

[0009] FIG. **2** is a vertical cross-sectional view of the exemplary structure after formation of a first insulating liner and a first sacrificial liner over the first stepped surfaces according to an embodiment of the present disclosure.

[0010] FIG. **3**A is a vertical cross-sectional view of the exemplary structure after formation of a first-tier retro-stepped dielectric material portion according to an embodiment of the present disclosure.

[0011] FIG. **3**B is a top-down view of the exemplary structure of FIG. **3**A. The hinged vertical plane A-A' is the cut plane of the vertical cross-sectional view of FIG. **3**A.

[0012] FIG. **3**C is a vertical cross-sectional view of the exemplary structure along the vertical plane C-C' of FIG. **3**B.

[0013] FIG. **3**D is a zoom-out top-down view of the exemplary structure of FIGS. **3**A-**3**C, which shows the area of a memory die, according to an embodiment of the present disclosure. Area B is the area of the top-down view of FIG. **3**B.

[0014] FIG. **4** is a vertical cross-sectional view of the exemplary structure after formation of an inter-tier dielectric layer and first-tier memory openings according to an embodiment of the present disclosure.

[0015] FIG. **5**A is a vertical cross-sectional view of the exemplary structure after formation of first-tier support openings and first-tier contact openings according to an embodiment of the present disclosure.

[0016] FIG. **5**B is a top-down view of the exemplary structure of FIG. **5**A. The hinged vertical plane A-A' is the cut plane of the vertical cross-sectional view of FIG. **5**A.

[0017] FIG. **5**C is a vertical cross-sectional view of the exemplary structure along the vertical plane C-C' of FIG. **5**B.

[0018] FIG. **5**D is a zoom-out top-down view of the exemplary structure of FIGS. **5**A-**5**C, which shows the area of a memory die, according to an embodiment of the present disclosure. Area B is the area of the top-down view of FIG. **5**B.

[0019] FIG. **6** is a vertical cross-sectional view of the exemplary structure after formation of first-tier sacrificial memory opening fill structures, first-tier sacrificial support opening fill structures, and first-tier sacrificial contact opening fill structures according to an embodiment of the present disclosure.

[0020] FIG. **7** is a vertical cross-sectional view of the exemplary structure after formation of a second-tier alternating stack of second insulating layers and second sacrificial material layers and second stepped surfaces according to an embodiment of the present disclosure.

[0021] FIG. **8** is a vertical cross-sectional view of the exemplary structure after formation of a second insulating liner and a second sacrificial liner over the second stepped surfaces according to an embodiment of the present disclosure.

[0022] FIG. **9**A is a vertical cross-sectional view of the exemplary structure after formation of a second retro-stepped dielectric material portion and an insulating cap layer according to an embodiment of the present disclosure.

[0023] FIG. **9**B is a top-down view of the exemplary structure of FIG. **9**A. The hinged vertical plane A-A' is the cut plane of the vertical cross-sectional view of FIG. **9**A.

[0024] FIG. **9**C is a vertical cross-sectional view of the exemplary structure along the vertical plane C-C' of FIG. **9**B.

[0025] FIG. **9**D is a zoom-out top-down view of the exemplary structure of FIGS. **9**A-**9**C, which shows the area of a memory die, according to an embodiment of the present disclosure. Area B is the area of the top-down view of FIG. **9**B.

[0026] FIG. **10**A is a vertical cross-sectional view of the exemplary structure after formation of multi-tier support openings and multi-tier contact openings according to an embodiment of the present disclosure.

[0027] FIG. **10**B is a top-down view of the exemplary structure of FIG. **10**A. The hinged vertical plane A-A' is the cut plane of the vertical cross-sectional view of FIG. **10**A.

[0028] FIG. **10**C is a vertical cross-sectional view of the exemplary structure along the vertical plane C-C' of FIG. **10**B.

[0029] FIG. **10**D is a zoom-out top-down view of the exemplary structure of FIGS. **10**A-**10**C, which shows the area of a memory die, according to an embodiment of the present disclosure. Area B is the area of the top-down view of FIG. **10**B.

[0030] FIG. **11** is a vertical cross-sectional view of the exemplary structure after formation of sacrificial support opening fill structures and sacrificial contact opening fill structures according to an embodiment of the present disclosure.

[0031] FIG. **12** is a vertical cross-sectional view of the exemplary structure after formation of inter-tier support openings according to an embodiment of the present disclosure.

[0032] FIG. **13** is a vertical cross-sectional view of the exemplary structure after formation of support pillar structures according to an embodiment of the present disclosure.

[0033] FIG. **14** is a vertical cross-sectional view of the exemplary structure after formation of memory openings according to an embodiment of the present disclosure.

[0034] FIG. **15** is a vertical cross-sectional view of the exemplary structure after formation of memory opening fill structures according to an embodiment of the present disclosure.

[0035] FIG. **16**A is a vertical cross-sectional view of the exemplary structure after formation of a contact-level dielectric layer and contact via cavities according to an embodiment of the present disclosure.

[0036] FIG. **16**B is a top-down view of the exemplary structure of FIG. **16**A. The hinged vertical plane A-A' is the plane of the vertical cross-sectional view of FIG. **16**A.

[0037] FIG. **16**C is a vertical cross-sectional view of the exemplary structure along the vertical plane C-C' of FIG. **16**B.

[0038] FIG. **17** is a vertical cross-sectional view of the exemplary structure after formation of first-stage in-process finned contact via cavities according to an embodiment of the present disclosure.

[0039] FIG. **18** is a vertical cross-sectional view of the exemplary structure after conformally depositing a conformal dielectric material layer according to an embodiment of the present disclosure.

[0040] FIG. **19** is a vertical cross-sectional view of the exemplary structure after formation of vertical stacks of annular insulating plates and according to an embodiment of the present disclosure.

[0041] FIG. **20** is a vertical cross-sectional view of the exemplary structure after laterally expanding the second-stage in-process finned contact via cavities to form third-stage in-process finned contact via cavities according to an embodiment of the present disclosure.

[0042] FIG. **21** is a vertical cross-sectional view of the exemplary structure after formation of sacrificial finned cavity fill material structures according to an embodiment of the present disclosure.

[0043] FIG. **22**A is a vertical cross-sectional view of the exemplary structure after formation of a sacrificial contact-level dielectric layer and lateral isolation trenches according to an embodiment of the present disclosure.

[0044] FIG. **22**B is a top-down view of the exemplary structure of FIG. **22**A. The hinged vertical plane A-A' is the plane of the vertical cross-sectional view of FIG. **22**A.

[0045] FIG. **22**C is a vertical cross-sectional view of the exemplary structure along the vertical plane C-C' of FIG. **22**B.

[0046] FIG. **23** is a vertical cross-sectional view of the exemplary structure after formation of laterally-extending cavities according to an embodiment of the present disclosure.

[0047] FIG. **24** is a vertical cross-sectional view of the exemplary structure after formation of backside blocking dielectric layers and a blocking dielectric liner according to an embodiment of the present disclosure.

[0048] FIG. **25** is a vertical cross-sectional view of the exemplary structure after formation of electrically conductive layers according to an embodiment of the present disclosure.

[0049] FIG. **26** is a vertical cross-sectional view of the exemplary structure after formation of source regions and insulating spacers according to an embodiment of the present disclosure.

[0050] FIG. **27** is a vertical cross-sectional view of the exemplary structure after formation of source contact via structures according to an embodiment of the present disclosure.

[0051] FIG. **28** is a vertical cross-sectional view of the exemplary structure after removal of the sacrificial finned cavity fill material structures according to an embodiment of the present disclosure.

[0052] FIG. **29** is a vertical cross-sectional view of the exemplary structure after expanding finned contact via cavities according to an embodiment of the present disclosure.

[0053] FIG. **30**A is a vertical cross-sectional view of the exemplary structure after formation of contact via structures according to an embodiment of the present disclosure.

[0054] FIG. **30**B is a top-down view of the exemplary structure of FIG. **30**A. The hinged vertical plane A-A' is the plane of the vertical cross-sectional view of FIG. **30**A.

[0055] FIG. **30**C is a vertical cross-sectional view of the exemplary structure along the vertical plane C-C' of FIG. **30**B.

DETAILED DESCRIPTION

[0056] As discussed above, the present disclosure is directed to a multi-tier memory array including laterally-staggered staircases and dielectric material portions and methods for manufacturing the same, the various aspects of which are described below.

[0057] The drawings are not drawn to scale. Multiple instances of an element may be duplicated where a single instance of the element is illustrated, unless absence of duplication of elements is expressly described or clearly indicated otherwise. Ordinals such as "first," "second," and "third" are employed merely to identify similar elements, and different ordinals may be employed across the specification and the claims of the instant disclosure. The term "at least one" element refers to all possibilities including the possibility of a single element and the possibility of multiple elements.

[0058] The same reference numerals refer to the same element or similar element. Unless otherwise indicated, elements having the same reference numerals are presumed to have the same composition and the same function. Unless otherwise indicated, a "contact" between elements refers to a direct contact between elements that provides an edge or a surface shared by the elements. If two or more elements are not in direct contact with each other or among one another, the two elements are "disjoined from" each other or "disjoined among" one another. As used herein, an element located "on" a second element can be located on the exterior side of a surface of the second element or on the interior side of the second element. As used herein, an element is located "directly on" a second element if there exist a physical contact between a surface of the element and a surface of the second element. As used herein, an element is "electrically connected to" a second element if there exists a conductive path consisting of at least one conductive material between the element and the second element. As used herein, a "prototype" structure or an "in-process" structure refers to a transient structure that is subsequently modified in the shape or composition of at least one component therein.

[0059] As used herein, a "layer" refers to a material portion including a region having a thickness. A layer may extend over the entirety of an underlying or overlying structure, or may have an extent less than the extent of an underlying or overlying structure. Further, a layer may be a region of a homogeneous or inhomogeneous continuous structure that has a thickness less than the thickness of the continuous structure. For example, a layer may be located between any pair of horizontal planes between, or at, a top surface and a bottom surface of the continuous structure. A layer may extend horizontally, vertically, and/or along a tapered surface. A substrate may be a layer, may include one or more layers therein, or may have one or more layer thereupon, thereabove, and/or therebelow.

[0060] Generally, a semiconductor die, or a semiconductor package, can include a memory chip. Each semiconductor package contains one or more dies (for example one, two, or four). The die is the smallest unit that can independently execute commands or report status. Each die contains one or more planes (typically one or two). Identical, concurrent operations can take place on each plane, although with some restrictions. Each plane contains a number of blocks, which are the smallest unit that can be erased by in a single erase operation. Each block contains a number of pages, which are the smallest unit that can be programmed, i.e., a smallest unit on which a read operation can be performed.

[0061] Referring to FIGS. **1**A-**1**D, an exemplary structure according to an embodiment of the present disclosure is illustrated, which includes a substrate **8** containing a semiconductor material layer **9** at least in an upper portion thereof. The semiconductor material layer **9** may comprise a single crystalline semiconductor material layer or a polycrystalline semiconductor material layer. The substrate **8** may or may not comprise additional layers (such as dielectric material layers embedding metal interconnect structures) and/or semiconductor devices (such as a peripheral circuit for controlling operation of a three-dimensional memory array to be subsequently formed) underneath the semiconductor material layer. In one embodiment, the substrate **8** may comprise a commercially available semiconductor wafer, such as a single crystalline silicon wafer. The semiconductor material layer **9** may comprise an upper portion of the silicon wafer, a doped well in the silicon wafer, an epitaxial silicon layer on the silicon wafer, etc.

[0062] The exemplary structure comprises two memory array regions **100** that are laterally spaced from each other along a first horizontal direction (e.g., word line direction) hd**1** by a contact region **300**. Each memory array region **100** is a region in which a three-dimensional memory array is to be subsequently formed. The contact region **300** is a region in which layer contact via structures contacting electrically conductive lines that function as word lines of the three-

dimensional memory array are to be subsequently formed. The contact region **300** may comprise a first staircase region **301** in which first contact via structures providing electrical connections to first electrically conductive layers are subsequently formed, and a second staircase region **302** in which second contact via structures providing electrical connections to second electrically conductive layers are subsequently formed. The memory array region **100** can be provided adjacent to the contact region **300**.

[0063] An optional dielectric isolation layer **6** can be formed in an upper portion of the substrate **8**. The dielectric isolation layer **6** may comprise a silicon oxide layer which is located in the contact region **300** and may optionally extend into the memory array region **100**.

[0064] A first-tier alternating stack of first insulating layers **132** and first sacrificial material layers **142** can be formed over the substrate **8**. The first insulating layers **132** comprise an insulating material such as undoped silicate glass or a doped silicate glass, and the first sacrificial material layers **142** comprise a sacrificial material such as silicon nitride or a silicon-germanium alloy. The first-tier alternating stack (**132**, **142**) may comprise multiple repetitions of a unit layer stack including a first insulating layer **132** and a first sacrificial material layer **142**. The total number of repetitions of the unit layer stack within the first-tier alternating stack (**132**, **142**) may be, for example, in a range from 8 to 1,024, such as from 32 to 256, although lesser and greater number of repetitions may also be employed. Each of the first insulating layers **132** may have a thickness in a range from 20 nm to 100 nm, such as from 30 nm to 60 nm, although lesser and greater thicknesses may also be employed. Each of the first sacrificial material layers **142** may have a thickness in a range from 20 nm to 100 nm, such as from 30 nm to 60 nm, although lesser and greater thicknesses may also be employed.

[0065] First stepped surfaces are formed in the first staircase region **301**. As used herein, "stepped surfaces" refer to a set of surfaces that include at least two horizontal surfaces and at least two vertical surfaces such that each horizontal surface is adjoined to a first vertical surface that extends upward from a first edge of the horizontal surface, and is adjoined to a second vertical surface that extends downward from a second edge of the horizontal surface. A first stepped cavity is formed within each volume from which portions of the first-tier alternating stack (**132**, **142**) are removed through formation of the first stepped surfaces. A "stepped cavity" refers to a cavity having stepped surfaces.

[0066] Each first stepped cavity can have various first stepped surfaces such that the horizontal cross-sectional shape of the first stepped cavity changes in steps as a function of the vertical distance from the top surface of the substrate **8**. In one embodiment, the first stepped cavities can be formed by repetitively performing a set of processing steps. The set of processing steps can include, for example, an etch process of a first type that vertically increases the depth of a cavity by one or more levels, and an etch process of a second type that laterally expands the area to be vertically etched in a subsequent etch process of the first type. As used herein, a "level" of a structure including alternating plurality is defined as the relative position of a pair of a first material layer and a second material layer within the structure.

[0067] Each first sacrificial material layer **142** other than a topmost first sacrificial material layer **142** within the first-tier alternating stack (**132**, **142**) laterally extends farther than any overlying first sacrificial material layer **142** within the first-tier alternating stack (**132**, **142**) in the terrace region. The first stepped surfaces of the first-tier alternating stack (**132**, **142**) continuously extend from the bottommost layer within the first-tier alternating stack (**132**, **142**) to the topmost layer within the first-tier alternating stack (**132**, **142**). Generally, the first stepped surfaces continuously extends from a bottommost layer within the first-tier alternating stack (**132**, **142**) at least to a topmost layer within the first-tier alternating stack (**132**, **142**).

[0068] Each set of first stepped surfaces may comprise first horizontally-extending surface segments and first vertically-extending surface segments. The first vertically-extending surface segments are laterally spaced from each other along the first horizontal direction hd**1**, which may be a separation direction between the two memory array regions **100** (e.g., word line direction). The first vertically-extending surface segments can be parallel to a second horizontal direction (e.g., bit line direction) hd**2** which is perpendicular to the first horizontal direction hd**1**. Each contiguous set of first stepped surfaces can be formed within a respective first staircase region **301**. A plurality of first staircase regions **301** laterally spaced from each other along the second horizontal direction hd**2** can be provided in the contact region **300**, as shown in FIGS. **1**B and **1**D. Contiguous sets of first stepped surfaces can be formed in first stepped cavities **133** that are laterally spaced apart from each other along the second horizontal direction hd**2**. Each void within the first-tier alternating stack (**132**, **142**) that overlies a respective contiguous set of first stepped surfaces constitutes a first stepped cavity **133**.

[0069] The pattern of the first stepped cavities **133** can be repeated along the second horizontal direction hd**2** with a periodicity to provide a periodic pattern, as shown in FIG. **1**D. The unit pattern that is repeated along the second horizontal direction hd**2** is herein referred to as a repetition unit RU, as shown in FIGS. **1**B and **1**D. The width of a repetition unit RU may be in a range from 2 microns to 20 microns, although lesser and greater widths may also be employed. In one embodiment, each first stepped cavity may have a respective width along the second horizontal direction hd**2** that is in a range from 25% to 75% of the width of a repetition unit RU along the second horizontal direction hd**2**.

[0070] In summary, first stepped surfaces can be formed in a first staircase region **301** by patterning the first-tier alternating stack (**132**, **142**) such that first vertical surface segments of the first stepped surfaces are laterally spaced apart along a first horizontal direction hd**1**, and are interconnected to each other by first horizontally-extending surface segments of the first stepped surfaces. The first staircase region **301** has a first area having a first width along a second horizontal direction hd**2** that is perpendicular to the first horizontal direction hd**1** in a plan view. The first width may be in a range from 25% to 75% of the pitch of the first stepped cavities along the second horizontal direction hd**2**.

[0071] Referring to FIG. **2**, a first insulating liner **152** and a first sacrificial liner **154** can be sequentially deposited over the first stepped surfaces. The first insulating liner **152** may be formed by a first conformal deposition process, and may comprise an insulating material such as undoped silicate glass (i.e., silicon oxide) or a doped silicate glass. The thickness of the first insulating liner **152** may be in a range

from 10 nm to 50 nm, such as from 15 nm to 30 nm, although lesser and greater thicknesses may also be employed. The first sacrificial liner **154** may be formed by a second conformal deposition process, and may comprise a sacrificial material that can be subsequently removed selective to the material of the first insulating liner **152**. In one embodiment, the first sacrificial liner **154** may comprise silicon nitride. The thickness of the first sacrificial liner **154** is greater than the thickness of the first sacrificial material layers **142**, and may be in a range from 40 nm to 150 nm, such as from 60 nm to 100 nm, although lesser and greater thicknesses may also be employed.

[0072] Referring to FIGS. **3**A-**3**D, a dielectric fill material such as silicon oxide can be deposited in each first stepped cavity **133**. Excess portions of the deposited dielectric fill material can be removed from above the horizontal plane including the top surface of the first sacrificial liner **154**, for example, by chemical mechanical polishing (CMP). A recess etch process can be performed to vertically recess a remaining portion of the dielectric fill material by a vertical recess distance that is the same as the thickness of the first sacrificial liner **154**. Subsequently, an isotropic etch process can be performed to remove a horizontally-extending portion of the first sacrificial liner **154** selective to the material of the first insulating liner **152**. Each remaining portion of the dielectric fill material that fills a respective first stepped cavity **133** constitutes a first-tier retro-stepped dielectric material portion **165**. Each first-tier retro-stepped dielectric material portion **165** can be retro-stepped.

[0073] As used herein, a "retro-stepped" element refers to an element that has first stepped surfaces and a horizontal cross-sectional area that increases monotonically as a function of a vertical distance from a top surface of a substrate on which the element is present. If silicon oxide is employed for the first-tier retro-stepped dielectric material portion **165**, the silicon oxide of the first-tier retro-stepped dielectric material portion **165** may, or may not, be doped with dopants such as B, P, and/or F. In one embodiment, each first-tier retro-stepped dielectric material portion **165** overlies and contacts the first stepped surfaces, and has a top surface that is coplanar with the top surface of the horizontally-extending portion of the first insulating liner **152** that overlies the first-tier alternating stack (**132**, **142**) in the memory array region **100**. The first-tier retro-stepped dielectric material portions **165** may be arranged along the second horizontal direction hd**2** with the periodicity of the repetition unit RU.

[0074] Referring to FIG. **4**, a dielectric material layer can be formed over the first insulating liner **152** and the first-tier retro-stepped dielectric material portion **165**. The dielectric material layer is herein referred to as an inter-tier dielectric layer **180**. The inter-tier dielectric layer **180** comprises a dielectric material such as silicon oxide, and may have a thickness in a range from 50 nm to 200 nm, such as 80 nm to 160 nm, although lesser and greater thicknesses may also be employed.

[0075] A first photoresist layer (not shown) can be applied over the inter-tier dielectric layer **180**, and can be lithographically patterned to form an array of openings in the memory array region **100**. An anisotropic etch process can be performed to transfer the pattern of the openings in the first photoresist layer through the inter-tier dielectric layer **180**, the first insulating liner **152**, and the first-tier alternating stack (**132**, **142**) and optionally into an upper portion of the semiconductor material layer **9**. First-tier memory openings **149** can be formed through the inter-tier dielectric layer **180**, the first insulating liner **152**, and the first-tier alternating stack (**132**, **142**). The depth of overetch of the first-tier memory openings **149** into the semiconductor material layer **9** may be in a range from 0 nm to 50 nm, such as from 5 nm to 30 nm, although greater overetch depths may also be employed. The first photoresist layer can be subsequently removed, for example, by ashing. The pattern of the first-tier memory openings **149** may be repeated with the periodicity of the repetition unit RU along the second horizontal direction hd**2**.

[0076] Referring to FIGS. **5**A-**5**D, a second photoresist layer (not shown) can be applied over the inter-tier dielectric layer **180**, and can be lithographically patterned to form openings in the contact region **300**. An anisotropic etch process can be performed to transfer the pattern of the openings in the second photoresist layer through the inter-tier dielectric layer **180**, the first sacrificial liner **154**, the first insulating liner **152**, the first-tier retro-stepped dielectric material portion **165**, and portions of the first-tier alternating stack (**132**, **142**) that underlie the first-tier retro-stepped dielectric material portion **165**, and optionally into an upper portion of the dielectric isolation layer **6** (if present) or the semiconductor material layer **9** (if the dielectric isolation layer **6** is omitted).

[0077] First-tier contact openings **139** can be formed in areas in which layer contact via structures are to be subsequently formed. The layer contact via structures are contact via structures that will contact subsequently formed electrically conductive layers. First-tier support openings **119** can be formed in areas that laterally surround the first-tier contact openings **139**. Support pillar structures are subsequently formed in the volumes of the first-tier support openings **119**, and are employed as structural support structures during replacement of the first sacrificial material layers **142** with first electrically conductive layers. The second photoresist layer can be subsequently removed, for example, by ashing.

[0078] The first-tier memory openings **149** may be arranged in rows that extend along a first horizontal direction (e.g., word line direction) hd**1**. Rows of the first-tier memory openings **149** may be laterally spaced apart from each other along a second horizontal direction hd**2** (which may be a bit line direction), which may be perpendicular to the first horizontal direction hd**1**. The first-tier contact openings **139** may be arranged in rows that laterally extend along the first horizontal direction hd**1**. The pattern of the first-tier contact openings **139** and the first-tier support openings **119** may be repeated with the periodicity of the repetition unit RU along the second horizontal direction hd**2**.

[0079] Referring to FIG. **6**, an optional etch stop liner (not shown) and a first sacrificial fill material can be deposited in the first-tier memory openings **149**, the first-tier support openings **119**, and the first-tier contact openings **139**. The optional etch stop liner (if present) comprises a thin silicon oxide layer having a thickness in a range from 1 nm to 6 nm. The first sacrificial fill material may comprise a carbon-based material (such as amorphous carbon or diamond-like carbon), a semiconductor material (such as amorphous silicon or polysilicon), a dielectric fill material (such as borosilicate glass or organosilicate glass), or a polymer material.

[0080] A recess etch process can be performed to remove portions of the first sacrificial fill material from above the horizontal plane including the top surface of the inter-tier

dielectric layer **180**. In one embodiment, each remaining portion of the first sacrificial fill material has a top surface within a horizontal plane including a top surface of the inter-tier dielectric layer **180**. Remaining portions of the first sacrificial fill material that fill the first-tier memory openings **149** constitute first-tier sacrificial memory opening fill structures **148**. Remaining portions of the first sacrificial fill material that fill the first-tier support openings **119** constitute first-tier sacrificial support opening fill structures **118**. Remaining portions of the first sacrificial fill material that fill the first-tier contact openings **139** constitute first-tier sacrificial contact opening fill structures **138**.

[0081] Referring to FIG. **7**, a second-tier alternating stack of second insulating layers **232** and second sacrificial material layers **242** can be formed over the first-tier alternating stack (**132**, **142**). The second insulating layers **232** comprise an insulating material, such as undoped silicate glass (i.e., silicon oxide) or a doped silicate glass, and the second sacrificial material layers **242** comprise a sacrificial material, such as silicon nitride. The second-tier alternating stack (**232**, **242**) may comprise multiple repetitions of a unit layer stack including a second insulating layer **232** and a second sacrificial material layer **242**. The total number of repetitions of the unit layer stack within the second-tier alternating stack (**232**, **242**) may be, for example, in a range from 8 to 1,024, such as from 32 to 256, although lesser and greater number of repetitions may also be employed. Each of the second insulating layers **232** may have a thickness in a range from 20 nm to 100 nm, such as from 30 nm to 60 nm, although lesser and greater thicknesses may also be employed. Each of the second sacrificial material layers **242** may have a thickness in a range from 20 nm to 100 nm, such as from 30 nm to 60 nm, although lesser and greater thicknesses may also be employed. While two alternating stacks are provided in this embodiment, in other embodiment only one alternating stack or more than two alternating stacks (e.g., three alternating stacks) may be used.

[0082] Second stepped surfaces are formed in the second staircase region **302**. Each set of second stepped surfaces may comprise second horizontally-extending surface segments and second vertically-extending surface segments. The second vertically-extending surface segments are laterally spaced from each other along the first horizontal direction hd**1**. The second vertically-extending surface segments can be parallel to a second horizontal direction hd**2**. Each contiguous set of second stepped surfaces can be formed within a respective second staircase region **302**. Contiguous sets of second stepped surfaces can be formed in second stepped cavities **233** that are laterally spaced apart from each other along the second horizontal direction hd**2**. Each void within the second-tier alternating stack (**232**, **242**) that overlies a respective contiguous set of second stepped surfaces constitutes a second stepped cavity **233**. The pattern of the second stepped cavities **233** can be repeated along the second horizontal direction hd**2** with the periodicity of the repetition units RU along the second horizontal direction hd**2**. Thus, the second staircase regions **302** can be repeated along the second horizontal direction hd**2** with the periodicity of the repetition units RU along the second horizontal direction hd**2**.

[0083] In one embodiment, the second staircase regions **302** may be laterally offset relative to the first staircase regions **301** along the second horizontal direction hd**2** in a plan view, such as a top-down view. Thus, the pattern of the first staircase regions **301** and the pattern of the second staircase regions **302** may alternate along the second horizonal direction hd**2** with the same periodicity as the periodicity of the repetition units RU along the second horizontal direction hd**2**. Peripheral portions of a first staircase region **301** may have an areal overlap with a pair of second staircase regions **302** in a plan view, and peripheral portions of a second staircase region **302** may have an areal overlap with a pair of first staircase regions **301** in the plan view. If an area of a first staircase region **301** has an overlap with an area of a second staircase region **302** in a plan view, the width of such an overlap area may be in a range from 0.01% to 25% of the width of a repetition unit RU along the second horizontal direction hd**2**. Generally, a neighboring pair of a first staircase region **301** and a second staircase region **302** is laterally offset relative to each other along the second horizontal direction hd**2** that is perpendicular to the lateral separation direction between two memory array regions **100** (i.e., the first horizontal direction hd**1**.)

[0084] Thus, a second stepped cavity **233** is formed within each volume from which portions of the second-tier alternating stack (**232**, **242**) are removed through formation of the second stepped surfaces. Each second stepped cavity **233** can have a respective set of second stepped surfaces such that the horizontal cross-sectional shape of the second stepped cavity changes in steps as a function of the vertical distance from the top surface of the substrate **8**. In one embodiment, the second stepped cavity **233** can be formed by repetitively performing a set of processing steps. The set of processing steps can include, for example, an etch process of a second type that vertically increases the depth of a cavity by one or more levels, and an etch process of a second type that laterally expands the area to be vertically etched in a subsequent etch process of the second type.

[0085] Each second sacrificial material layer **242** other than a topmost second sacrificial material layer **242** within the second-tier alternating stack (**232**, **242**) laterally extends farther than any overlying second sacrificial material layer **242** within the second-tier alternating stack (**232**, **242**) in each second staircase region **302**. The second stepped surfaces of the second-tier alternating stack (**232**, **242**) continuously extend from the bottommost layer within the second-tier alternating stack (**232**, **242**) to the topmost layer within the second-tier alternating stack (**232**, **242**). The second stepped surfaces may continuously extend from a bottommost layer within the second-tier alternating stack (**232**, **242**) at least to a topmost layer within the second-tier alternating stack (**232**, **242**).

[0086] In summary, second stepped surfaces can be formed in a second staircase region **302** by patterning the second-tier alternating stack (**232**, **242**) such that second vertical surface segments of the second stepped surfaces are laterally spaced apart along the first horizontal direction hd**1** and are interconnected to each other by second horizontally-extending surface segments of the second stepped surfaces. The second staircase region **302** has a second area having a second width along the second horizontal direction hd**2** in the plan view, and the second area is laterally shifted relative to the first area (i.e., the area of a neighboring first staircase region **301**) along the second horizontal direction hd**2** by a lateral offset distance that is greater than one half of the first width (i.e., the width of the first staircase region **301**) and is less than the first width so that a partial overlap between the second area and the first area is present in the plan view.

[0087] Referring to FIG. **8**, a second insulating liner **252** and a second sacrificial liner **254** can be sequentially deposited over the second stepped surfaces. The second insulating liner **252** may be formed by a conformal deposition process, and may comprise an insulating material such as undoped silicate glass or a doped silicate glass. The thickness of the second insulating liner **252** may be the same as that of the first insulating liner **152**. The second sacrificial liner **254** may be formed by a conformal deposition process, and may comprise a sacrificial material that can be subsequently removed selective to the material of the second insulating liner **252**. In one embodiment, the second sacrificial liner **254** may comprise silicon nitride. The thickness of the second sacrificial liner **254** is greater than the thickness of the second sacrificial material layers **242**, and may be the same as that of the first sacrificial liner **154**.

[0088] A photoresist layer (not shown) can be applied over the second sacrificial liner **254**, and can be lithographically patterned such that the photoresist layer covers the memory array region **100** and the second staircase region **302**, and does not cover the first staircase region **301**. A first etch process can be performed to remove unmasked portions of the second sacrificial liner **254** in the first staircase region **301**. A second etch process can be performed to remove unmasked portions of the second insulating liner **252** in the first staircase region **301**. The photoresist layer can be subsequently removed, for example, by ashing.

[0089] Referring to FIGS. **9**A-**9**D, a dielectric fill material, such as silicon oxide, can be deposited in the second stepped cavity. Excess portions of the deposited dielectric fill material can be removed from above the horizontal plane including the top surface of the second sacrificial liner **254**, for example, by chemical mechanical planarization (CMP). A recess etch process can be performed to vertically recess a remaining portion of the dielectric fill material by a vertical recess distance that is the same as the thickness of the second sacrificial liner **254**. Subsequently, an isotropic etch process can be performed to remove a horizontally-extending portion of the second sacrificial liner **254** selective to the material of the second insulating liner **252**. A remaining portion of the dielectric fill material that fills the second stepped cavity constitutes a second retro-stepped dielectric material portion **265**.

[0090] If silicon oxide is employed for the second retro-stepped dielectric material portion **265**, the silicon oxide of the second retro-stepped dielectric material portion **265** may, or may not, be doped with dopants such as B, P, and/or F. In one embodiment, the second retro-stepped dielectric material portion **265** overlies and contacts the second stepped surfaces, and has a top surface that is coplanar with the top surface of the horizontally-extending portion of the second insulating liner **252** that overlies the second-tier alternating stack (**232**, **242**) in the memory array region **100**.

[0091] In one embodiment, each first-tier retro-stepped dielectric material portion **165** may have a respective first area in a plan view, and each second-tier retro-stepped dielectric material portion **265** may have a respective second area in the plan view. For each neighboring pair of a first-tier retro-stepped dielectric material portion **165** and a second-tier retro-stepped dielectric material portion **265**, the second area of the second-tier retro-stepped dielectric material portion **265** may be laterally shifted relative to the first area of the first-tier retro-stepped dielectric material portion **165** along the second horizontal direction hd**2** by a lateral offset distance that is greater than one half of the width of the first-tier retro-stepped dielectric material portion **165**, and is less than the width of the first-tier retro-stepped dielectric material portion **165**, so that a partial overlap is present in the plan view between the neighboring pair of the first-tier retro-stepped dielectric material portion **165** and the second-tier retro-stepped dielectric material portion **265**.

[0092] Referring to FIGS. **10**A-**10**D, an insulating cap layer **270** can be formed over the second insulating liner **252** and the second retro-stepped dielectric material portion **265**. The insulating cap layer **270** comprises a dielectric material, such as silicon oxide, and may have a thickness in a range from 50 nm to 200 nm, such as 80 nm to 260 nm, although lesser and greater thicknesses may also be employed.

[0093] A photoresist layer (not shown) can be applied over the insulating cap layer **270**, and can be lithographically patterned to form openings over areas of the first-tier sacrificial contact opening fill structures **138** and the first-tier sacrificial support opening fill structures **118**. An anisotropic etch process can be performed to transfer the pattern of the openings in the photoresist layer through the insulating cap layer **270**, the second retro-stepped dielectric material portion **265**, the second sacrificial liner **254**, the second insulating liner **252**, and portions of the second-tier alternating stack (**232**, **242**) that underlie the second retro-stepped dielectric material portion **265**. Subsequently, the sacrificial fill material of the first-tier sacrificial contact opening fill structures **138** and the first-tier sacrificial support opening fill structures **118** can be removed selective to the materials of the insulating cap layer, the first-tier alternating stack (**132**, **142**), the second-tier alternating stack (**232**, **242**), the inter-tier dielectric layer **180** and the dielectric isolation layer **6**. For example, a selective etch process or an ashing process (for carbon sacrificial material) may be performed to remove the sacrificial fill material of the first-tier sacrificial contact opening fill structures **138** and the first-tier sacrificial support opening fill structures **118**.

[0094] Multi-tier contact openings **39**, which are also referred to as contact openings **39**, can be formed in volumes from which the first-tier sacrificial contact opening fill structures **138** are removed and in volumes that overlie the volumes of the first-tier sacrificial contact opening fill structures **138** and vertically extend through the second-tier alternating stack (**232**, **242**) and/or the second retro-stepped dielectric material portion **265** and through the insulating cap layer **270**. Multi-tier support openings **19**, which are also referred to as support openings **19**, can be formed in volumes from which the first-tier sacrificial support opening fill structures **118** are removed and in volumes that overlie the volumes of the first-tier sacrificial support opening fill structures and vertically extend through the second-tier alternating stack (**232**, **242**) and/or the second retro-stepped dielectric material portion **265** and through the insulating cap layer **270**. The photoresist layer can be subsequently removed, for example, by ashing.

[0095] Referring to FIG. **11**, an optional etch stop liner (not shown) and a second sacrificial fill material can be deposited in the multi-tier support openings **19** and the multi-tier contact openings **39**. The optional etch stop liner (if present) comprises a thin silicon oxide layer having a thickness in a range from 2 nm to 6 nm. The second sacrificial fill material may comprise a carbon-based material (such as amorphous carbon or diamond-like carbon), a semiconductor material (such as amorphous silicon or poly-

silicon), a dielectric fill material (such as borosilicate glass or organosilicate glass), or a polymer material.

[0096] A recess etch process can be performed to remove portions of the second sacrificial fill material from above the horizontal plane including the top surface of the insulating cap layer **270**. In one embodiment, each remaining portion of the second sacrificial fill material has a top surface within a horizontal plane including a top surface of the insulating cap layer **270**. Remaining portions of the second sacrificial fill material that fill the multi-tier support openings **19** constitute sacrificial support opening fill structures **18**. Remaining portions of the second sacrificial fill material that fill the multi-tier contact openings **39** constitute sacrificial contact opening fill structures **38**.

[0097] Referring to FIG. **12**, a photoresist layer (not shown) can be applied over the insulating cap layer **270**, and can be lithographically patterned to form openings in areas that overlie the sacrificial support opening fill structures **18**. The sacrificial support opening fill structures **18** can be removed selective to the materials of the insulating cap layer **270**, the alternating stacks {(**132**, **142**), (**232**, **242**)}, the inter-tier dielectric layer **180**, and the dielectric isolation layer **6**. An anisotropic etch process, an isotropic etch process, or an ashing process may be employed. The photoresist layer can be subsequently removed, for example, by ashing. The cavities formed by removal of the sacrificial support opening fill structures **18** comprise the multi-tier support openings **19**, which are referred to as support openings going forward.

[0098] Referring to FIG. **13**, a dielectric fill material, such as undoped silicate glass (i.e., silicon oxide) or a doped silicate glass can be deposited in the multi-tier support openings **19**. Excess portions of the dielectric fill material can be removed from above the horizontal plane including the top surface of the insulating cap layer **270**, for example, by performing a recess etch process. Each remaining portion of the dielectric fill material that fills a respective multi-tier support opening **19** comprises a support pillar structure **20**. An array of support pillar structures **20** can be formed in the contact region **300**.

[0099] Referring to FIG. **14**, a photoresist layer (not shown) may be applied over the insulating cap layer **270**, and can be lithographically patterned to form openings in areas of the first-tier sacrificial memory opening fill structures **148**. An anisotropic etch process can be formed to form openings through the insulating cap layer **270**, and the second-tier alternating stack (**232**, **242**) underneath the openings in the photoresist layer and over the first-tier sacrificial memory opening fill structures **148**. The first-tier sacrificial memory opening fill structures **148** can be subsequently removed selective to the materials of the insulating cap layer **270**, the alternating stacks {(**132**, **142**), (**232**, **242**)}, and the inter-tier dielectric layer **180**. Multi-tier memory openings **49**, which are also referred to as memory openings **49**, are formed in the volumes from which the first-tier sacrificial memory opening fill structures **148** are removed and in the volumes of the cavities that overlie the volumes from which the first-tier sacrificial memory opening fill structures **148** are removed. The photoresist layer can be subsequently removed, for example, by ashing.

[0100] Referring to FIG. **15**, a sequence of processing steps can be performed to form a memory opening fill structure **58** within each inter-tier memory opening **49** and to form a support pillar structure **20** within each inter-tier support opening **19** at the same time. For example, a memory film **50** can be formed within each of the memory openings **49** and the support openings **19**. The memory films **50** may include any memory material that can store information by charge trapping, a change in electrical resistivity, a change in the direction of ferroelectric polarization (e.g., in a ferroelectric material), or any other material that can store information therein. For example, each memory film **50** may comprise a layer stack including a blocking dielectric layer **52**, a charge storage material layer **54**, and a tunneling dielectric layer **56**. In one embodiment, the memory films **50** can be formed by depositing material layers and/or material portions and by removing excess portions of the material layers and/or the material portions from outside and the bottoms of the memory openings **49** and the support openings **19**, for example, by performing an anisotropic etch process (e.g., a sidewall spacer etch process). In one embodiment, the blocking dielectric layer **52** may comprise a silicon oxide or an aluminum oxide layer. The charge storage material layer **54** may comprise a silicon nitride layer. The tunneling dielectric layer **56** may comprise a silicon oxide layer or an "ONO" stack of silicon oxide/silicon nitride/silicon oxide layers.

[0101] A vertical semiconductor channel **60** can be formed in each of the memory openings **49** and the support openings **19** by conformal deposition of a semiconductor channel material (e.g., amorphous silicon or polysilicon) having a doping of a first conductivity type. The semiconductor channel material may have a doping of a same conductivity type as the horizontal semiconductor channels (not expressly shown) located in the substrate **8**. A dielectric fill material can be deposited in the remaining volumes of the memory openings **49** and the support openings **19**, and can be vertically recessed to form a dielectric core **62**. A semiconductor material (e.g., amorphous silicon or polysilicon) having a doping of a second conductivity type can be deposited over each dielectric core **62** at a top end of each vertical semiconductor channel **60** to form a drain region **63** within each of the memory openings **49** and the support openings **19**. The second conductivity type is opposite of the first conductivity type. Each contiguous combination of a memory film **50** and a vertical semiconductor channel **60** constitutes a memory stack structure **55**. Each memory stack structure **55** comprises a respective vertical stack of memory elements. For example, each vertical stack of memory elements may comprise portions of the charge storage material layer **54** located at the levels of the sacrificial material layers (**142**, **242**) which are subsequently replaced with electrically conductive layers.

[0102] In summary, the memory opening fill structures **58** are formed in the memory openings **49**, and support pillar structures **20** are formed in the support openings **19**. Each of the memory opening fill structures **58** comprises a respective vertical semiconductor channel **60**, a respective vertical stack of memory elements (e.g., portions of a memory film **50**), a drain region **63** and an optional dielectric core **62**. In one embodiment, the dielectric support pillar structures **20** are formed separately (e.g., before or after) from the memory opening fill structures **58**. In an alternative embodiment, the support pillar structures **20** may be formed simultaneously with formation of the memory opening fill structures **58**, and may have the same set of material portions as the memory opening fill structures **58**. In this case, each of the support pillar structures **20** comprises a dummy vertical

semiconductor channel (which is not electrically connected to a bit line), a dummy memory film, a dummy drain region, and an optional dielectric core which comprise the same materials as those of the memory opening fill structures **58**. Drain-select-level dielectric isolation structures **72** can be formed through an uppermost set of second sacrificial material layers **242**. The memory stack structures **55** vertically extend through each layer within the first-tier alternating stack (**132**, **142**) and with the second-tier alternating stack (**232**, **242**) in a memory array region **100**.

[0103] Referring to FIGS. **16**A-**16**C, a contact-level dielectric layer **280** may be optionally formed over the insulating cap layer **270**. A photoresist layer may be applied above the contact-level dielectric layer **280**, and can be lithographically patterned to form openings in areas that overlie the sacrificial contact opening fill structures **38**. An anisotropic etch process can be performed to transfer the pattern of the openings in the photoresist layer through the contact-level dielectric layer **280**. Cavities can be formed through the contact-level dielectric layer **280** over each of the sacrificial contact opening fill structures **38**. The sacrificial contact opening fill structures **38** can be subsequently removed selective to the materials of the contact-level dielectric layer **280**, the insulating cap layer **270**, the alternating stacks {(**132**, **142**), (**232**, **242**)}, the inter-tier dielectric layer **180**, and the optional dielectric isolation layer **6** (if present). Contact via cavities **81** are formed in the volumes from which the sacrificial contact opening fill structures **38** are removed and in the volumes of the cavities that overlie the volumes from which the sacrificial contact opening fill structures **38** are removed. The photoresist layer can be subsequently removed, for example, by ashing.

[0104] The contact via cavities **81** comprise first contact via cavities **81**A that are formed in the first staircase region **301** and extending through each layer in the second-tier alternating stack (**232**, **242**), a first-tier retro-stepped dielectric material portion **165**, and a subset of layers in the first-tier alternating stack (**132**, **142**); and second contact via cavities **81**B that are formed in the second staircase region **302** and extending through a second retro-stepped dielectric material portion **265**, a subset of layers in the second-tier alternating stack (**232**, **242**), and each layer in the first-tier alternating stack (**132**, **142**).

[0105] The first contact via cavities **81**A vertically extend through each layer within the second-tier alternating stack (**232**, **242**) and through a respective first-tier retro-stepped dielectric material portion **165**. The second contact via cavities **81**B vertically extend through each layer within the first-tier alternating stack (**132**, **142**) and through a respective second-tier retro-stepped dielectric material portion **265**. The second contact via cavities **81**B are laterally spaced from the first-tier retro-stepped dielectric material portions **165**. The first contact via cavities **81**A are laterally spaced from the second-tier retro-stepped dielectric material portions **265**. In one embodiment, each of the contact via cavities **81** vertically extends through an horizontal plane including a bottom surface of a bottommost layer within the first-tier alternating stack (**132**, **142**).

[0106] Referring to FIG. **17**, a first isotropic etch process can be performed to isotropically recess the material of the sacrificial material layers (**142**, **242**), the first sacrificial liner **154**, and the second sacrificial liner **254** selective to the materials of the contact-level dielectric layer **280**, the insulating cap layer **270**, the insulating layers (**132**, **232**), the inter-tier dielectric layer **180**, and the dielectric isolation layer **6** (if present). For example, if the sacrificial material layers (**142**, **242**), the first sacrificial liner **154**, and the second sacrificial liner **254** comprise silicon nitride, a wet etch process employing hot phosphoric acid can be performed to laterally recess the sacrificial material layers (**142**, **242**).

[0107] Generally, sidewalls of the sacrificial material layers (**142**, **242**), the first sacrificial liner **154**, and the second sacrificial liner **254** may be laterally recessed relative to sidewalls of the insulating layers (**132**, **232**) and the retro-stepped dielectric material portions (**165**, **265**) around the contact via cavities **81**. Lateral recesses **41** are formed in volumes from which the materials of the sacrificial material layers (**142**, **242**) are removed. The lateral recesses **41** may have a width of 50 nm to 250 nm, such as 100 nm to 150 nm, and may be set to obtain a desired electric field between word lines and layer contact via structures to be formed in subsequent steps, as will be described below. A first annular cavity **155** can be formed in each volume from which an annular portion of the first sacrificial liner **154** is removed around a respective one of the first contact via cavities **81**A. A second annular cavity **255** can be formed in each volume from which an annular portion of the second sacrificial liner **254** is removed around a respective one of the second contact via cavities **81**B.

[0108] Generally, the first isotropic etch process etches proximal portions of the first sacrificial liner **154**, at least one first sacrificial material layers **142**, and the second sacrificial material layers **242** from around each first contact via cavity **81**A to form a respective finned cavity, which is herein referred to as a first-type first-stage in-process finned contact via cavity **82**A. Further, the first isotropic etch process etches proximal portions of the second sacrificial liner **254**, the first sacrificial material layers **142**, and at least one second sacrificial material layers **242** from around each second contact via cavity **81**B to form a respective finned cavity, which is herein referred to as a second-type first-stage in-process finned contact via cavity **82**B. The first-type first-stage in-process finned contact via cavities **82**A and the second-type first-stage in-process finned contact via cavities **82**A comprise first-stage in-process finned contact via cavities **82**.

[0109] Each first-type first-stage in-process finned contact via cavity **82**A comprises a cylindrical cavity including the volume of a respective first contact via cavity **82**A, a first annular cavity **155**, and at least one lateral recess **41** formed by removal of an annular portion of a respective first sacrificial material layer **142**. Each second-type first-stage in-process finned contact via cavity **82**B comprises a cylindrical cavity including the volume of a respective second contact via cavity **82**B, a second annular cavity **255**, and lateral recesses **41** formed by removal of annular portions of first sacrificial material layers **142** and at least one second sacrificial material layer **242**.

[0110] Physically exposed, recessed surfaces of the sacrificial material layers (**142**, **242**), the first sacrificial liner **154**, and the second sacrificial liner **254** after the first isotropic etch process comprises sidewall segments that are laterally offset by a uniform lateral offset distance from sidewalls of the insulating layers (**132**, **232**) and the retro-stepped dielectric material portions (**165**, **265**) around the cylindrical cavity of a respective first-stage in-process finned contact

via cavity **82**. The uniform lateral offset distance can be the same as the etch distance of the first isotropic etch process.

[0111] Referring to FIG. **18**, a conformal dielectric material layer **40**L can be deposited in the first-stage in-process finned contact via cavities **82** by a conformal deposition process such as a low-pressure chemical vapor deposition process or an atomic layer deposition process. The conformal dielectric material layer **40**L can be conformally deposited to completely fill volumes of the lateral recesses **41** without completely filling the volumes of the first annular cavities **155** or the second annular cavities **255**. The conformal dielectric material layer **40**L comprises a material that is different from the materials of the sacrificial material layers (**142**, **242**). For example, the conformal dielectric material layer **40**L comprises silicon oxide.

[0112] As discussed above the first sacrificial liner **154** and the second sacrificial liner **254** have thicknesses that are greater than the thicknesses of the sacrificial material layers (**142**, **242**). Thus, the first annular cavities **155** or the second annular cavities **255** have greater heights than the heights of the lateral recesses **41**. The thickness of the conformal dielectric material layer **40**L can be greater than one half of the height of the lateral recesses **41**, and can be less than one half of the height of the first annular cavities **155** or the second annular cavities **255**. Thus, the volumes of the first annular cavities **155** or the second annular cavities **255** can be partially filled with the conformal dielectric material layer **40**L, while unfilled volumes are still present within each of the first annular cavities **155** or the second annular cavities **255**.

[0113] Referring to FIG. **19**, an isotropic recess etch process can be performed to isotropically recess the conformal dielectric material layer **40**L. For example, if the conformal dielectric material layer **40**L comprises silicon oxide, a wet etch process employing dilute hydrofluoric acid can be performed to isotropically recess the conformal dielectric material layer **40**L around cavities through the alternating stacks {(**132**, **142**), (**232**, **242**)}. The duration of the isotropic etch process can be selected such that the isotropic recess etch process completely removes the material of the conformal dielectric material layer **40**L from inside each of the first annular cavities **155** and the second annular cavities **255**. Remaining portions of the conformal dielectric material layer **40**L that fill the lateral recesses **41** (i.e., the volumes from which portions of the sacrificial material layers (**142**, **242**) are removed) constitute annular insulating plates **40** (e.g., insulating fins).

[0114] The remaining volumes of the first-stage in-process finned contact via cavities **82** are herein referred to as second-stage in-process finned contact via cavities **83**. The second stage in-process finned contact via cavities **83** may comprise first-type second-stage in-process finned contact via cavities **83**A that extend through each layer within the second alternating stack (**232**, **242**), a first-tier retro-stepped dielectric material portion **165**, and a respective subset of layers within the first-tier alternating stack (**132**, **142**), and second-type second-stage in-process finned contact via cavities **83**B that extend through a second retro-stepped dielectric material portion **265**, a respective subset of layers within the second-tier alternating stack (**232**, **242**), and each layer within the first-tier alternating stack (**132**, **142**). Each second-stage in-process finned contact via cavity **83** comprises a cylindrical cavity portion **83**C having a cylindrical shape and vertically extending form the top surface of the contact-level dielectric layer **280** to the dielectric isolation layer **6** (if present, or alternatively to the substrate **8**), and annular cavity portions **83**F that is adjoined to and laterally surrounds the cylindrical cavity portion **83**C. Each annular cavity portion **83**F can be bounded by an annular bottom surface of a retro-stepped dielectric material portion (**165**, **265**), a cylindrical sidewall of a sacrificial liner (**154**, **254**), and an annular top surface segment of an insulating liner (**152**, **252**).

[0115] At least one annular insulating plate **40** can be present around each second stage in-process finned contact via cavity **83**. The annular insulating plates **40** may comprise first-tier annular insulating plates **401** that are formed within the first-tier alternating stack (**132**, **142**), and second-tier annular insulating plates **402** that are formed within the second-tier alternating stack (**232**, **242**). Each second-stage in-process finned contact via cavities **83** can be laterally surrounded by a respective set of annular insulating plates **40**.

[0116] A first-type second-stage in-process finned contact via cavity **83**A may comprise a first cylindrical surface vertically extending through the first-tier retro-stepped dielectric material portion **165** and each layer within the second-tier alternating stack (**232**, **242**) and having a bottom periphery that is adjoined to an inner periphery of the annular top surface of an annular cavity portion **83**F, and a second cylindrical surface vertically extending through a subset of layers within the first-tier alternating stack (**132**, **142**) and having a top periphery that is adjoined to an annular bottom surface the annular cavity portion **83**F. A second-type second-stage in-process finned contact via cavity **83**B may comprise a first cylindrical surface vertically extending through the second retro-stepped dielectric material portion **265** and having a bottom periphery that is adjoined to an inner periphery of the annular top surface of an annular cavity portion **83**F, and a second cylindrical surface vertically extending through a subset of layers within the second-tier alternating stack (**232**, **242**) and each layer within the first-tier alternating stack (**132**, **142**) and having a top periphery that is adjoined to an annular bottom surface the annular cavity portion **83**F. Generally, each second-stage in-process finned contact via cavity **83** comprises an entirety of a volume of a respective contact via cavity **81** and a volume formed by removal of a portion of a sacrificial liner (**154**, **254**) during the first isotropic etch process.

[0117] Referring to FIG. **20**, a second isotropic etch process can be performed to isotropically recess the materials of the sacrificial liners (**154**, **254**) selective to the materials of the contact-level dielectric layer **280**, the insulating cap layer **270**, the insulating layers (**132**, **232**), the inter-tier dielectric layer **180**, the dielectric isolation layer **6** (if present), and the annular insulating plates **40**. For example, if the sacrificial liners (**154**, **254**) comprise silicon nitride, a wet etch process employing hot phosphoric acid can be performed to isotropically recess the sacrificial liners (**154**, **254**). The volume of each annular cavity portion **83**F can be laterally expanded by the second isotropic etch process. The second-stage in-process finned contact via cavities **83**, as expanded by the second isotropic etch process, are herein referred to as third-stage in-process finned contact via cavities **85**.

[0118] Generally, the third-stage in-process finned contact via cavities **85** can be formed by laterally recessing sidewalls of the sacrificial liners (**154**, **254**) around the second-

stage in-process finned contact via cavities **83** by performing the second isotropic etch process. The lateral recess distance of the second isotropic etch process may be in a range from 20 nm to 300 nm, such as from 40 nm to 150 nm, although lesser and greater lateral etch distances may also be employed. The third-stage in-process finned contact via cavities **85** comprise first-type third-stage in-process finned contact via cavities **85**A that are formed in the first staircase region **301**, and second-type third-stage in-process finned contact via cavities **85**B that are formed in the second staircase region **302**. Each of the third-stage in-process finned contact via cavities **85** comprises a cylindrical cavity portion **85**C and an annular cavity portion **85**F. In one embodiment, each annular cavity portion **85**F may have a stepped top surface that includes a first annular top surface segment which is an annular bottom surface segment of a retro-stepped dielectric material portion (**165**, **265**), a cylindrical surface segment that is adjoined to an outer periphery of the first annular top surface segment, and a second annular top surface segment which is another annular bottom surface segment of the retro-stepped dielectric material portion (**165**, **265**).

[0119] Referring to FIG. **21**, a sacrificial fill material can be deposited in the third-stage in-process finned contact via cavities **85**. The sacrificial fill material may comprise a semiconductor material (such as amorphous silicon or polysilicon), a carbon-based material (such as amorphous carbon or diamond-like carbon), a dielectric fill material (such as borosilicate glass or organosilicate glass), or a polymer material. Optionally, a thin etch stop liner (not illustrated) may be deposited prior to filling of the third-stage in-process finned contact via cavities **85** with the sacrificial fill material. The thin etch stop liner may comprise silicon oxide or a dielectric metal oxide, and may have a thickness in a range from 2 nm to 6 nm, although lesser and greater thicknesses may also be employed.

[0120] Portions of the sacrificial fill material overlying the horizontal plane including the top surface of the contact-level dielectric layer **280** can be removed by a planarization process, which may comprise a recess etch process or a chemical mechanical polishing process. Each remaining portion of the sacrificial fill material that fills a respective one of the third-stage in-process finned contact via cavities **85** constitutes a sacrificial finned cavity fill material structure **84**. Each sacrificial finned cavity fill material structure **84** comprises a respective cylindrical fill material portion **84**C and at least one fin-shaped fill material portion **84**F. Each fin-shaped fill material portion **84**F has a respective annular shape.

[0121] The sacrificial finned cavity fill material structure **84** comprise first-type sacrificial finned cavity fill material structures **84**A that are formed in the first-type third-stage in-process finned contact via cavities **85**A, and second-type sacrificial finned cavity fill material structures **84**B that are formed in the second-type third-stage in-process finned contact via cavities **85**B. The first-type sacrificial finned cavity fill material structures **84**A vertically extend through each layer within the second-tier alternating stack (**232**, **242**) and through the first-tier retro-stepped dielectric material portion **165**. The second-type sacrificial finned cavity fill material structures **84**B vertically extend through the second-tier retro-stepped dielectric material portion **265** and each layer within the first-tier alternating stack (**132**, **142**).

[0122] Each of the second-type sacrificial finned cavity fill material structures **84**B is laterally surrounded by a vertical stack of first-tier annular insulating plates **401**. Each of the first-tier annular insulating plates **401** is laterally surrounded by a respective one of the first sacrificial material layers **142** and comprises a respective inner cylindrical sidewall that contacts a respective one of the second-type sacrificial finned cavity fill material structures **84**B. Each of the first-type sacrificial finned cavity fill material structures **84**A is laterally surrounded by a vertical stack of second-tier annular insulating plates **402**. Each of the second-tier annular insulating plates **402** is laterally surrounded by a respective one of the second sacrificial material layers **242** and comprises a respective inner cylindrical sidewall that contacts a respective one of the first-type sacrificial finned cavity fill material structures **84**A.

[0123] Referring to FIGS. **22**A-**22**C, a sacrificial contact-level dielectric layer **282** can be formed over the contact-level dielectric layer **280**. The sacrificial contact-level dielectric layer **282** comprises a dielectric material, such as undoped silicate glass or a doped silicate glass, and may have a thickness in a range from 10 nm to 200 nm, such as from 20 nm to 100 nm, although lesser and greater thicknesses may also be employed.

[0124] A photoresist layer (not shown) can be applied over the sacrificial contact-level dielectric layer **282** and can be lithographically patterned to form openings within areas extending across the memory array region **100** and the contact region **300**. The openings in the photoresist layer can laterally extend along the first horizontal direction hd**1** between each neighboring cluster of memory opening fill structures **58**. Lateral isolation trenches **79** can be formed by transferring the pattern in the photoresist layer through the sacrificial contact-level dielectric layer **282**, the contact-level dielectric layer **280**, the second-tier alternating stack (**232**, **242**), and the first-tier alternating stack (**132**, **142**), the retro-stepped dielectric material portions (**165**, **265**), and into the substrate **8**. Portions of the sacrificial contact-level dielectric layer **282**, the contact-level dielectric layer **280**, the second-tier alternating stack (**232**, **242**), and the first-tier alternating stack (**132**, **142**), the retro-stepped dielectric material portions (**165**, **265**) that underlie the openings in the photoresist layer can be removed to form the lateral isolation trenches **79**. In one embodiment, the lateral isolation trenches **79** can be formed between clusters (e.g., blocks) of memory opening fill structures **58**. The clusters of the memory opening fill structures **58** can be laterally spaced apart along the second horizontal direction hd**2** by the lateral isolation trenches **79**. In one embodiment, a memory block can be provided between each neighboring pair of lateral isolation trenches **79**.

[0125] The lateral isolation trenches **79** comprise first lateral isolation trenches **791** that divide a respective first-tier retro-stepped dielectric material portion **165** into a respective pair of first-tier retro-stepped dielectric material portions **165**, and second lateral isolation trenches **792** that divide a respective second-tier retro-stepped dielectric material portion **265** into a respective pair of second-tier retro-stepped dielectric material portions **265**. The first lateral isolation trenches **791** and the second lateral isolation trenches **792** alternate along the second horizontal direction hd**2**. The pitch between a neighboring pair of first lateral isolation trenches **791** can be the same as the width of a repetition unit RU along the second horizontal direction hd**2**.

The pitch between a neighboring pair of second lateral isolation trenches **792** can be the same as the width of a repetition unit RU along the second horizontal direction hd**2**.

[0126] Each alternating stack {(**132**, **142**), (**232**, **242**)} of insulating layers (**132**, **232**) and sacrificial material layers (**142**, **242**) can be formed between a neighboring pair of a first lateral isolation trench **791** and a second lateral isolation trench **792**. The first lateral isolation trench **791** laterally extends along the first horizontal direction hd**1** and comprises a first lengthwise sidewall that contains a lengthwise sidewall of a first-tier retro-stepped dielectric material portion **165**. Each layer within the first-tier alternating stack (**132**, **142**) and within the second-tier alternating stack (**232**, **242**) comprises a respective first sidewall that is exposed to the first lateral isolation trench **791**. The second lateral isolation trench **792** laterally extends along the first horizontal direction hd**1** and comprises a second lengthwise sidewall that contains a lengthwise sidewall of a second-tier retro-stepped dielectric material portion **265**. Each layer within the second-tier alternating stack (**232**, **242**) and within the second-tier alternating stack (**232**, **242**) comprises a respective second sidewall that is exposed to the second lateral isolation trench **792**.

[0127] Referring to FIG. **23**, an etchant that selectively etches the materials of the first and second sacrificial material layers (**142**, **242**), the first sacrificial liner **154**, and the second sacrificial liner **254** with respect to the materials of the first and second insulating layers (**132**, **232**), the material of the outermost layer of the memory films **50** of the memory opening fill structures **58**, and the material of the support pillar structures **20** can be introduced into the lateral isolation trenches **79**, for example, employing an isotropic etch process. First laterally-extending cavities **143** are formed in volumes from which the first sacrificial material layers **142** are removed. Second laterally-extending cavities **243** are formed in volumes from which the second sacrificial material layers **242** are removed. A first staircase-shaped cavity **153** is formed in the volume from which the first sacrificial liner **154** is removed. A second staircase-shaped cavity **253** is formed in the volume from which the second sacrificial liner **254** is removed.

[0128] The isotropic etch process can be a wet etch process employing a wet etch solution, or can be a gas phase (dry) etch process in which the etchant is introduced in a vapor phase into the lateral isolation trenches **79**. For example, if the first and second sacrificial material layers (**142**, **242**), the first sacrificial liner **154**, and the second sacrificial liner **254** include silicon nitride, the etch process can be a wet etch process in which the exemplary structure is immersed within a wet etch tank including phosphoric acid, which etches silicon nitride selective to silicon oxide and silicon.

[0129] The annular insulating plates **40** and the sacrificial finned cavity fill material structures **84** vertically extend from the dielectric isolation layer **6** (if present, or from the substrate **8**) to the contact-level dielectric layer **280**, and provide structural support for the portions of the insulating layers (**132**, **232**) that are present in the contact region **300** and for the retro-stepped dielectric material portions (**165**, **265**), after removal of the sacrificial material layers. The annular insulating plates **40** can enhance structural support for the insulating layers (**132**, **232**) and the retro-stepped dielectric material portions (**165**, **265**). The memory opening fill structures **58** provide structural support to the insulating layers (**132**, **232**) in the memory array region **100**.

[0130] Each of the first and second laterally-extending cavities (**143**, **243**) can be a laterally extending cavity having a lateral dimension that is greater than the vertical extent of the cavity. In other words, the lateral dimension of each of the first and second laterally-extending cavities (**143**, **243**) can be greater than the height of the respective laterally-extending cavity. A plurality of first laterally-extending cavities can be formed in the volumes from which the material of the first sacrificial material layers **142** is removed. A plurality of second laterally-extending cavities can be formed in the volumes from which the material of the second sacrificial material layers **242** is removed. Each of the first and second laterally-extending cavities can extend substantially parallel to the top surface of the substrate **8**. A laterally-extending cavity (**143**, **243**) can be vertically bounded by a top surface of an underlying insulating layer (**132** or **232**) and a bottom surface of an overlying insulating layer (**132** or **232**). In one embodiment, each of the first and second laterally-extending cavities (**143**, **243**) can have a uniform height throughout.

[0131] The first staircase-shaped cavity **153** can be formed over the first staircase-shaped surfaces and the first insulating liner **152**. As discussed above, the first sacrificial liner **154** can be formed by a conformal deposition process, and has a uniform thickness that is greater than the thickness of each first sacrificial material layer **142**.

[0132] Thus, after removal of the first sacrificial liner **154**, each horizontally-extending portion of the first staircase-shaped cavity **153** has a uniform height, which is the same as the uniform width of each vertically-extending portion of the first staircase-shaped cavity **153**. Each horizontally-extending portion of the second staircase-shaped cavity **253** has a uniform height, which is the same as the uniform width of each vertically-extending portion of the second staircase-shaped cavity **253**. The uniform widths and the uniform heights of the first staircase-shaped cavity **153** and the second staircase-shaped cavity **253** are greater than the thicknesses of the sacrificial material layers (**142**, **242**).

[0133] Referring to FIG. **24**, an optional blocking dielectric material (i.e., a dielectric material that can be employed to block tunneling of electrons) can be conformally deposited in the laterally-extending cavities (**143**, **243**), the first staircase-shaped cavity **153**, and the second staircase-shaped cavity **253**. In one embodiment, the blocking dielectric material comprises a dielectric metal oxide material, such as aluminum oxide, hafnium oxide, tantalum oxide, titanium oxide, yttrium oxide, etc. Alternatively or additionally, the blocking dielectric material may comprise silicon oxide, silicon nitride, silicon oxynitride, and/or silicon carbide nitride. The thickness of the blocking dielectric material may be in a range from 2 nm to 20 nm, such as from 6 nm to 12 nm, although lesser and greater thicknesses may also be employed.

[0134] A backside blocking dielectric layer **44** can be formed within each laterally-extending cavity (**143**, **243**). A blocking dielectric liner **144** can be formed in each of the first staircase-shaped cavity **153** and the second staircase-shaped cavity **253**. Each outer sidewall of the annular insulating plates **40** can be contacted by the backside blocking dielectric layer **44**. Each fin-shaped fill material portion **84**F of the sacrificial finned cavity fill material structures **84** can contact a respective blocking dielectric liner **144**. A first

blocking dielectric liner **144** that is formed within the first staircase-shaped cavity **153** may contact each of the first-type sacrificial finned cavity fill material structures **84**A. A second blocking dielectric liner **144** that is formed within the second staircase-shaped cavity **253** may contact each of the second-type sacrificial finned cavity fill material structures **84**B.

[0135] Referring to FIG. **25**, at least one conductive material can be conformally deposited in the plurality of laterally-extending cavities (**143**, **243**), in the staircase-shaped cavities (**153**, **253**), on the sidewalls of the lateral isolation trench **79**, and over the contact-level dielectric layer **280**. The at least one conductive material can include at least one metallic material, i.e., an electrically conductive material that includes at least one metal element.

[0136] The at least one metallic material can be deposited by a conformal deposition method, which can be, for example, chemical vapor deposition (CVD), atomic layer deposition (ALD), electroless plating, electroplating, and/or a combination thereof. The at least one metallic material can be an elemental metal, an intermetallic alloy of at least two elemental metals, a conductive nitride of at least one elemental metal, a conductive metal oxide, a conductive doped semiconductor material, a conductive metal-semiconductor alloy such as a metal silicide, alloys thereof, and combinations or stacks thereof. Non-limiting exemplary metallic materials that can be deposited in the laterally-extending cavities include tungsten, tungsten nitride, titanium, titanium nitride, tantalum, tantalum nitride, cobalt, and/or ruthenium. In one embodiment, the at least one metallic material may comprise a combination of a metallic barrier liner material and a metallic fill material. The metallic barrier liner material may comprise titanium nitride, tantalum nitride, tungsten nitride, molybdenum nitride, or a combination thereof. The metallic fill material may comprise titanium, tantalum, tungsten, cobalt, molybdenum, ruthenium, copper, etc. In one embodiment, the at least one metallic material can be deposited by chemical vapor deposition or atomic layer deposition.

[0137] According to an aspect of the present disclosure, the total thickness of the at least one conformally-deposited conductive material may be greater than one half of the height of the laterally-extending cavities (**143**, **243**), and can be less than one half the height of the horizontally-extending portions of the staircase-shaped cavities (**153**, **253**) (which is the same as the width of the vertically-extending portions of the staircase-shaped cavities (**153**, **253**). Thus, each of the laterally-extending cavities (**143**, **243**) can be completely filled with the at least one conformally-deposited conductive material, while the staircase-shaped cavities (**153**, **253**) are only partially filled and contain unfilled voids are present within.

[0138] The deposited at least one conductive material can be isotropically etched back the at least one conformally-deposited conductive material from inside the staircase-shaped cavities (**153**, **253**), from the sidewalls of lateral isolation trenches **79**, and from above the sacrificial contact-level dielectric layers **282** by performing an isotropic etch back process. The etch distance of the isotropic etch back process may be the same as, or may be greater than, the total thickness of the deposited at least one conductive material. Each remaining portion of the deposited metallic material in the first laterally-extending cavities constitutes an electrically conductive layer **146**. Each remaining portion of the deposited metallic material in the second laterally-extending cavities constitutes a second electrically conductive layer **246**. Each electrically conductive layer (**146**, **246**) can be a conductive line structure (e.g., word line or select gate electrode). The at least one conductive material can be completely removed from inside the staircase-shaped cavities (**153**, **253**), and a blocking dielectric liner **144** can be physically exposed around each staircase-shaped cavity (**153**, **253**).

[0139] A plurality of electrically conductive layers **146** can be formed in the plurality of first laterally-extending cavities **143**, and a plurality of second electrically conductive layers **246** can be formed in the plurality of second laterally-extending cavities **243**. Thus, the first and second sacrificial material layers (**142**, **242**) can be replaced with the first and second electrically conductive material layers (**146**, **246**), respectively. Specifically, each first sacrificial material layer **142** can be replaced with a backside blocking dielectric layer **44** and a first electrically conductive layer **146**, and each second sacrificial material layer **242** can be replaced with a backside blocking dielectric layer **44** and a second electrically conductive layer **246**. A backside cavity is present in the portion of each lateral isolation trench **79** that is not filled with the continuous metallic material layer.

[0140] Each of the memory opening fill structures **58** (which contains a respective memory stack structures **55**) comprises a vertical stack of memory elements located at each level of the electrically conductive layers (**146**, **246**). A subset of the middle electrically conductive layers (**146**, **246**) can comprise the word lines for the memory elements. At least one uppermost electrically conductive layer **246** may comprise a drain side select gate electrode. At least one bottommost electrically conductive layer **146** may comprise a source side select gate electrode.

[0141] The backside blocking dielectric layers **44** can be interposed between each neighboring pair of a first electrically conductive layer **146** and a first insulating layer **132** within the first-tier alternating stack (**132**, **146**), and can be interposed between each neighboring pair of a second electrically conductive layer **246** and a second insulating layer **232**. In one embodiment, a subset of the backside blocking dielectric layers **44** embeds a respective one of the first electrically conductive layers **146**, and is interposed between the respective one of the first electrically conductive layers **146** and a respective one of the first insulating layers **132**. A subset of the backside blocking dielectric layers **44** embeds a respective one of the second electrically conductive layers **246**, and is interposed between the respective one of the second electrically conductive layers **246** and a respective one of the second insulating layers **232**. In one embodiment, each annular insulating plate **40** may contact a sidewall of a respective one of the backside blocking dielectric layers **44**. Each fin-shaped fill material portion **84**F of the sacrificial finned cavity fill material structures **84** can contacts a sidewall of a respective blocking dielectric liner **144**. The blocking dielectric liners **144** and the backside blocking dielectric layers **44** may have the same material composition and the same thickness. A first-tier alternating stack of first insulating layers **132** and first electrically conductive layers **146** can be formed underneath the inter-tier dielectric layer **180**, and a second-tier alternating stack of second insulating layers **232** and second electrically conductive layers **246** can be formed over the inter-tier dielectric layer **180**.

[0142] In summary, the first sacrificial material layers **142** and the second sacrificial material layers **242** can be replaced with first electrically conductive layers **146** and second electrically conductive layers **246**, respectively. A replaced first-tier alternating stack (**132**, **146**) and a replaced second-tier alternating stack (**232**, **246**) are formed between each neighboring pair of lateral isolation trenches **79**. A first-tier alternating stack (**132**, **146**) of first insulating layers **132** and first electrically conductive layers **146** is located over a substrate between each neighboring pair of lateral isolation trenches **79**. The first-tier alternating stack (**132**, **146**) comprises a first staircase region **301** having first stepped surfaces in which first vertical surface segments of the first stepped surfaces are laterally spaced apart along a first horizontal direction hd**1** and are interconnected to each other by first horizontally-extending surface segments of the first stepped surfaces. A first-tier retro-stepped dielectric material portion **165** overlies the first stepped surfaces. A second-tier alternating stack (**232**, **246**) of second insulating layers **232** and second electrically conductive layers **246** is located over the first-tier alternating stack (**132**, **146**) and the first-tier retro-stepped dielectric material portion **165** between each neighboring pair of lateral isolation trenches **79**. The second-tier alternating stack (**232**, **246**) comprises a second staircase region **302** having second stepped surfaces in which second vertical surface segments of the second stepped surfaces are laterally spaced apart along the first horizontal direction hd**1** and are interconnected to each other by second horizontally-extending surface segments of the second stepped surfaces. A second-tier retro-stepped dielectric material portion **265** overlies the second stepped surfaces. Memory stack structures **55** vertically extend through each layer within the first-tier alternating stack (**132**, **146**) and through each layer within the second-tier alternating stack (**232**, **246**) in a memory array region **100**.

[0143] Referring to FIG. **26**, dopants of the second conductivity type may optionally be implanted into surface portions of the semiconductor material layer **9** that underlie the lateral isolation trenches **79** to form source regions **61**. The source regions **61** may comprise dopants of the second conductivity type at an atomic concentration in a range from $5.0\times10^{18}/cm^3$ to $2.0\times10^{21}/cm^3$. Alternatively, formation of the source regions **61** may be omitted at this time and instead a top source contact is formed over the bottom tips of the vertical semiconductor channels after removal of the substrate **8**.

[0144] A dielectric fill material can be conformally deposited in the staircase-shaped cavities (**153**, **253**) and in the peripheral portions of the lateral isolation trenches **79** by a conformal deposition process. The dielectric fill material may comprise silicon oxide or silicon nitride. The thickness of the deposited dielectric fill material can greater than one half of the height of the horizontally-extending portions of the staircase-shaped cavities (**153**, **253**) so that the staircase-shaped cavities (**153**, **253**) are filled within the dielectric fill material. The portion of the dielectric fill material that fills the first staircase-shaped cavity **153** constitutes a first dielectric fill material layer **174**. The portion of the dielectric fill material that fills the second staircase-shaped cavity **253** constitutes a second dielectric fill material layers **274**. A contiguous combination of the first dielectric fill material layer **174** and a blocking dielectric liner **144** constitutes a first composite dielectric layer (**144**, **174**). A contiguous combination of the second dielectric fill material layer **274** and a blocking dielectric liner **144** constitutes a second composite dielectric layer (**144**, **274**).

[0145] An anisotropic etch process can be performed to remove horizontally-extending portions of the dielectric fill material from above the top surface of the sacrificial contact-level dielectric layer **282** and at the bottom of each of the lateral isolation trenches **79**. Each remaining tubular portion of the dielectric fill material that remains in a respective lateral isolation trenches **79** constitutes an insulating spacer **74**. A lateral isolation cavity **79'** can be present within each unfilled volume of the lateral isolation trenches **79** that is laterally surrounded by a respective one of the insulating spacers **74**.

[0146] Generally, a first composite dielectric layer (**144**, **174**) can be interposed between the first stepped surfaces and the first-tier retro-stepped dielectric material portion **165** and including a first blocking dielectric liner **144** and a first dielectric fill material layer **174** embedded within the first blocking dielectric liner **144**. The first blocking dielectric liner **144** contacts each top surface of the first dielectric fill material layer **174** each bottom surface of the first dielectric fill material layer **174**, and a subset of sidewalls of the first dielectric fill material layer **174**. A second composite dielectric layer (**144**, **274**) can be interposed between the second stepped surfaces and the second retro-stepped dielectric material portion **265** and including a second blocking dielectric liner **144** and a second dielectric fill material layer **274** embedded within the blocking dielectric liner **144**. The second blocking dielectric liner **144** contacts each top surface of the second dielectric fill material layer **274** each bottom surface of the second dielectric fill material layer **274**, and a subset of sidewalls of the second dielectric fill material layer **274**.

[0147] Each composite dielectric layer {(**144**, (**174** or **274**)} comprises horizontally-extending portions and vertically-extending portions that are interconnected over the stepped surfaces. A vertical thickness of the horizontally-extending portions and a lateral thickness of the vertically-extending portions are the same for each composite dielectric layer {(**144**, (**174** or **274**)}, and are greater than an inter-layer gap between vertically neighboring pairs of the first insulating layers **132** within the first-tier alternating stack (**132**, **146**), and are greater than an inter-layer gap between vertically neighboring pairs of the second insulating layers **232** within the second-tier alternating stack (**232**, **246**).

[0148] Referring to FIG. **27**, at least one conductive fill material can optionally be deposited in unfilled volumes of the lateral isolation trenches **79**. Portions of the at least one conductive material that overlie the horizontal plane including the top surface of the sacrificial contact-level dielectric layer **282** can be removed by a planarization process such as a recess etch process and/or a chemical mechanical polishing process. Each remaining portion of the at least one conductive fill material that fills a respective lateral isolation trench **79** constitutes a source contact via structure **76**. Alternatively, if the source region **61** is omitted, then the source contact via structure **76** can also be omitted at this step. Instead, the lateral isolation trenches **79** may be completely filled with the insulating spacers **74**.

[0149] Referring to FIG. **28**, a photoresist layer (not shown) can be applied over the sacrificial contact-level dielectric layer **282**, and can be lithographically patterned to form openings in areas that overlap with top surfaces of the

sacrificial finned cavity fill material structures **84**. An anisotropic etch process can be performed to form etch through unmasked portions of the sacrificial contact-level dielectric layer **282** to physically expose top surfaces of the sacrificial finned cavity fill material structures **84**. A selective etch process can be performed to remove the sacrificial fill material of the sacrificial finned cavity fill material structures **84** selective to materials of the annular insulating plates **40**, the retro-stepped dielectric material portions (**165**, **265**), and the dielectric isolation layer **6** (if present). Finned contact via cavities **87** are formed in volumes from which the sacrificial finned cavity fill material structures **84** are removed. The finned contact via cavities **87** comprises first finned contact via cavities **87**A to which the first-tier retro-stepped dielectric material portion **165** is exposed, and second finned contact via cavities **87**B to which the first-tier retro-stepped dielectric material portion **165** is not exposed. Each finned contact via cavity **87** comprises a cylindrical cavity portion **87**C and a fin cavity portion **87**F.

[0150] Referring to FIG. **29**, an optional isotropic etch process can be performed to isotropically etch the material of the first insulating liner **152** and the second insulating liner **252**. The duration of the isotropic etch can be selected such that the etch distance for the material of the first insulating liner **152** and the second insulating liner **252** is greater than the thicknesses of the first insulating liner **152** and the second insulating liner **252**. Thus, each physically exposed portion of the first insulating liner **152** and the second insulating liner **252** that underlie the fin cavity portions **87**F are etched through. Each of the electrically conductive layers (**146**, **246**) has a respective annular top surface segment that is physically exposed to a respective one of the fin cavity portions **87**F of the finned contact via cavities **87**. An annular tapered concave surface of an insulating liner (**152**, **252**) can be physically exposed around each fin cavity portion **87**F. The isotropic etch for the first insulating liner **152** and the second insulating liner **252** may comprise a dilute hydrofluoric acid etch.

[0151] Optionally, the isotropic etch may be continued to remove exposed portions of the respective blocking dielectric liner **144** and the respective backside blocking dielectric layer **44**. If the respective blocking dielectric liner **144** and the backside blocking dielectric layer **44** comprise aluminum oxide, then the isotropic etch may comprise a hot phosphoric acid etch.

[0152] In one embodiment, surface portions of the retro-stepped dielectric material portions (**165**, **265**), the annular insulating plates **40**, the contact-level dielectric layer **280**, the inter-tier dielectric layer **180**, and the dielectric isolation layer **6** can be collaterally isotropically recessed during the isotropic etch process.

[0153] Referring to FIGS. **30**A-**30**C, at least one conductive material, such as at least one metallic material, can be deposited in the finned contact via cavities **87**. The at least one conductive material may comprise a combination of a metallic barrier liner material (such as TiN, TaN, WN, MoN, or a combination thereof) and a metallic fill material (such as W, Ti, Ta, Mo, Ru, Co, Cu, etc.). Excess portions of the at least one conductive material can be removed from above the horizontal plane including the top surface of the contact-level dielectric layer **280** by a planarization process such as a chemical mechanical polishing process. In one embodiment, the sacrificial contact-level dielectric layer **282** and portions of the insulating spacers **74** and the source contact via structures **76** that overlie the horizontal plane including the top surface of the contact-level dielectric layer **280** can be collaterally removed during the planarization process. Each remaining portion of the at least one conductive material that fills a respective finned contact via cavity **87** constitutes a contact via structure, which is herein referred to as a layer contact via structure **86**.

[0154] The layer contact via structures **86** comprise first contact via structures **86**A that are formed in the first finned contact via cavities **87**A and second contact via structures **86**B that are formed in the second finned contact via cavities **87**B. Each of the layer contact via structures **86** vertically extends at least from a bottommost surface of the first-tier alternating stack (**132**, **146**) to a horizontal plane located at or above a top surface of the memory opening fill structure **58**. Each layer contact via structure **86** comprises a respective conductive pillar portion **86**C and a respective conductive fin portion **86**F that laterally protrudes from the respective conductive pillar portion **86**C and has a first annular bottom surface segment ABSS**1** contacting an annular top surface segment of one of the electrically conductive layers (**146**, **246**). Each conductive fin portion **86**F may also have a second annular bottom surface segment ABSS**2** contacting an annular top surface segment of an annular insulating plate **40**, which may be a topmost annular insulating plate **40** within a vertical stack of annular insulating plates **40** underlying the respective conductive fin portion **86**F. Segments ABSS**1** and ABSS**2** may be horizontally co-planar. Each conductive fin portion **86**F may have an annular top surface ATS that contacts an annular bottom surface segment of one of the retro-stepped dielectric material portions (**165**, **265**).

[0155] A plurality of first contact via structures **86**A vertically extends through the first-tier retro-stepped dielectric material portion **165** and each layer within a second-tier alternating stack (**232**, **246**). A plurality of second contact via structures **86**B vertically extends through the second retro-stepped dielectric material portion **265** and each layer within a first-tier alternating stack (**132**, **146**). In one embodiment, each annular insulating plate **40** within a vertical stack of annular insulating plates **40** has a lateral width which laterally offsets a respective electrically conductive layer (**146**, **246**) from the conductive pillar portion **86**C by a uniform lateral offset distance, which is herein referred to as a first lateral offset distance lod**1**. Each conductive fin portion **86**F of a layer contact via structure **86** may have an outer sidewall that is laterally spaced from a sidewall of the conductive pillar portion **86**C of the layer contact via structure **86** by a second lateral offset distance lod**2**.

[0156] Referring to FIGS. **30**B and **30**C, the first electrically conductive layers **146** of the first tier continuously extend along the first horizontal direction hd**1** between adjacent memory array regions **100** through the respective lower lane section **310** of the contact region **300**. The second electrically conductive layers **246** of the second tier continuously extend along the first horizontal direction hd**1** between adjacent memory array regions **100** through the respective upper lane section **312** of the contact region **300**. The lower lane section **310** is laterally offset from the upper lane section **312** along the second horizontal direction hd**2** by the tapered lane section **314** of the contact region **300**. The first-tier alternating stack (**132**, **146**) is tapered in the opposite direction from the second-tier alternating stack

(**232**, **246**) in the tapered lane section **314** between a pair of adjacent lateral isolation trench fill structures (**74**, **76**), as shown in FIG. **30**C.

[0157] Referring collective to FIGS. **1**A-**30**C and according to various embodiments of the present disclosure, a memory device is provided, which comprises: a first-tier alternating stack (**132**, **146**) of first insulating layers **132** and first electrically conductive layers **146** located over a substrate, wherein the first-tier alternating stack (**132**, **146**) comprises a first staircase region **301** having first stepped surfaces; a first-tier retro-stepped dielectric material portion **165** overlying the first stepped surfaces; a second-tier alternating stack (**232**, **246**) of second insulating layers **232** and second electrically conductive layers **246** located over the first-tier alternating stack (**132**, **146**) and the first-tier retro-stepped dielectric material portion **165**, wherein the second-tier alternating stack (**232**, **246**) comprises a second staircase region **302** having second stepped surfaces; a second-tier retro-stepped dielectric material portion **265** overlying the second stepped surfaces; memory stack structures **55** vertically extending through each layer within the first-tier alternating stack (**132**, **146**) and through each layer within the second-tier alternating stack (**232**, **246**) in a memory array region **100**; and first-type layer contact via structures **86**A vertically extending through each layer within the second-tier alternating stack (**232**, **246**) and through the first-tier retro-stepped dielectric material portion **165**, wherein each of the first-type layer contact via structures **86**A contacts a respective one of the first electrically conductive layers **146**.

[0158] In one embodiment, the memory device comprises second-type layer contact via structures **86**B vertically extending through the second-tier retro-stepped dielectric material portion **265**, wherein each of the second-type layer contact via structures **86**B contacts a respective one of the second electrically conductive layers **246**. In one embodiment, the second-type layer contact via structures **86**B vertically extend through each layer within the first-tier alternating stack (**132**, **146**). In one embodiment, one of the second-type layer contact via structures **86**B is laterally surrounded by a vertical stack of first-tier annular insulating plates **401**; and each of the first-tier annular insulating plates **401** is laterally surrounded by a respective one of the first electrically conductive layers **146** and comprises a respective inner cylindrical sidewall that contacts said one of the second-type layer contact via structures **86**B.

[0159] In one embodiment, each of the second-type layer contact via structures **86**B contacts an annular top surface and a cylindrical surface of the respective one of the second electrically conductive layers **246**. In one embodiment, one of the second-type layer contact via structures **86**B contacts one of second electrically conductive layers **246** and vertically extends through and is electrically isolated from each second electrically conductive layer **246** that underlies said one of the second electrically conductive layers **246**. In one embodiment, said each second electrically conductive layer **246** that underlies said one of the second electrically conductive layers **246** is contacted by an outer sidewall of a respective annular insulating plate **40** that laterally surrounds, and contacts, said one of the second-type layer contact via structures **86**B. In one embodiment, each of the second-type layer contact via structures **86**B is in contact with the second-tier retro-stepped dielectric material portion **265** and does not contact the first-tier retro-stepped dielectric material portion **165**; and each of the first-type layer contact via structures **86**A is in contact with the first-tier retro-stepped dielectric material portion **165** and does not contact the second-tier retro-stepped dielectric material portion **265**.

[0160] In one embodiment, each of the first-type layer contact via structures **86**A vertically extend through an horizontal plane including a bottom surface of a bottommost layer within the first-tier alternating stack (**132**, **146**). In one embodiment, each of the first-type layer contact via structures **86**A contact an annular top surface and a cylindrical surface of the respective one of the first electrically conductive layers **146**.

[0161] In one embodiment, one of the first-type layer contact via structures **86**A contacts one of first electrically conductive layers **146** and vertically extends through, and is electrically isolation from, each first electrically conductive layer **146** that underlies said one of the first electrically conductive layers **146**. In one embodiment, said each first electrically conductive layer **146** that underlies said one of the first electrically conductive layers **146** is contacted by an outer sidewall of a respective annular insulating plate **40** that laterally surrounds, and contacts, said one of the first-type layer contact via structures **86**A.

[0162] In one embodiment, one of the first-type layer contact via structures **86**A is laterally surrounded by a vertical stack of second-tier annular insulating plates **402**; and each of the second-tier annular insulating plates **402** is laterally surrounded by a respective one of the second electrically conductive layers **246** and comprises a respective inner cylindrical sidewall that contacts said one of the first-type layer contact via structures **86**A.

[0163] In one embodiment, the memory device comprises: a first lateral isolation trench fill structure (**74**, **76**) that laterally extends along the first horizontal direction hd**1** and comprises a first lengthwise sidewall that contacts a lengthwise sidewall of the first-tier retro-stepped dielectric material portion **165**, wherein each layer within the first-tier alternating stack (**132**, **146**) and within the second-tier alternating stack (**232**, **246**) comprises a respective first sidewall that contacts the first lengthwise sidewall of the first lateral isolation trench fill structure (**74**, **76**); and a second lateral isolation trench fill structure (**74**, **76**) that laterally extends along the first horizontal direction hd**1** and comprises a second lengthwise sidewall that contacts a lengthwise sidewall of the second-tier retro-stepped dielectric material portion **265**, wherein each layer within the second-tier alternating stack (**232**, **246**) and within the second-tier alternating stack (**232**, **246**) comprises a respective second sidewall that contacts the second lengthwise sidewall of the second lateral isolation trench fill structure (**74**, **76**).

[0164] In one embodiment, the second lateral isolation trench fill structure (**74**, **76**) is laterally spaced from the first lateral isolation trench fill structure (**74**, **76**) along a second horizontal direction hd**2** which is perpendicular to the first horizontal direction hd**1** by a uniform lateral spacing; the first-tier retro-stepped dielectric material portion **165** does not contact the second lateral isolation trench fill structure (**74**, **76**); and the second-tier retro-stepped dielectric material portion **265** does not contact the first lateral isolation trench fill structure (**74**, **76**).

[0165] Embodiments of the present disclosure can be employed to provide a row of first contact via structures **86**A contacting a respective first electrically conductive layer **146** and a row of second contact via structures **86**B contacting a

respective second electrically conductive layer **246** between each neighboring pair of lateral isolation trench fill structures (**74**, **76**). The row of first contact via structures **86**A and the row of second contact via structures **86**B can be laterally offset relative to each other along the second horizontal direction hd**2**. Thus, the row of first contact via structures **86**A and the row of second contact via structures **86**B can be formed in a parallel configuration between a neighboring pair of lateral isolation trench fill structure (**74**, **76**), and the length of the contact region **300** along the first horizontal direction hd**1** can be shortened compared to a conventional configuration in which contact via structures for contacting electrically conductive layers are arranged in a single row. Furthermore, dedicated continuous conductive bridge region in which electrically conductive layers (**146**, **246**) continuously extends along the first horizontal direction hd**1** between adjacent memory array regions **100** can be omitted because the electrically conductive layers (**146**, **246**) continuously extend along the first horizontal direction hd**1** between adjacent memory array regions **100** through the respective lower lane section **310** and upper lane section **312** of the contact region **300**. Furthermore, the electrical resistance of the strip portion of each electrically conductive layer (**146**, **246**) that is located in the contact region **300** between two memory array regions **100** can be reduced through reduction of the length of the strip portions of the electrically conductive layers (**146**, **246**) located in the contact region **300**.

[0166] Although the foregoing refers to particular preferred embodiments, it will be understood that the disclosure is not so limited. It will occur to those of ordinary skill in the art that various modifications may be made to the disclosed embodiments and that such modifications are intended to be within the scope of the disclosure. Compatibility is presumed among all embodiments that are not alternatives of one another. The word "comprise" or "include" contemplates all embodiments in which the word "consist essentially of" or the word "consists of" replaces the word "comprise" or "include," unless explicitly stated otherwise. Whenever two or more elements are listed as alternatives in a same paragraph of in different paragraphs, a Markush group including a listing of the two or more elements is also impliedly disclosed. Whenever the auxiliary verb "can" is employed in this disclosure to describe formation of an element or performance of a processing step, an embodiment in which such an element or such a processing step is not performed is also expressly contemplated, provided that the resulting apparatus or device can provide an equivalent result. As such, the auxiliary verb "can" as applied to formation of an element or performance of a processing step should also be interpreted as "may" or as "may, or may not" whenever omission of formation of such an element or such a processing step is capable of providing the same result or equivalent results, the equivalent results including somewhat superior results and somewhat inferior results. Where an embodiment employing a particular structure and/or configuration is illustrated in the present disclosure, it is understood that the present disclosure may be practiced with any other compatible structures and/or configurations that are functionally equivalent provided that such substitutions are not explicitly forbidden or otherwise known to be impossible to one of ordinary skill in the art. If publications, patent applications, and/or patents are cited herein, each of such documents is incorporated herein by reference in their entirety.

What is claimed is:

1. A memory device, comprising:

a first-tier alternating stack of first insulating layers and first electrically conductive layers, wherein the first-tier alternating stack comprises a first staircase region having first stepped surfaces;

a first-tier retro-stepped dielectric material portion overlying the first stepped surfaces;

a second-tier alternating stack of second insulating layers and second electrically conductive layers located over the first-tier alternating stack and the first-tier retro-stepped dielectric material portion, wherein the second-tier alternating stack comprises a second staircase region having second stepped surfaces;

a second-tier retro-stepped dielectric material portion overlying the second stepped surfaces;

memory stack structures vertically extending through each layer within the first-tier alternating stack and through each layer within the second-tier alternating stack in a memory array region; and

first-type layer contact via structures vertically extending through each layer within the second-tier alternating stack and through the first-tier retro-stepped dielectric material portion, wherein each of the first-type layer contact via structures contacts a respective one of the first electrically conductive layers.

2. The memory device of claim **1**, further comprising second-type layer contact via structures vertically extending through the second-tier retro-stepped dielectric material portion, wherein each of the second-type layer contact via structures contacts a respective one of the second electrically conductive layers.

3. The memory device of claim **2**, wherein the second-type layer contact via structures vertically extend through each layer within the first-tier alternating stack.

4. The memory device of claim **3**, wherein:

one of the second-type layer contact via structures is laterally surrounded by a vertical stack of first-tier annular insulating plates; and

each of the first-tier annular insulating plates is laterally surrounded by a respective one of the first electrically conductive layers and comprises a respective inner cylindrical sidewall that contacts said one of the second-type layer contact via structures.

5. The memory device of claim **2**, wherein each of the second-type layer contact via structures contacts an annular top surface of the respective one of the second electrically conductive layers.

6. The memory device of claim **2**, wherein one of the second-type layer contact via structures contacts one of second electrically conductive layers and vertically extends through and is electrically isolated from each second electrically conductive layer that underlies said one of the second electrically conductive layers.

7. The memory device of claim **6**, wherein said each second electrically conductive layer that underlies said one of the second electrically conductive layers is contacted by an outer sidewall of a respective annular insulating plate that laterally surrounds and contacts said one of the second-type layer contact via structures.

8. The memory device of claim **2**, wherein:

each of the second-type layer contact via structures is in contact with the second-tier retro-stepped dielectric material portion and does not contact the first-tier retro-stepped dielectric material portion; and

each of the first-type layer contact via structures is in contact with the first-tier retro-stepped dielectric material portion and does not contact the second-tier retro-stepped dielectric material portion.

9. The memory device of claim **1**, wherein each of the first-type layer contact via structures vertically extend through an horizontal plane including a bottom surface of a bottommost layer within the first-tier alternating stack.

10. The memory device of claim **1**, wherein each of the first-type layer contact via structures contact an annular top surface of the respective one of the first electrically conductive layers.

11. The memory device of claim **1**, wherein:

one of the first-type layer contact via structures contacts one of first electrically conductive layers and vertically extends through and is electrically isolation from each first electrically conductive layer that underlies said one of the first electrically conductive layers; and

said each first electrically conductive layer that underlies said one of the first electrically conductive layers is contacted by an outer sidewall of a respective annular insulating plate that laterally surrounds and contacts said one of the first-type layer contact via structures.

12. The memory device of claim **1**, wherein:

one of the first-type layer contact via structures is laterally surrounded by a vertical stack of second-tier annular insulating plates; and

each of the second-tier annular insulating plates is laterally surrounded by a respective one of the second electrically conductive layers and comprises a respective inner cylindrical sidewall that contacts said one of the first-type layer contact via structures.

13. The memory device of claim **1**, wherein:

first vertical surface segments of the first stepped surfaces are laterally spaced apart along a first horizontal direction and are interconnected to each other by first horizontally-extending surface segments of the first stepped surfaces; and

second vertical surface segments of the second stepped surfaces are laterally spaced apart along the first horizontal direction and are interconnected to each other by second horizontally-extending surface segments of the second stepped surfaces.

14. The memory device of claim **13**, further comprising:

a first lateral isolation trench fill structure that laterally extends along the first horizontal direction and comprises a first lengthwise sidewall that contacts a lengthwise sidewall of the first-tier retro-stepped dielectric material portion, wherein each layer within the first-tier alternating stack and within the second-tier alternating stack comprises a respective first sidewall that contacts the first lengthwise sidewall of the first lateral isolation trench fill structure; and

a second lateral isolation trench fill structure that laterally extends along the first horizontal direction and comprises a second lengthwise sidewall that contacts a lengthwise sidewall of the second-tier retro-stepped dielectric material portion, wherein each layer within the second-tier alternating stack and within the second-tier alternating stack comprises a respective second sidewall that contacts the second lengthwise sidewall of the second lateral isolation trench fill structure.

15. The memory device of claim **14**, wherein:

the second lateral isolation trench fill structure is laterally spaced from the first lateral isolation trench fill structure along a second horizontal direction which is perpendicular to the first horizontal direction by a uniform lateral spacing;

the first-tier retro-stepped dielectric material portion does not contact the second lateral isolation trench fill structure; and

the second-tier retro-stepped dielectric material portion does not contact the first lateral isolation trench fill structure.

16. The memory device of claim **15**, further comprising additional memory stack structures vertically extending through each layer within the first-tier alternating stack and through each layer within the second-tier alternating stack in an additional memory array region, wherein each of the memory stack structures and each of the additional memory stack structures comprises a memory film and a vertical semiconductor channel.

17. The memory device of claim **16**, wherein:

the memory array region is laterally spaced from the additional memory array region by a contact region containing the first staircase region, the second staircase region, the first-tier retro-stepped dielectric material portion, the second-tier retro-stepped dielectric material portion, and the first-type layer contact via structures;

the first electrically conductive layers continuously extend along the first horizontal direction between the memory array region and the additional memory array region through a lower lane section of the contact region;

the second electrically conductive layers continuously extend along the first horizontal direction between the memory array region and the additional memory array region through an upper lane section of the contact region;

the lower lane section is laterally offset from the upper lane section along the second horizontal direction by a tapered lane section of the contact region; and

the first-tier alternating stack is tapered in an opposite direction from the second-tier alternating stack in the tapered lane section between the first lateral isolation trench fill structure and the second t lateral isolation trench fill structure.

18. A method of forming a memory device, comprising:

forming a first-tier alternating stack of first insulating layers and first sacrificial material layers over a substrate;

forming first stepped surfaces in a first staircase region by patterning the first-tier alternating stack such that first vertical surface segments of the first stepped surfaces are laterally spaced apart along a first horizontal direction and are interconnected to each other by first horizontally-extending surface segments of the first stepped surfaces, wherein the first staircase region has a first area having a first width along a second horizontal direction that is perpendicular to the first horizontal direction in a plan view;

forming a first-tier retro-stepped dielectric material portion over the first stepped surfaces;

forming a second-tier alternating stack of second insulating layers and second sacrificial material layers over the first-tier alternating stack and the first-tier retro-stepped dielectric material portion;

forming second stepped surfaces in a second staircase region by patterning the second-tier alternating stack such that second vertical surface segments of the second stepped surfaces are laterally spaced apart along the first horizontal direction and are interconnected to each other by second horizontally-extending surface segments of the second stepped surfaces, wherein the second staircase region has a second area having a second width along the second horizontal direction in the plan view, and the second area is laterally shifted relative to the first area along the second horizontal direction by a lateral offset distance that is greater than one half of the first width and is less than the first width so that a partial overlap between the second area and the first area is present in the plan view;

forming memory stack structures through each layer within the first-tier alternating stack and with the second-tier alternating stack in at least one memory array region;

forming first and second lateral isolation trenches, wherein the first lateral isolation trench cuts through the second-tier alternating stack, the first-tier alternating stack, and the first-tier retro-stepped dielectric material portion and does not contact the second-tier retro-stepped dielectric material portion, and the second lateral isolation trench cuts through the second-tier alternating stack, the second-tier retro-stepped dielectric material portion, and the first-tier alternating stack and does not contact the first-tier retro-stepped dielectric material portion; and

replacing the first sacrificial material layers and the second sacrificial material layers with first electrically conductive layers and second electrically conductive layers, respectively, to form a replaced first-tier alternating stack and a replaced second-tier alternating stack.

19. The method of claim **18**, further comprising forming layer contact via structures, wherein the layer contact via structures comprise:

first-type layer contact via structures vertically extending through each layer within the replaced second-tier alternating stack and through the first-tier retro-stepped dielectric material portion, wherein each of the first-type layer contact via structures contacts a respective one of the first electrically conductive layers; and

second-type layer contact via structures vertically extending through the second-tier retro-stepped dielectric material portion, wherein each of the second-type layer contact via structures contact a respective one of the second electrically conductive layers.

20. The method of claim **19**, wherein:

the second-type layer contact via structures vertically extend through each layer within the replaced first-tier alternating stack;

one of the second-type layer contact via structures is laterally surrounded by a vertical stack of first-tier annular insulating plates;

each of the first-tier annular insulating plates is laterally surrounded by a respective one of the first electrically conductive layers and comprises a respective inner cylindrical sidewall that contacts said one of the second-type layer contact via structures;

each of the second-type layer contact via structures is formed directly on an annular top surface of the respective one of the second electrically conductive layers; and

one of the second-type layer contact via structures is formed directly on one of second electrically conductive layers and vertically extends through and is electrically isolation from each second electrically conductive layer that underlies said one of the second electrically conductive layers.

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