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(54) **PACKAGE STRUCTURE INCLUDING INACTIVE ELEMENT, ASSEMBLY STRUCTURE AND METHOD OF MANUFACTURING THE SAME**

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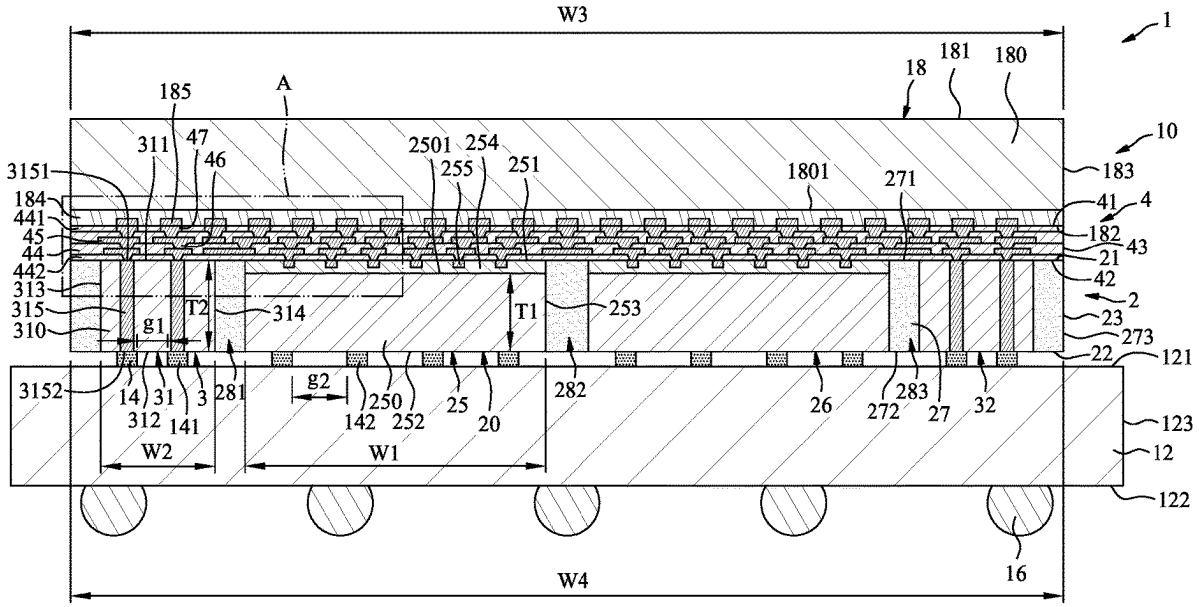
(57) **ABSTRACT**

A package structure, an assembly structure and a manufacturing method are provided. The package structure includes at least one semiconductor device, at least one inactive element and an encapsulant. The at least one inactive element is disposed around the at least one semiconductor device, and includes a main portion and at least one through via extending through the main portion. The encapsulant encapsulates the at least one semiconductor device and the at least one inactive element. A first surface of the encapsulant is substantially coplanar with a first surface of the at least one inactive element and a first surface of the at least one semiconductor device. A second surface of the encapsulant is substantially coplanar with a second surface of the at least one inactive element and a second surface of the at least one semiconductor device.



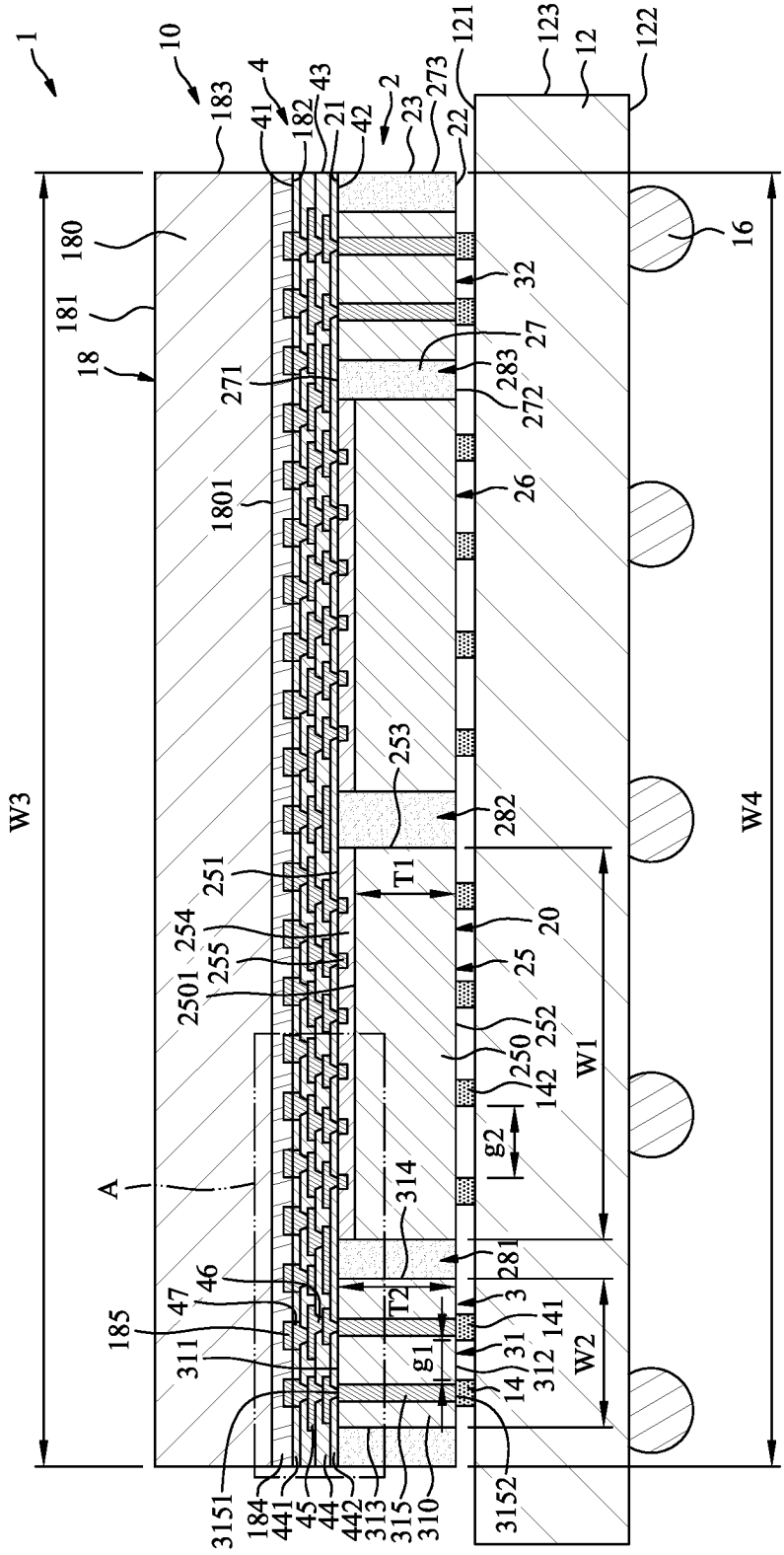

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FIG. 1

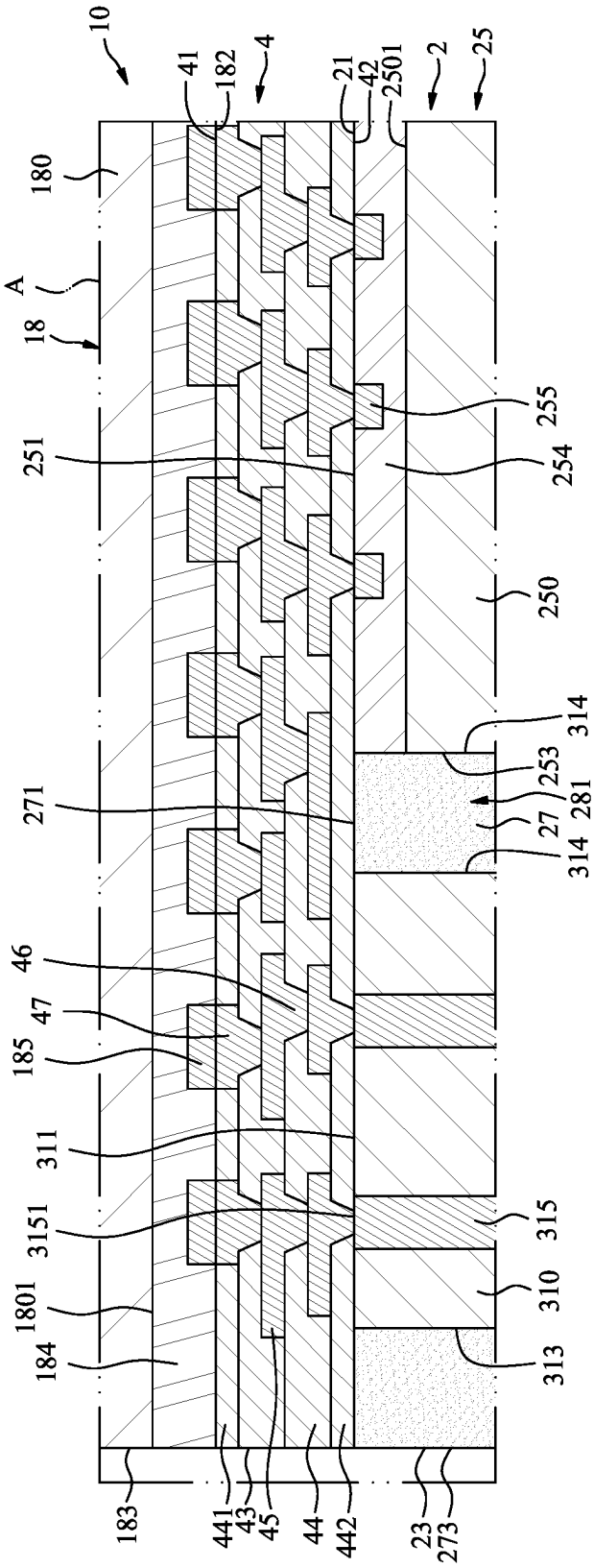
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FIG. 2

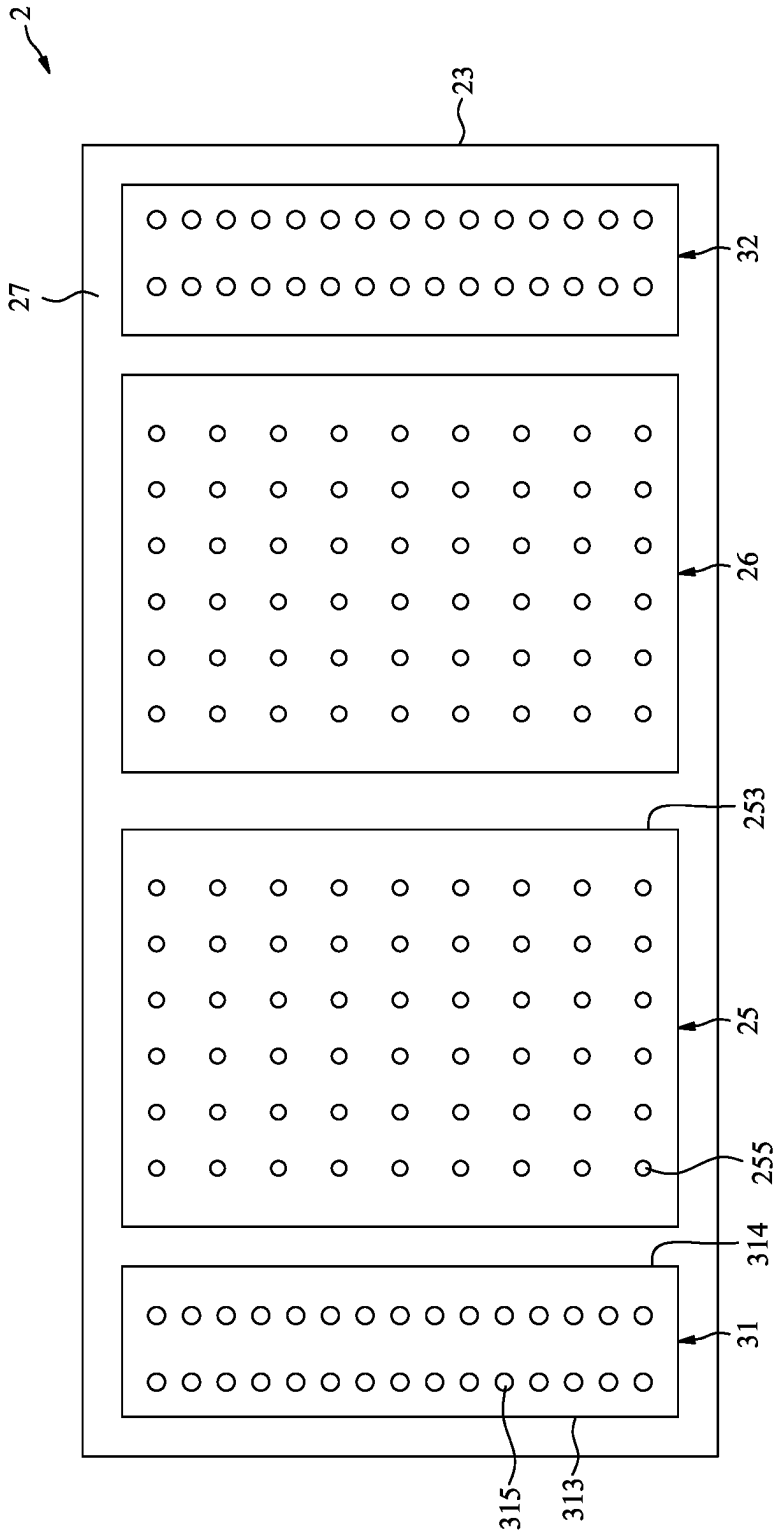

FIG. 3

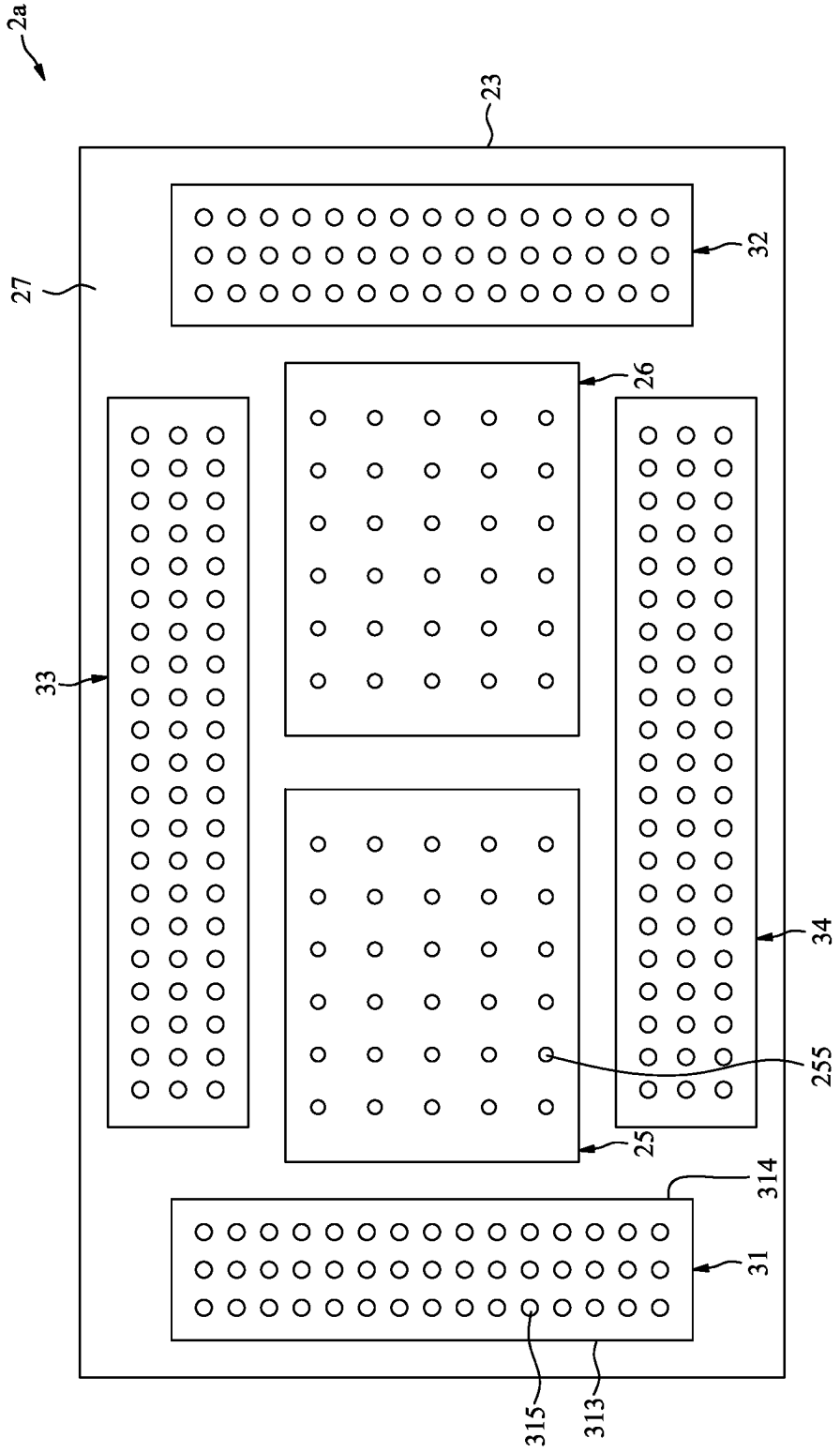

FIG. 4

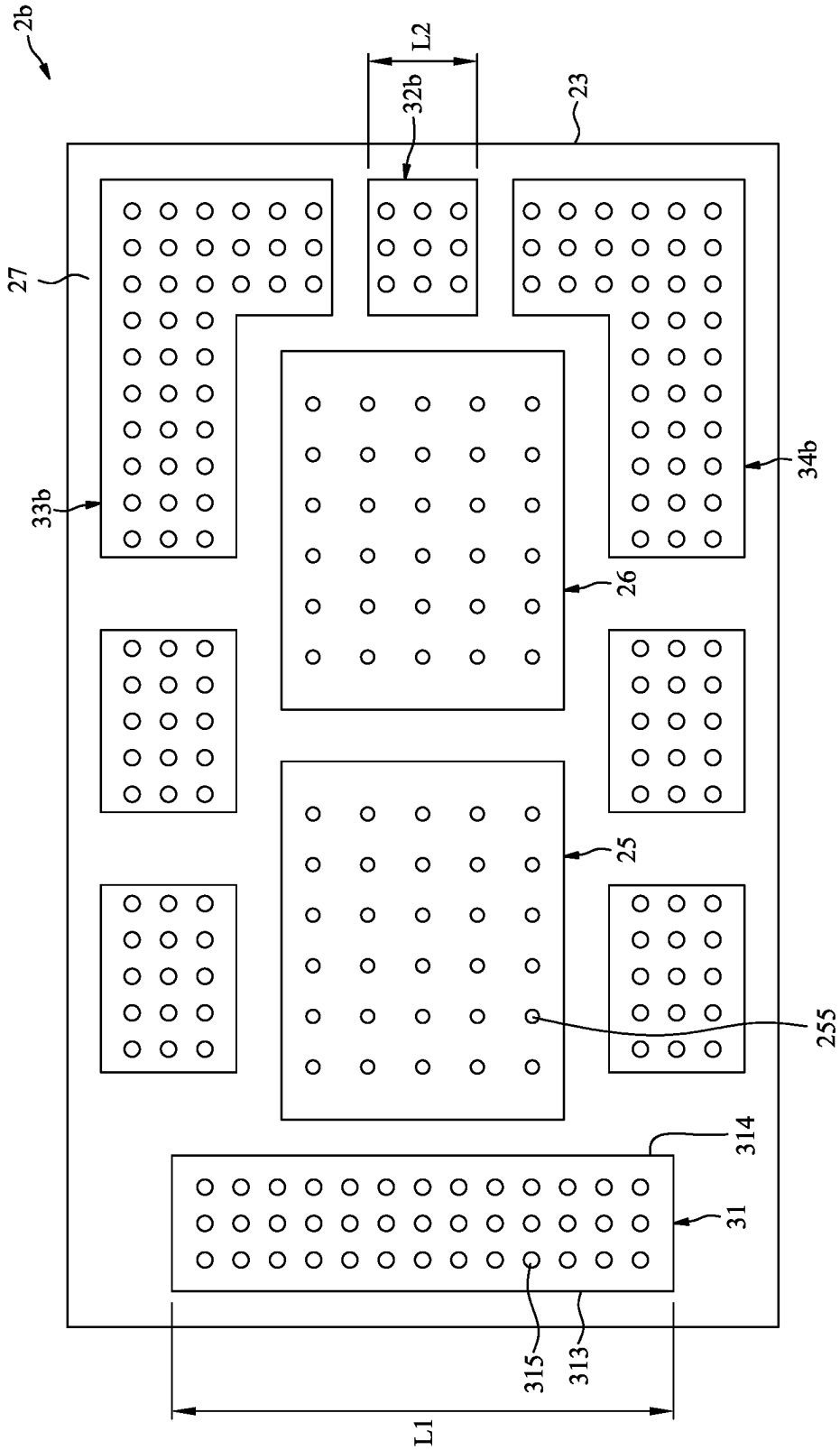

FIG. 5

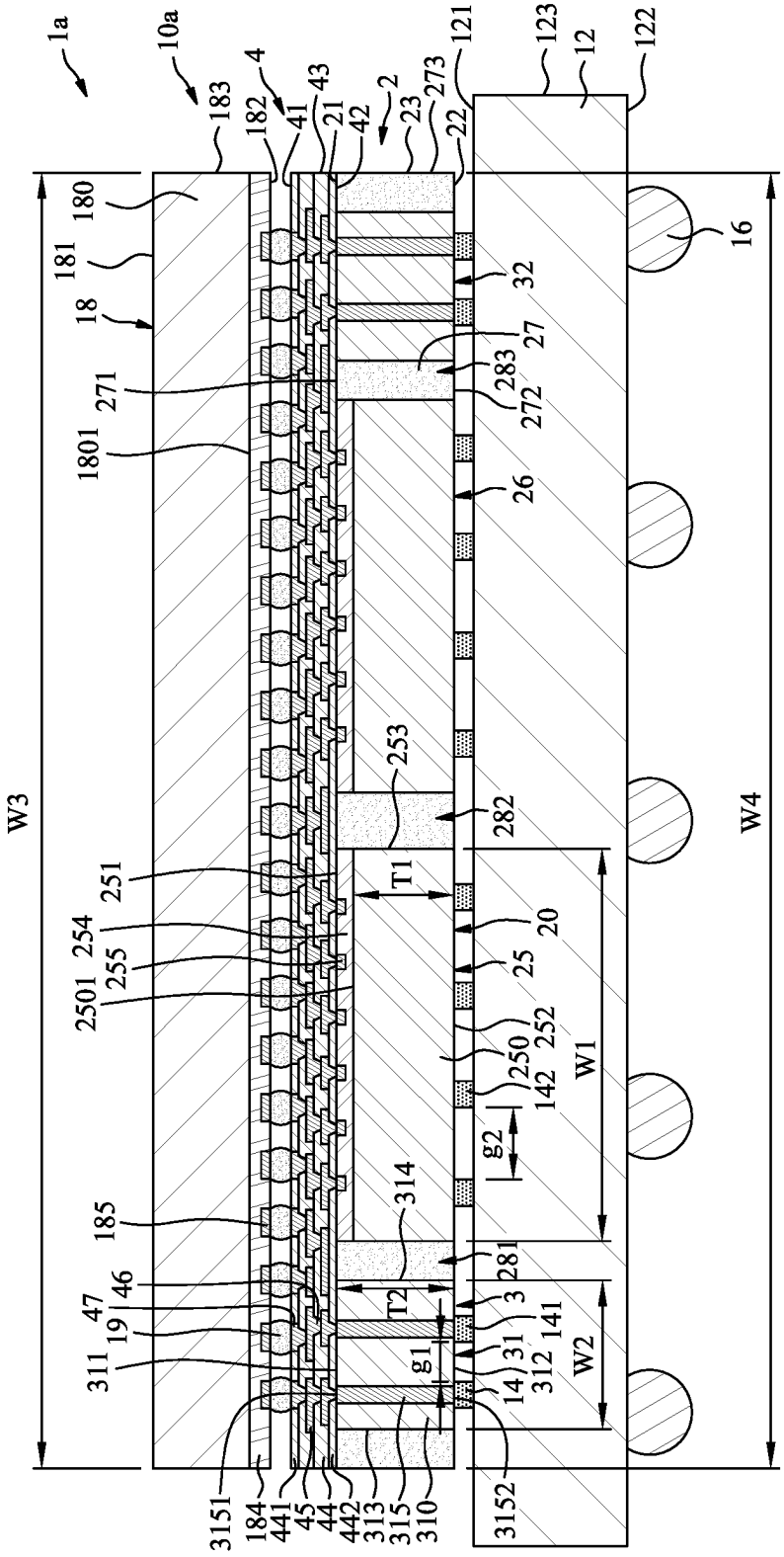
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FIG. 6

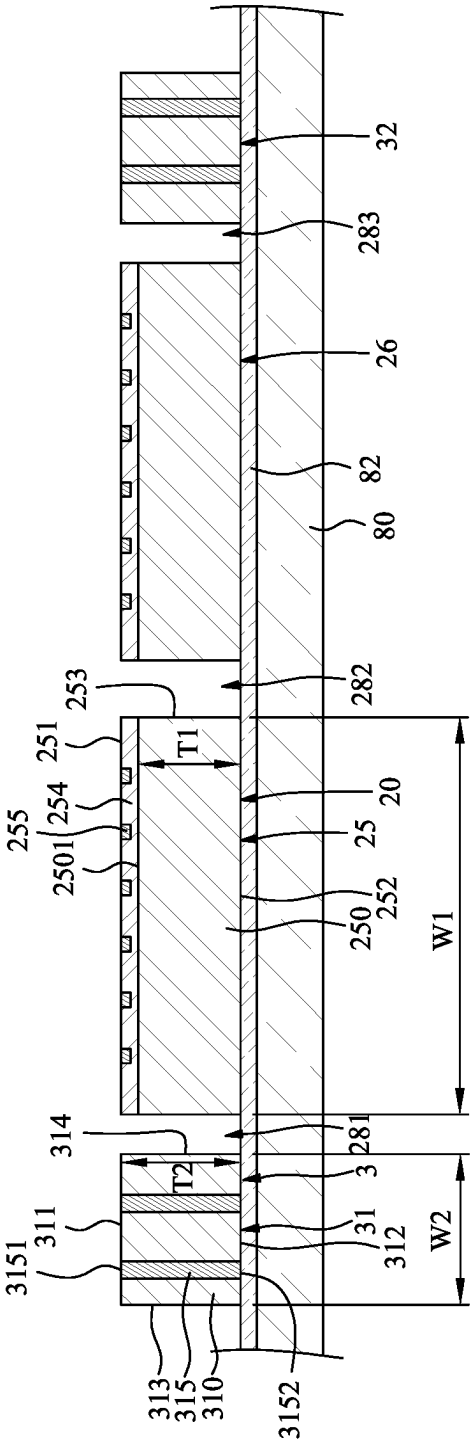
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FIG. 7

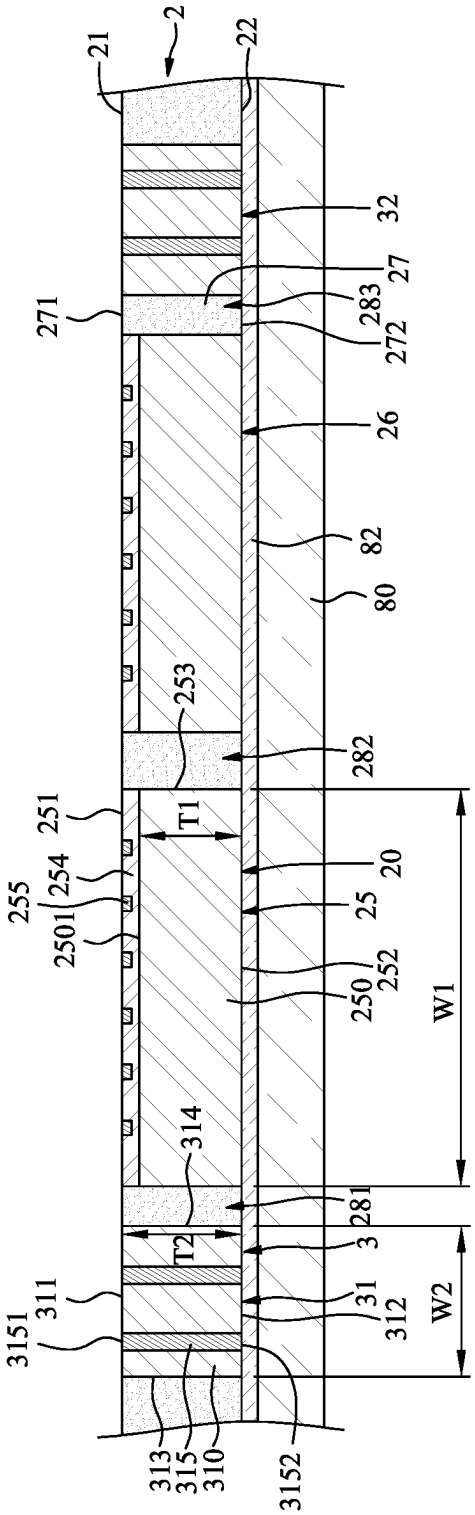
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FIG. 8

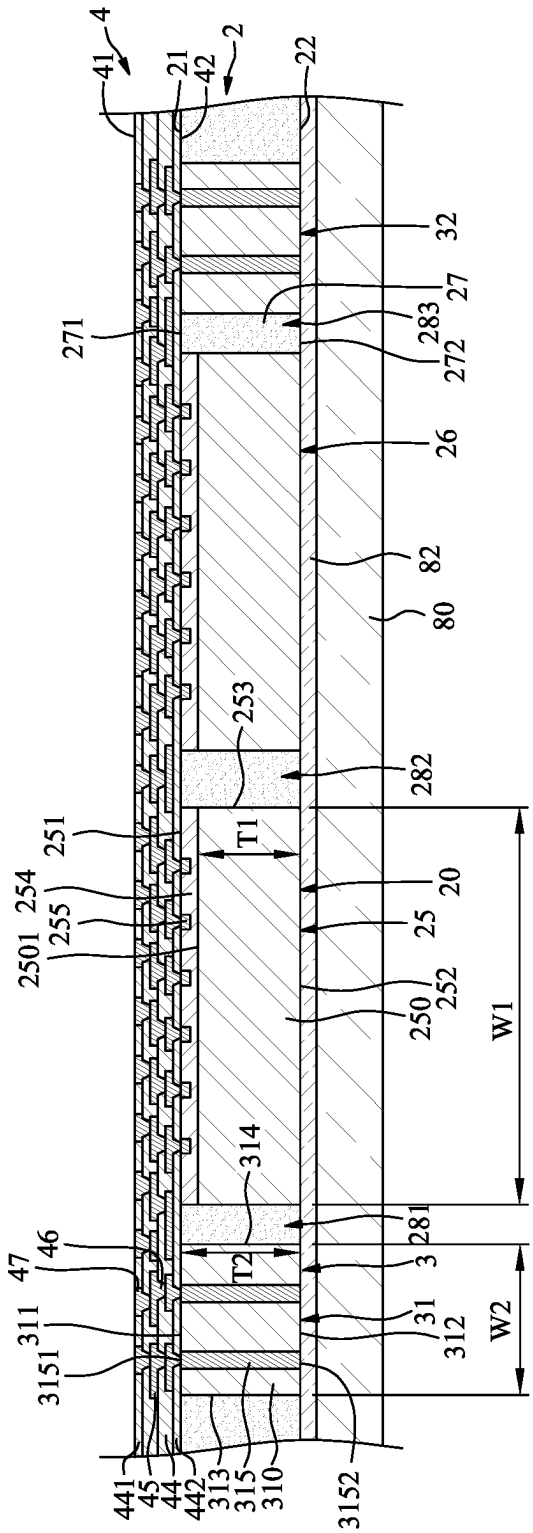
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FIG. 9

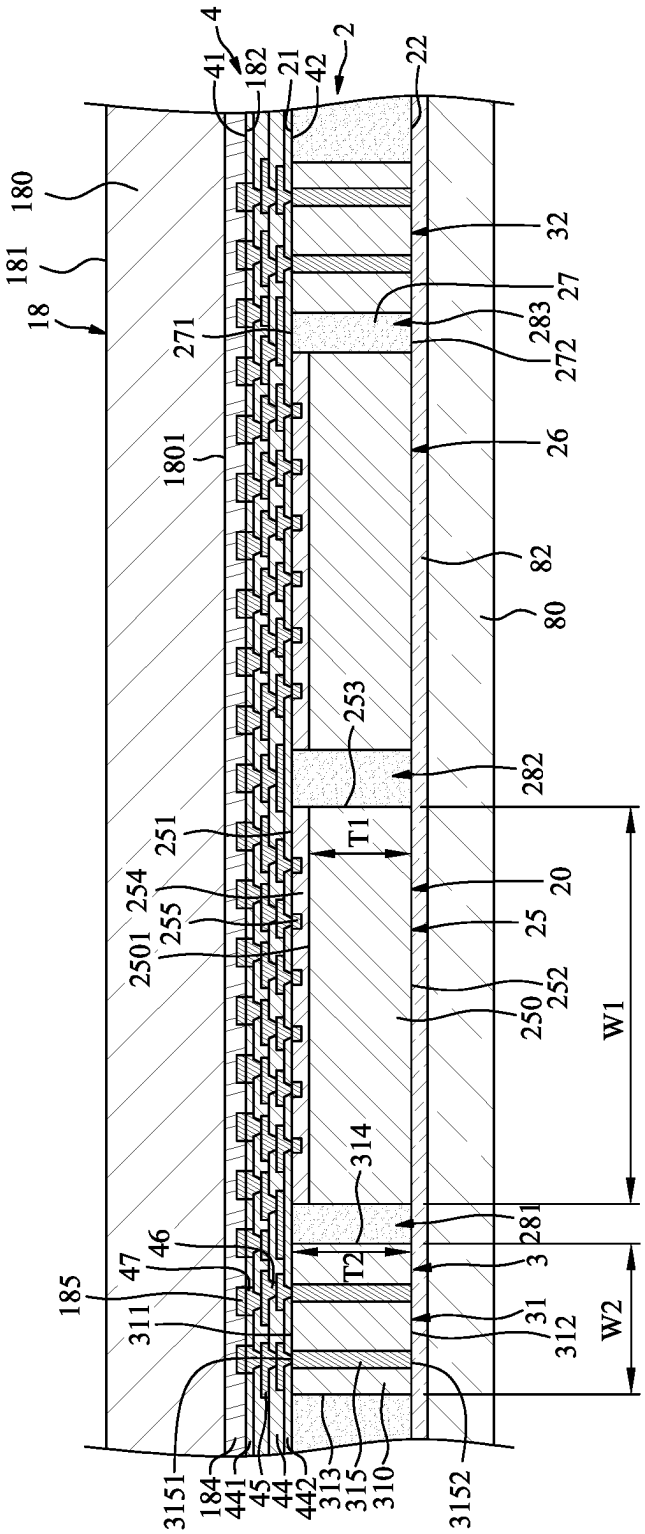
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FIG. 10

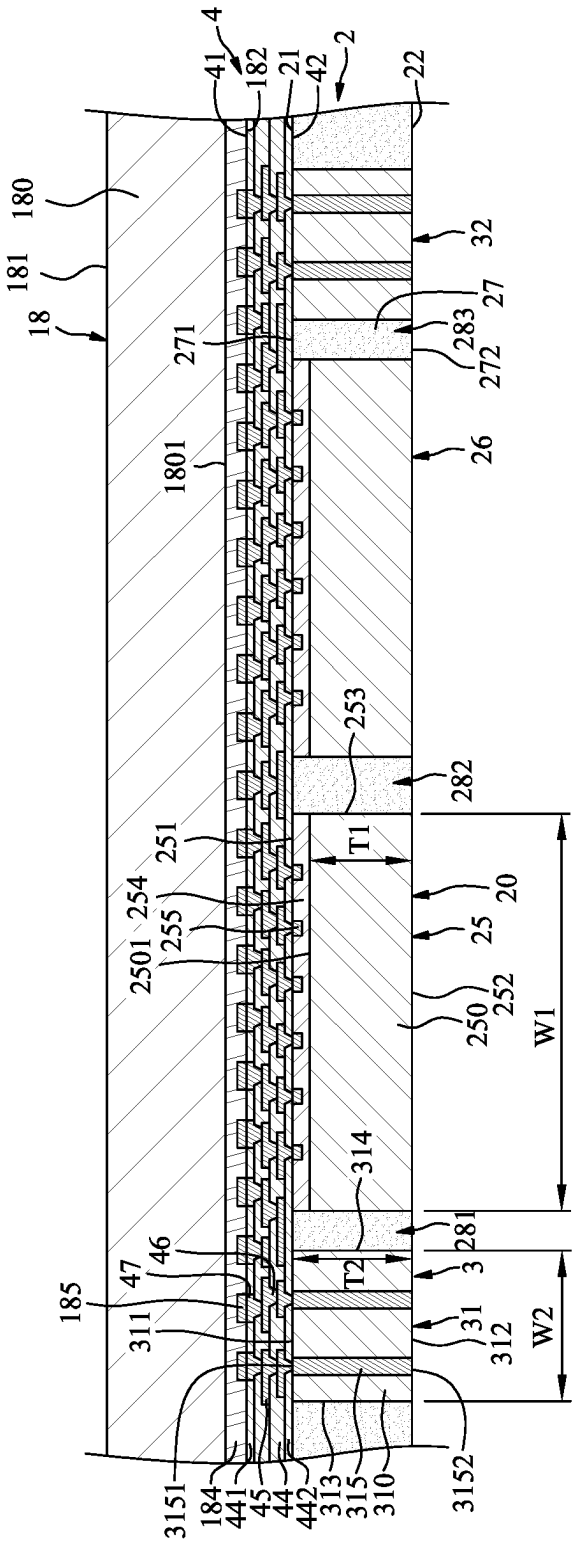
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FIG. 11

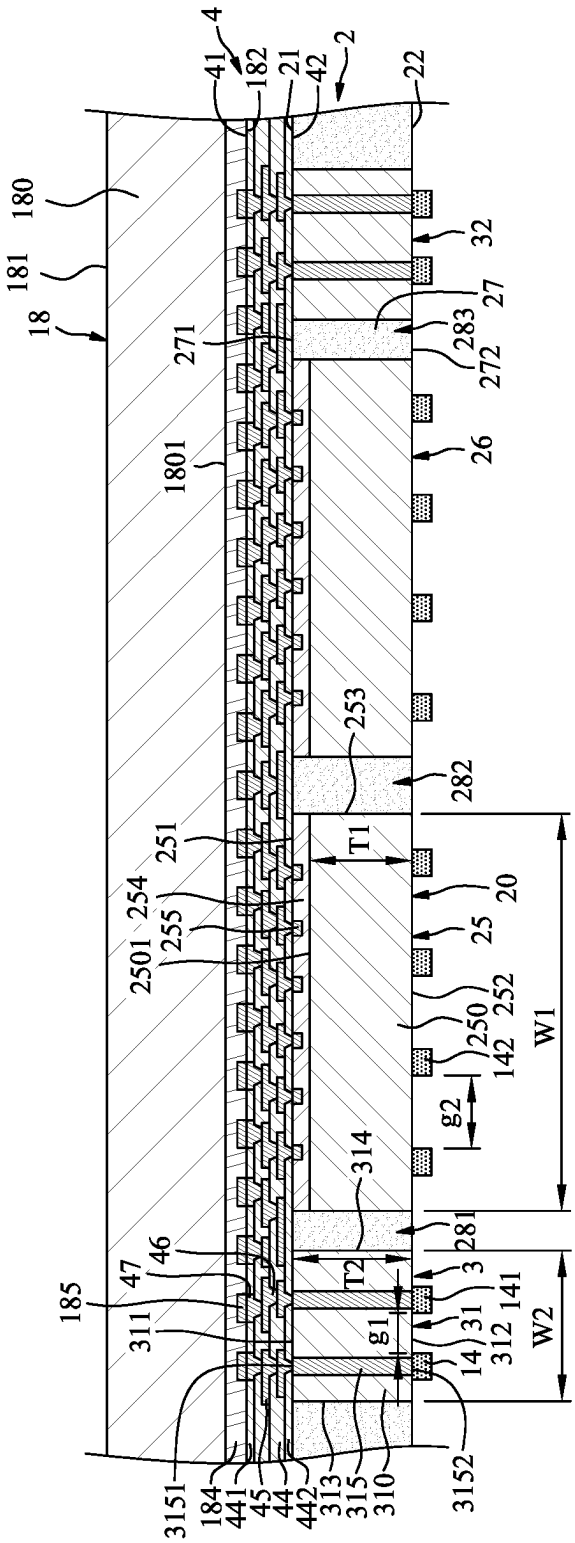
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FIG. 12

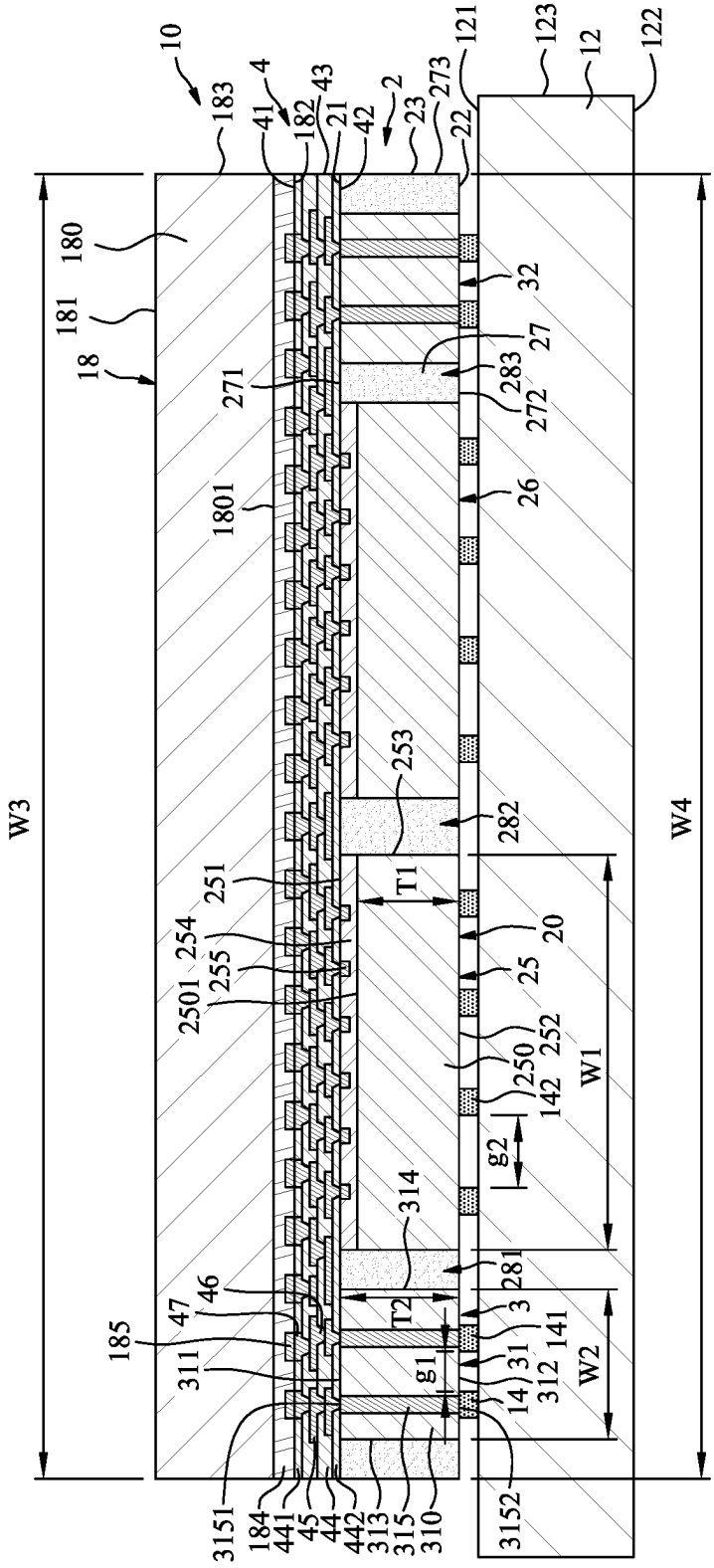
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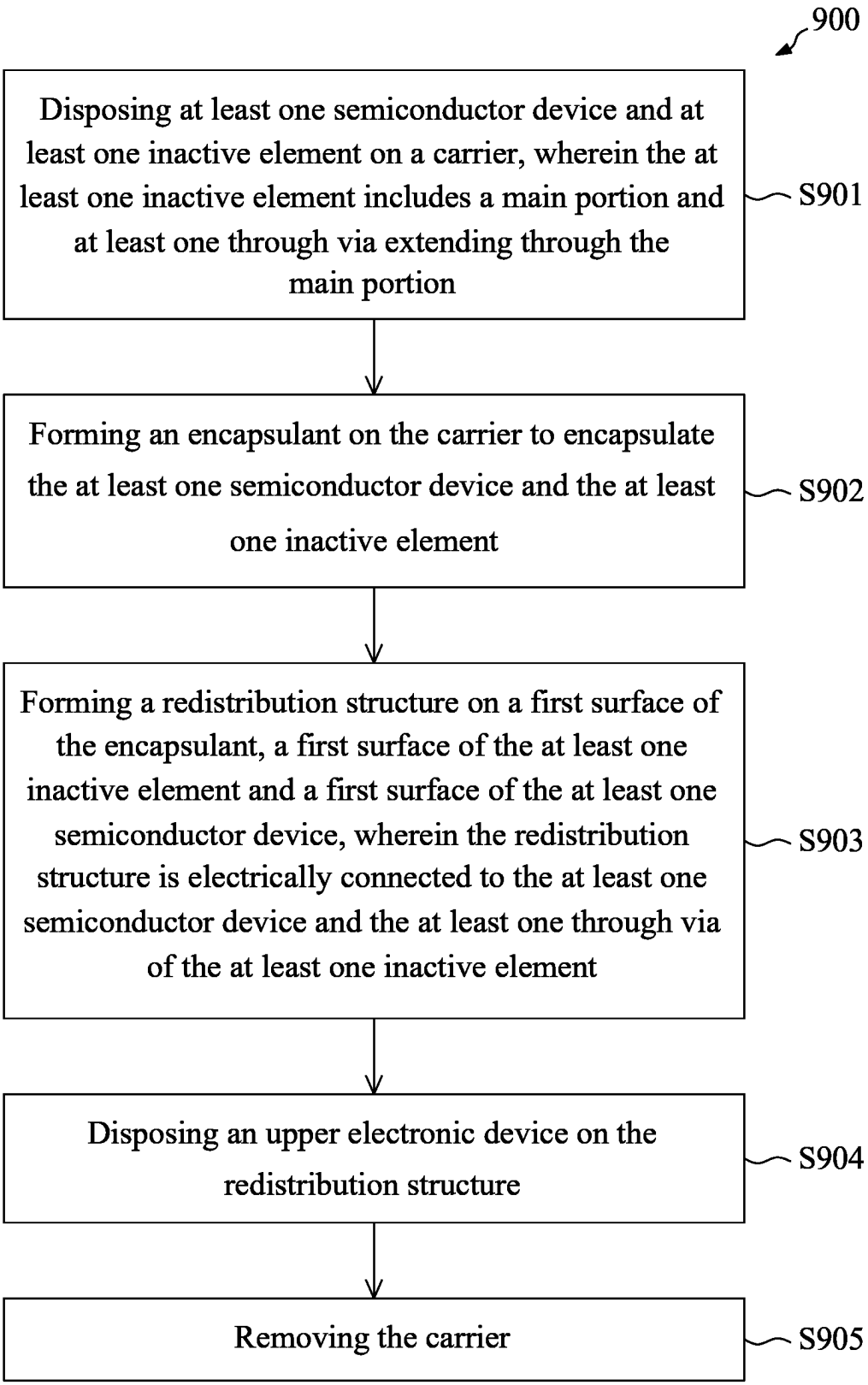
FIG. 13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Disposing at least one semiconductor device and at least one inactive element on a carrier, wherein the at least one inactive element includes a main portion and at least one through via extending through the main portion
S901
Forming an encapsulant on the carrier to encapsulate the at least one semiconductor device and the at least one inactive element
S902
Forming a redistribution structure on a first surface of the encapsulant, a first surface of the at least one inactive element and a first surface of the at least one semiconductor device, wherein the redistribution structure is electrically connected to the at least one semiconductor device and the at least one through via of the at least one inactive element
S903
Disposing an upper electronic device on the redistribution structure
S904
Removing the carrier
S905

FIG. 14

PACKAGE STRUCTURE INCLUDING INACTIVE ELEMENT, ASSEMBLY STRUCTURE AND METHOD OF MANUFACTURING THE SAME

TECHNICAL FIELD

[0001] The present disclosure relates to a package structure, an assembly structure and a method of manufacturing the same, and more particularly, to a package structure including at least one inactive element, an assembly structure including the package structure, and a method of manufacturing the same.

DISCUSSION OF THE BACKGROUND

[0002] Semiconductor electronic devices are widely used in various electronic applications, and their dimensions are constantly being reduced to meet the demands of current applications. However, scaling down semiconductor electronic devices presents several challenges that affect their final electrical characteristics, quality, cost, and yield. As semiconductor electronic devices become smaller, they require multifunctional and high-volume data processing capabilities. Consequently, there is an increasing need to enhance the integration level of semiconductor devices used in these electronic devices. However, due to the limitations of semiconductor integration technology, it is challenging to meet all the required functions with just a single semiconductor chip. To address this issue, semiconductor packages have been developed, which involve including multiple semiconductor chips.

[0003] This Discussion of the Background section is provided for background information only. The statements in this Discussion of the Background are not an admission that the subject matter disclosed herein constitutes prior art with respect to the present disclosure, and no part of this Discussion of the Background may be used as an admission that any part of this application constitutes prior art with respect to the present disclosure.

SUMMARY

[0004] One aspect of the present disclosure provides a package structure including at least one semiconductor device, at least one inactive element and an encapsulant. The at least one inactive element is disposed around the at least one semiconductor device, and includes a main portion and at least one through via extending through the main portion. The encapsulant encapsulates the at least one semiconductor device and the at least one inactive element. A first surface of the encapsulant is substantially coplanar with a first surface of the at least one inactive element and a first surface of the at least one semiconductor device. A second surface of the encapsulant is substantially coplanar with a second surface of the at least one inactive element and a second surface of the at least one semiconductor device.

[0005] Another aspect of the present disclosure provides an assembly structure including a substrate, a molded structure, a redistribution structure and an upper electronic device. The molded structure is disposed over and electrically connected to the substrate. The molded structure includes at least one semiconductor device, at least one inactive element and an encapsulant encapsulating the at least one semiconductor device and the at least one inactive element. The redistribution structure is disposed on and electrically connected to the molded structure. The upper electronic device is disposed over and electrically connected to the redistribution structure. The at least one inactive element is configured to provide a vertical conduction path between the upper electronic device and the substrate. The upper electronic device is not electrically connected to the substrate through the at least one semiconductor device.

[0006] Another aspect of the present disclosure provides a manufacturing method. The manufacturing method includes: disposing at least one semiconductor device and at least one inactive element on a carrier, wherein the at least one inactive element includes a main portion and at least one through via extending through the main portion; forming an encapsulant on the carrier to encapsulate the at least one semiconductor device and the at least one inactive element; forming a redistribution structure on a first surface of the encapsulant, a first surface of the at least one inactive element and a first surface of the at least one semiconductor device, wherein the redistribution structure is electrically connected to the at least one semiconductor device and the at least one through via of the at least one inactive element; disposing an upper electronic device on the redistribution structure; and removing the carrier.

[0007] The foregoing has outlined rather broadly the features and technical advantages of the present disclosure in order that the detailed description of the disclosure that follows may be better understood. Additional features and advantages of the disclosure will be described hereinafter, and form the subject of the claims of the disclosure. It should be appreciated by those skilled in the art that the conception and specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures or processes for carrying out the same purposes of the present disclosure. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the disclosure as set forth in the appended claims.

BRIEF DESCRIPTION OF THE DRA WINGS

[0008] A more complete understanding of the present disclosure may be derived by referring to the detailed description and claims when considered in connection with the Figures, where like reference numbers refer to similar elements throughout the Figures, and:

[0009] FIG. **1** is a schematic cross-sectional view of an assembly structure in accordance with some embodiments of the present disclosure.

[0010] FIG. **2** is an enlarged view of an area "A" of FIG. **1**.

[0011] FIG. **3** is a top view of the molded structure of the assembly structure of FIG. **1**.

[0012] FIG. **4** is a top view of a molded structure in accordance with some embodiments of the present disclosure.

[0013] FIG. **5** is a top view of a molded structure in accordance with some embodiments of the present disclosure.

[0014] FIG. **6** is a schematic cross-sectional view of an assembly structure in accordance with some embodiments of the present disclosure.

[0015] FIG. **7** to FIG. **13** illustrate various stages of a method of manufacturing an assembly structure, in accordance with some embodiments of the present disclosure.

[0016] FIG. **14** is a flowchart of a method of manufacturing an assembly structure, in accordance with some embodiments of the present disclosure.

DETAILED DESCRIPTION

[0017] Embodiments, or examples, of the disclosure illustrated in the drawings are now described using specific language. It shall be understood that no limitation of the scope of the disclosure is hereby intended. Any alteration or modification of the described embodiments, and any further applications of principles described in this document, are to be considered as normally occurring to one of ordinary skill in the art to which the disclosure relates. Reference numerals may be repeated throughout the embodiments, but this does not necessarily mean that feature(s) of one embodiment apply to another embodiment, even if they share the same reference numeral.

[0018] It shall be understood that, although the terms first, second, third, etc., may be used herein to describe various elements, components, regions, layers or sections, these elements, components, regions, layers or sections are not limited by these terms. Rather, these terms are merely used to distinguish one element, component, region, layer or section from another region, layer or section. Thus, a first element, component, region, layer or section discussed below could be termed a second element, component, region, layer or section without departing from the teachings of the present inventive concept.

[0019] The terminology used herein is for the purpose of describing particular example embodiments only and is not intended to be limited to the present inventive concept. As used herein, the singular forms "a," "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It shall be further understood that the terms "comprises" and "comprising," when used in this specification, point out the presence of stated features, integers, steps, operations, elements, or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, or groups thereof.

[0020] FIG. **1** is a schematic cross-sectional view of an assembly structure **1** in accordance with some embodiments of the present disclosure. FIG. **2** is an enlarged view of an area "A" of FIG. **1**. In some embodiments, the assembly structure **1** may be a semiconductor electronic device, a semiconductor electronic structure or a package structure. In some embodiments, the assembly structure **1** may include a package structure **10**, a substrate **12**, a plurality of bumps **14** and a plurality of external connectors **16**.

[0021] The substrate **12** may be a semiconductor substrate, and may include, for example, silicon (Si), doped silicon, germanium (Ge), silicon germanium (SiGe), silicon carbide (SiC), silicon germanium carbide (SiGeC), gallium (Ga), gallium arsenide (GaAs), indium (In), indium arsenide (InAs), indium phosphide (InP) or other IV-IV, III-V or II-VI semiconductor materials. In some embodiments, the substrate **12** may include a semiconductor-on-insulator substrate, such as a silicon-on-insulator (SOI) substrate, a silicon germanium-on-insulator (SGOI) substrate, or a germanium-on-insulator (GOI) substrate. In some embodiments, the substrate **12** may include organic material, glass, ceramic material or the like. For example, the substrate **12** may be made of a cured photoimageable dielectric (PID) material such as epoxy or polyimide (PI) including photoinitiators. For example, the substrate **12** may include a homogeneous material. For example, the material of the substrate **12** may include epoxy type FR5, FR4, Bismaleimide triazine (BT), print circuit board (PCB) material, Prepreg (PP), Ajinomoto build-up film (ABF) or other suitable materials.

[0022] The substrate **12** may have a first surface **121** (e.g., a top surface), a second surface **122** (e.g., a bottom surface) and a lateral surface **123**. The second surface **122** (e.g., the bottom surface) may be opposite to the first surface **121** (e.g., the top surface). The lateral surface **123** may extend between the first surface **121** (e.g., the top surface) and the second surface **122** (e.g., the bottom surface).

[0023] The package structure **10** may be disposed over the first surface **121** of the substrate **12**, and may be attached to the first surface **121** of the substrate **12** through the bumps **14**. The external connectors **16** may be disposed on the second surface **122** of the substrate **12** to provide electrical connections, for example, I/O connections, of the substrate **12**. Each of the external connector **16** may include a reflowable material such as a solder ball.

[0024] The package structure **10** may include a molded structure **2**, a redistribution structure **4** and an upper electronic device **18**. The molded structure **2** may be disposed over and electrically connected to the substrate **12**. The molded structure **2** may have a first surface **21** (e.g., a top surface), a second surface **22** (e.g., a bottom surface) and a lateral surface **23**. The second surface **22** (e.g., the bottom surface) may be opposite to the first surface **21** (e.g., the top surface). The lateral surface **23** may extend between the first surface **21** (e.g., the top surface) and the second surface **22** (e.g., the bottom surface).

[0025] The molded structure **2** may include at least one semiconductor device **20**, at least one inactive element **3** and an encapsulant **27**. The semiconductor device **20** may include a semiconductor die or a chip, such as a memory die (e.g., dynamic random access memory (DRAM) die, static random access memory (SRAM) die, etc.). The semiconductor device **20** may include a first semiconductor device **25** and a second semiconductor device **26** disposed side by side. In some embodiments, the size and the function of the first semiconductor device **25** may be same as the size and the function of the second semiconductor device **26**. The structure of the first semiconductor device **25** may be same as the structure of the second semiconductor device **26**. Both of the first semiconductor device **25** and the second semiconductor device **26** may be memory dice.

[0026] The first semiconductor device **25** may have a first surface **251** (e.g., a top surface or an active surface), a second surface **252** (e.g., a bottom surface or a backside surface) and a lateral surface **253**. The second surface **252** (e.g., the bottom surface) may be opposite to the first surface **251** (e.g., the top surface). The lateral surface **253** may extend between the first surface **251** (e.g., the top surface) and the second surface **252** (e.g., the bottom surface).

[0027] The first semiconductor device **25** may include a main portion **250** and an active circuit structure **254** disposed on a top surface **2501** of the main portion **250**. A material of the main portion **250** may include, for example, silicon (Si), doped silicon, germanium (Ge), silicon germanium (SiGe), silicon carbide (SiC), silicon germanium carbide (SiGeC), gallium (Ga), gallium arsenide (GaAs), indium (In), indium arsenide (InAs), indium phosphide (InP) or other IV-IV, III-V or II-VI semiconductor materials.

[0028] The active circuit structure **254** may include a plurality of dielectric layers, a plurality of circuit layers and a plurality of pads **255**. The dielectric layers may cover the circuit layers. The pads **255** may be electrically connected to the circuit layers, and embedded in the dielectric layers. The pads **255** may be exposed from the first surface **251** of the first semiconductor device **25**.

[0029] The inactive element **3** may be disposed around the semiconductor device **20** (including, e.g., the first semiconductor device **25** and the second semiconductor device **26**). The inactive element **3** may be also referred to as "a dummy die". The inactive element **3** may include a first inactive element **31** and a second inactive element **32** disposed around the first semiconductor device **25** and the second semiconductor device **26**. A structure of the first inactive element **31** may be same as or similar to a structure of the second inactive element **32**.

[0030] The first inactive element **31** may have a first surface **311** (e.g., a top surface), a second surface **312** (e.g., a bottom surface) and two lateral surfaces **313**, **314**. The second surface **312** (e.g., the bottom surface) may be opposite to the first surface **311** (e.g., the top surface). The lateral surfaces **313**, **314** may extend between the first surface **311** (e.g., the top surface) and the second surface **312** (e.g., the bottom surface).

[0031] The first inactive element **31** may include a main portion **310** and at least one through via **315** (or through silicon via (TSV)) extending through the main portion **310**. The main portion **310** may have a first surface **311** (e.g., a top surface), a second surface **312** (e.g., a bottom surface) and two lateral surfaces **313**, **314**. The second surface **312** (e.g., the bottom surface) may be opposite to the first surface **311** (e.g., the top surface). The lateral surfaces **313**, **314** may extend between the first surface **311** (e.g., the top surface) and the second surface **312** (e.g., the bottom surface). Thus, the first surface **311**, the second surface **312** and the lateral surfaces **313**, **314** of the first inactive element **31** may be the first surface **311**, the second surface **312** and the lateral surfaces **313**, **314** of the main portion **310**, respectively.

[0032] A material of the main portion **310** may include, for example, silicon (Si), doped silicon, germanium (Ge), silicon germanium (SiGe), silicon carbide (SiC), silicon germanium carbide (SiGeC), gallium (Ga), gallium arsenide (GaAs), indium (In), indium arsenide (InAs), indium phosphide (InP) or other IV-IV, III-V or II-VI semiconductor materials. In some embodiments, the material of the main portion **250** of the first semiconductor device **25** may be same as the material of the main portion **310** of the first inactive element **31**.

[0033] A width W**1** of the first semiconductor device **25** (or the main portion **250**) may be greater than a width W**2** of the first inactive element **31** (or the main portion **310**). A thickness T**1** of the main portion **250** of the first semiconductor device **25** may be less than a thickness T**2** of the main portion **310** of the first inactive element **31**.

[0034] The semiconductor device **20** (including, e.g., the first semiconductor device **25** and the second semiconductor device **26**) does not include a vertical conduction path in the main portion thereof. That is, the semiconductor device **20** (including, e.g., the first semiconductor device **25** and the second semiconductor device **26**) may be free of a vertical conduction path to the substrate **12**. For example, the first semiconductor device **25** does not include a vertical conduction path in the main portion **250** thereof.

[0035] The through via **315** of the first inactive element **31** may have a first surface **3151** (e.g., a top surface) and a second surface **3152** (e.g., a bottom surface) opposite to the first surface **3151** (e.g., the top surface). The first surface **3151** of the first through via **315** of the first inactive element **31** may be substantially coplanar with and exposed from the first surface **311** of the first inactive element **31**. The second surface **3152** of the through via **315** of the first inactive element **31** may be substantially coplanar with and exposed from the second surface **312** of the first inactive element **31**. That is, the through via **315** of the first inactive element **31** may extend from the first surface **311** of the main portion **310** to the second surface **312** of the main portion **310**.

[0036] Thus, the through via **315** of the first inactive element **31** may provide a vertical conduction path extending through the main portion **310** of the first inactive element **31**, and may be configured to transmit signals or power. Thus, the redistribution structure **4** and the upper electronic device **18** may be electrically connected to the substrate **12** through the through via **315** of the first inactive element **31** rather than through the semiconductor device **20** (including, e.g., the first semiconductor device **25** and the second semiconductor device **26**). There is no need to form a through via in the main portion (e.g., the main portion **250**) of the semiconductor device **20** (e.g., the first semiconductor device **25** and the second semiconductor device **26**).

[0037] In some embodiments, the inactive element **3** does not include a horizontal conduction path (e.g., a horizontal circuit layer) on the main portion thereof. For example, the first inactive element **31** does not include a horizontal conduction path (e.g., a horizontal circuit layer) on the main portion **310** thereof. There is no horizontal conduction path on the first surface **311** of the main portion **310** nor on the second surface **312** of the main portion **310**. The inactive element **3** only include the vertical conduction path.

[0038] The encapsulant **27** may encapsulate the semiconductor device **20** (including, e.g., the first semiconductor device **25** and the second semiconductor device **26**) and the inactive element **3** (including, e.g., the first inactive element **31** and the second inactive element **32**). For example, the encapsulant **27** may be disposed in a space **281** between the first semiconductor device **25** and the first inactive element **31**, a space **282** between the first semiconductor device **25** and the second semiconductor device **26**, and a space **283** between the second semiconductor device **26** and the second inactive element **32**. A material of the encapsulant **27** may include a molding compound with or without fillers.

[0039] The encapsulant **27** may have a first surface **271** (e.g., a top surface), a second surface **272** (e.g., a bottom surface) and a lateral surface **273**. The second surface **272** (e.g., the bottom surface) may be opposite to the first surface **271** (e.g., the top surface). The lateral surface **273** may extend between the first surface **271** (e.g., the top surface) and the second surface **272** (e.g., the bottom surface).

[0040] The first surface **271** of the encapsulant **27** may be substantially coplanar with or aligned with the first surface **311** of the first inactive element **31** and the first surface **251** of the first semiconductor device **25**. Thus, the first surface **21** of the molded structure **2** may include the first surface **271** of the encapsulant **27**, the first surface **311** of the first inactive element **31** and the first surface **251** of the first semiconductor device **25**. In addition, the second surface **272** of the encapsulant **27** may be substantially coplanar with or aligned with the second surface **312** of the first

inactive element **31** and the second surface **252** of the first semiconductor device **25**. Thus, the second surface **22** of the molded structure **2** may include the second surface **272** of the encapsulant **27**, the second surface **312** of the first inactive element **31** and the second surface **252** of the first semiconductor device **25**.

[0041] The redistribution structure **4** may be disposed on and electrically connected to the first surface **21** of the molded structure **2**. For example, the redistribution structure **4** may be disposed on the first surface **271** of the encapsulant **27**, the first surface **311** of the first inactive element **31** and the first surface **251** of the first semiconductor device **25**, and electrically connected to the first semiconductor device **25** and the through via **315** of the first inactive element **31**.

[0042] The redistribution structure **4** may be a fan-out structure. The redistribution structure **4** may have a first surface **41** (e.g., a top surface), a second surface **42** (e.g., a bottom surface) and a lateral surface **43**. The second surface **42** (e.g., the bottom surface) may be opposite to the first surface **41** (e.g., the top surface). The lateral surface **43** may extend between the first surface **41** (e.g., the top surface) and the second surface **42** (e.g., the bottom surface). The second surface **42** of the redistribution structure **4** may contact the first surface **21** of the molded structure **2** directly.

[0043] The redistribution structure **4** may include a plurality of dielectric layers **44**, a plurality of circuit layers **45**, a plurality of inner vias **46** and a plurality of pads **47**. The dielectric layers **44** may be made of a cured photoimageable dielectric (PID) material such as epoxy or polyimide (PI) including photoinitiators. The material of the dielectric layers **44** may be the same with each other. In some embodiments, the material of the topmost dielectric layer **441** may be different from the material of the other dielectric layers **44**. The topmost dielectric layer **441** may be a hybrid bonding (HB) dielectric layer, and may include SiO_2, SiCN and/or SiON. In some embodiments, the bottommost dielectric layer **442** may be omitted. The circuit layers **45** may be disposed on the first surface **21** of the molded structure **2** directly.

[0044] The circuit layers **45** may be covered by or embedded in the dielectric layers **44**. The circuit layers **45** may be fan-out circuit layers. The inner vias **46** may be embedded in the dielectric layers **44**, and may connect adjacent two of the circuit layers **45**. The inner vias **46** may taper toward the molded structure **2**. The pads **47** may be electrically connected to the circuit layers **45**, and embedded in the dielectric layers **44** (e.g., the topmost dielectric layer **441**). The pads **47** may be exposed from the first surface **41** of the redistribution structure **4**. Each of the pads **47** may be a hybrid bonding (HB) pad, and may include Cu or Al.

[0045] The upper electronic device **18** may be disposed over and electrically connected to the first surface **41** of the redistribution structure **4**. The upper electronic device **18** may be also disposed over and electrically connected to the first surface **21** of the molded structure **2** (including, e.g., the first surface **271** of the encapsulant **27**, the first surface **311** of the first inactive element **31** and the first surface **251** of the first semiconductor device **25**).

[0046] The upper electronic device **18** may include a semiconductor die or a chip, such as a signal processing die (e.g., digital signal processing (DSP) die), a logic die (e.g., application processor (AP), system-on-a-chip (SoC), central processing unit (CPU), graphics processing unit (GPU), microcontroller, etc.), a radio frequency (RF) die, a sensor die, a micro-electro-mechanical-system (MEMS) die, a front-end die (e.g., analog front-end (AFE) dies) or other active components.

[0047] The upper electronic device **18** may have a first surface **181** (e.g., a top surface or a backside surface), a second surface **182** (e.g., a bottom surface or an active surface) and a lateral surface **183**. The second surface **182** (e.g., the bottom surface) may be opposite to the first surface **181** (e.g., the top surface). The lateral surface **183** may extend between the first surface **181** (e.g., the top surface) and the second surface **182** (e.g., the bottom surface).

[0048] The upper electronic device **18** may include a main portion **180** and an active circuit structure **184** disposed on a bottom surface **1801** of the main portion **180**. A material of the main portion **180** may include, for example, silicon (Si), doped silicon, germanium (Ge), silicon germanium (SiGe), silicon carbide (SiC), silicon germanium carbide (SiGeC), gallium (Ga), gallium arsenide (GaAs), indium (In), indium arsenide (InAs), indium phosphide (InP) or other IV-IV, III-V or II-VI semiconductor materials.

[0049] The active circuit structure **184** may include a plurality of dielectric layers, a plurality of circuit layers and a plurality of pads **185**. The dielectric layers may cover the circuit layers. The pads **185** may be electrically connected to the circuit layers, and embedded in the dielectric layers. The pads **185** may be exposed from the second surface **182** of the upper electronic device **18**. The active circuit structure **184** may include a bottommost dielectric layer surrounding the pads **185**. The bottommost dielectric layer may be a hybrid bonding (HB) dielectric layer, and may include SiO_2, SiCN and/or SiON. Each of the pads **185** may be a hybrid bonding (HB) pad, and may include Cu or Al.

[0050] The upper electronic device **18** may be attached to and electrically connected to the first surface **41** of the redistribution structure **4** by hybrid bonding. That is, the second surface **182** of the upper electronic device **18** may contact the first surface **41** of the redistribution structure **4** directly. Thus, the active circuit structure **184** of the upper electronic device **18** may be attached to, may connect to and may contact the topmost dielectric layer **441** of the redistribution structure **4** directly. The pads **185** of the upper electronic device **18** may be attached to, may connect to and may contact the pads **47** of the redistribution structure **4** directly.

[0051] The size and the function of the upper electronic device **18** may be different from the size and the function of the semiconductor device **20** (including, e.g., the first semiconductor device **25** and the second semiconductor device **26**). A width W**3** of the upper electronic device **18** may be substantially equal to a width W**4** of the molded structure **2** or a width W**4** of the encapsulant **27**. The lateral surface **183** of the upper electronic device **18** may be substantially aligned with the lateral surface **23** of the molded structure **2** or the lateral surface **273** of the encapsulant **27**. The upper electronic device **18** may vertically overlap the inactive element **3** (including, e.g., the first inactive element **31** and the second inactive element **32**).

[0052] The bumps **14** may be disposed on the second surface **22** of the molded structure **2**. For example, the bumps **14** may include a plurality of first bumps **141** and a plurality of second bumps **142**. The first bumps **141** may be disposed on the second surface **3152** (e.g., the bottom surface) of the through via **315**. Thus, the first bumps **141** may physically connect and electrically connect the through

via **315** and the first surface **121** of the substrate **12**. The second bumps **142** may be disposed on the second surface of the semiconductor device **20** (e.g., the second surface **252** of the first semiconductor device **25**). Thus, second bumps **142** may connect the second surface of the semiconductor device **20** (e.g., the second surface **252** of the first semiconductor device **25**) and the first surface **121** of the substrate **12**. The second bumps **142** may have no electrical function, and may be dummy pads.

[0053] In some embodiments, the first bumps **141** and the second bumps **142** may be formed concurrently at a manufacturing stage. In some embodiments, the first bumps **141** and/or the second bumps **142** may include a reflowable material configured to control a gap between the molded structure **2** and the substrate **12** so as to prevent the molded structure **2** from tilting with respect to the substrate **12**. In addition, a first gap g**1** between adjacent two of the first bumps **141** may be less than a second gap g**2** between adjacent two of the second bumps **142**.

[0054] FIG. **3** is a top view of the molded structure **2** of the assembly structure **1** of FIG. **1**. The first inactive element **31** may include a plurality of rows of through vias **315**, for example, two rows of through vias **315**. The pads **255** of the first semiconductor device **25** may be arranged in an array. The size and the structure of the second semiconductor device **26** may be same as the size and the structure of the first semiconductor device **25**. The size and the structure of the second inactive element **32** may be same as the size and the structure of the first inactive element **31**. The second inactive element **32** and the first inactive element **31** may be disposed on opposite sides of the second semiconductor device **26** and the first semiconductor device **25**.

[0055] In the embodiment illustrated in FIG. **1** to FIG. **3**, the inactive element **3** (including, e.g., the first inactive element **31** and the second inactive element **32**) is configured to provide a vertical conduction path between the upper electronic device **18** and the substrate **12**. The upper electronic device **18** is not electrically connected to the substrate **12** through the semiconductor device **20** (e.g., the first semiconductor device **25** and the second semiconductor device **26**). It is not necessary to form a through via in the main portion (e.g., the main portion **250**) of the semiconductor device **20** (e.g., the first semiconductor device **25** and the second semiconductor device **26**). The vertical conduction path may be disposed outside the semiconductor device **20** (e.g., the first semiconductor device **25** and the second semiconductor device **26**). Thus, the design flexibility is increased, and the manufacturing cost is reduced.

[0056] In addition, the active surface of the semiconductor device **20** (e.g., the first surface **251** (or the active surface) of the first semiconductor device **25**) faces the active surface of the upper electronic device **18** (e.g., the first surface **181** of the upper electronic device **18**), thus, the upper electronic device **18** can read from and/or write to the semiconductor device **20** (e.g., the first semiconductor device **25**) quickly. Thus, the performance the package structure **10** can be improved.

[0057] FIG. **4** is a top view of a molded structure **2***a* in accordance with some embodiments of the present disclosure. The molded structure **2***a* may be similar to the molded structure **2** of FIG. **3**, and the differences are described as follows. The first inactive element **31** and the second inactive element **32** may include three rows of through vias **315**. The molded structure **2***a* may further include a third first inactive element **33** and a fourth inactive element **34**. The third first inactive element **33** and the fourth inactive element **34** may be disposed on opposite sides of the second semiconductor device **26** and the first semiconductor device **25**. The size and the structure of the third first inactive element **33** and the fourth inactive element **34** may be same as or similar to the size and the structure of the first inactive element **31** and the second inactive element **32**. The first inactive element **31**, the second inactive element **32**, the third first inactive element **33** and the fourth inactive element **34** may surround the second semiconductor device **26** and the first semiconductor device **25**.

[0058] FIG. **5** is a top view of a molded structure **2***b* in accordance with some embodiments of the present disclosure. The molded structure **2***b* may be similar to the molded structure **2***a* of FIG. **4**, and the differences are described as follows. A size of the first inactive element **31** may be different from and a size of the second inactive element **32***b* from the top view. For example, a length L**1** of the first inactive element **31** may be greater than a length L**2** of the second inactive element **32***b*. In addition, each of the third first inactive element **33***b* and the fourth inactive element **34***b* may be in an L shape, and may be disposed adjacent to or disposed around a corner of the second semiconductor device **26**.

[0059] FIG. **6** is a schematic cross-sectional view of an assembly structure **1***a* in accordance with some embodiments of the present disclosure. The assembly structure **1***a* may be similar to the assembly structure **1** of FIG. **1** except for the structure of the package structure **10***a*. In the package structure **10***a*, the second surface **182** of the upper electronic device **18** does not contact the first surface **41** of the redistribution structure **4**. The second surface **182** of the upper electronic device **18** is spaced apart from the first surface **41** of the redistribution structure **4**. The pads **185** of the upper electronic device **18** may be electrically connected to the pads **47** of the redistribution structure **4** through a plurality of solder materials **19**. The solder materials **19** may include a reflowable material such as AgSn. Thus, the upper electronic device **18** is electrically connected to the redistribution structure **4** through solder bonding instead of hybrid bonding. The pads **185** of the upper electronic device **18** and the pads **47** of the redistribution structure **4** may be solder bonding pads.

[0060] FIG. **7** to FIG. **13** illustrate various stages of a method of manufacturing an assembly structure **1**, in accordance with some embodiments of the present disclosure.

[0061] Referring to FIG. **7**, at least one semiconductor device **20** and at least one inactive element **3** may be disposed side by side on a carrier **80**. In some embodiments, the carrier **80** may include a release layer **82** on a surface thereof. The semiconductor device **20** and the inactive element **3** may be disposed on the release layer **82**. In some embodiments, the singulated semiconductor device **20** (e.g., the first semiconductor device **25** and the second semiconductor device **26**) and the singulated inactive element **3** (e.g., the first inactive element **31** and the second inactive element **32**) may be reconstructed or rearranged on the release layer **82** of the carrier **80**. In some embodiments, only known good dice, e.g., the known good semiconductor device **20** (e.g., the first semiconductor device **25** and the second semiconductor device **26**) and the known good inactive element **3** (e.g., the first inactive element **31** and the second inactive element **32**) are used.

[0062] In some embodiments, the size and the function of the first semiconductor device **25** may be same as the size and the function of the second semiconductor device **26**. Both of the first semiconductor device **25** and the second semiconductor device **26** may be memory dice.

[0063] The first semiconductor device **25** may have a first surface **251** (e.g., a top surface or an active surface), a second surface **252** (e.g., a bottom surface or a backside surface) and a lateral surface **253**. The second surface **252** (e.g., the bottom surface) may be opposite to the first surface **251** (e.g., the top surface). The lateral surface **253** may extend between the first surface **251** (e.g., the top surface) and the second surface **252** (e.g., the bottom surface).

[0064] The first semiconductor device **25** may include a main portion **250** and an active circuit structure **254** disposed on a top surface **2501** of the main portion **250**. The active circuit structure **254** may include a plurality of dielectric layers, a plurality of circuit layers and a plurality of pads **255**. The dielectric layers may cover the circuit layers. The pads **255** may be electrically connected to the circuit layers, and embedded in the dielectric layers. The pads **255** may be exposed from the first surface **251** of the first semiconductor device **25**. The active circuit structure **254** and the pads **255** may face up. The second surface **252** (e.g., the bottom surface) of the first semiconductor device **25** may contact the release layer **82** of the carrier **80**.

[0065] The inactive element **3** may include a first inactive element **31** and a second inactive element **32** disposed around the first semiconductor device **25** and the second semiconductor device **26**. A structure of the first inactive element **31** may be same as or similar to a structure of the second inactive element **32**.

[0066] The first inactive element **31** may have a first surface **311** (e.g., a top surface), a second surface **312** (e.g., a bottom surface) and two lateral surfaces **313**, **314**. The second surface **312** (e.g., the bottom surface) may be opposite to the first surface **311** (e.g., the top surface). The lateral surfaces **313**, **314** may extend between the first surface **311** (e.g., the top surface) and the second surface **312** (e.g., the bottom surface).

[0067] A space **281** may be formed between the first semiconductor device **25** and the first inactive element **31**. A space **282** may be formed between the first semiconductor device **25** and the second semiconductor device **26**. A space **283** may be formed between the second semiconductor device **26** and the second inactive element **32**.

[0068] The first inactive element **31** may include a main portion **310** and at least one through via **315** (or through silicon via (TSV)) extending through the main portion **310**. The main portion **310** may have a first surface **311** (e.g., a top surface), a second surface **312** (e.g., a bottom surface) and two lateral surfaces **313**, **314**. The second surface **312** (e.g., the bottom surface) may be opposite to the first surface **311** (e.g., the top surface). The lateral surfaces **313**, **314** may extend between the first surface **311** (e.g., the top surface) and the second surface **312** (e.g., the bottom surface). Thus, the first surface **311**, the second surface **312** and the lateral surfaces **313**, **314** of the first inactive element **31** may be the first surface **311**, the second surface **312** and the lateral surfaces **313**, **314** of the main portion **310**, respectively.

[0069] In some embodiments, the material of the main portion **250** of the first semiconductor device **25** may be same as the material of the main portion **310** of the first inactive element **31**.

[0070] A width W**1** of the first semiconductor device **25** (or the main portion **250**) may be greater than a width W**2** of the first inactive element **31** (or the main portion **310**). A thickness T**1** of the main portion **250** of the first semiconductor device **25** may be less than a thickness T**2** of the main portion **310** of the first inactive element **31**.

[0071] The semiconductor device **20** (including, e.g., the first semiconductor device **25** and the second semiconductor device **26**) does not include a vertical conduction path in the main portion thereof. For example, the first semiconductor device **25** does not include a vertical conduction path in the main portion **250** thereof.

[0072] The through via **315** of the first inactive element **31** may have a first surface **3151** (e.g., a top surface) and a second surface **3152** (e.g., a bottom surface) opposite to the first surface **3151** (e.g., the top surface). The first surface **3151** of the first through via **315** of the first inactive element **31** may be substantially coplanar with and exposed from the first surface **311** of the first inactive element **31**. The second surface **3152** of the through via **315** of the first inactive element **31** may be substantially coplanar with and exposed from the second surface **312** of the first inactive element **31**. That is, the through via **315** of the first inactive element **31** may extend from the first surface **311** of the main portion **310** to the second surface **312** of the main portion **310**.

[0073] In some embodiments, the inactive element **3** does not include a horizontal conduction path (e.g., a horizontal circuit layer) on the main portion thereof. For example, the first inactive element **31** does not include a horizontal conduction path (e.g., a horizontal circuit layer) on the main portion **310** thereof. There is no horizontal conduction path on the first surface **311** of the main portion **310** nor on the second surface **312** of the main portion **310**. The inactive element **3** only include the vertical conduction path. The second surface **312** of the inactive element **3** may contact the release layer **82** of the carrier **80**.

[0074] Referring to FIG. **8**, an encapsulant **27** may be formed on the release layer **82** of the carrier **80** to encapsulate the semiconductor device **20** (including, e.g., the first semiconductor device **25** and the second semiconductor device **26**) and the inactive element **3** (e.g., the first inactive element **31** and the second inactive element **32**). The encapsulant **27** may be disposed in the space **281**, the space **282** and the space **283**.

[0075] Then, a grinding process may be conducted to form a molded structure **2** on the carrier **80**. The molded structure **2** may include the semiconductor device **20**, the inactive element **3** and the encapsulant **27**. The molded structure **2** may have a first surface **21** (e.g., a top surface) and a second surface **22** (e.g., a bottom surface) opposite to the first surface **21** (e.g., the top surface).

[0076] The encapsulant **27** may have a first surface **271** (e.g., a top surface) and a second surface **272** (e.g., a bottom surface) opposite to the first surface **271** (e.g., the top surface). The first surface **271** of the encapsulant **27** may be substantially coplanar with or aligned with the first surface **311** of the first inactive element **31** and the first surface **251** of the first semiconductor device **25**. Thus, the first surface **21** of the molded structure **2** may include the first surface **271** of the encapsulant **27**, the first surface **311** of the first inactive element **31** and the first surface **251** of the first semiconductor device **25**. In addition, the second surface **272** of the encapsulant **27** may be substantially coplanar with or aligned with the second surface **312** of the first

inactive element **31** and the second surface **252** of the first semiconductor device **25**. Thus, the second surface **22** of the molded structure **2** may include the second surface **272** of the encapsulant **27**, the second surface **312** of the first inactive element **31** and the second surface **252** of the first semiconductor device **25**.

[0077] Referring to FIG. **9**, a redistribution structure **4** may be formed or disposed on the first surface **21** of the molded structure **2**. For example, the redistribution structure **4** may be formed or disposed on the first surface **271** of the encapsulant **27**, the first surface **311** of the first inactive element **31** and the first surface **251** of the first semiconductor device **25**. The redistribution structure **4** may be electrically connected to the semiconductor device **20** (e.g., the first semiconductor device **25** and the second semiconductor device **26**) and through via **315** of the inactive element **3** (e.g., the first inactive element **31** and the second inactive element **32**).

[0078] The redistribution structure **4** may be a fan-out structure. The redistribution structure **4** may have a first surface **41** (e.g., a top surface) and a second surface **42** (e.g., a bottom surface) opposite to the first surface **41** (e.g., the top surface). The second surface **42** of the redistribution structure **4** may contact the first surface **21** of the molded structure **2** directly.

[0079] The redistribution structure **4** may include a plurality of dielectric layers **44**, a plurality of circuit layers **45**, a plurality of inner vias **46** and a plurality of pads **47**. The material of the dielectric layers **44** may be the same with each other. In some embodiments, the material of the topmost dielectric layer **441** may be different from the material of the other dielectric layers **44**. The topmost dielectric layer **441** may be a hybrid bonding (HB) dielectric layer. In some embodiments, the bottommost dielectric layer **442** may be omitted. The circuit layers **45** may be disposed on the first surface **21** of the molded structure **2** directly.

[0080] The circuit layers **45** may be covered by or embedded in the dielectric layers **44**. The circuit layers **45** may be fan-out circuit layers. The inner vias **46** may be embedded in the dielectric layers **44**, and may connect adjacent two of the circuit layers **45**. The inner vias **46** may taper toward the molded structure **2**. The pads **47** may be electrically connected to the circuit layers **45**, and embedded in the dielectric layers **44** (e.g., the topmost dielectric layer **441**). The pads **47** may be exposed from the first surface **41** of the redistribution structure **4**. Each of the pads **47** may be a hybrid bonding (HB) pad.

[0081] Referring to FIG. **10**, an upper electronic device **18** may be disposed on and electrically connected to the first surface **41** of the redistribution structure **4**. The upper electronic device **18** may be in a wafer type, a panel type or a chip type. The upper electronic device **18** may have a first surface **181** (e.g., a top surface or a backside surface) and a second surface **182** (e.g., a bottom surface or an active surface) opposite to the first surface **181** (e.g., the top surface).

[0082] The upper electronic device **18** may include a main portion **180** and an active circuit structure **184** disposed on a bottom surface **1801** of the main portion **180**. The active circuit structure **184** may include a plurality of dielectric layers, a plurality of circuit layers and a plurality of pads **185**. The dielectric layers may cover the circuit layers. The pads **185** may be electrically connected to the circuit layers, and embedded in the dielectric layers. The pads **185** may be exposed from the second surface **182** of the upper electronic device **18**. The active circuit structure **184** may include a bottommost dielectric layer surrounding the pads **185**. The bottommost dielectric layer may be a hybrid bonding (HB) dielectric layer. Each of the pads **185** may be a hybrid bonding (HB) pad.

[0083] The upper electronic device **18** may be attached to and electrically connected to the first surface **41** of the redistribution structure **4** by hybrid bonding. That is, the second surface **182** of the upper electronic device **18** may contact the first surface **41** of the redistribution structure **4** directly. Thus, the active circuit structure **184** of the upper electronic device **18** may be attached to, may connect to and may contact the topmost dielectric layer **441** of the redistribution structure **4** directly. The pads **185** of the upper electronic device **18** may be attached to, may connect to and may contact the pads **47** of the redistribution structure **4** directly.

[0084] Referring to FIG. **11**, the release layer **82** and the carrier **80** may be removed from the molded structure **2**.

[0085] Referring to FIG. **12**, a plurality of bumps **14** may be formed or disposed on the second surface **22** of the molded structure **2**. For example, the bumps **14** may include a plurality of first bumps **141** and a plurality of second bumps **142**. The first bumps **141** may be formed or disposed on the second surface **3152** (e.g., the bottom surface) of the through via **315**. The second bumps **142** may be formed or disposed on the second surface of the semiconductor device **20** (e.g., the second surface **252** of the first semiconductor device **25**).

[0086] In some embodiments, the first bumps **141** and the second bumps **142** may be formed concurrently at a same stage. In some embodiments, the first bumps **141** and/or the second bumps **142** may include a reflowable material. In addition, a first gap g**1** between adjacent two first bumps **141** may be less than a second gap g**2** between adjacent two second bumps **142**. Alternatively, the first gap g**1** may be equal to the second gap g**2**.

[0087] Referring to FIG. **13**, the encapsulant **27**, the redistribution structure **4** and the upper electronic device **18** may be diced to form a package structure **10**. Thus, a lateral surface **183** of the upper electronic device **18** may be substantially aligned with a lateral surface **23** of the molded structure **2** (or a lateral surface **273** of the encapsulant **27**) and a lateral surface **43** of the redistribution structure **4**. A width W**3** of the upper electronic device **18** may be substantially equal to a width W**4** of the molded structure **2** or a width W**4** of the encapsulant **27**.

[0088] Then, the bumps **14** (e.g., the first bumps **141** and the second bumps) may be attached to a substrate **12**. Thus, the package structure **10** may be attached to the substrate **12** through the bumps **14** (e.g., the first bumps **141** and the second bumps).

[0089] Then, a plurality of external connectors **16** may be formed or disposed on a second surface **122** of the substrate **12** to provide electrical connections, for example, I/O connections, of the substrate **12**. Therefore, the assembly structure **1** of FIG. **1** is obtained.

[0090] FIG. **14** illustrates a flow chart of a method **900** of manufacturing an assembly structure **1** in accordance with some embodiments of the present disclosure.

[0091] In some embodiments, the method **900** may include a step S**901**, disposing at least one semiconductor device and at least one inactive element on a carrier, wherein

the at least one inactive element includes a main portion and at least one through via extending through the main portion. For example, as shown in FIG. **7**, at least one semiconductor device **20** (e.g., the second surface **252** of the first semiconductor device **25**) and at least one inactive element **3** (e.g., the first inactive element **31** and the second inactive element **32**) may be disposes on a carrier **80**. The inactive element **31** may include a main portion **310** and at least one through via **315** extending through the main portion **310**.

[0092] In some embodiments, the method **900** may include a step S**902**, forming an encapsulant on the carrier to encapsulate the at least one semiconductor device and the at least one inactive element. For example, as shown in FIG. **8**, an encapsulant **27** may be formed on the carrier **80** to encapsulate the at least one semiconductor device **20** (e.g., the second surface **252** of the first semiconductor device **25**) and the at least one inactive element **3** (e.g., the first inactive element **31** and the second inactive element **32**).

[0093] In some embodiments, the method **900** may include a step S**903**, forming a redistribution structure on a first surface of the encapsulant, a first surface of the at least one inactive element and a first surface of the at least one semiconductor device, wherein the redistribution structure is electrically connected to the at least one semiconductor device and the at least one through via of the at least one inactive element. For example, as shown in FIG. **9**, a redistribution structure **4** may be formed on a first surface **271** of the encapsulant **27**, a first surface **311** of the at least one inactive element **31** and a first surface **251** of the at least one semiconductor device **25**. The redistribution structure **4** may be electrically connected to the at least one semiconductor device **25** and the at least one through via **315** of the at least one inactive element **31**.

[0094] In some embodiments, the method **900** may include a step S**904**, disposing an upper electronic device on the redistribution structure. For example, as shown in FIG. **10**, an upper electronic device **18** may be disposed on the redistribution structure **4**.

[0095] In some embodiments, the method **900** may include a step S**905**, disposing an upper electronic device on the redistribution structure. For example, as shown in FIG. **11**, the carrier **80** may be removed.

[0096] One aspect of the present disclosure provides an electronic device including a first semiconductor chip, a second semiconductor chip and a third semiconductor chip. The second semiconductor chip is stacked on the first semiconductor chip, and is electrically connected to the first semiconductor chip by hybrid bonding. The third semiconductor chip is stacked on the second semiconductor chip, and is electrically connected to the second semiconductor chip through a plurality of bumps.

[0097] Another aspect of the present disclosure provides an electronic device including a first assembly and a second assembly. The first assembly includes a first semiconductor chip and a second semiconductor chip stacked on the first semiconductor chip and electrically connected to the first semiconductor chip by hybrid bonding. The second assembly includes a third semiconductor chip and a fourth semiconductor chip stacked on the third semiconductor chip and electrically connected to the third semiconductor chip by hybrid bonding. The second assembly is electrically connected to the first assembly through a plurality of bumps.

[0098] Another aspect of the present disclosure provides a manufacturing method. The manufacturing method includes providing a first assembly including a first semiconductor chip and a second semiconductor chip stacked on the first semiconductor chip and electrically connected to the first semiconductor chip by hybrid bonding; providing a second assembly including a third semiconductor chip and a fourth semiconductor chip stacked on the third semiconductor chip and electrically connected to the third semiconductor chip by hybrid bonding; and electrically connecting the second assembly to the first assembly through a plurality of bumps.

[0099] Although the present disclosure and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the disclosure as defined by the appended claims. For example, many of the processes discussed above can be implemented in different methodologies and replaced by other processes, or a combination thereof.

[0100] Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, and composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the present disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present disclosure. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.

What is claimed is:

1. A package structure, comprising:

at least one semiconductor device;

at least one inactive element disposed around the at least one semiconductor device, and including a main portion and at least one through via extending through the main portion; and

an encapsulant encapsulating the at least one semiconductor device and the at least one inactive element, wherein a first surface of the encapsulant is substantially coplanar with a first surface of the at least one inactive element and a first surface of the at least one semiconductor device, and a second surface of the encapsulant is substantially coplanar with a second surface of the at least one inactive element and a second surface of the at least one semiconductor device.

2. The package structure of claim **1**, wherein a width of the at least one semiconductor device is greater than a width of the at least one inactive element.

3. The package structure of claim **1**, wherein the at least one semiconductor device include a main portion and an active circuit structure disposed on the main portion, wherein a thickness of the main portion of the at least one semiconductor device is less than a thickness of the main portion of the at least one inactive element.

4. The package structure of claim **3**, wherein a material of the main portion of the at least one semiconductor device is same as a material of the main portion of the at least one inactive element.

5. The package structure of claim **3**, wherein the active circuit structure includes at least one pad exposed from the first surface of the at least one semiconductor device.

6. The package structure of claim **3**, wherein the at least one semiconductor device does not include a vertical conduction path in the main portion of the at least one semiconductor device.

7. The package structure of claim **1**, wherein the at least one inactive element does not include a horizontal conduction path on the main portion of the at least one inactive element.

8. The package structure of claim **1**, wherein a first surface of the at least one through via of the at least one inactive element is exposed from the first surface of the at least one inactive element, and a second surface of the at least one through via of the at least one inactive element is exposed from the second surface of the at least one inactive element.

9. The package structure of claim **1**, wherein the at least one semiconductor device includes a first semiconductor device and a second semiconductor device disposed side by side, and the at least one inactive element includes a first inactive element and a second inactive element disposed around the first semiconductor device and the second semiconductor device.

10. The package structure of claim **9**, wherein the encapsulant is disposed in a space between the first semiconductor device and the first inactive element, a space between the first semiconductor device and the second semiconductor device, and a space between the second semiconductor device and the second inactive element.

11. The package structure of claim **1**, further comprising:

a redistribution structure disposed on the first surface of the encapsulant, the first surface of the at least one inactive element and the first surface of the at least one semiconductor device, and electrically connected to the at least one semiconductor device and the at least one through via of the at least one inactive element.

12. The package structure of package structure of claim **1**, further comprising:

an upper electronic device disposed over the first surface of the encapsulant, the first surface of the at least one inactive element and the first surface of the at least one semiconductor device, and electrically connected to the at least one semiconductor device and the at least one through via of the at least one inactive element.

13. The package structure of claim **12**, wherein a lateral surface of the upper electronic device is substantially aligned with a lateral surface of the encapsulant.

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