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(54) **SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SEMICONDUCTOR DEVICE**

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H10D 86/01 (2025.01)
H10D 86/60 (2025.01)
H10K 59/121 (2023.01)

(52) **U.S. Cl.**
CPC ***H10D 86/441*** (2025.01); ***H10D 86/021*** (2025.01); ***H10D 86/451*** (2025.01); ***H10D 86/60*** (2025.01); *H10K 59/1213* (2023.02)

(57) **ABSTRACT**

A semiconductor device (**10**) including a transistor having a minute size is provided. The semiconductor device includes a first transistor (**100**) and a second transistor (**200**). The first transistor includes a first conductive layer (**112***a*), a first insulating layer (**110**) over the first conductive layer, a second insulating layer (**120**) over the first insulating layer, a second conductive layer (**112***b*) over the second insulating layer, a first semiconductor layer (**108**), a third insulating layer (**106**), and a third conductive layer (**104**). The first insulating layer, the second insulating layer, and the second conductive layer have an opening reaching the first conductive layer. The first semiconductor layer is in contact with a top surface and a side surface of the second conductive layer, a side surface of the first insulating layer, the second insulating layer, and atop surface of the first conductive layer. The third insulating layer is provided over the first semiconductor layer. The third conductive layer is provided over the third insulating layer. The second transistor includes a second oxide semiconductor layer (**208**) over the second insulating layer, the third insulating layer over the second semiconductor layer, and a fourth conductive layer (**204**) including a region overlapping with the second semiconductor layer with the third insulating layer therebetween.

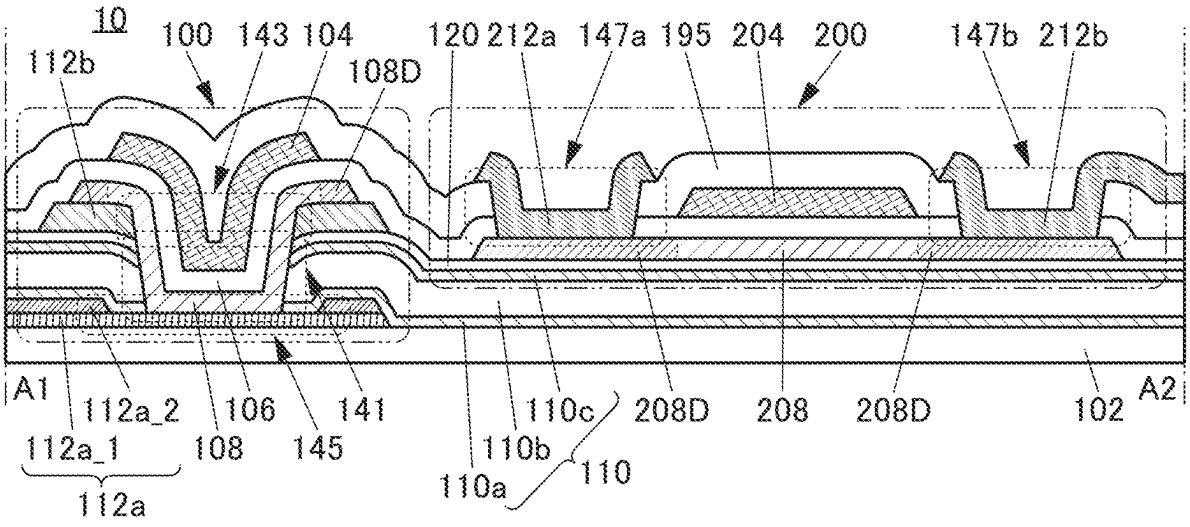


FIG. 1A

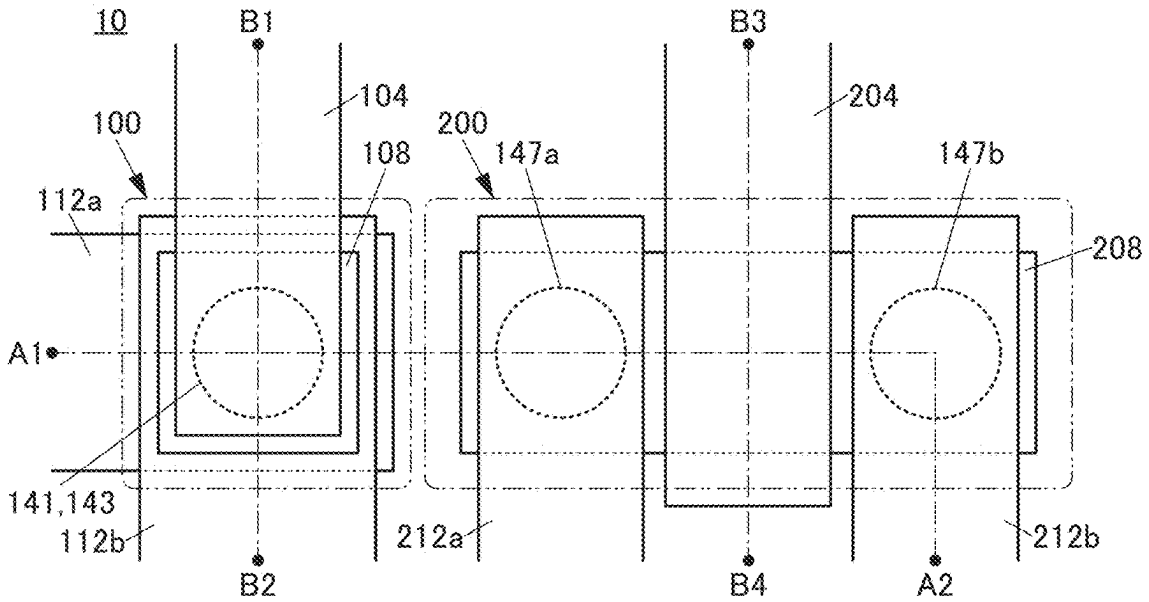


FIG. 1B

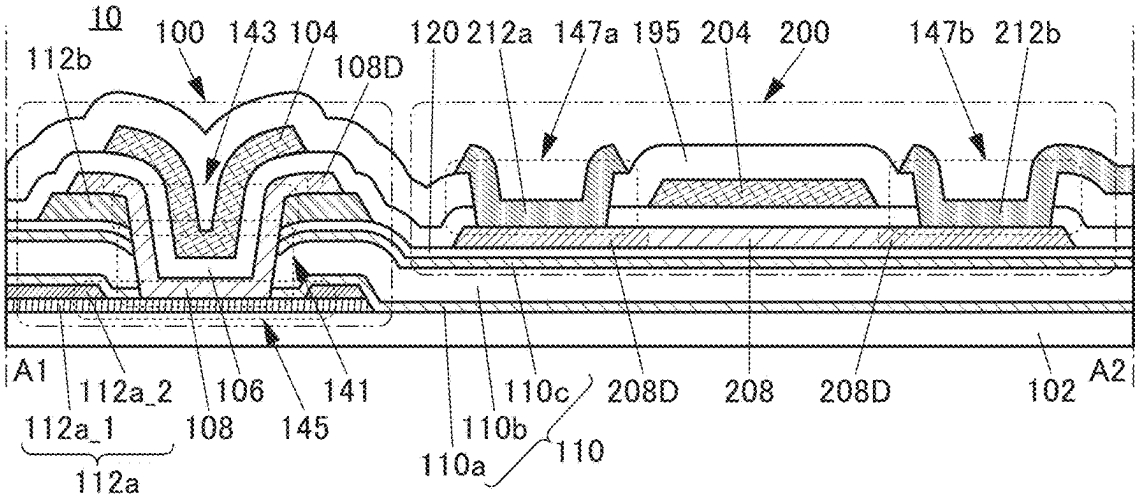


FIG. 1C

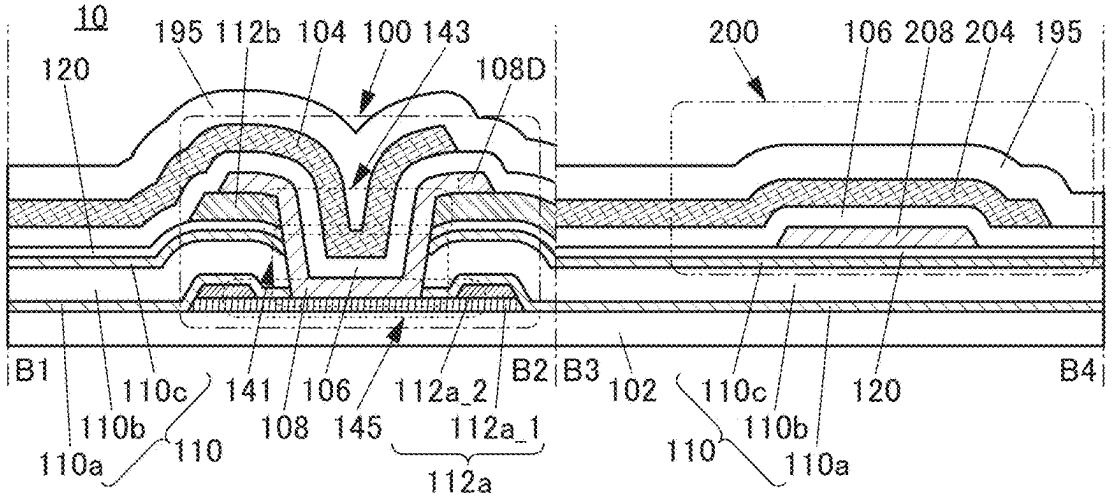


FIG. 2A

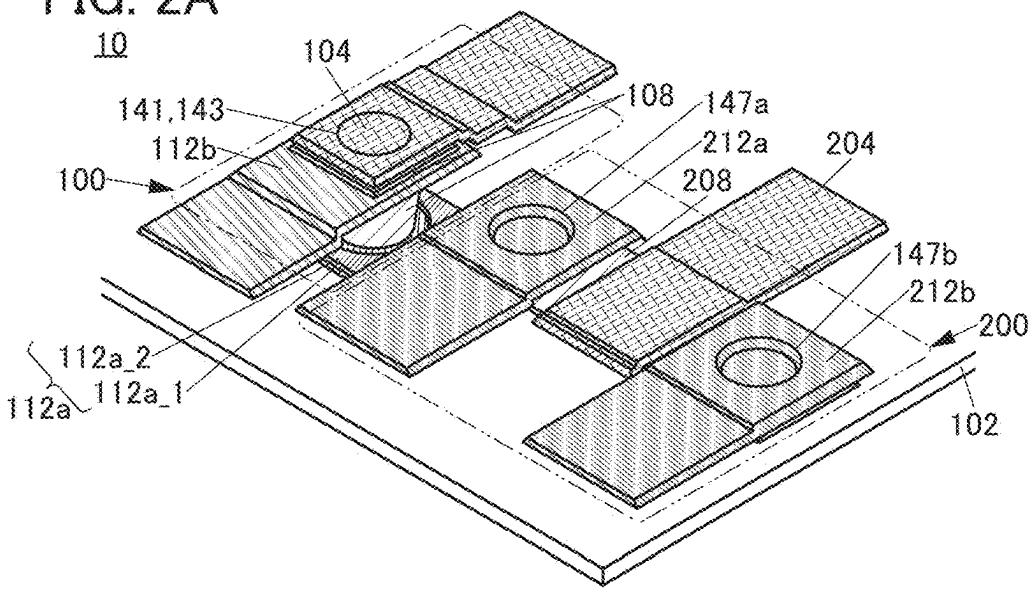


FIG. 2B

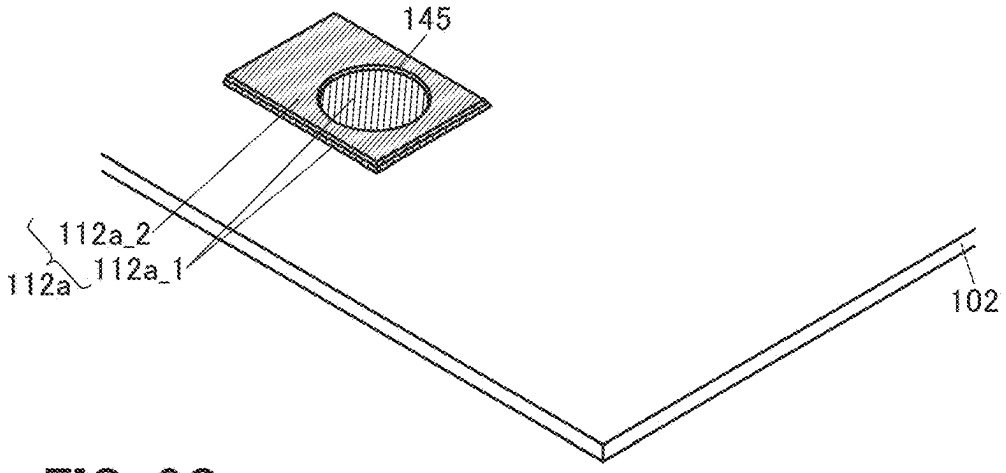


FIG. 2C

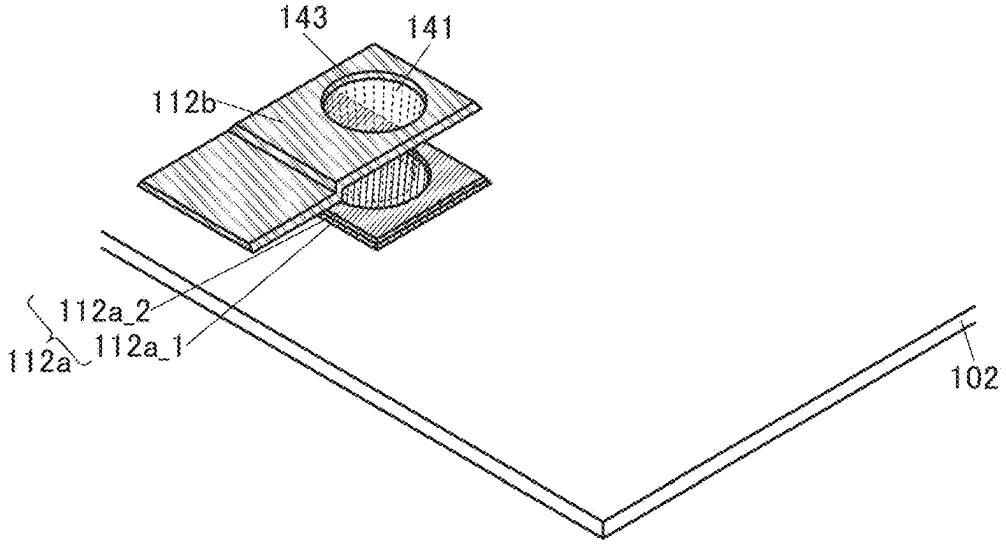


FIG. 3A

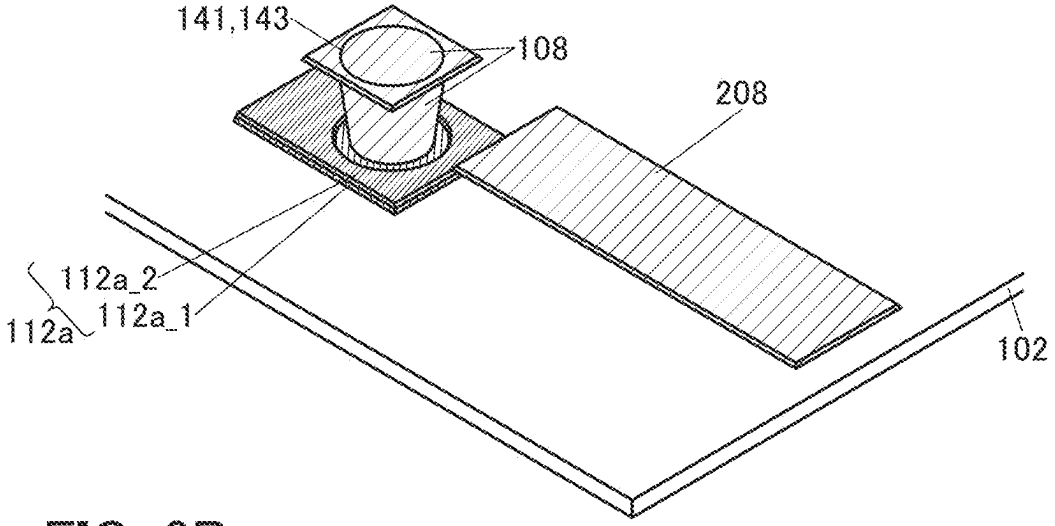

141,143
108
208
112a_2
112a_1
112a
102

FIG. 3B

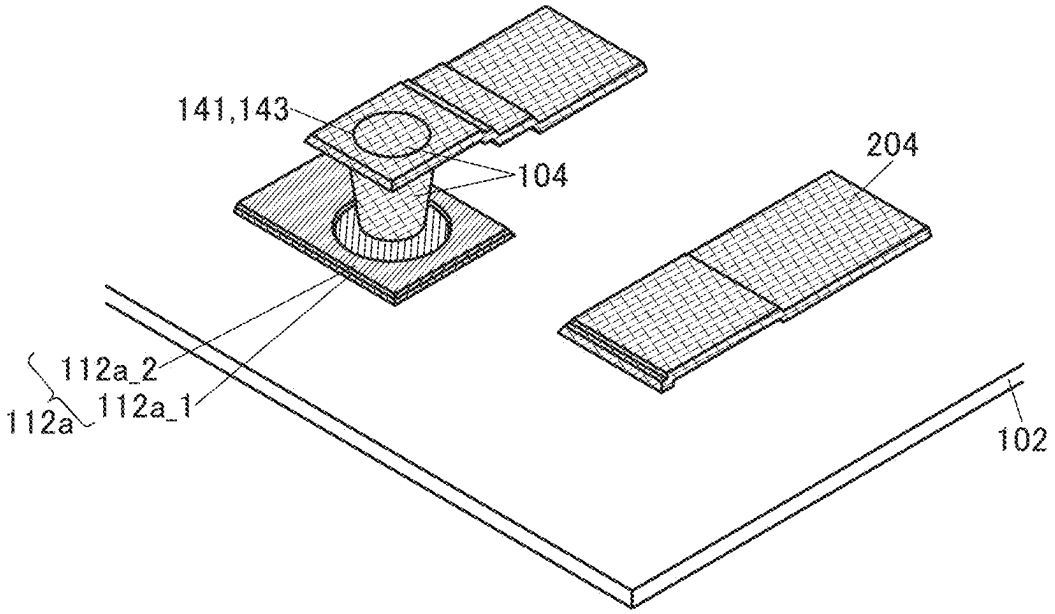

141,143
104
204
112a_2
112a_1
112a
102

FIG. 4A

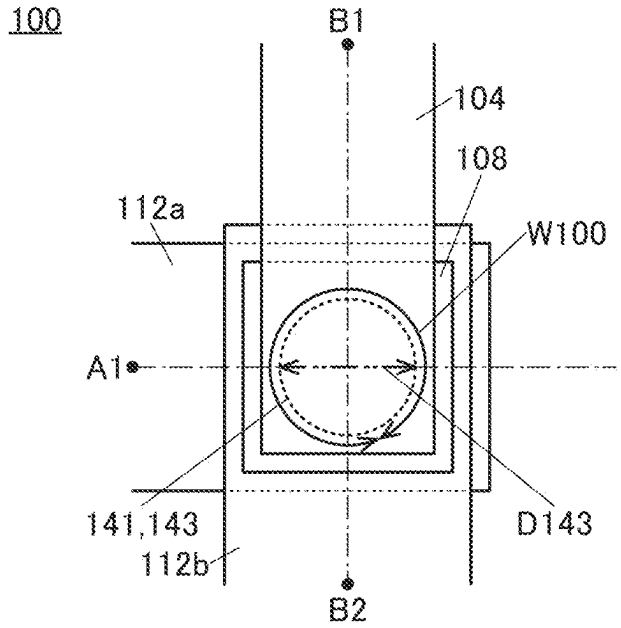

100
B1
104
108
112a
W100
A1
141,143
D143
112b
B2

FIG. 4B

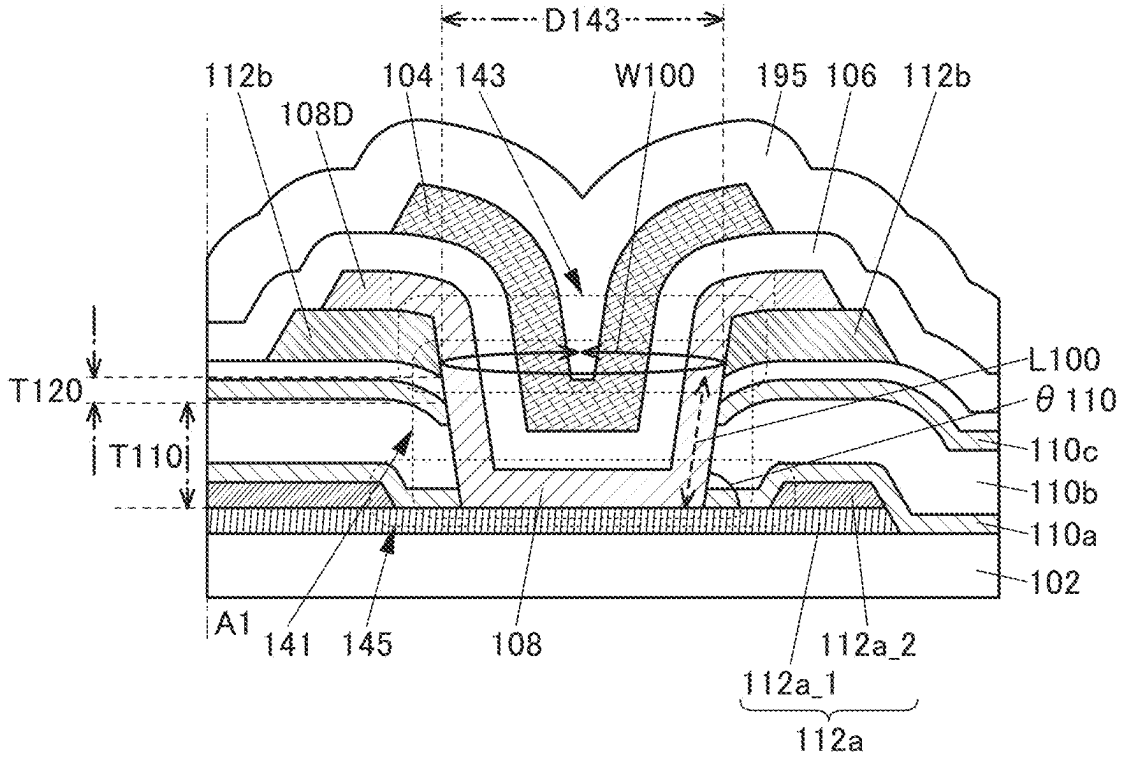

100
D143
112b
104
143
W100
195
106
112b
108D
T120
T110
L100
θ 110
110c
110b
110a
102
A1
141
145
108
112a_2
112a_1
112a

FIG. 5A

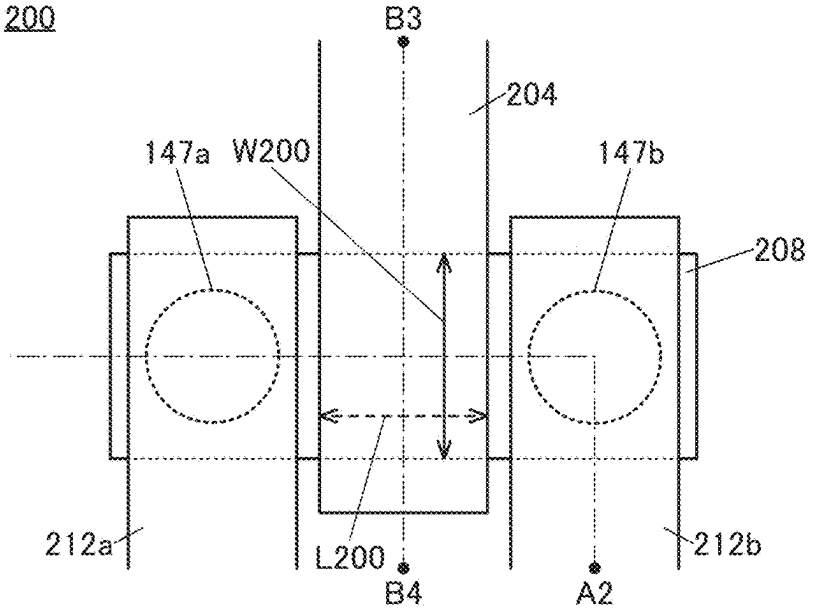


FIG. 5B

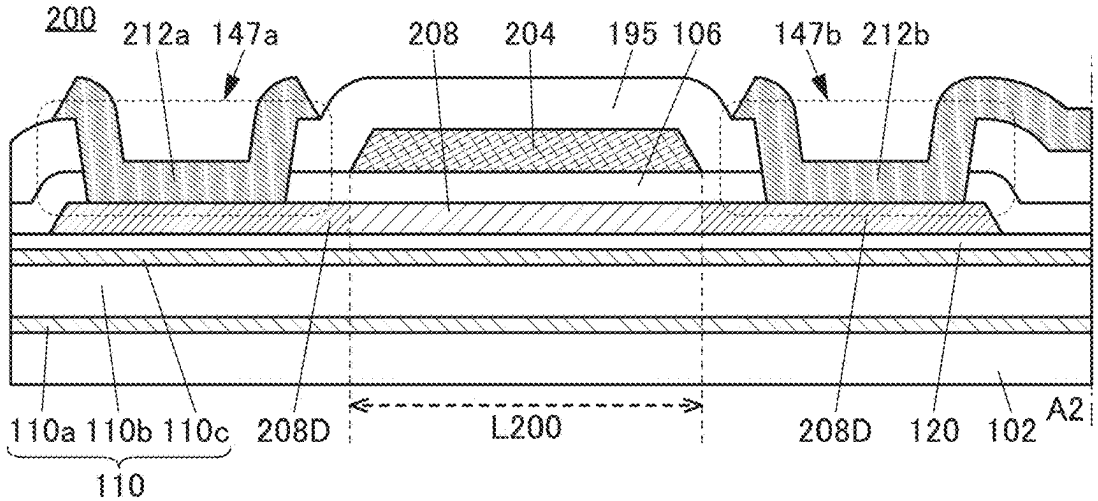


FIG. 5C

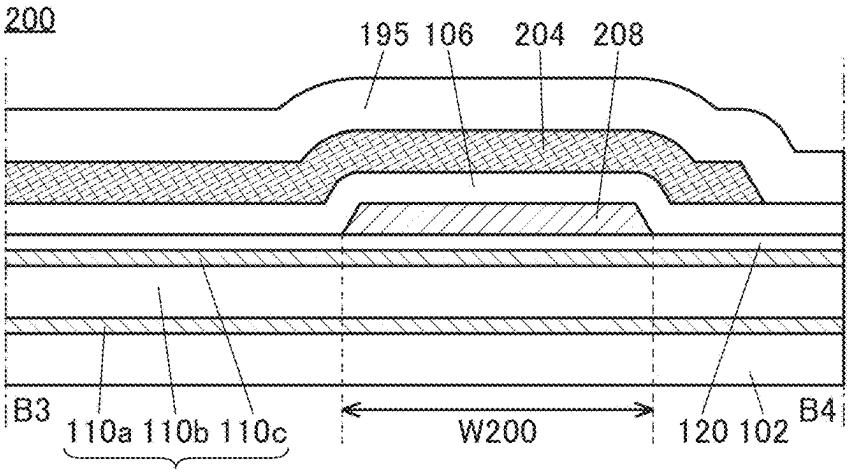


FIG. 6A

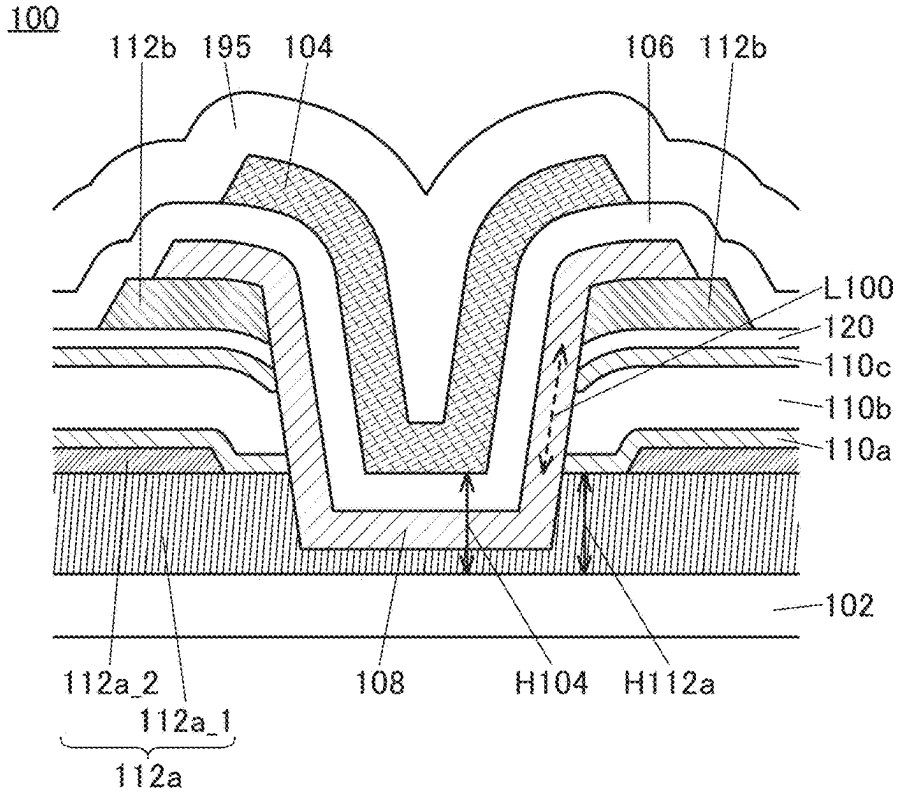

100
112b
195
104
106
112b
L100
120
110c
110b
110a
102
112a_2
112a_1
112a
108
H104
H112a

FIG. 6B

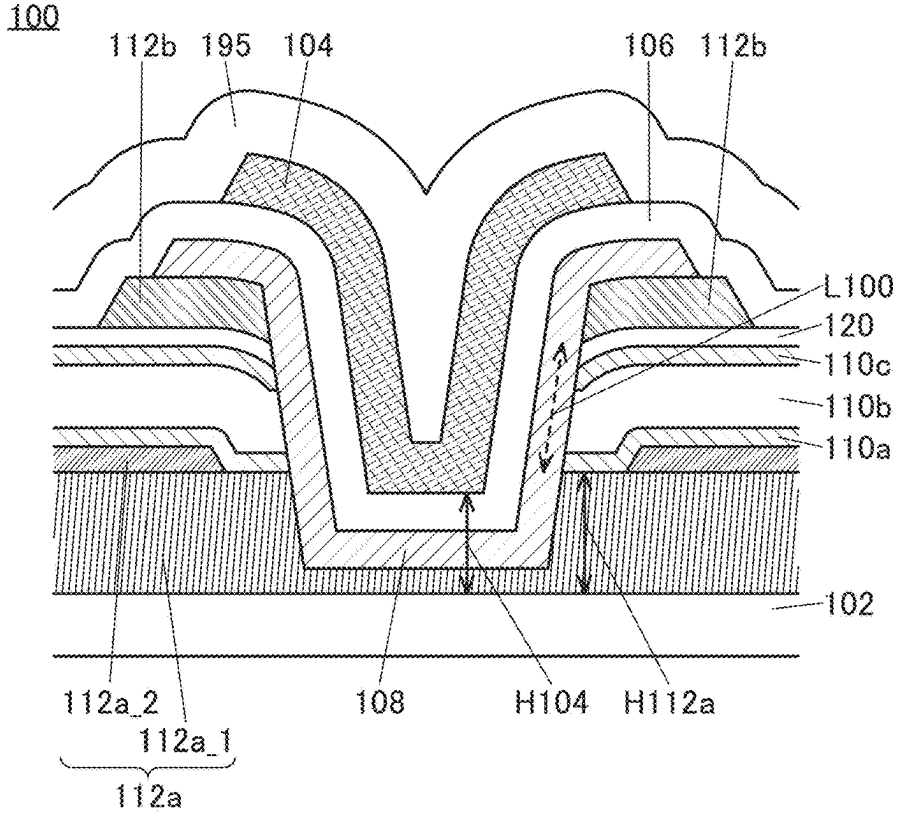

100
112b
195
104
106
112b
L100
120
110c
110b
110a
102
112a_2
112a_1
112a
108
H104
H112a

FIG. 7A

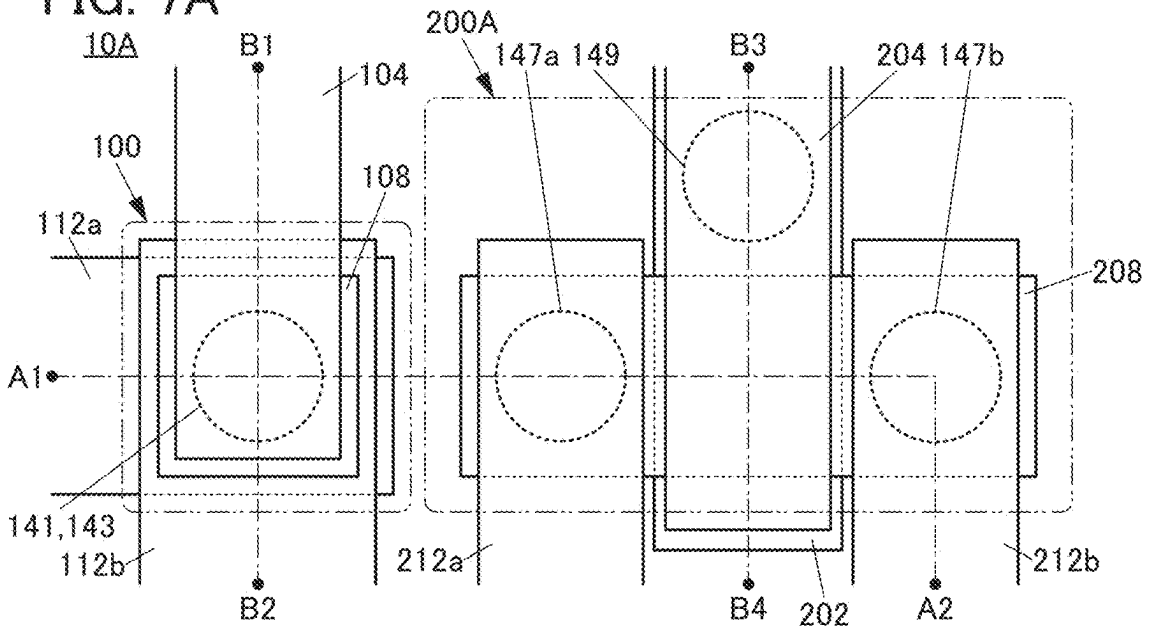


FIG. 7B

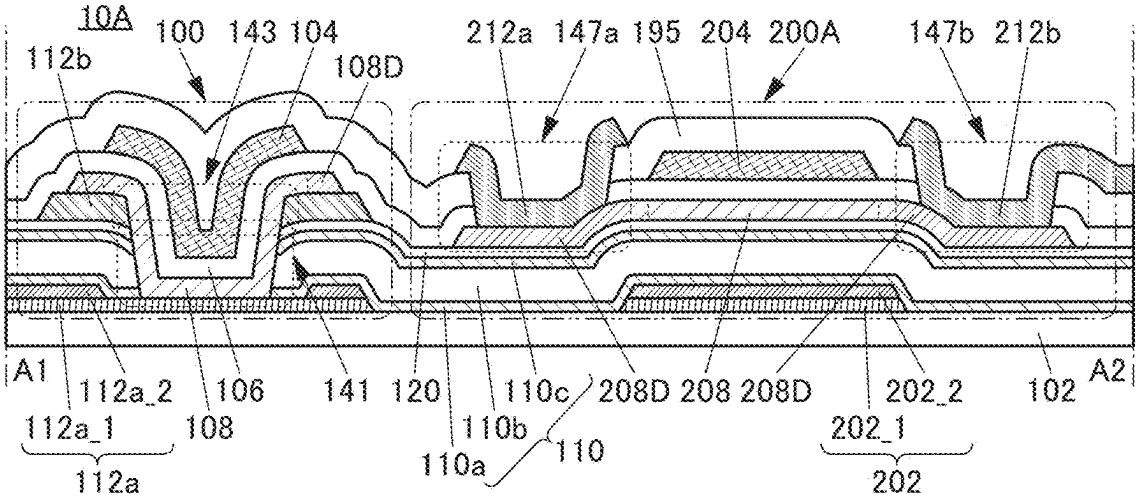


FIG. 7C

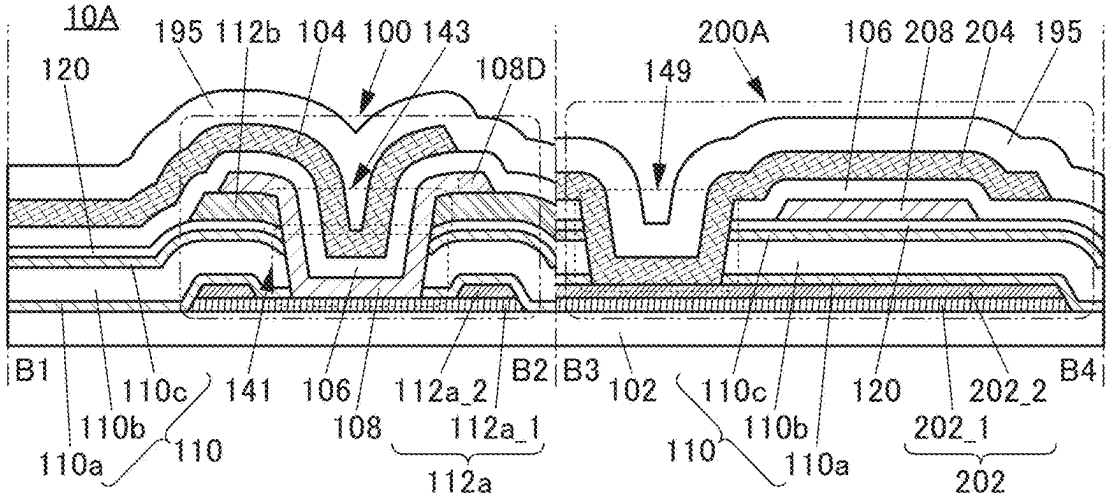


FIG. 8A

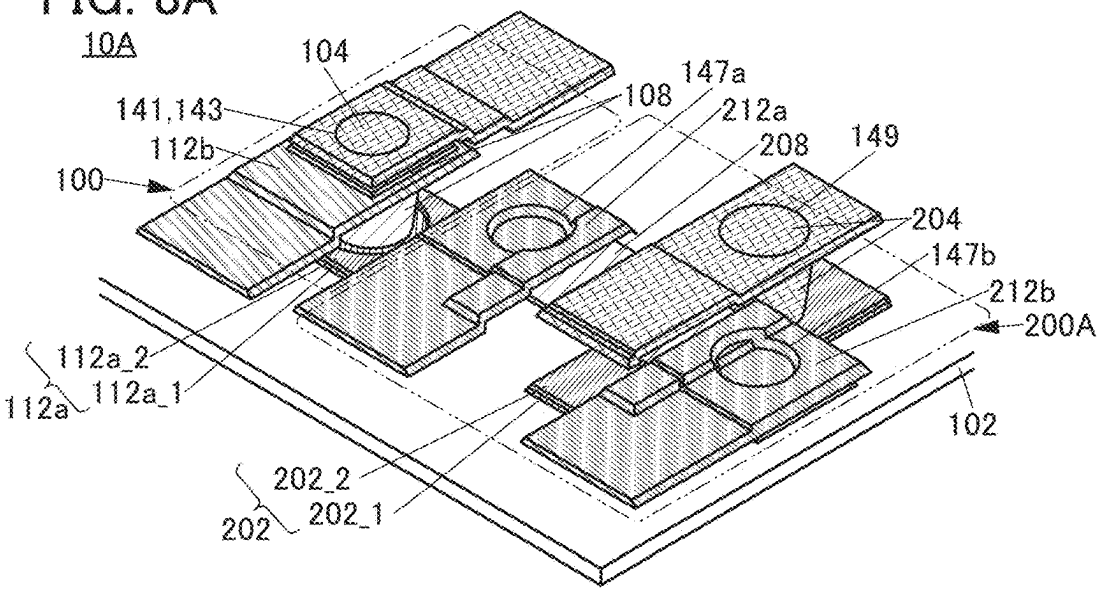


FIG. 8B

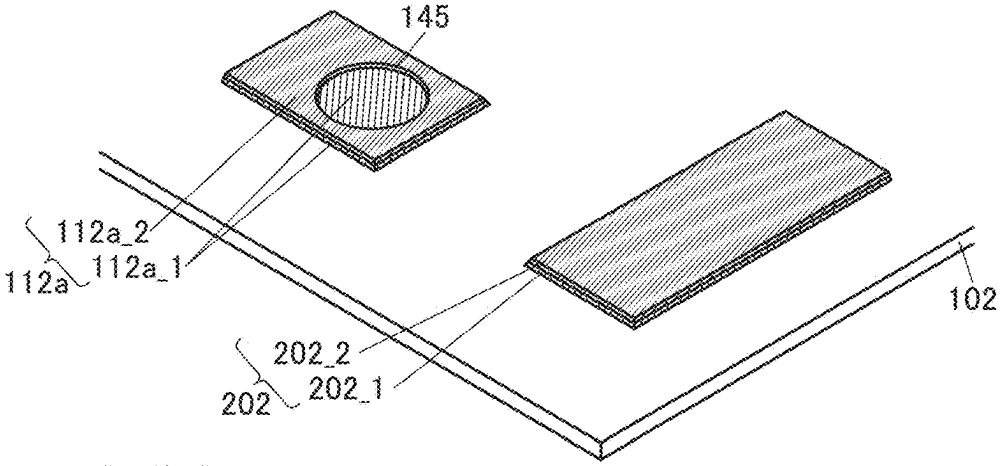


FIG. 8C

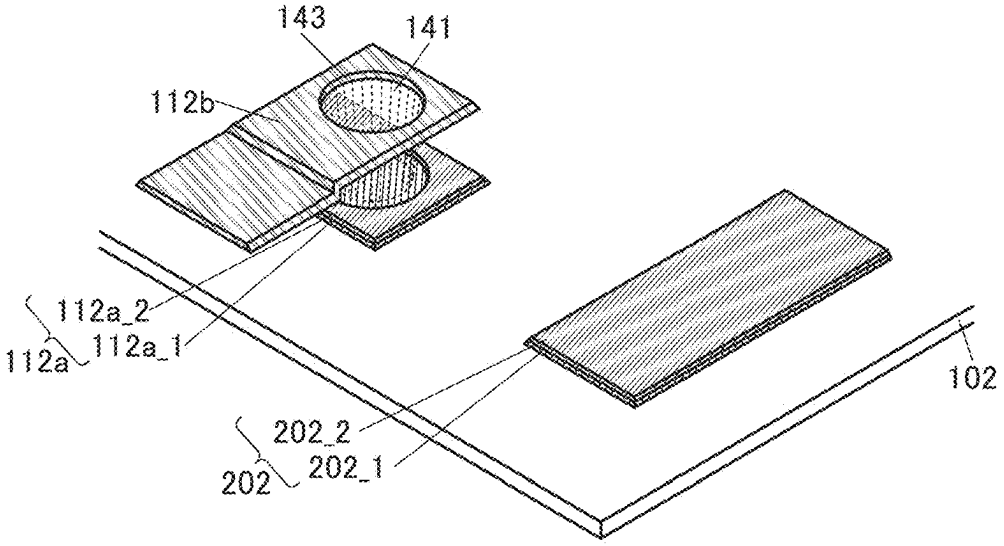


FIG. 9A

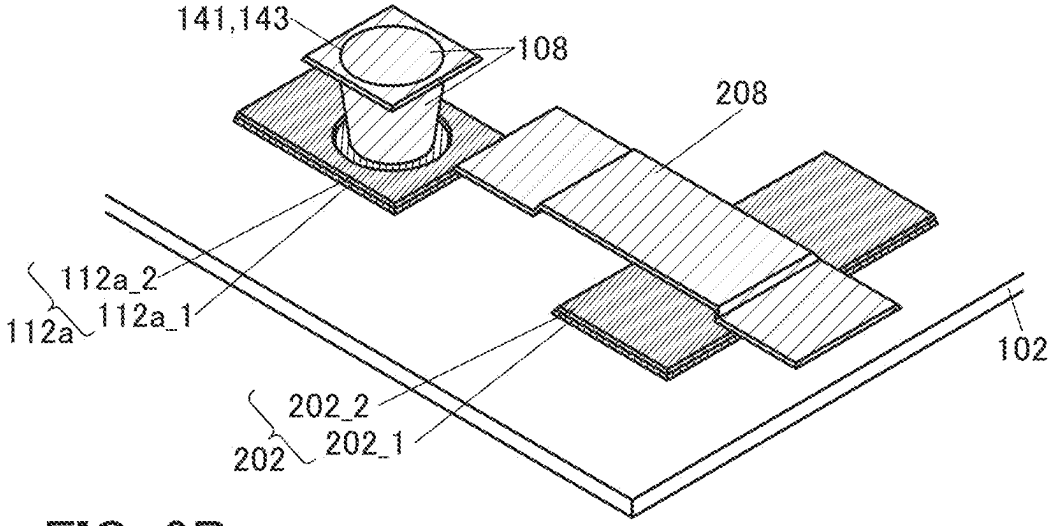

141,143
108
208
112a_2
112a_1
112a
102
202_2
202_1
202

FIG. 9B

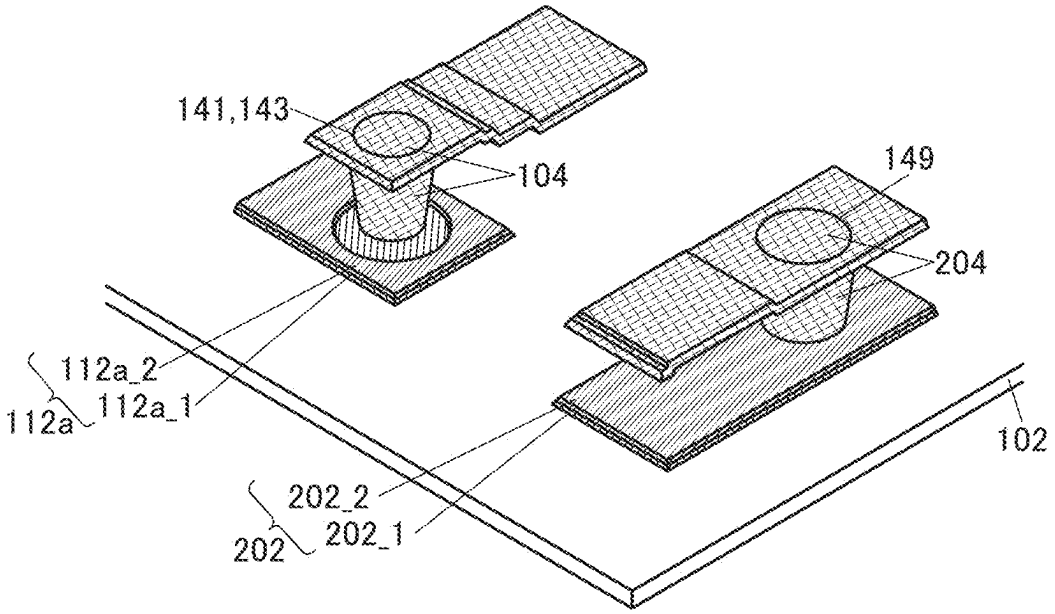

141,143
104
149
204
112a_2
112a_1
112a
102
202_2
202_1
202

FIG. 10A

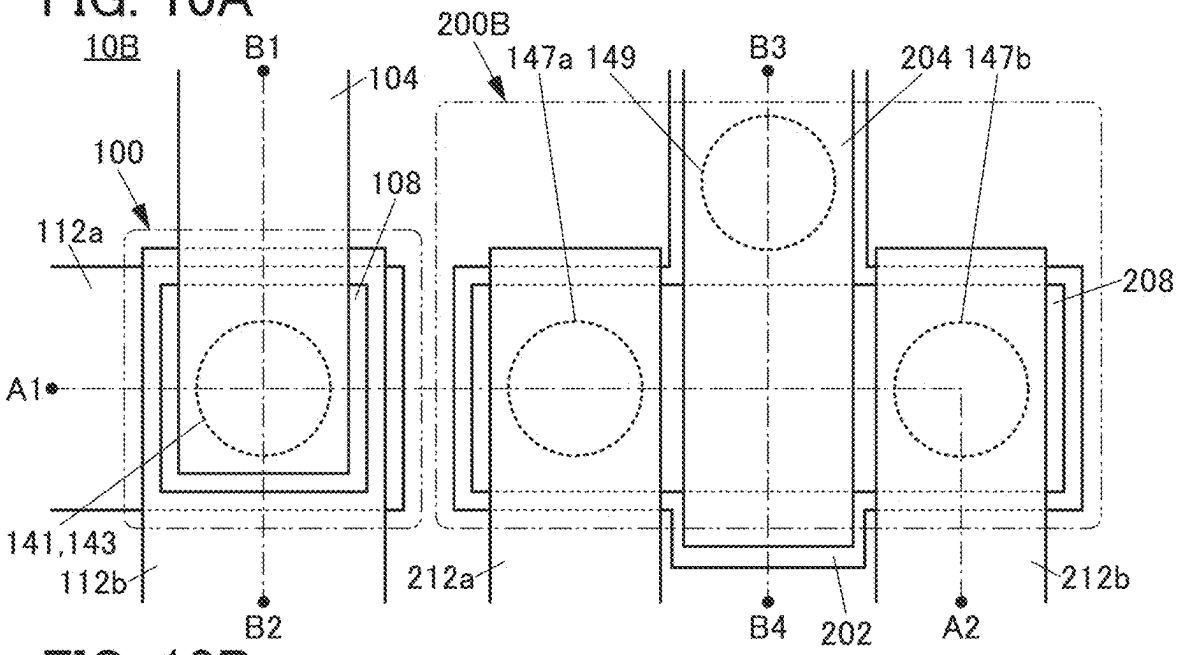


FIG. 10B

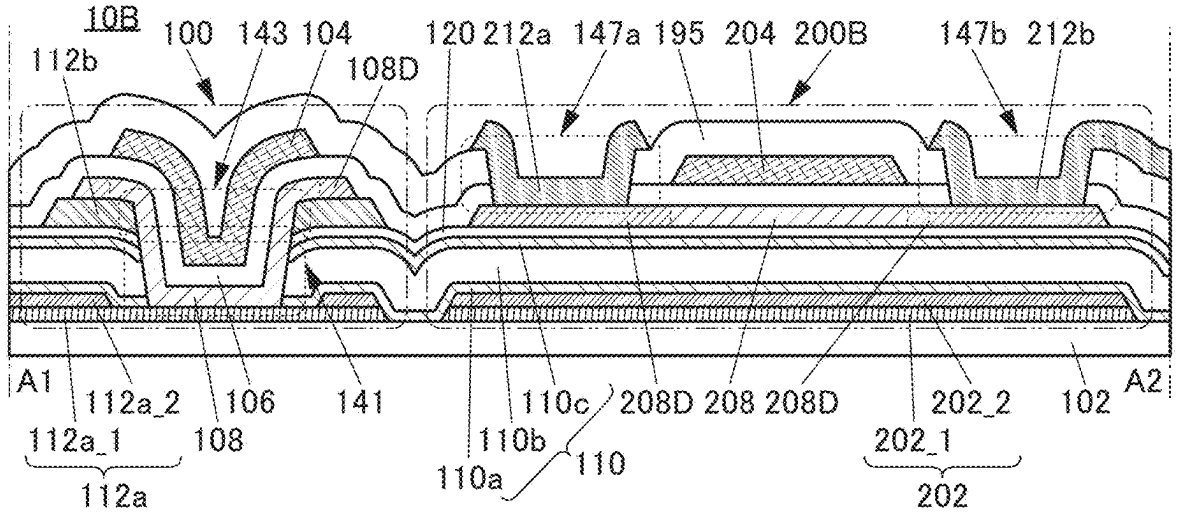


FIG. 11A

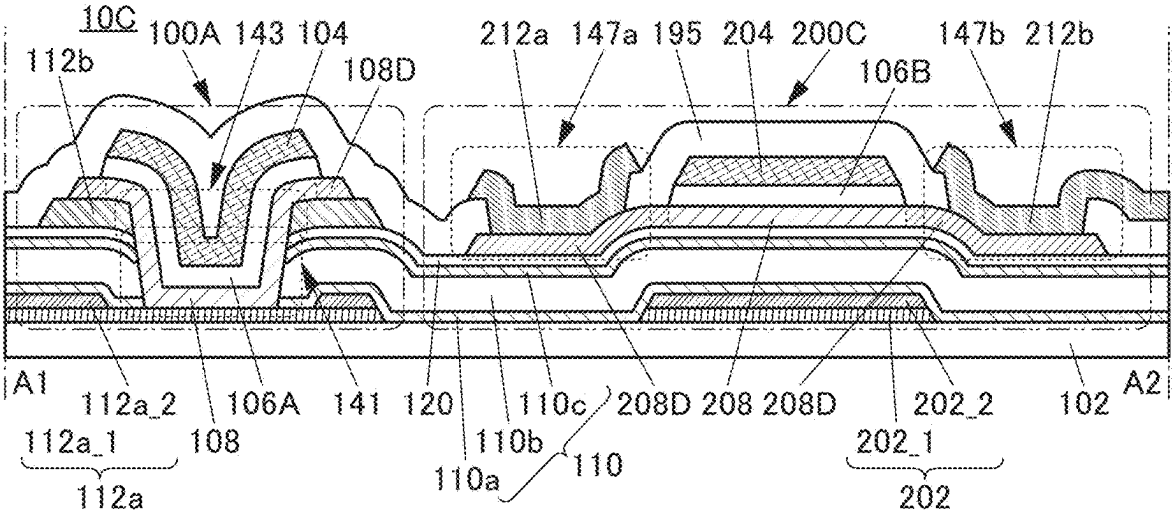


FIG. 11B

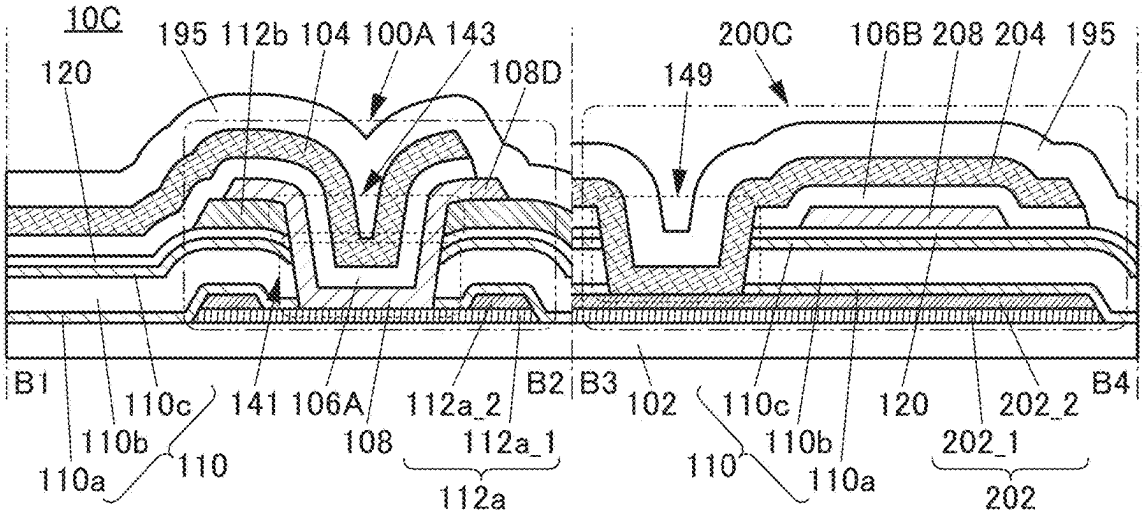


FIG. 12A

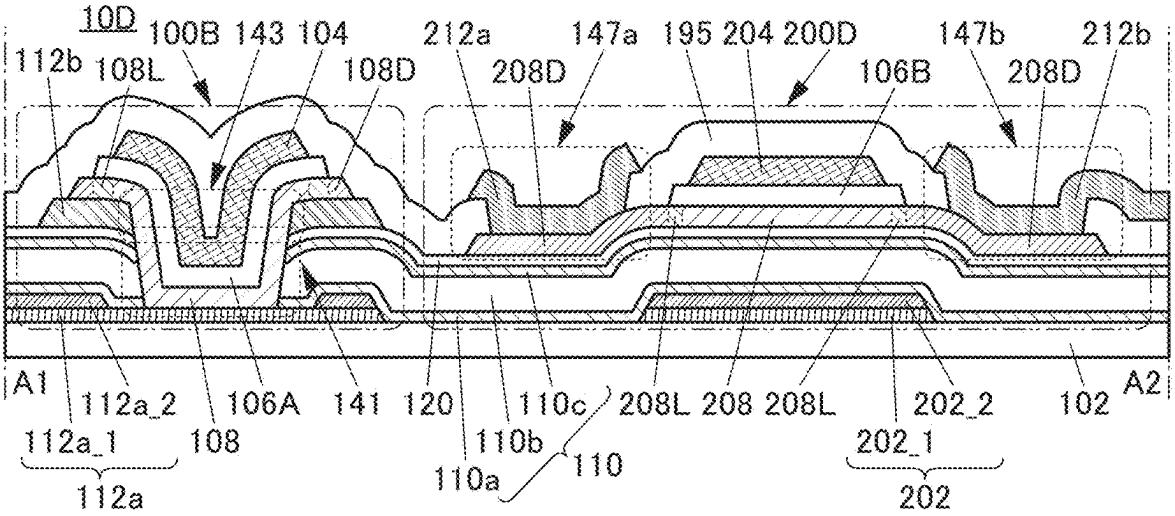


FIG. 12B

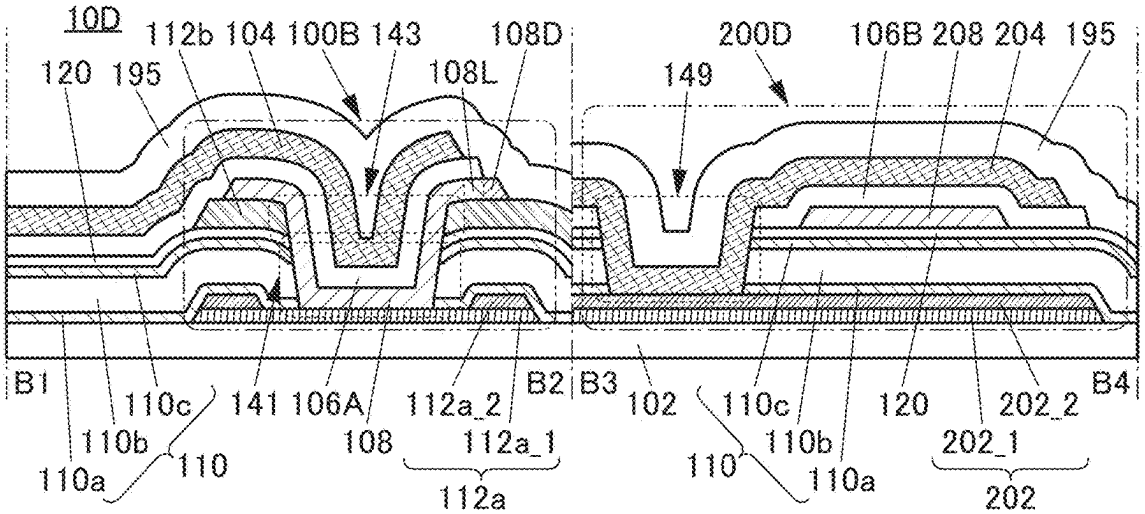


FIG. 13A

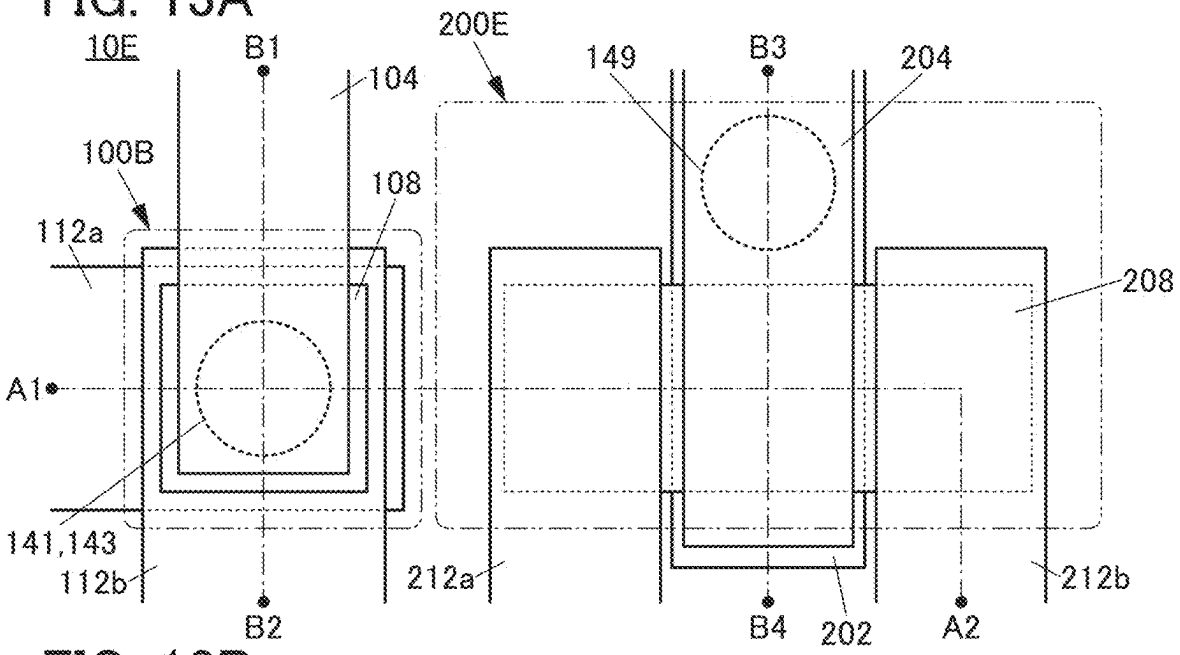


FIG. 13B

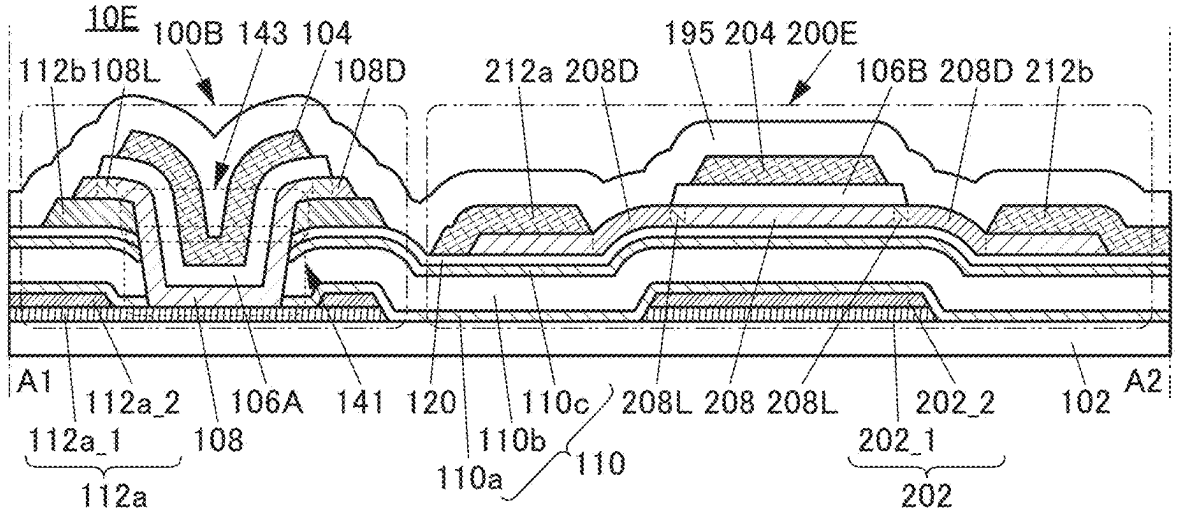


FIG. 14

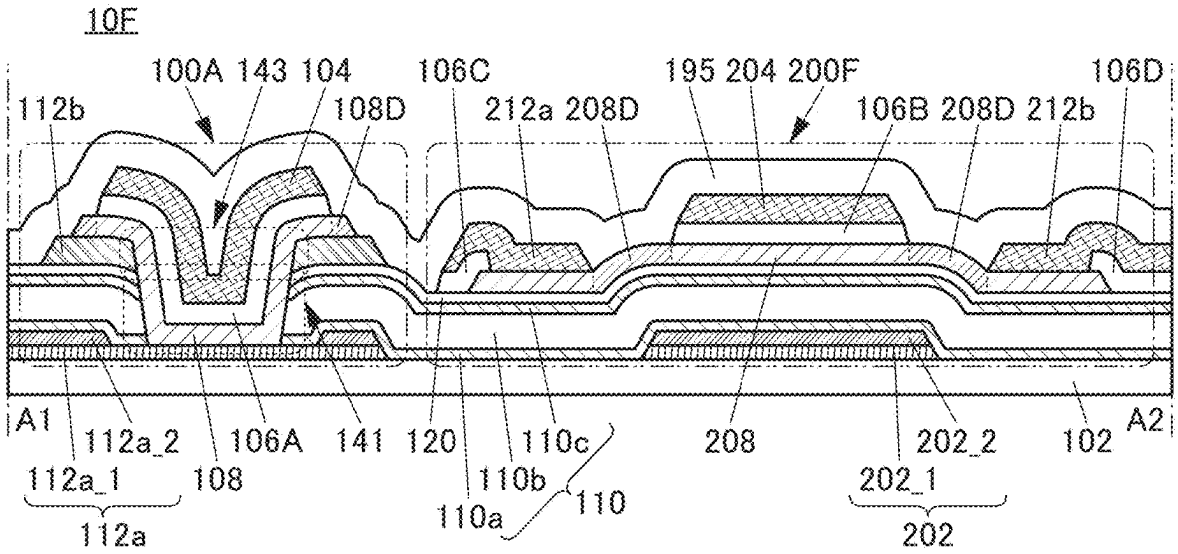

10F
100A
143
104
106C
195
204
200F
106D
112b
108D
212a
208D
106B
208D
212b
A1
112a_2
106A
141
120
110c
208
202_2
102
A2
112a_1
108
110b
110
202_1
110a
112a
202

FIG. 15A

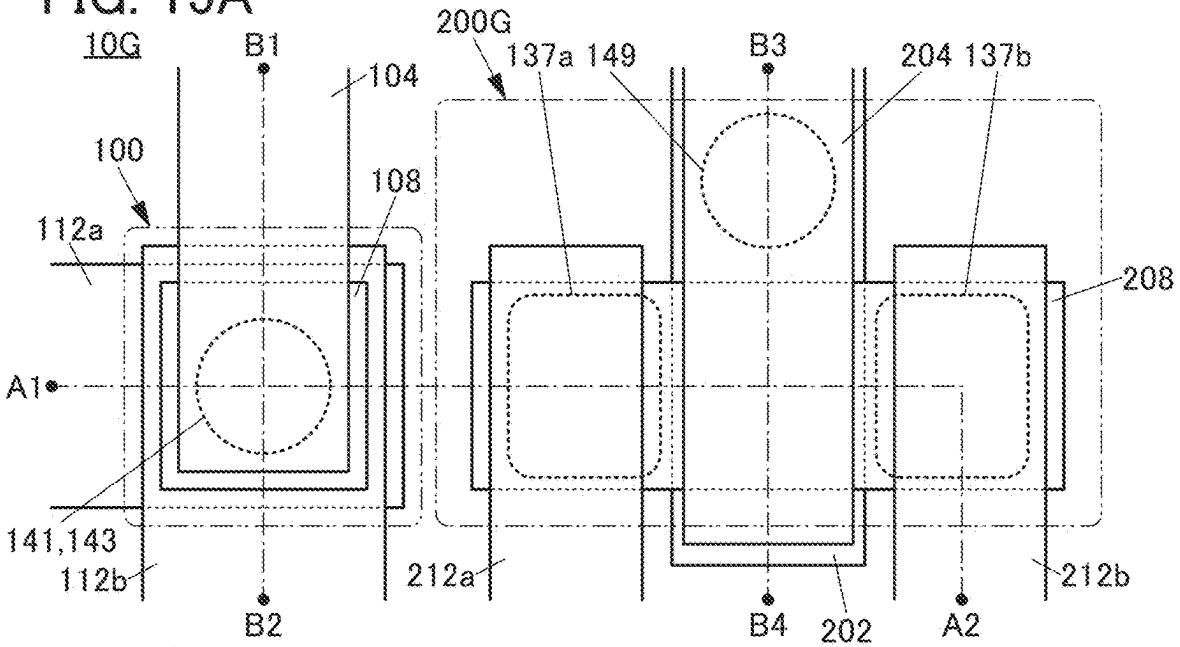


FIG. 15B

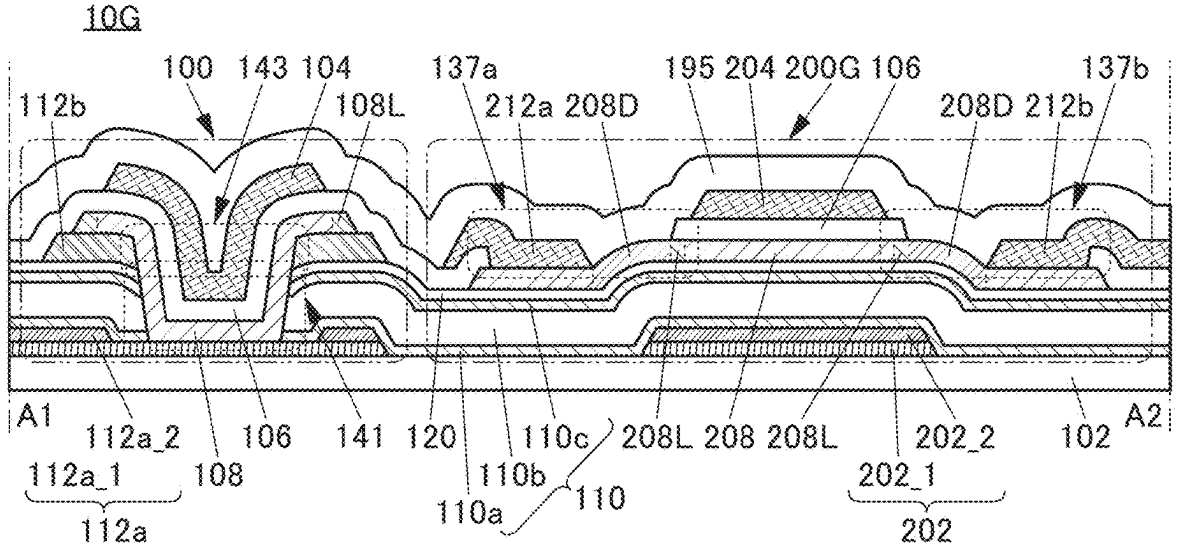


FIG. 16A

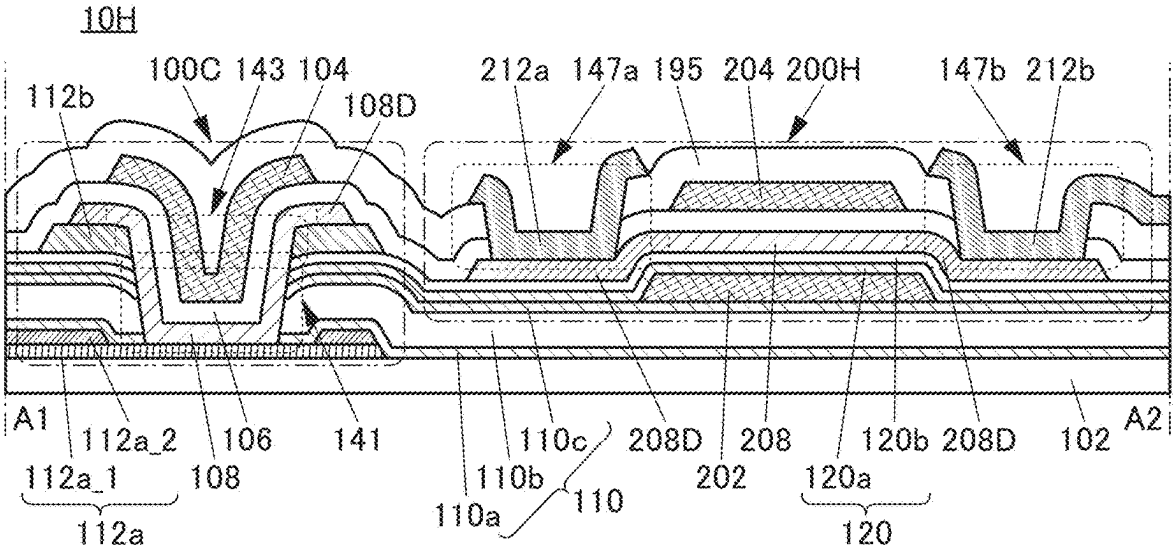
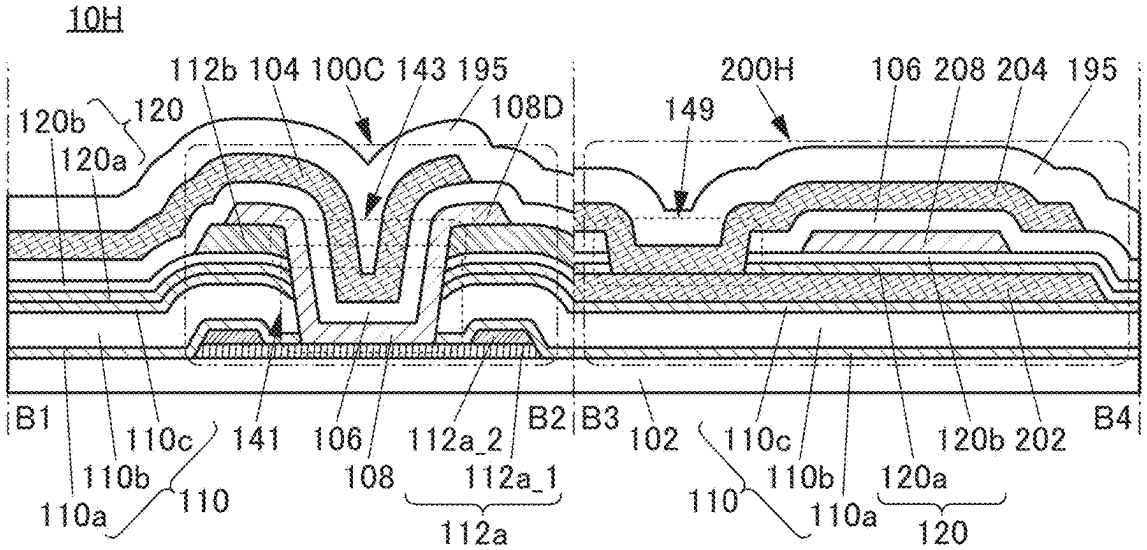


FIG. 16B



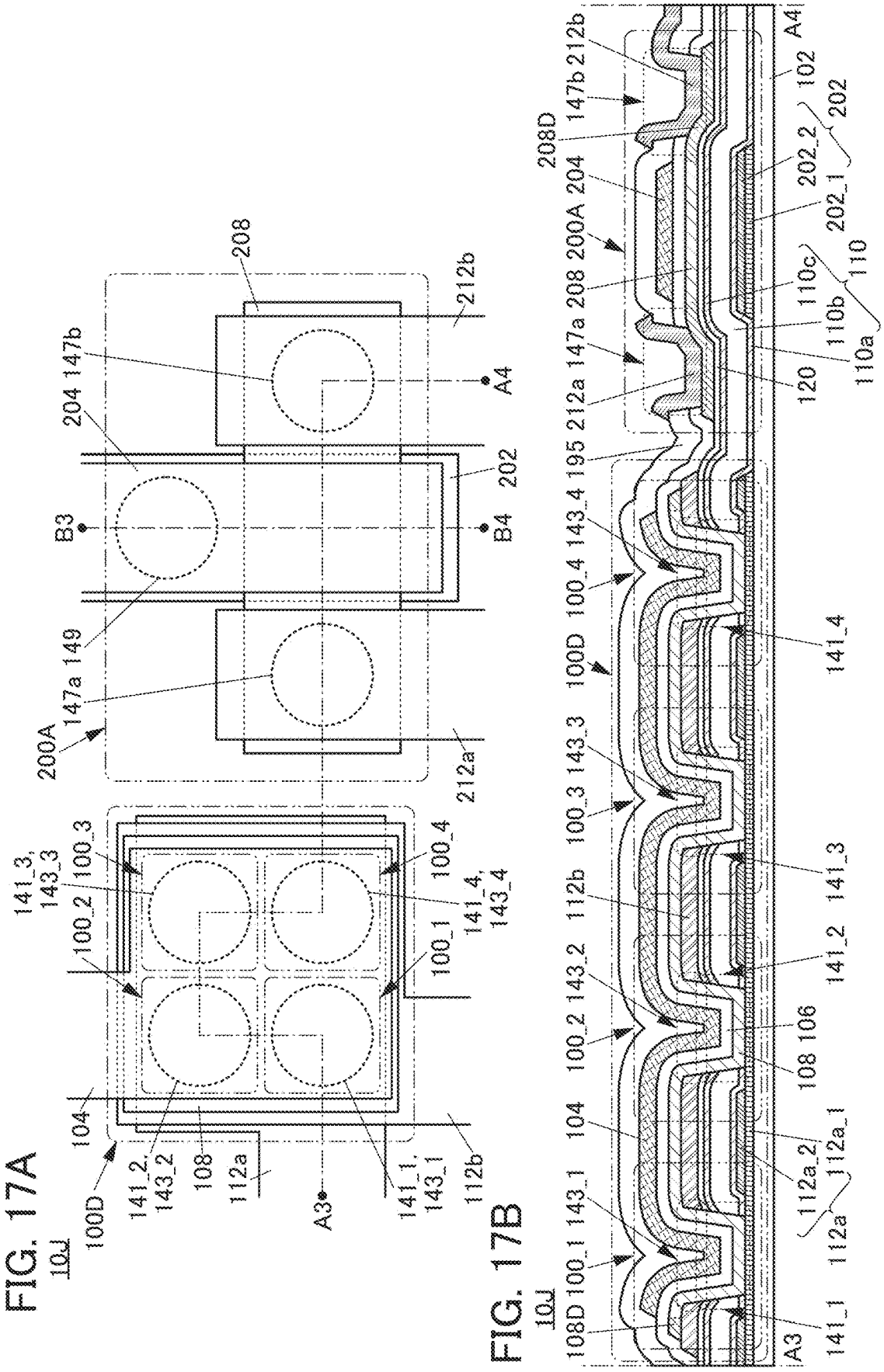


FIG. 17A
10J
100D
104
141_2,
143_2
108
112a
A3
141_1,
143_1
112b
100_2
141_3,
143_3
100_3
100_1
100_4
141_4,
143_4
200A
147a
149
B3
204
147b
208
212b
B4
202
A4
212a
FIG. 17B
10J
108D
100_1
143_1
104
100_2
143_2
112b
100_3
143_3
100D
100_4
143_4
195
212a
147a
208
200A
204
208D
147b
212b
A3
141_1
112a
112a_2
112a_1
108
106
141_2
141_3
141_4
120
110a
110b
110c
110
202_1
202_2
202
102
A4

FIG. 18A

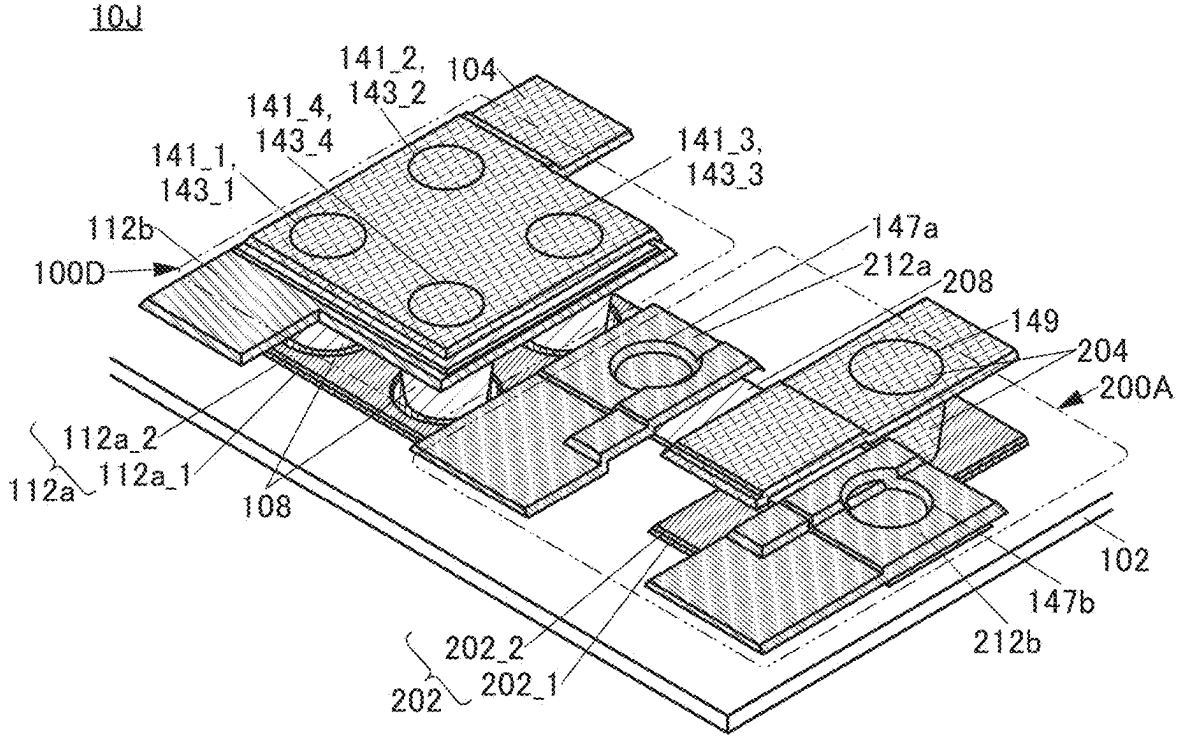


FIG. 18B

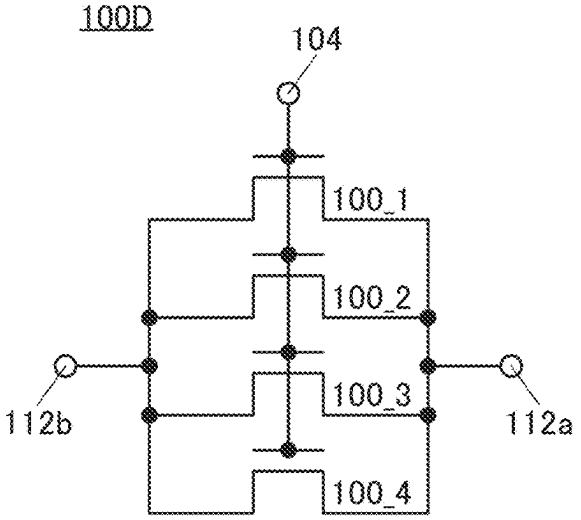


FIG. 18C

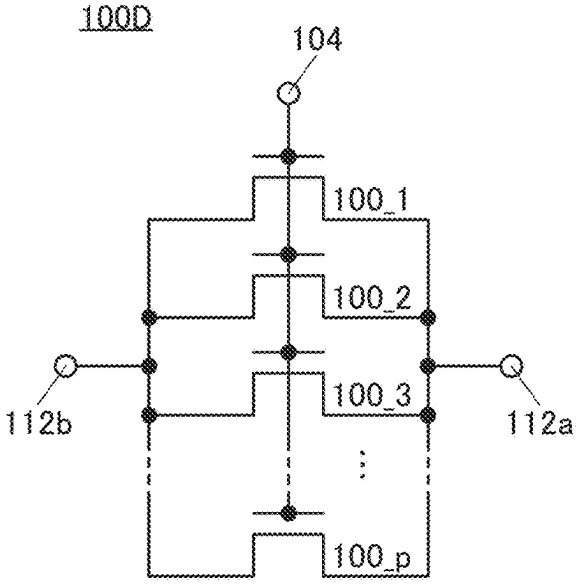


FIG. 19A

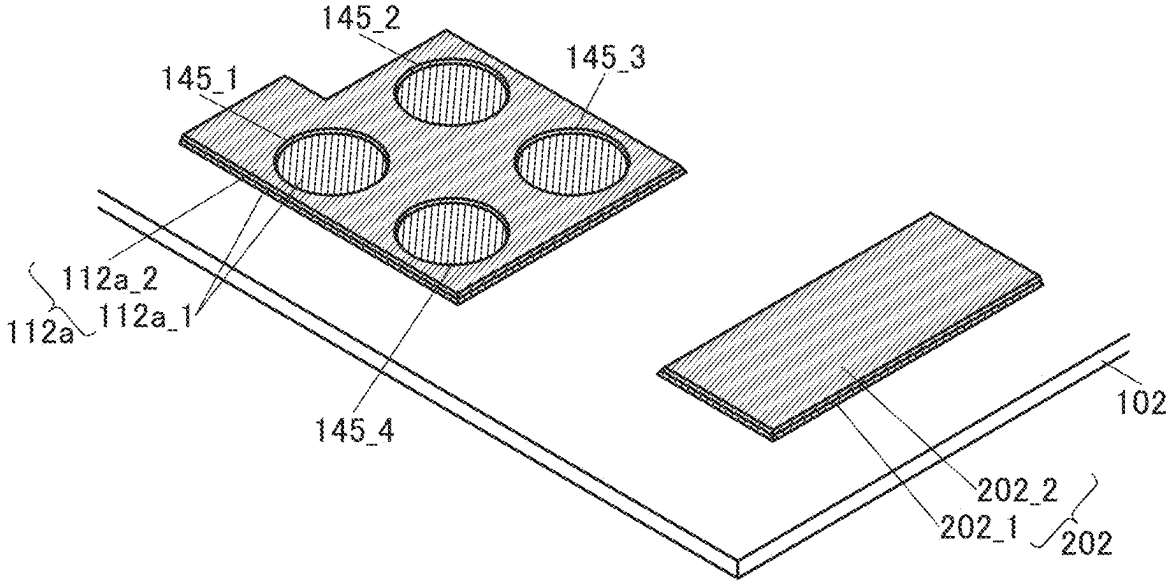


FIG. 19B

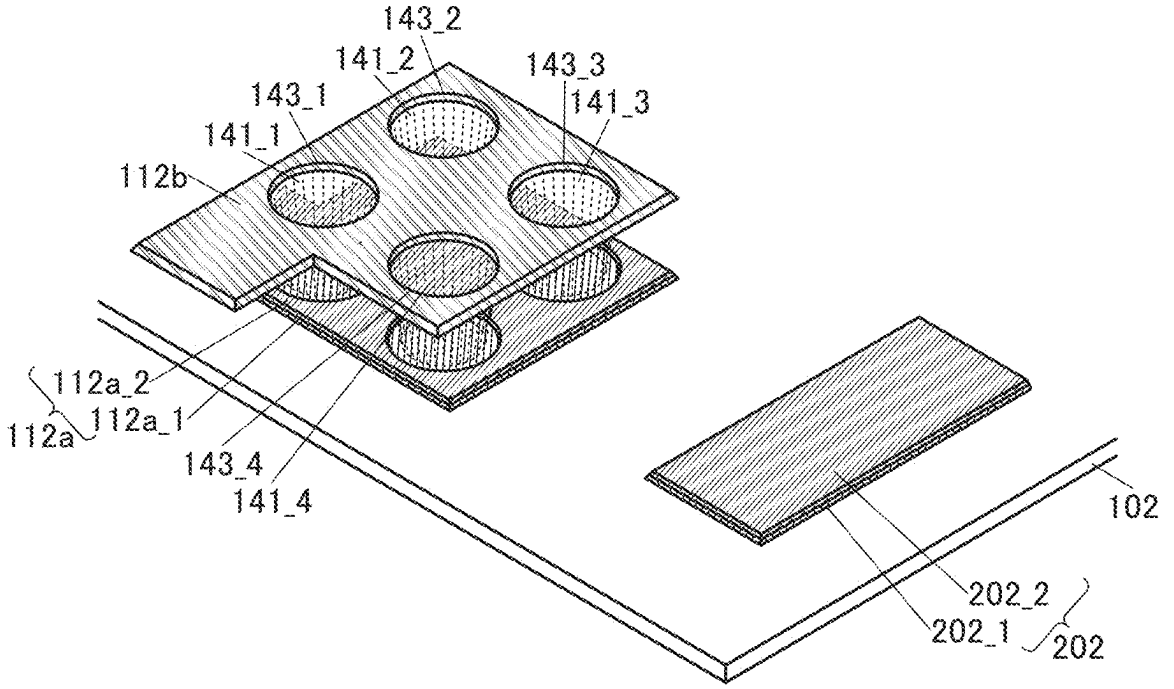


FIG. 20A

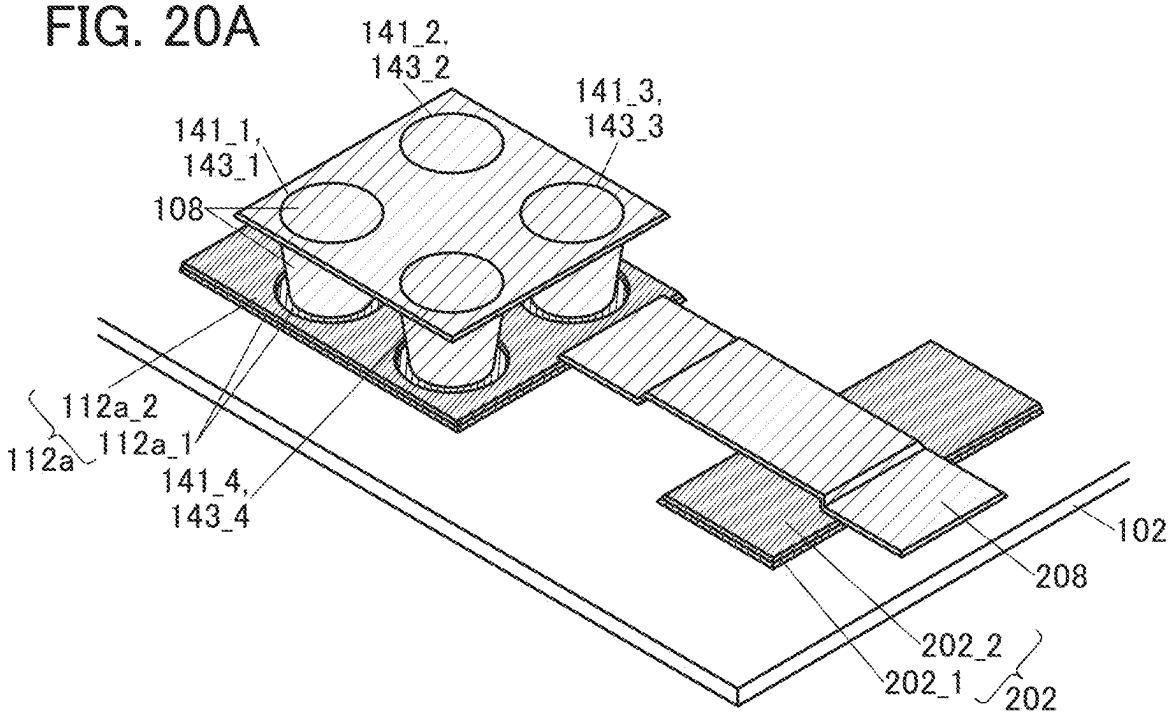
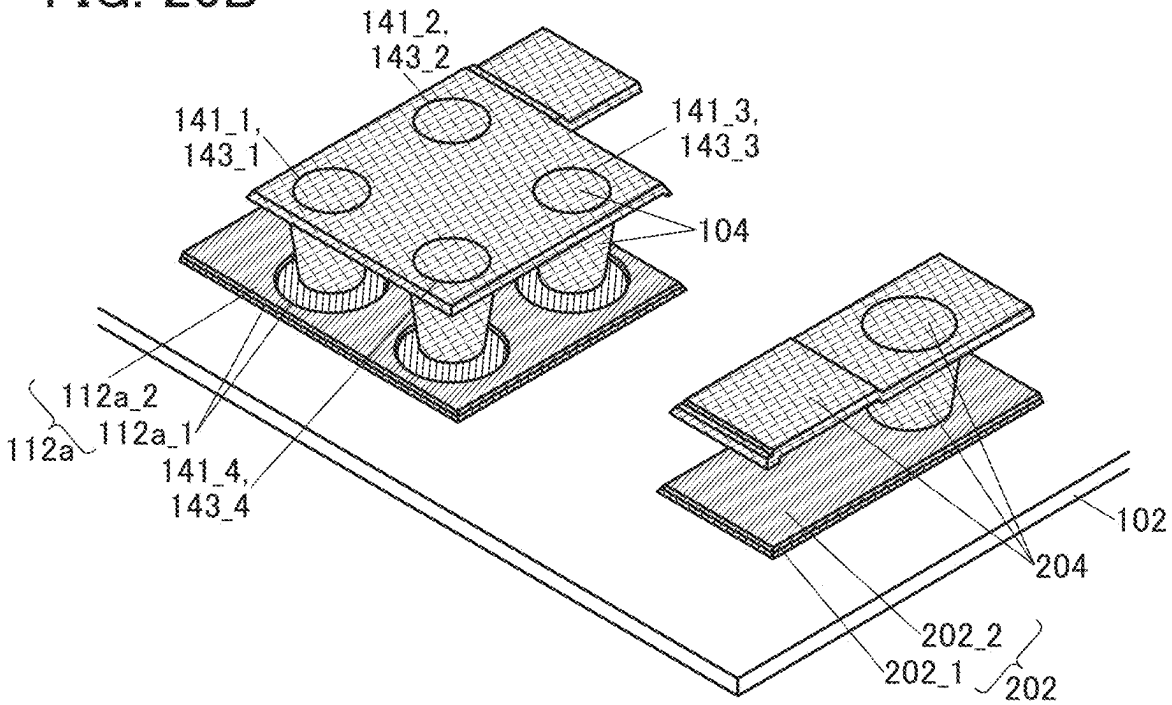


FIG. 20B



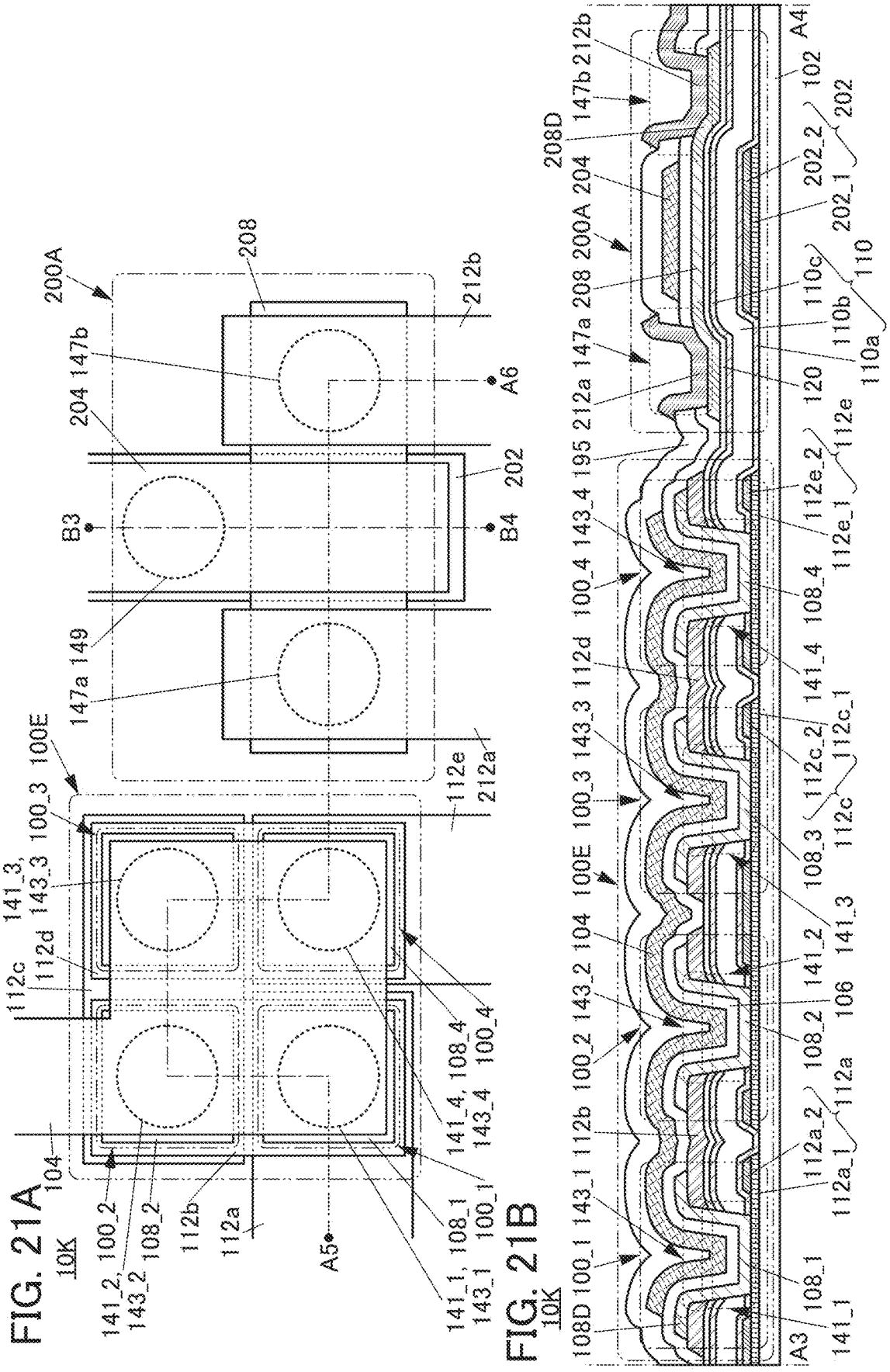


FIG. 21A
10K
200A
208
212b
147b
204
A6
B3
B4
202
149
147a
100E
100_3
141_3,
143_3
112d
112c
104
141_2, 100_2
143_2
108_2
112b
112a
A5
141_1, 108_1
143_1
100_1
141_4, 108_4
143_4
100_4
112e
212a
FIG. 21B
10K
108D
100_1
143_1
112b
100_2
143_2
104
100E
100_3
143_3
112d
100_4
143_4
195
212a
147a
208
200A
204
208D
147b
212b
A4
102
202
202_2
202_1
110
110c
110b
110a
120
112e
112e_2
112e_1
108_4
141_4
112c_1
112c_2
112c
108_3
141_3
106
141_2
108_2
112a
112a_2
112a_1
108_1
141_1
A3

FIG. 22A

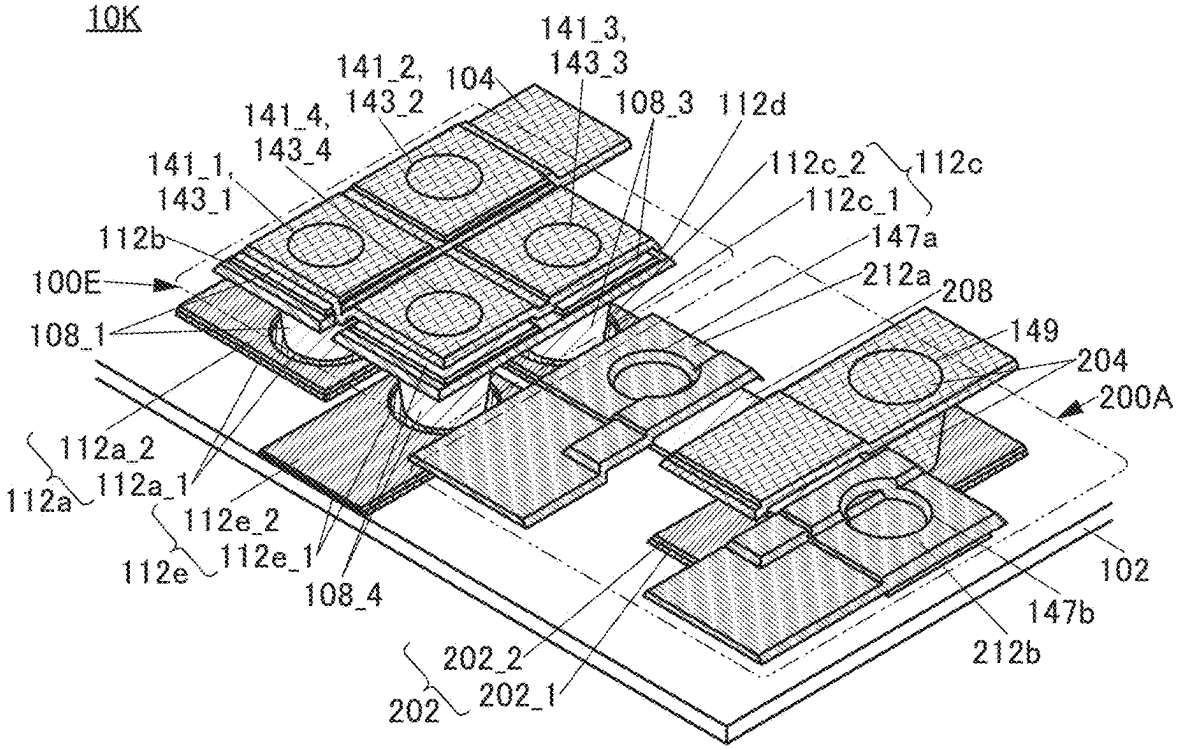


FIG. 22B

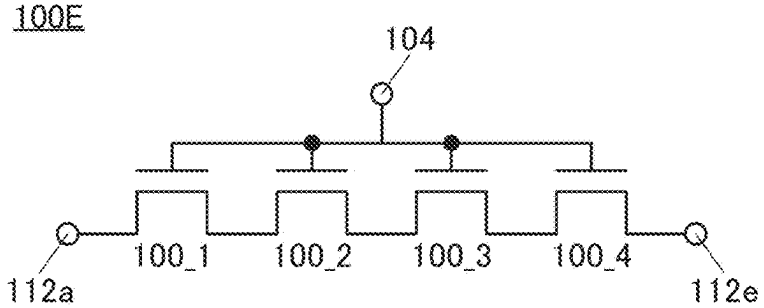


FIG. 22C

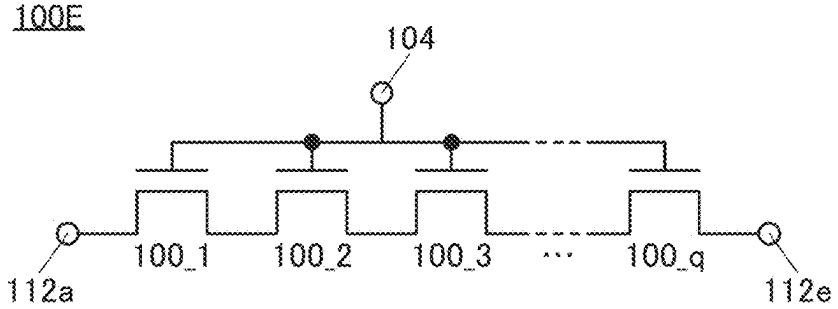


FIG. 23A

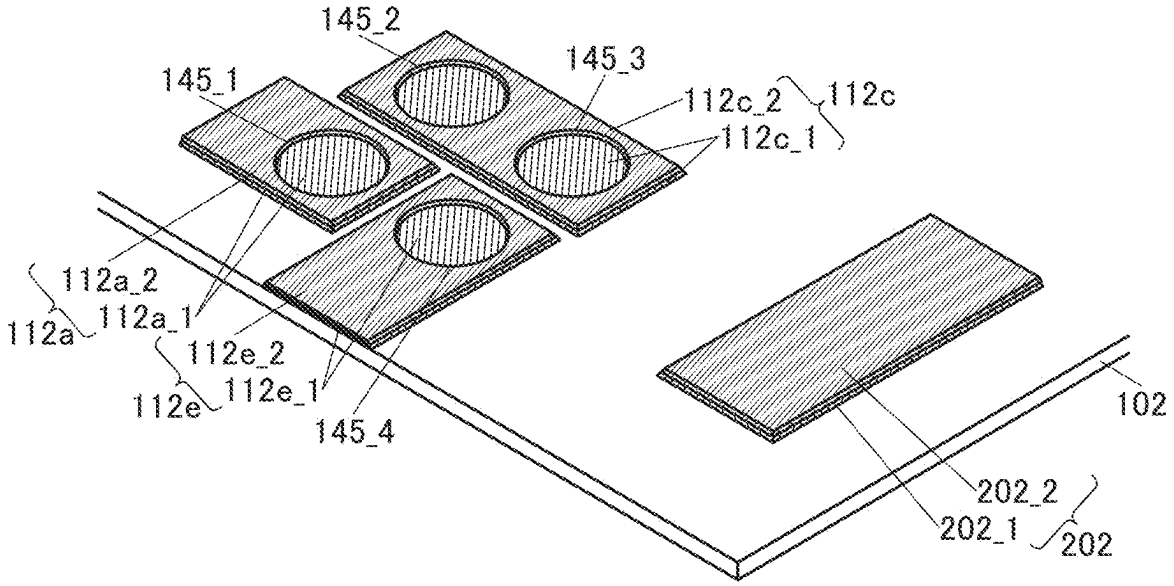


FIG. 23B

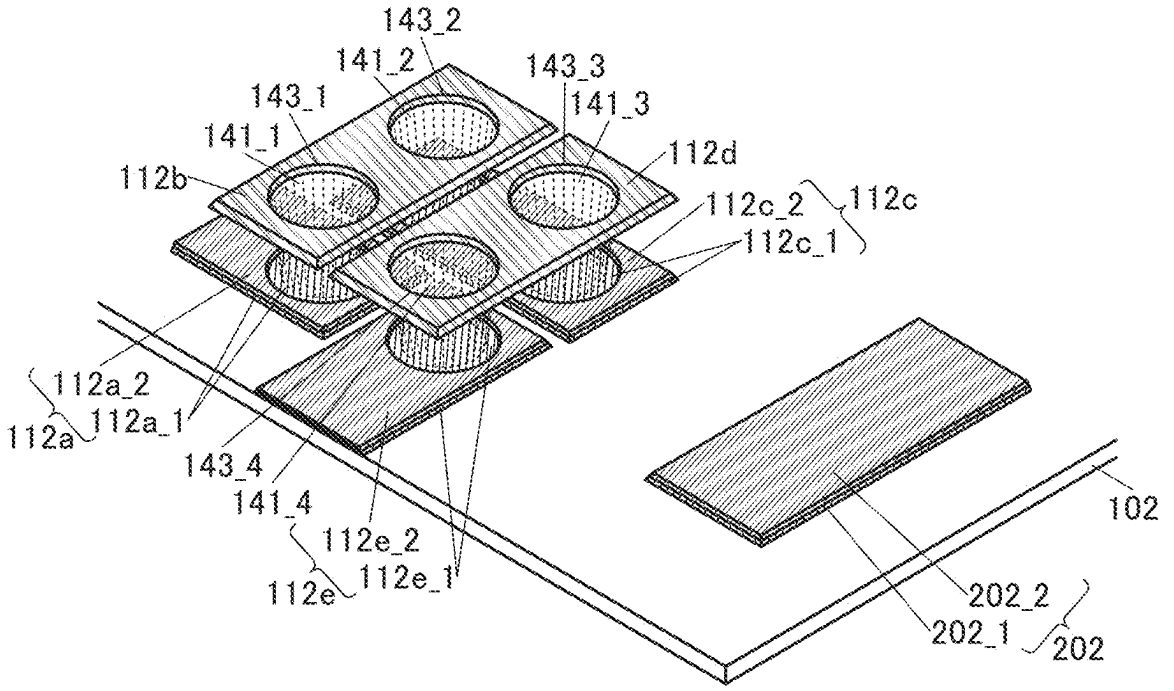


FIG. 24A

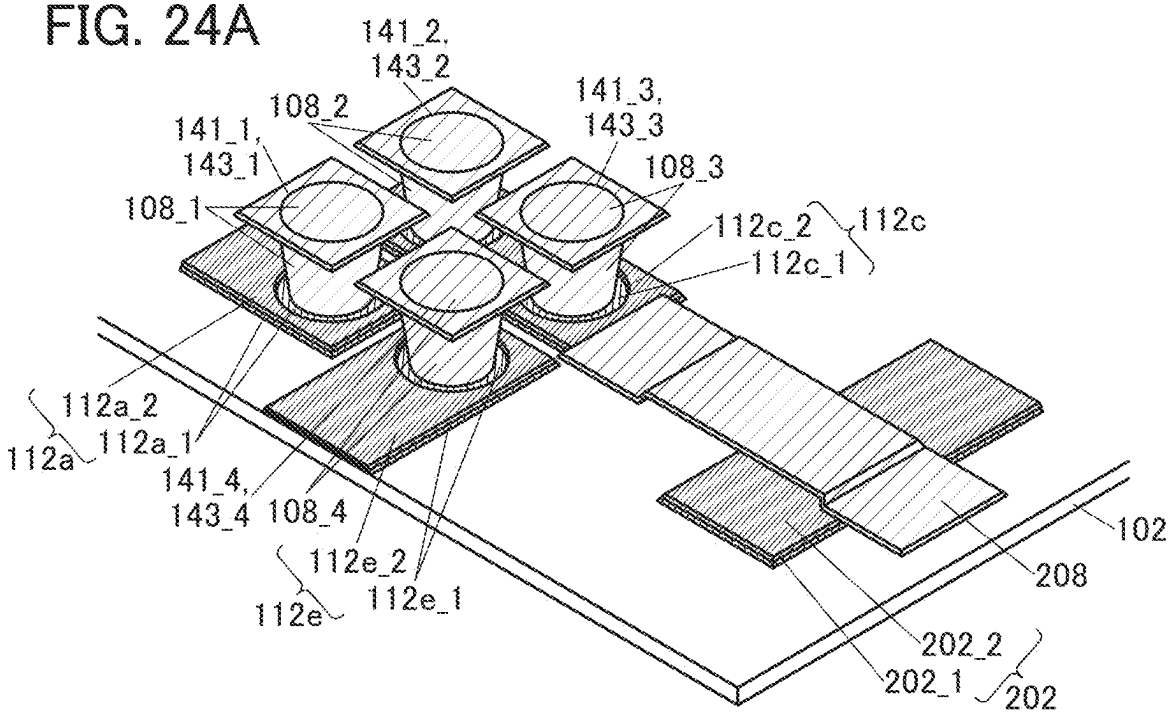


FIG. 24B

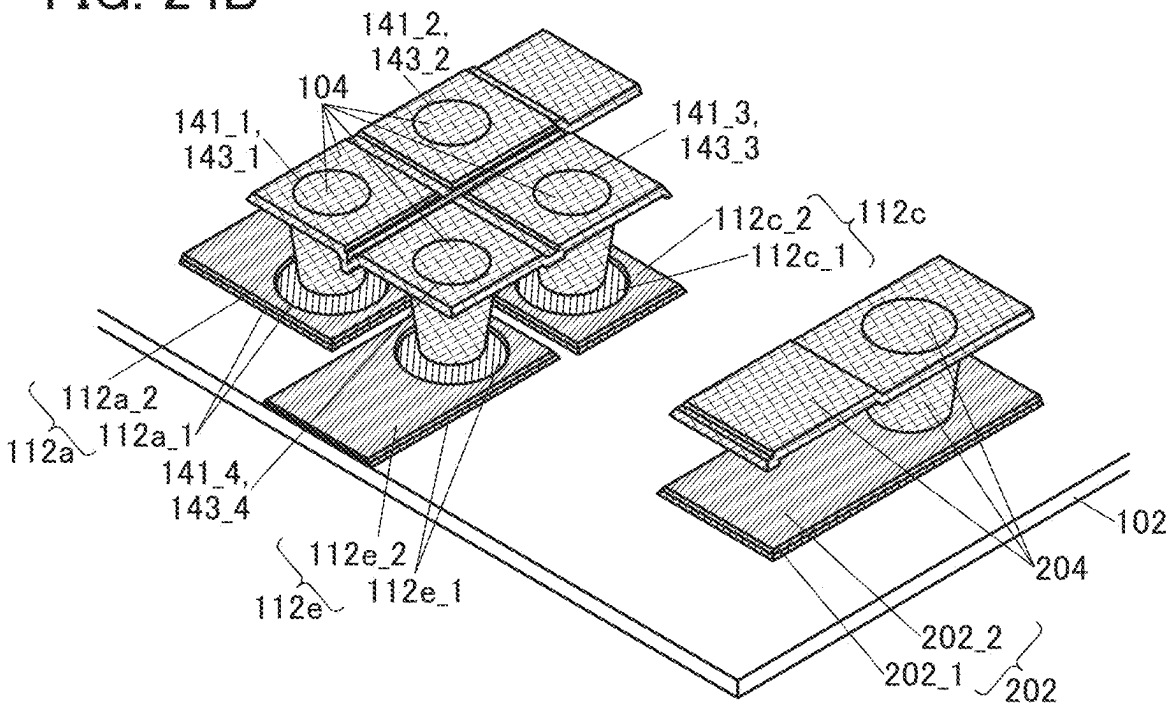


FIG. 25A

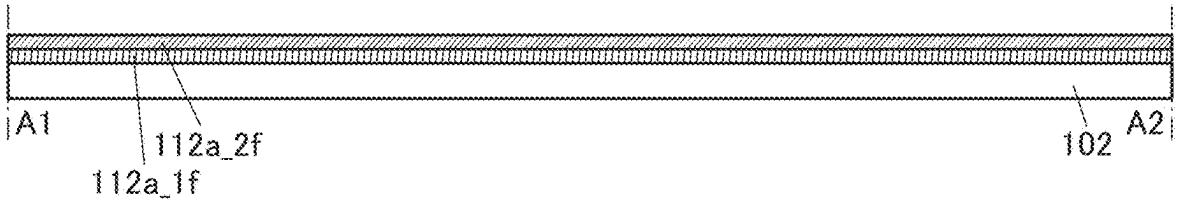


FIG. 25B

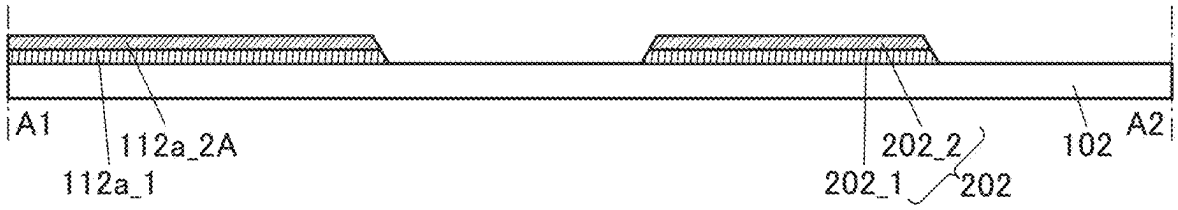


FIG. 25C

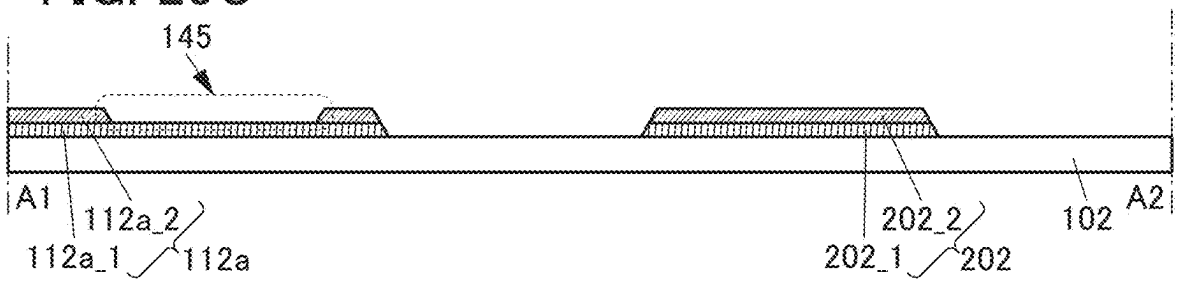


FIG. 25D

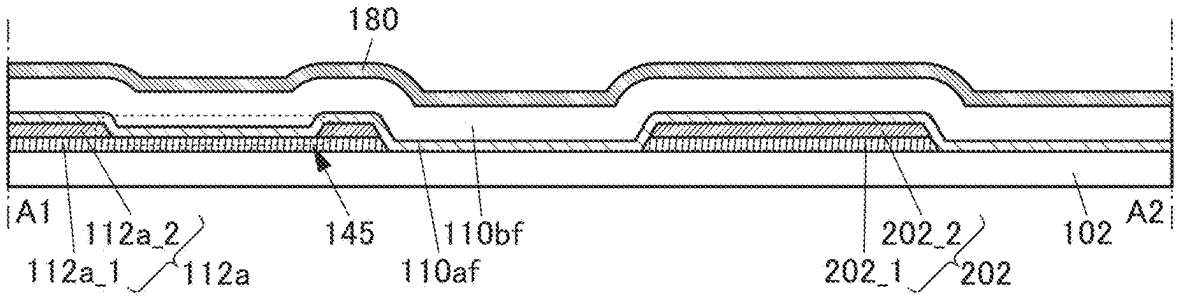


FIG. 25E

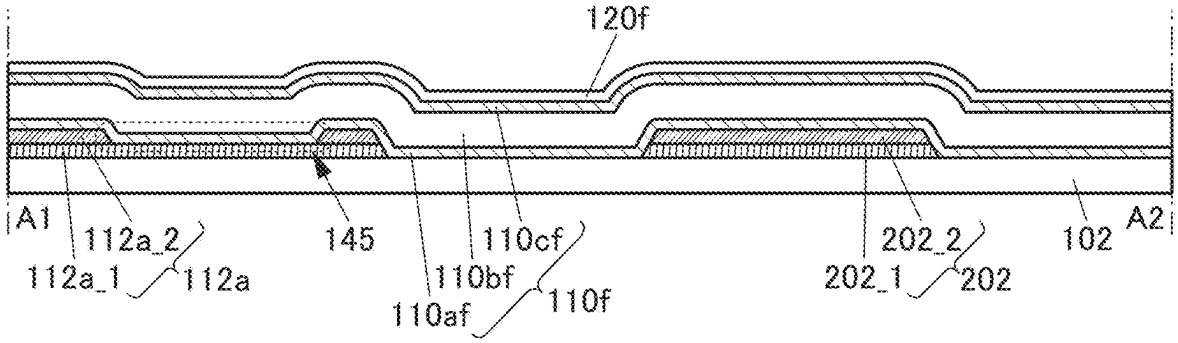


FIG. 26A

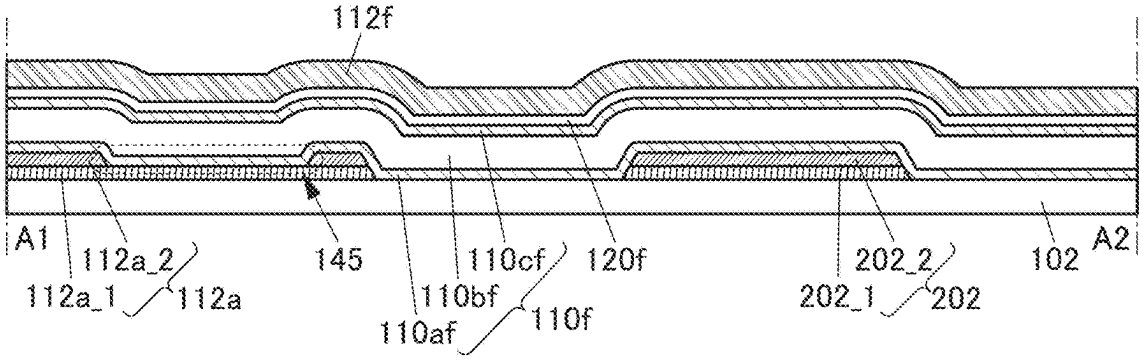


FIG. 26B

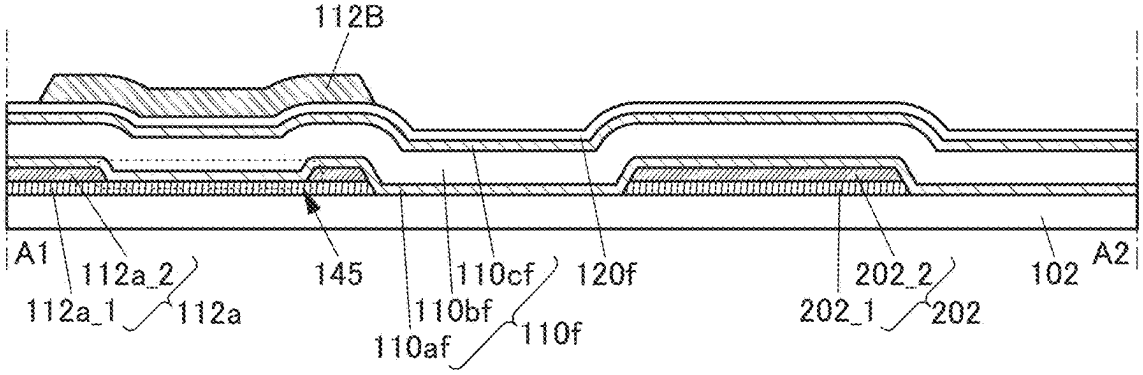


FIG. 26C

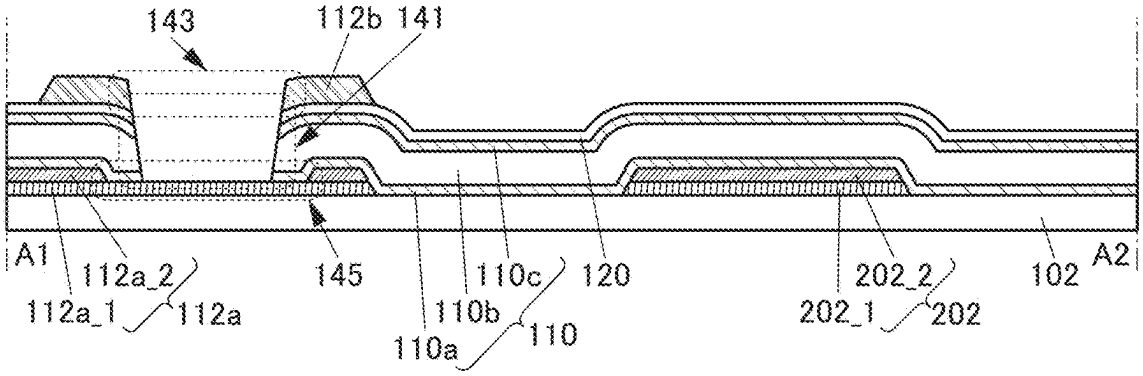


FIG. 26D

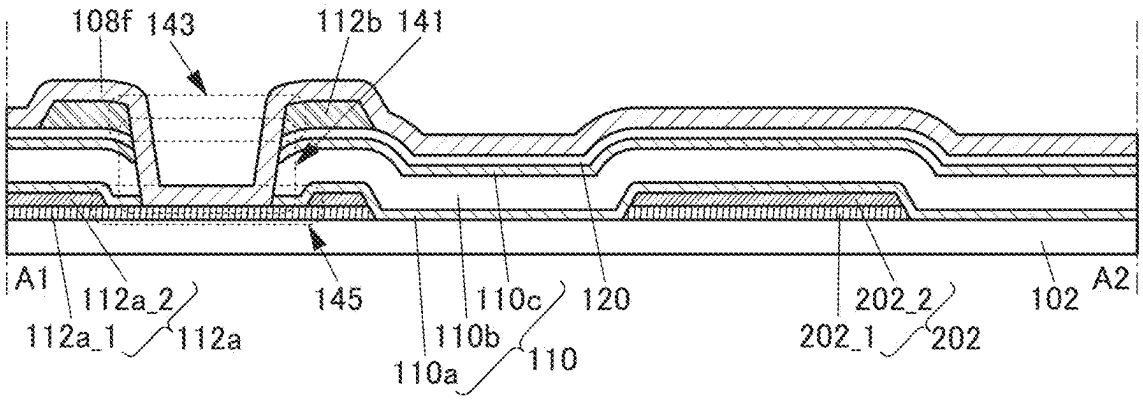


FIG. 27A

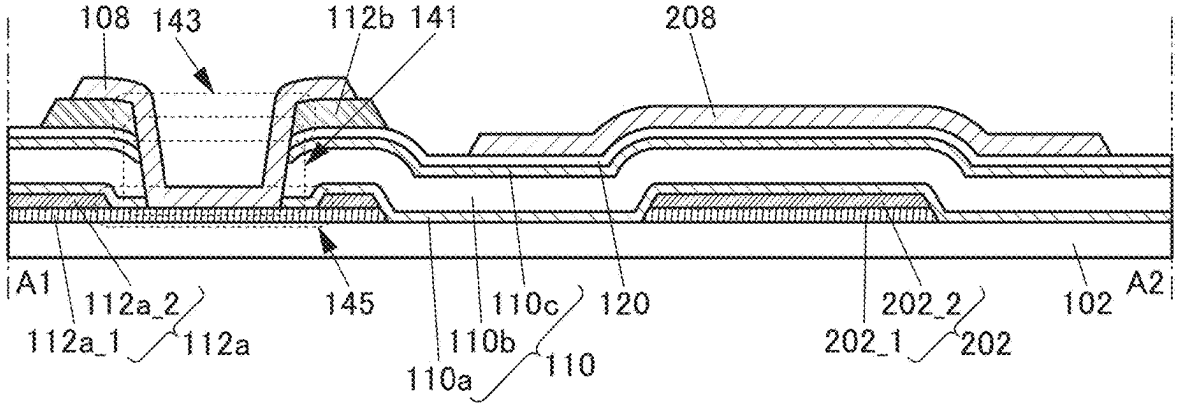


FIG. 27B

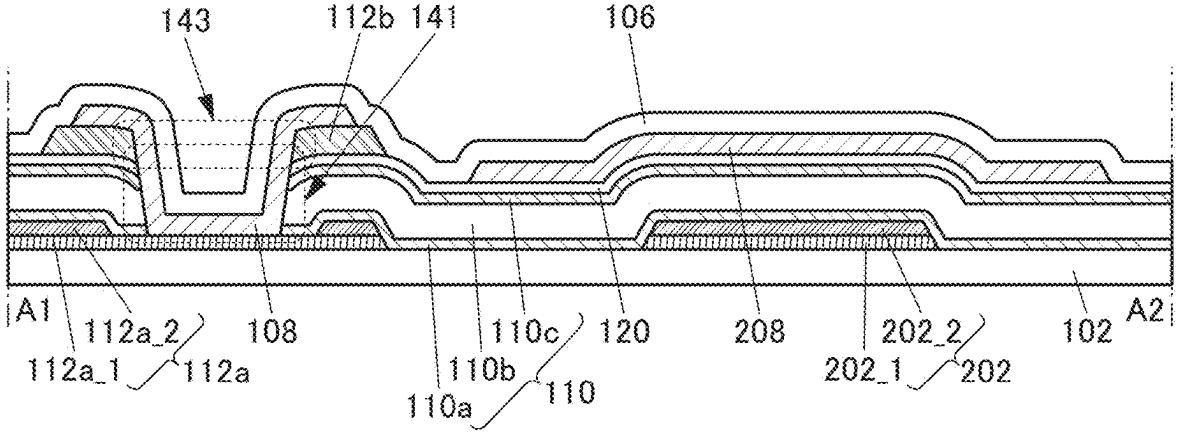


FIG. 27C

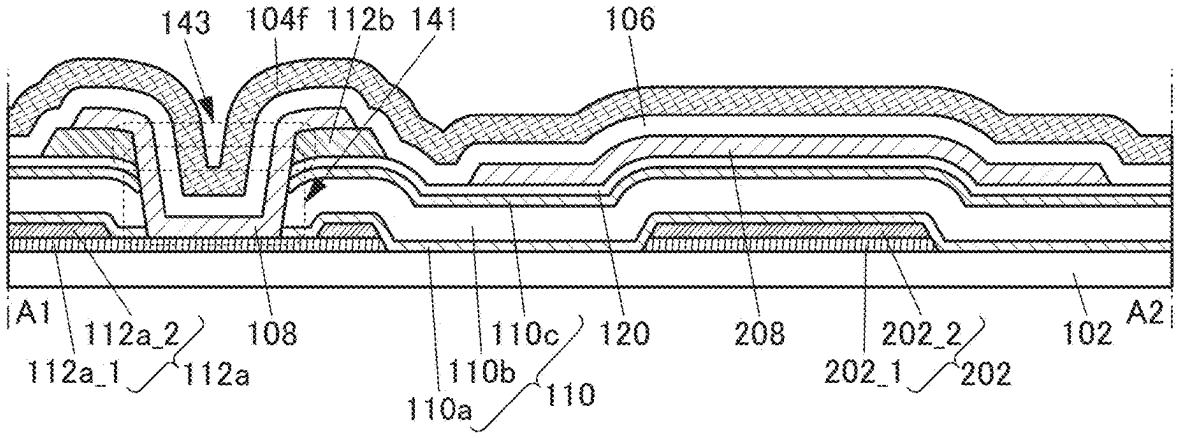


FIG. 28A

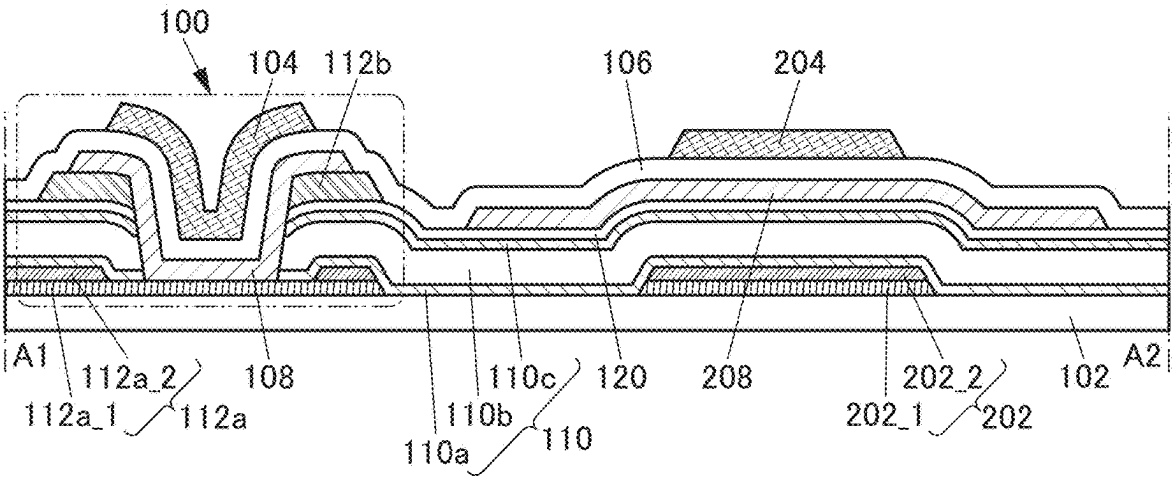


FIG. 28B

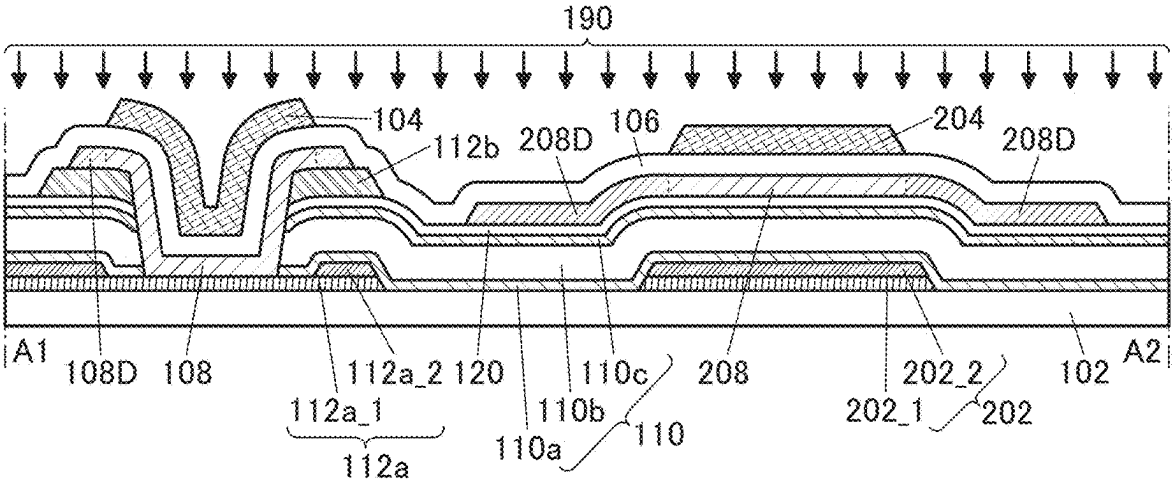


FIG. 28C

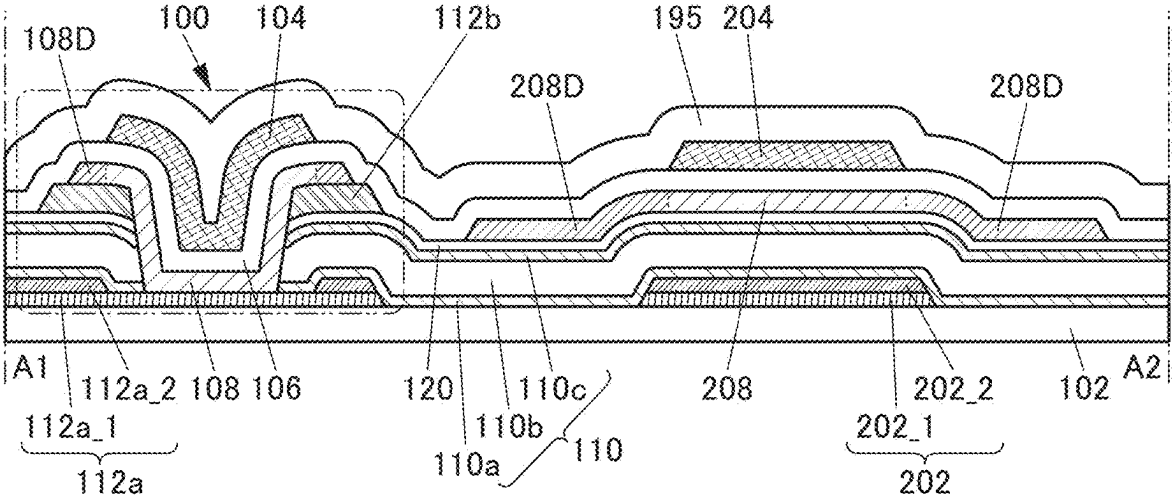


FIG. 29A

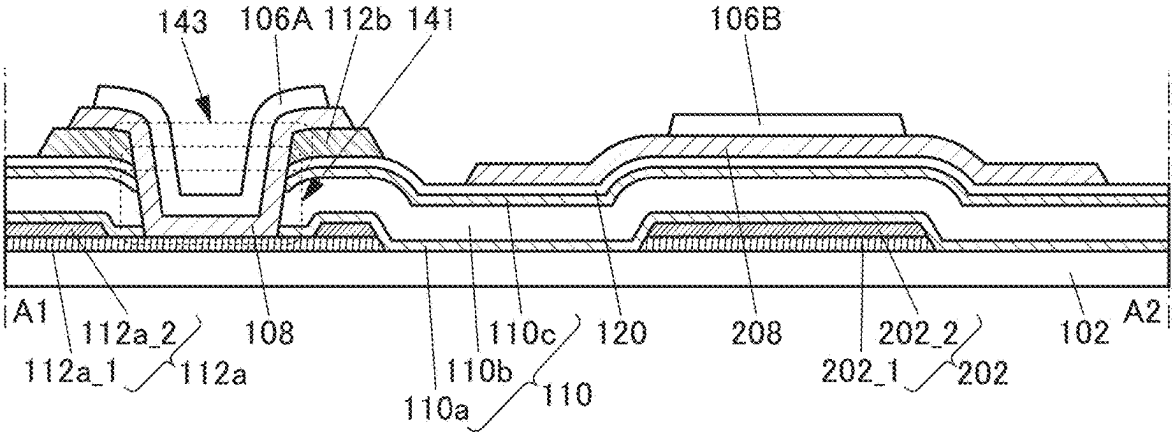


FIG. 29B

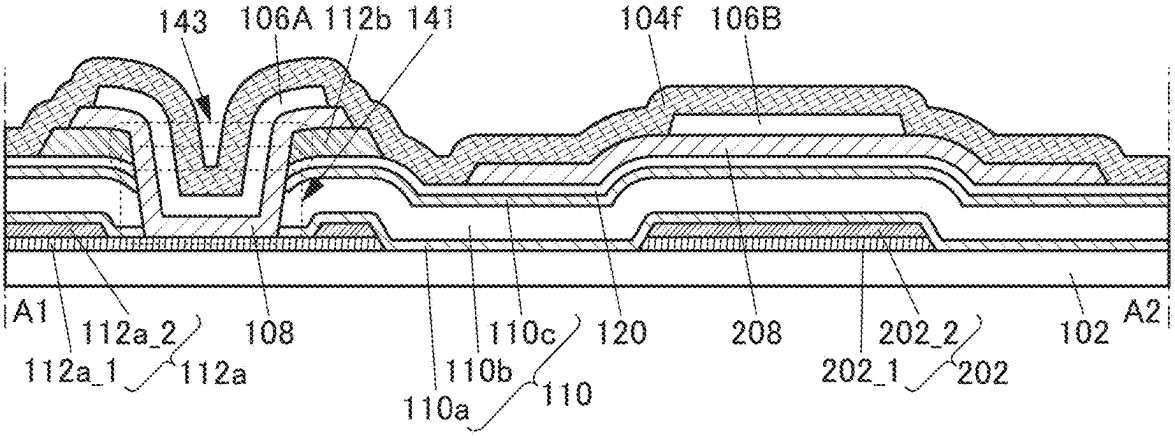


FIG. 30A

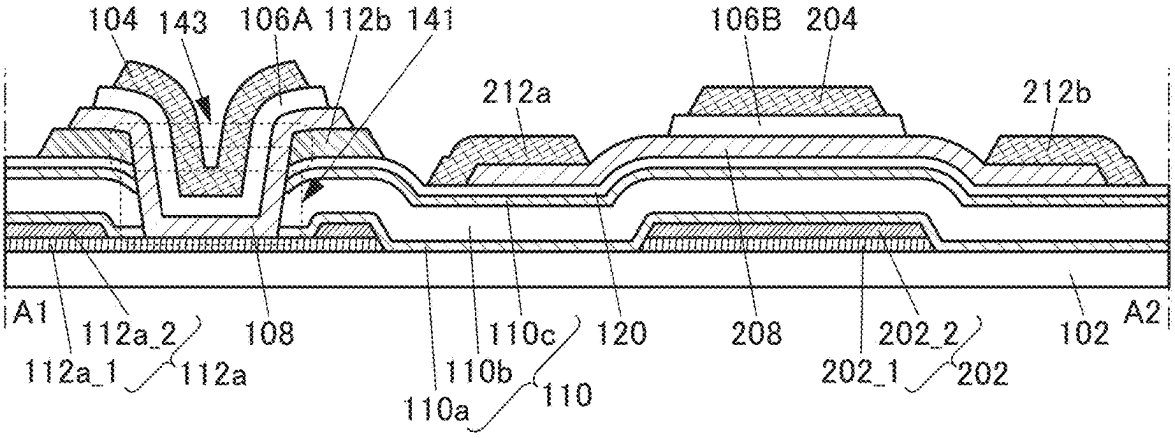


FIG. 30B

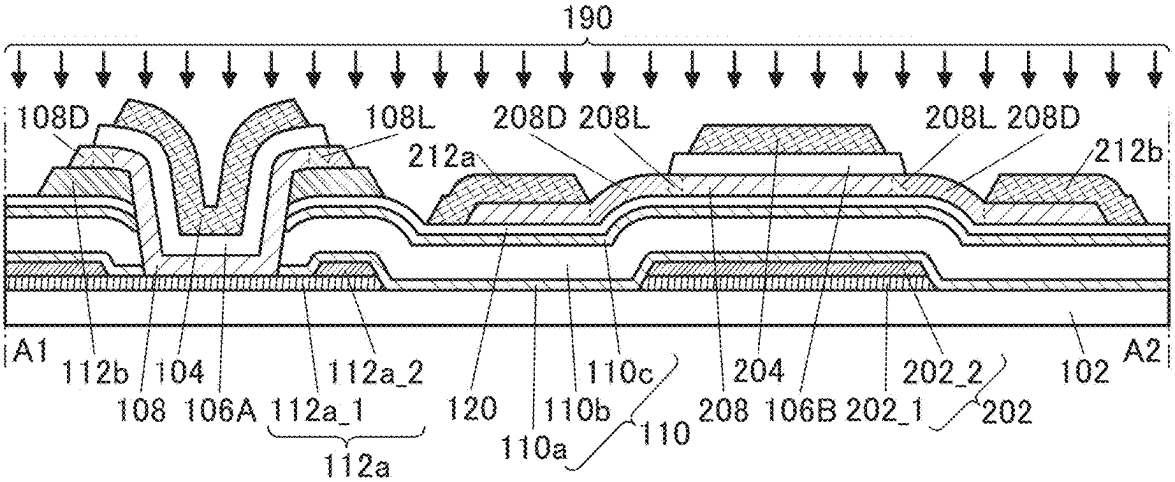


FIG. 31A

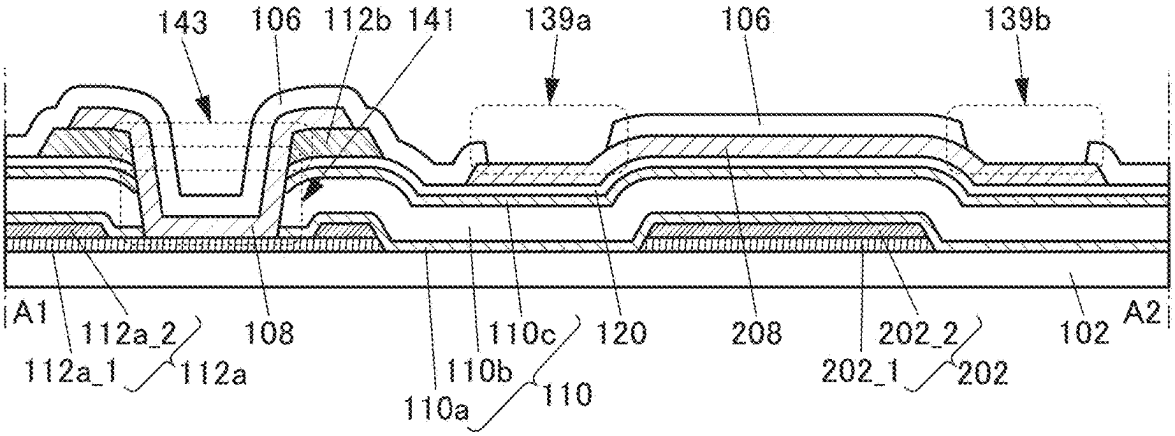


FIG. 31B

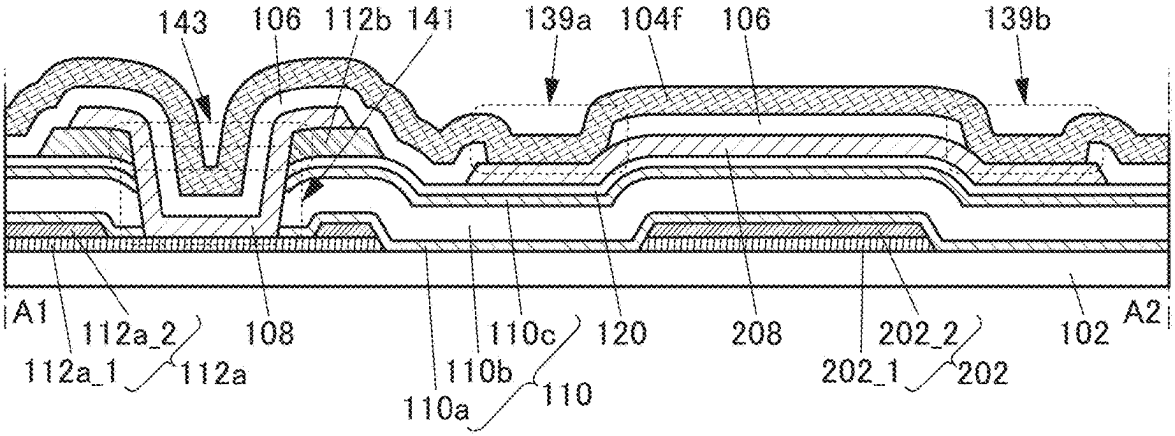


FIG. 32A

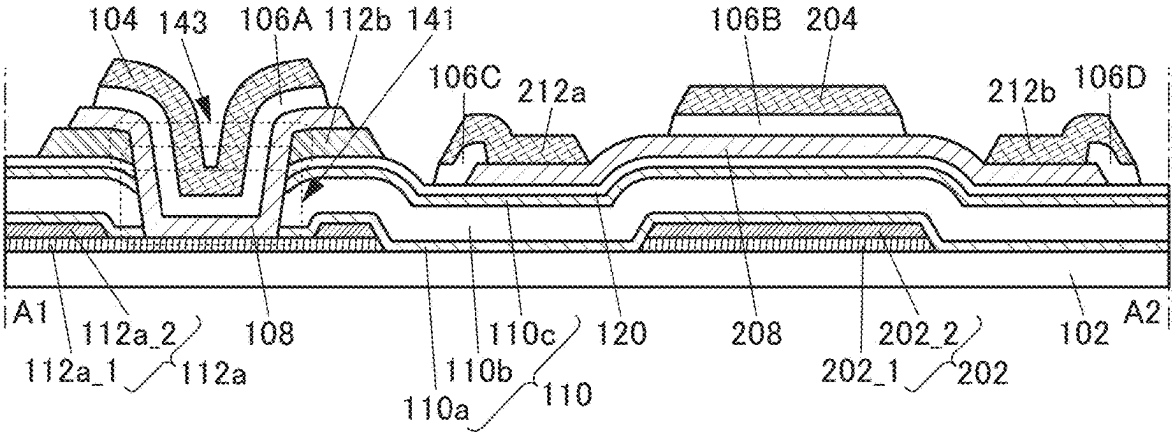


FIG. 32B

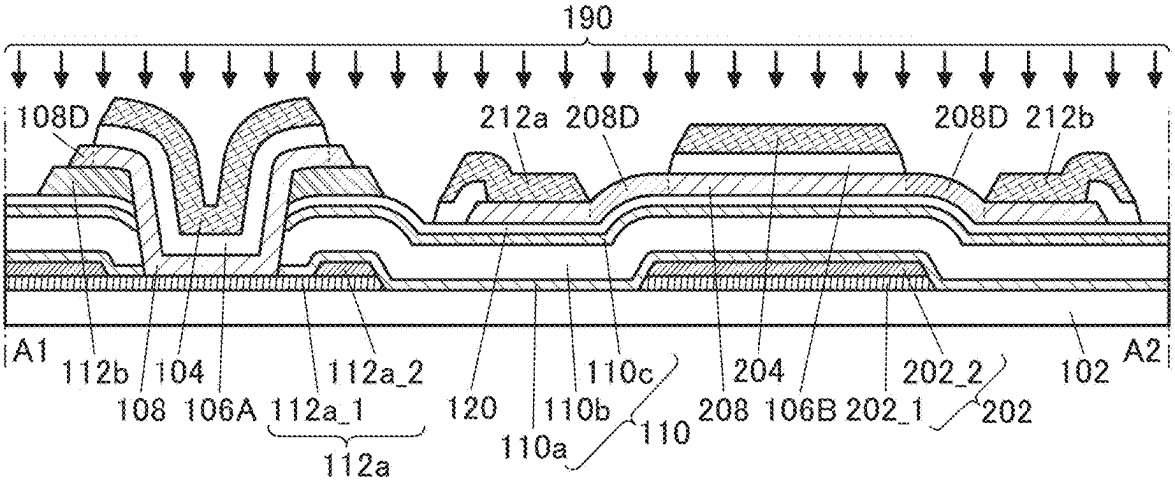


FIG. 33A

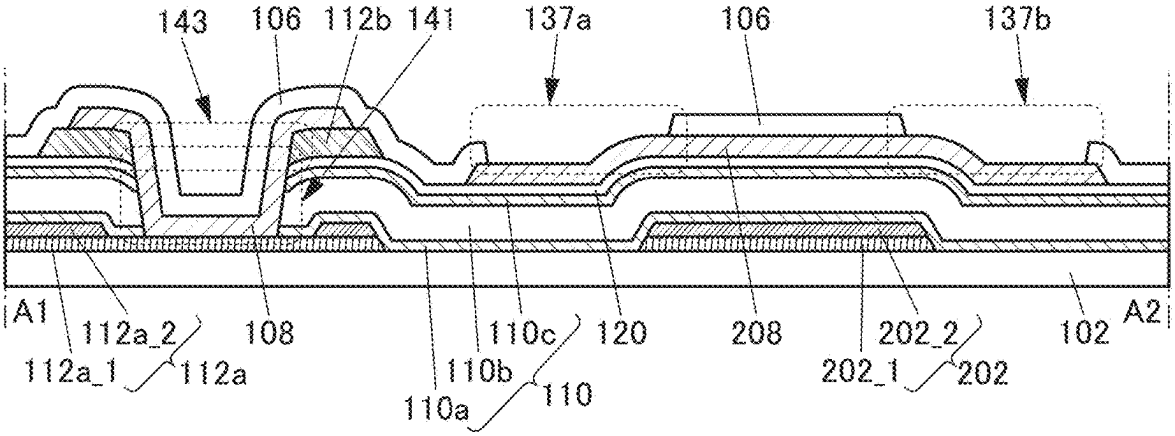


FIG. 33B

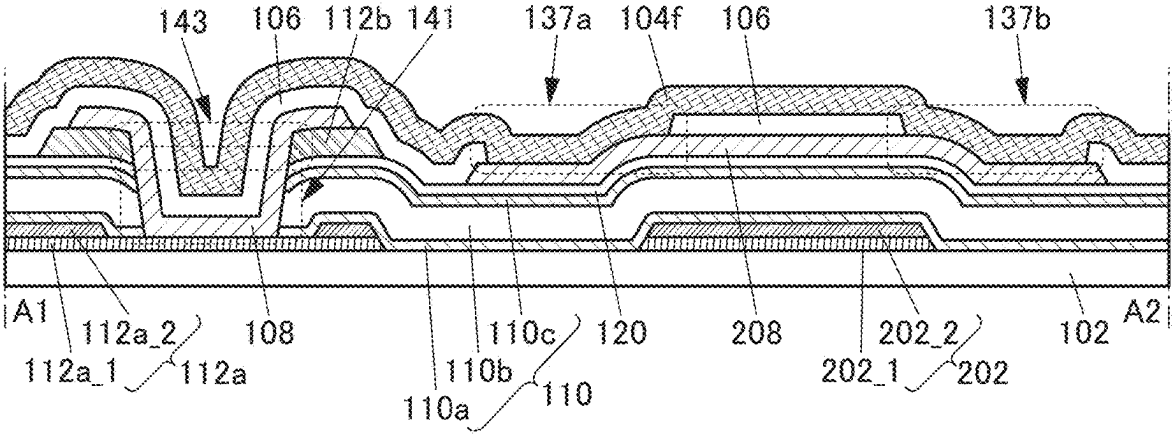


FIG. 34A

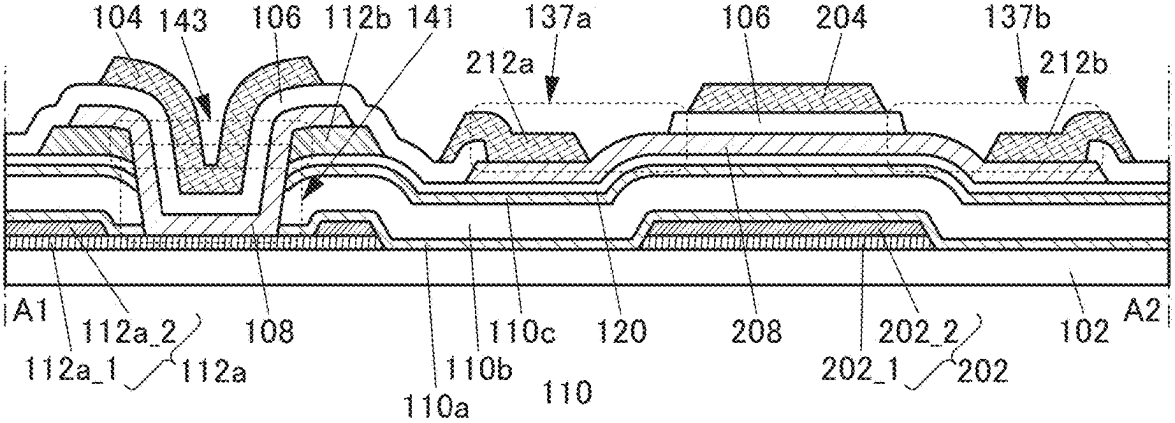


FIG. 34B

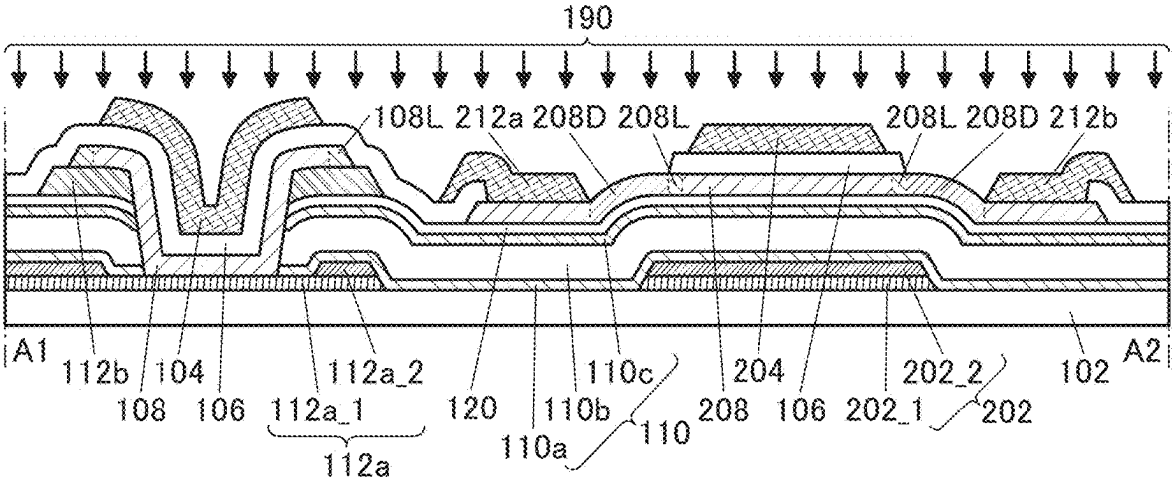


FIG. 35A

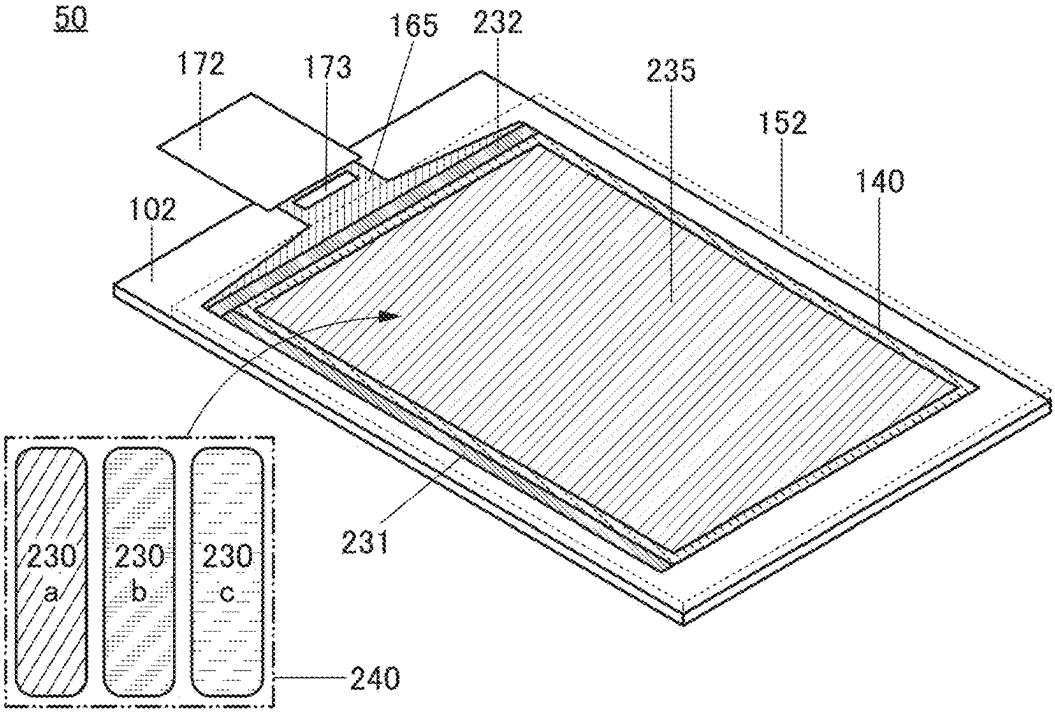


FIG. 35B

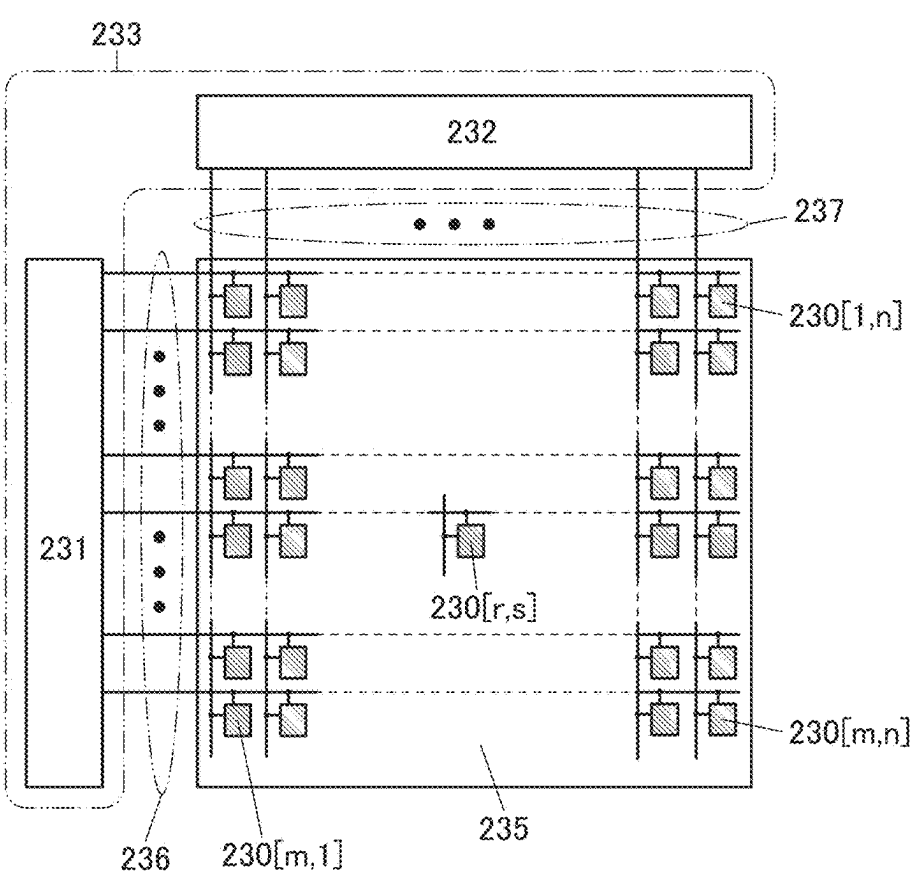


FIG. 36A

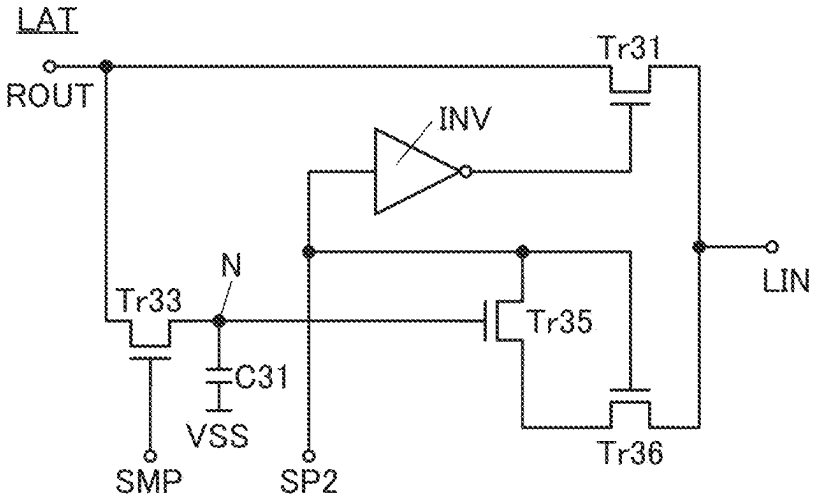


FIG. 36B

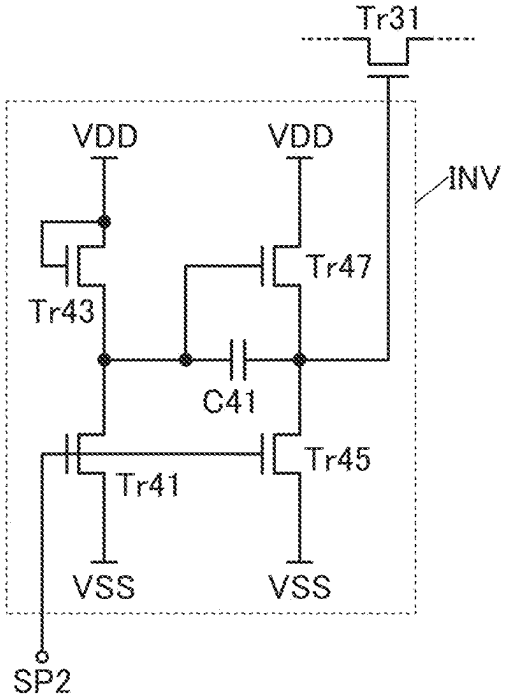


FIG. 37A

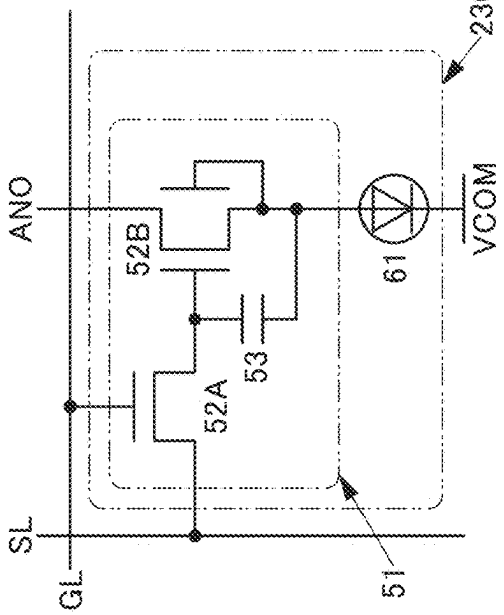


FIG. 37B

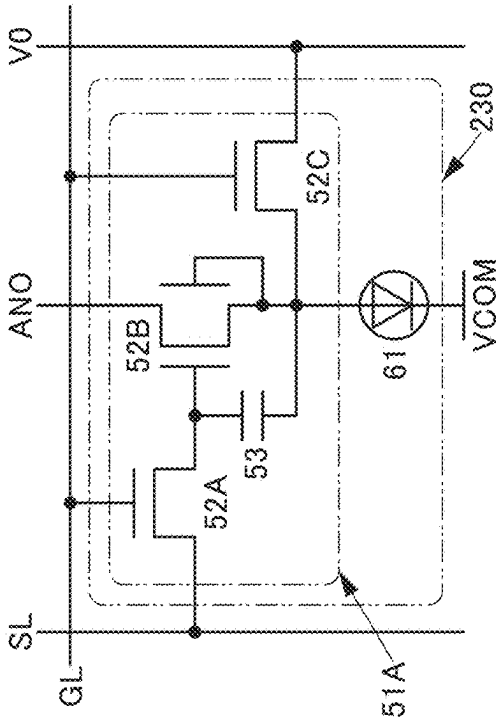
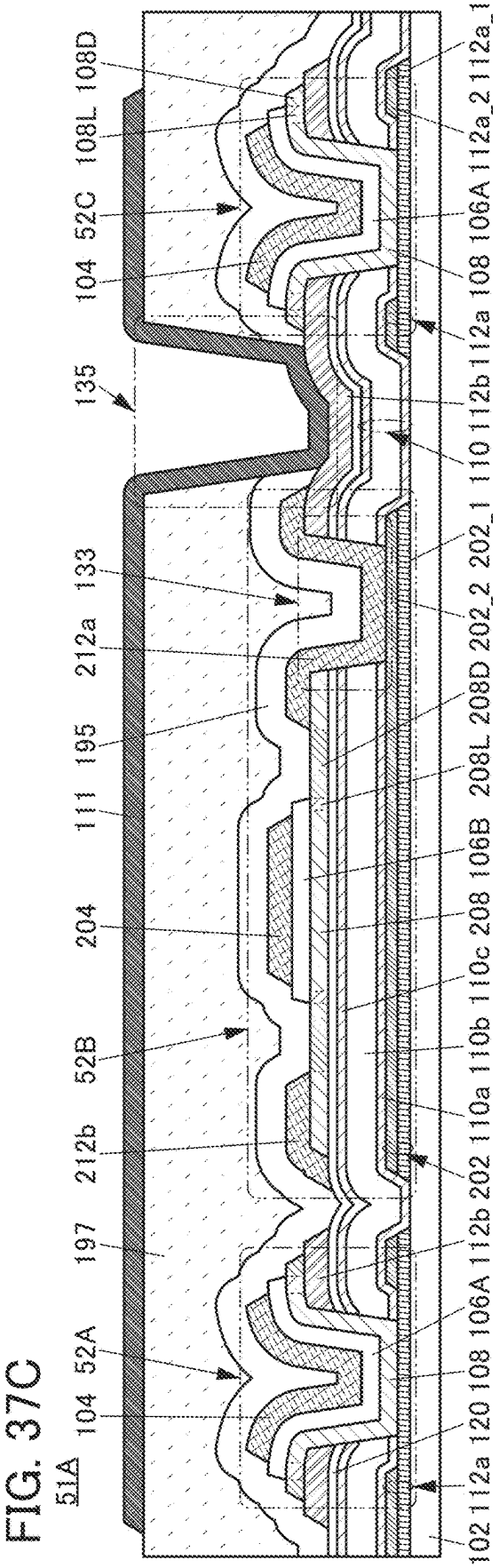


FIG. 37C



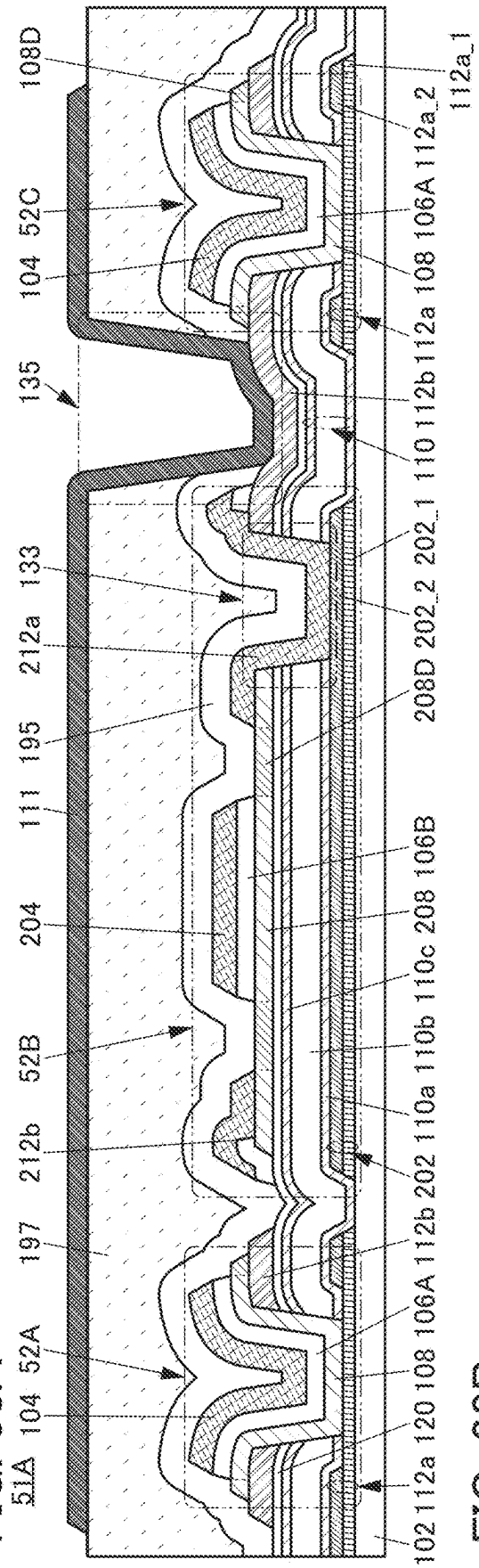


FIG. 38A

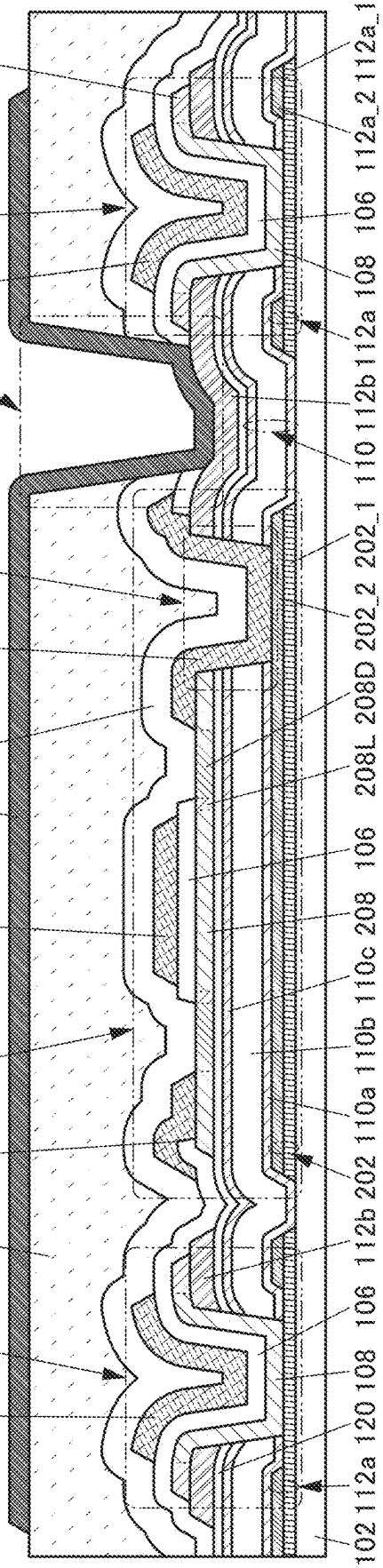


FIG. 38B

FIG. 39

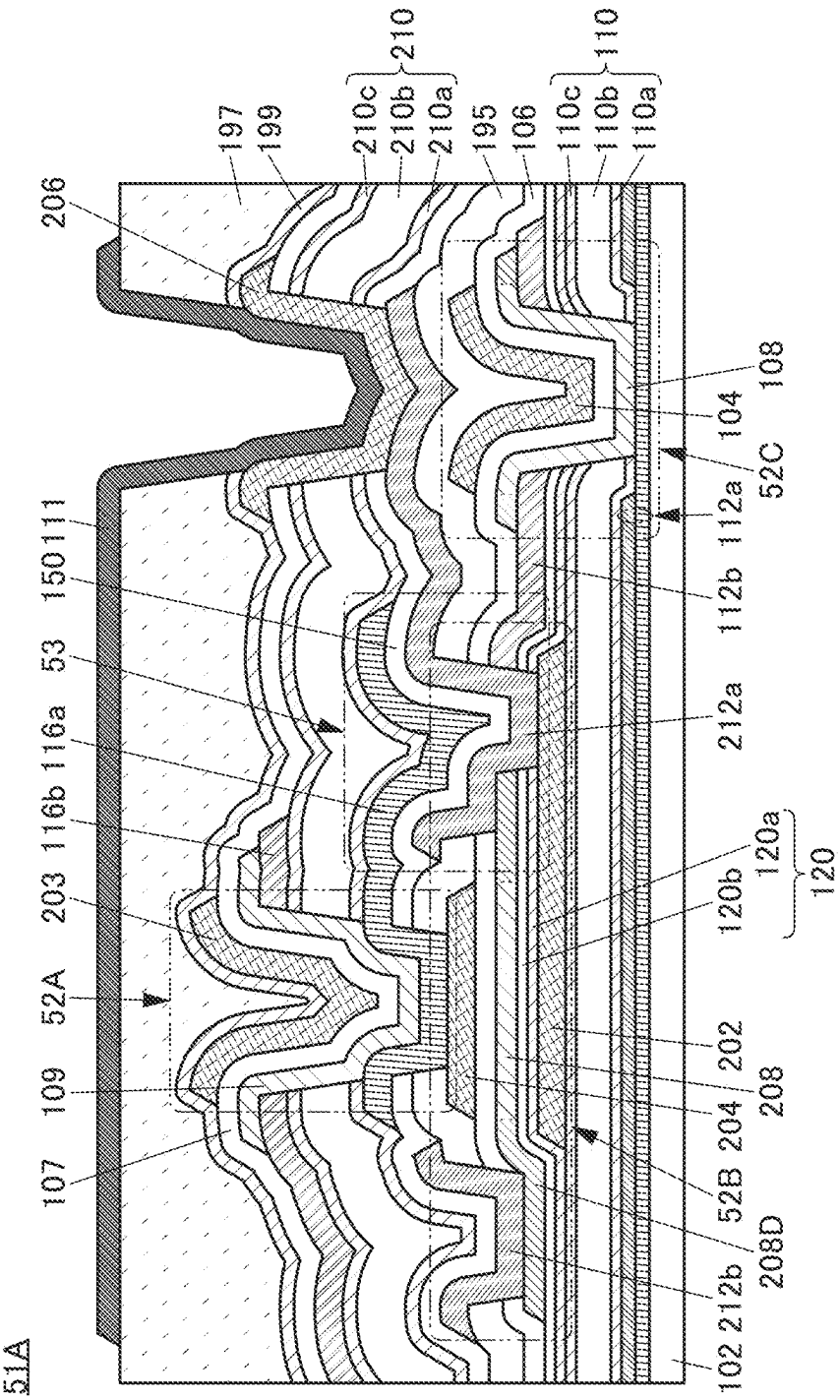

51A
206
197
199
210c
210b
210a
210
195
106
110c
110b
110a
110
108
104
52C
112a
112b
212a
120a
120b
120
202
208
204
52B
208D
212b
102
107
109
52A
203
116b
116a
53
150
111

FIG. 40

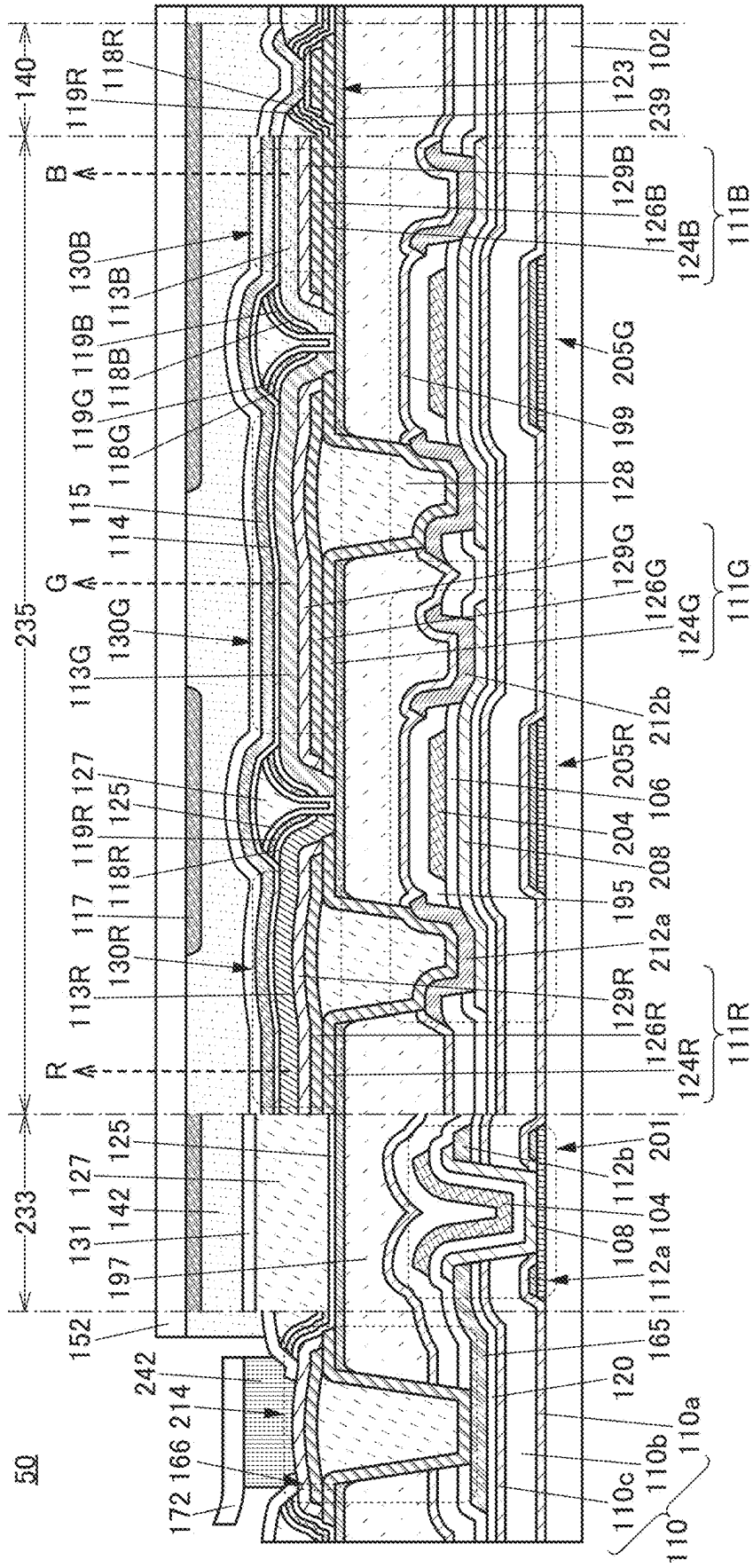

50
140
233
235
R
G
B
118R
119R
130B
113B
119B
118B
119G
118G
115
114
130G
113G
127
125
119R
118R
117
130R
113R
125
127
142
131
197
152
242
214
166
172
120
165
112a
104
108
112b
201
212a
195
208
204
106
205R
212b
129R
126R
124R
111R
129G
126G
124G
111G
128
199
205G
129B
126B
124B
111B
123
239
102
110a
110b
110c
110

FIG. 41A

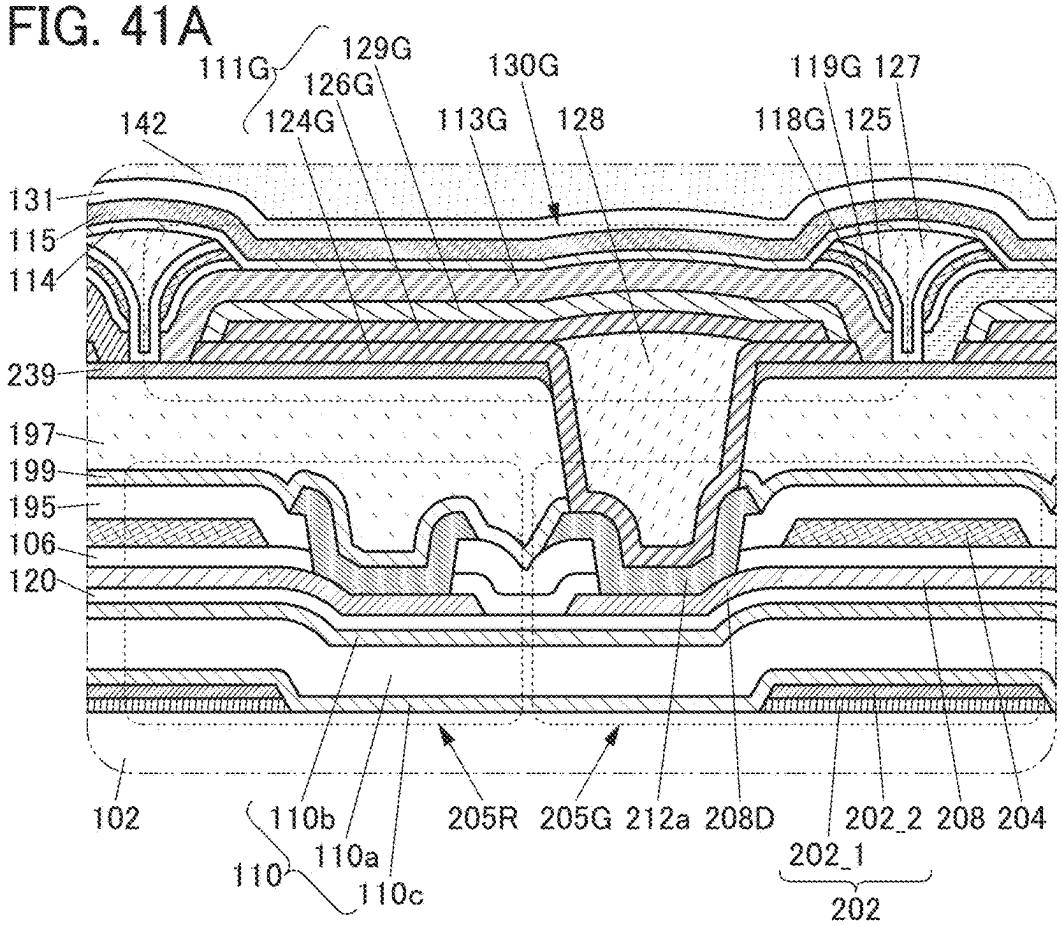


FIG. 41B

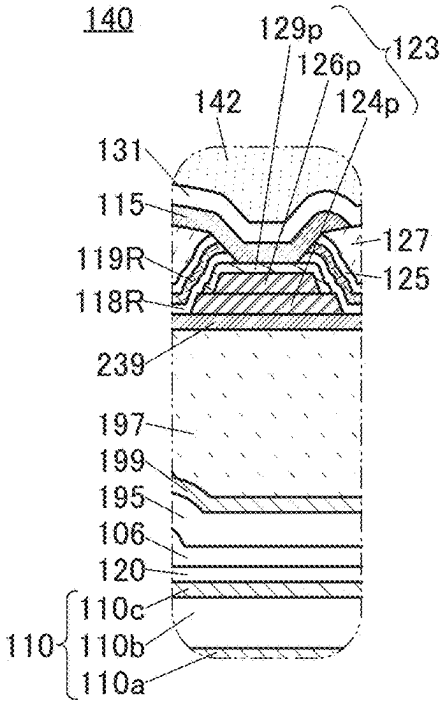


FIG. 41C

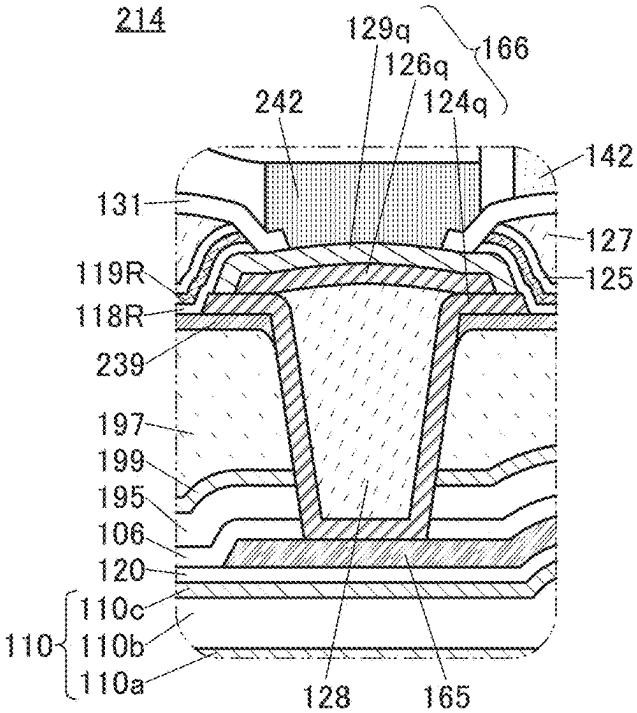


FIG. 42

50A

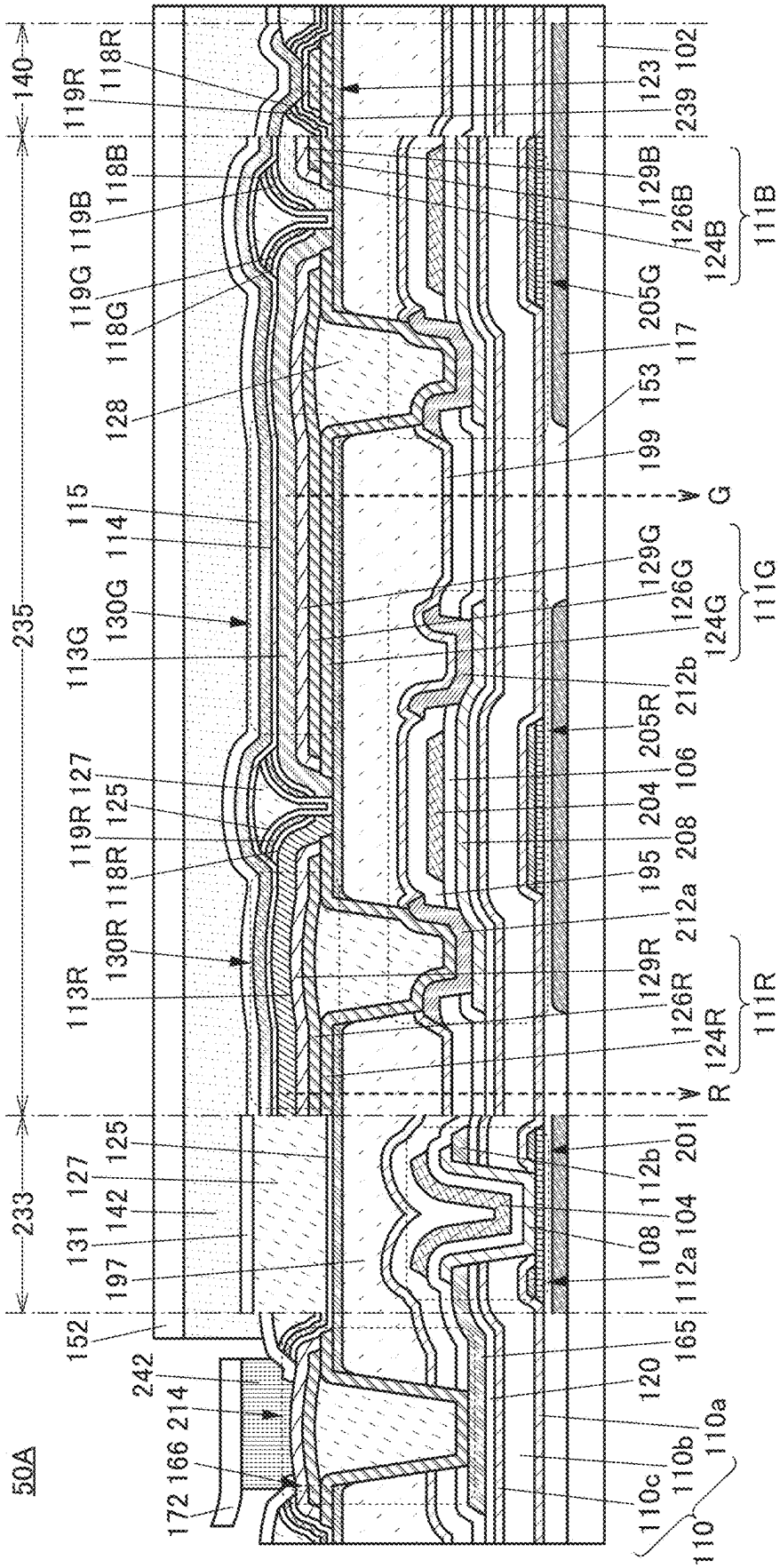

140
235
233
118R
119R
118B
119B
119G
118G
128
115
114
130G
113G
119R
127
125
118R
130R
113R
125
127
142
131
197
152
242
214
166
172
123
102
239
129B
126B
124B
111B
205G
117
153
199
G
129G
126G
124G
111G
212b
205R
106
204
208
195
212a
129R
126R
124R
111R
R
201
112b
104
108
112a
165
120
110a
110b
110c
110

FIG. 43A

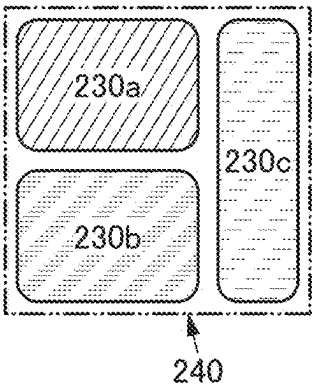


FIG. 43B

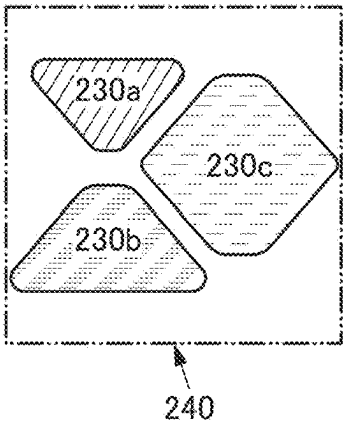


FIG. 43C

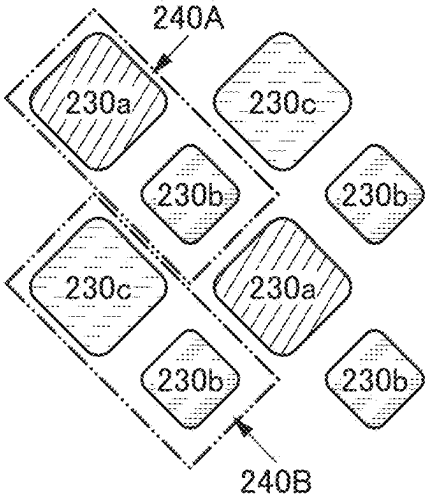


FIG. 43D

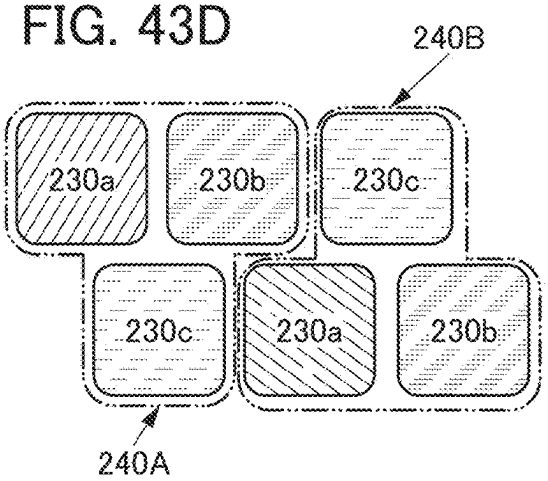


FIG. 43E

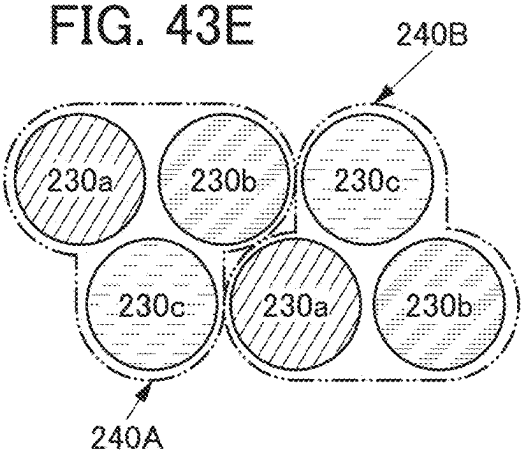


FIG. 43F

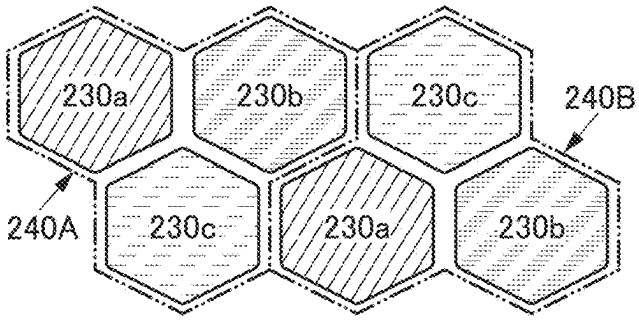


FIG. 43G

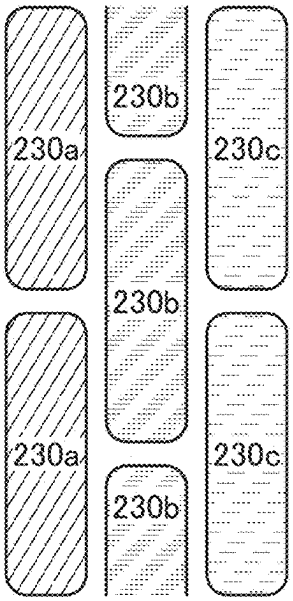


FIG. 44A

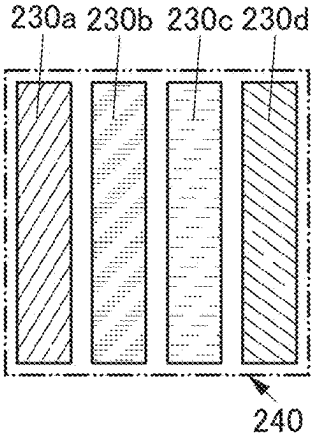


FIG. 44B

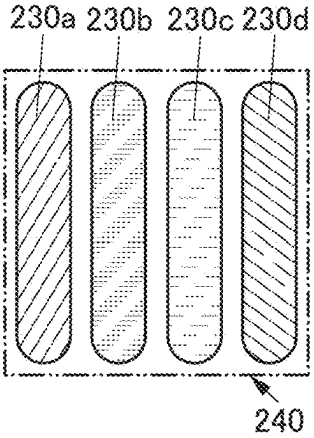


FIG. 44C

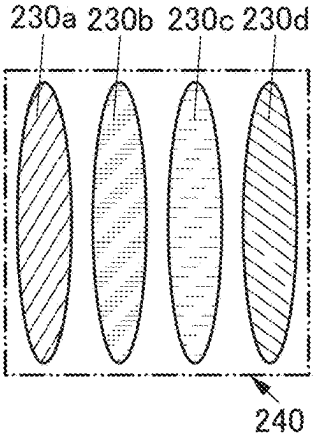


FIG. 44D

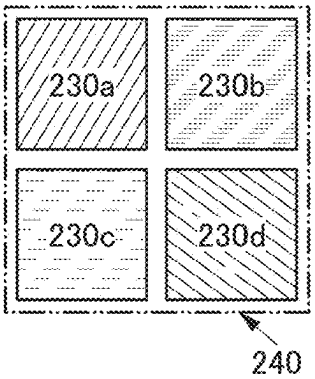


FIG. 44E

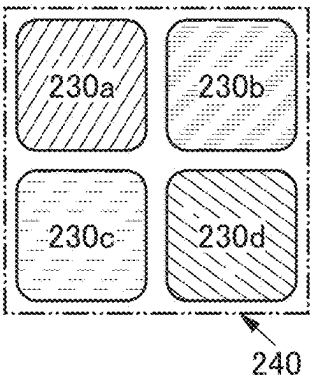


FIG. 44F

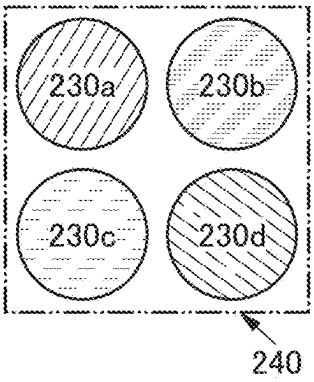


FIG. 44G

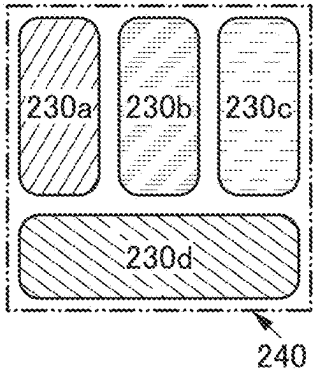


FIG. 44H

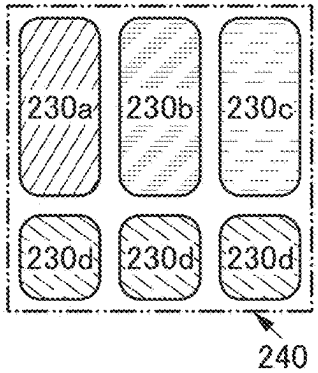


FIG. 44I

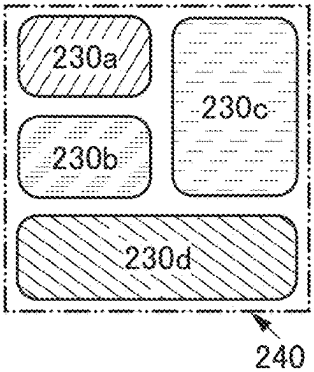


FIG. 44J

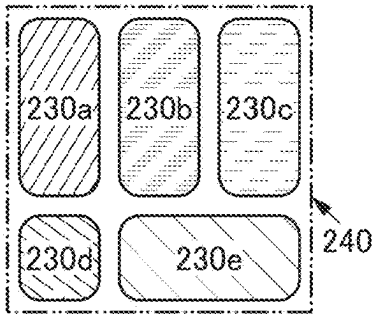


FIG. 44K

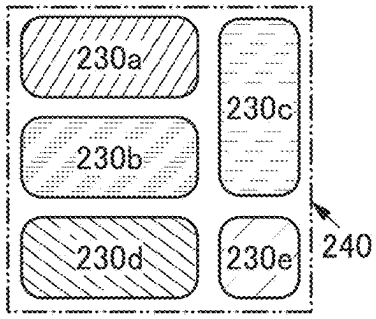


FIG. 45A

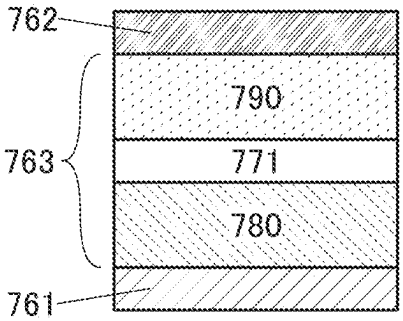


FIG. 45B

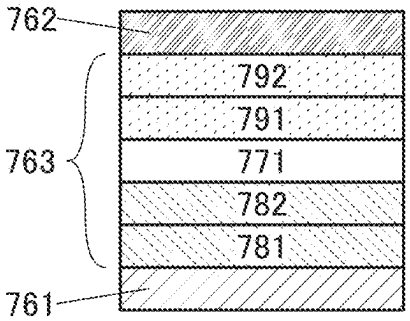


FIG. 45C

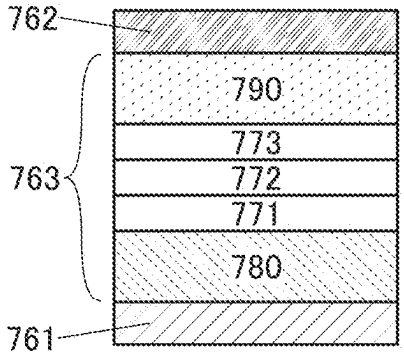


FIG. 45D

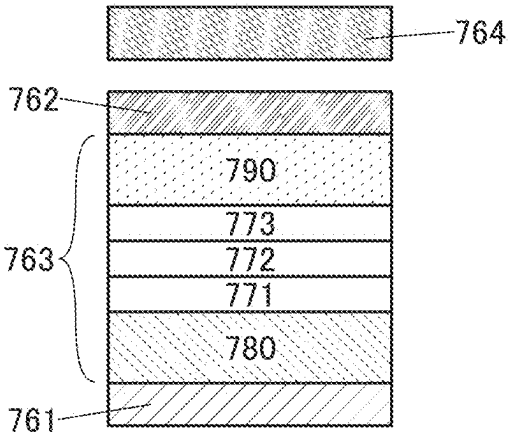


FIG. 45E

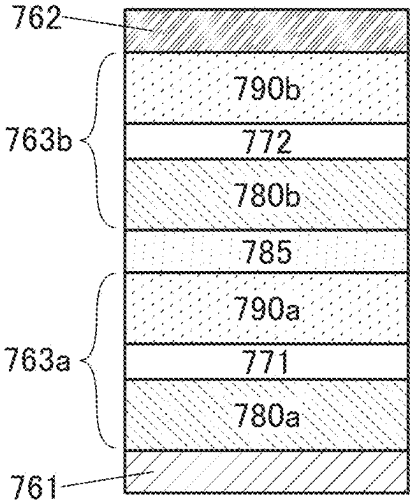


FIG. 45F

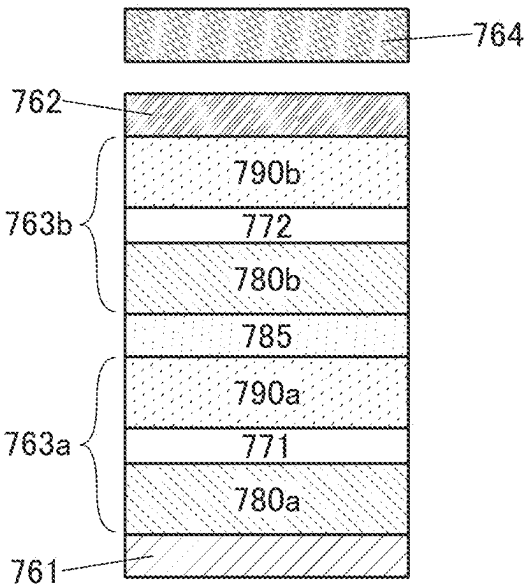


FIG. 46A

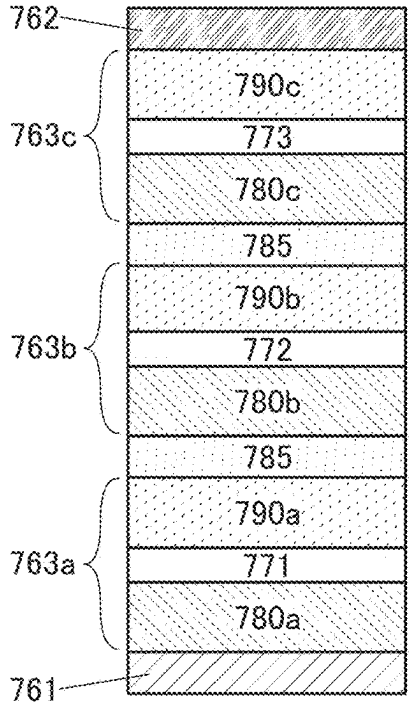


FIG. 46B

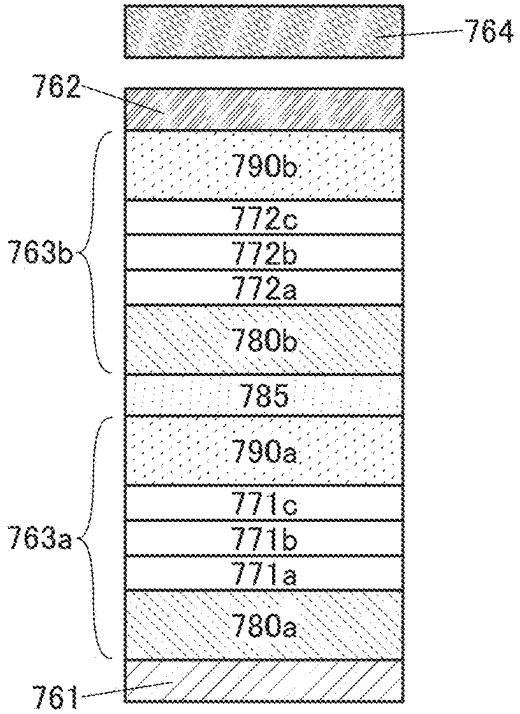


FIG. 46C

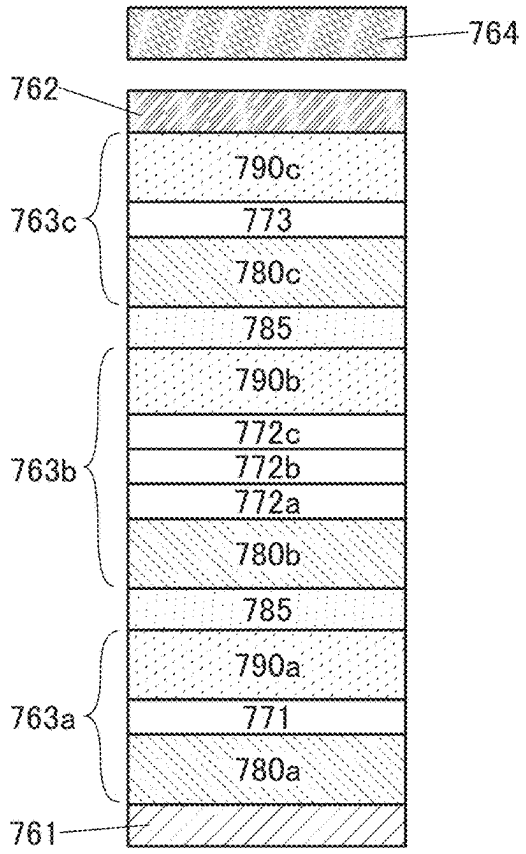


FIG. 47A

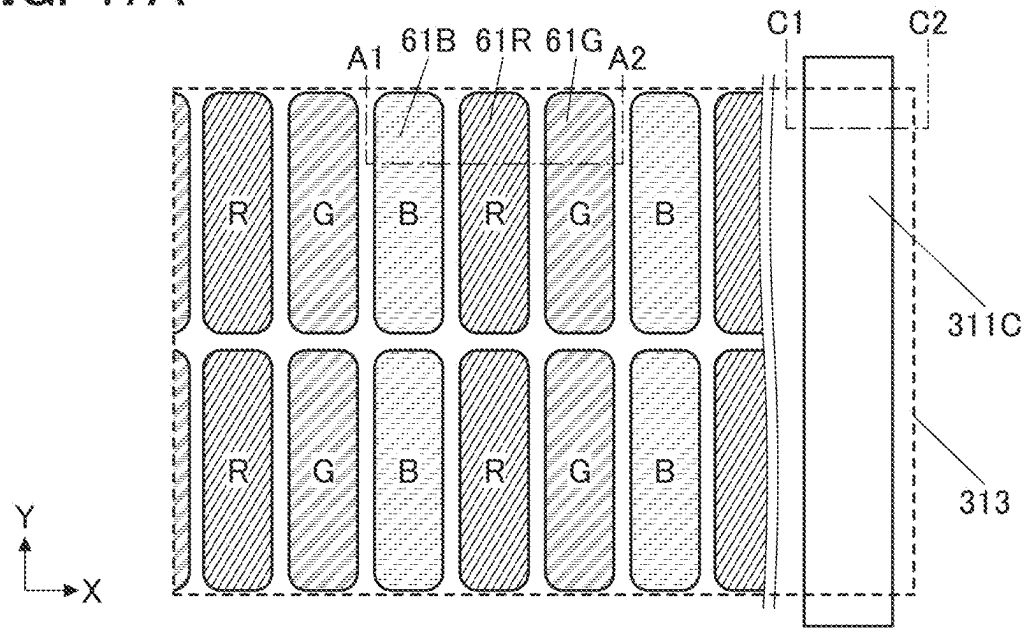


FIG. 47B

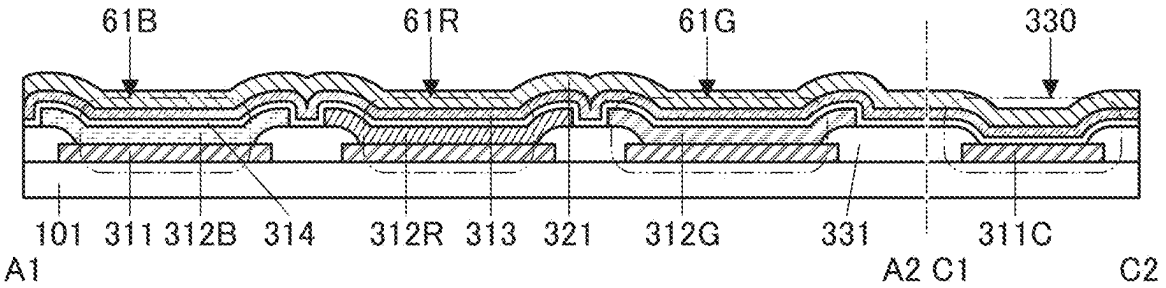


FIG. 48A

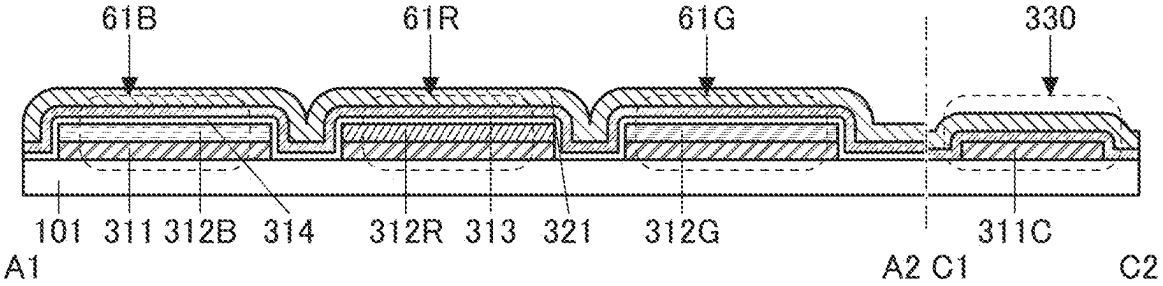


FIG. 48B

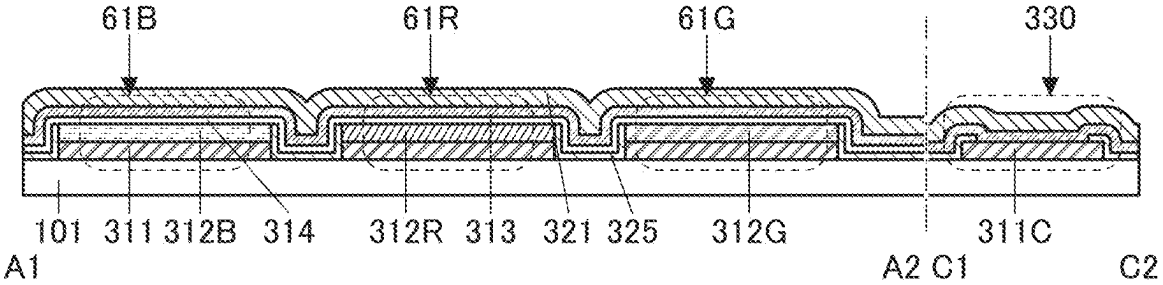


FIG. 48C

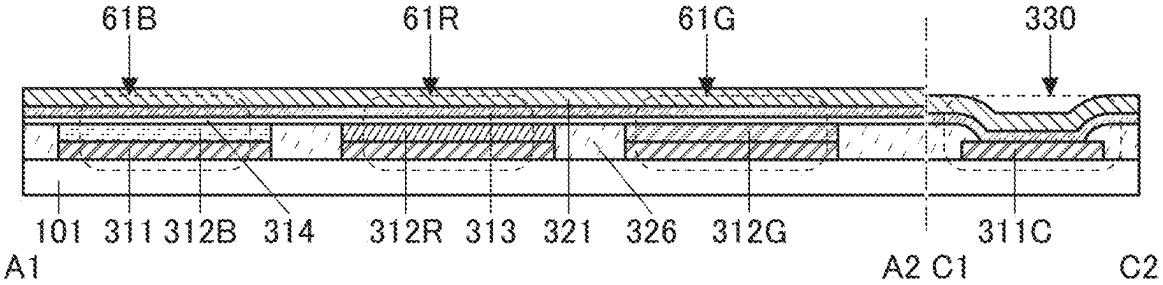


FIG. 48D

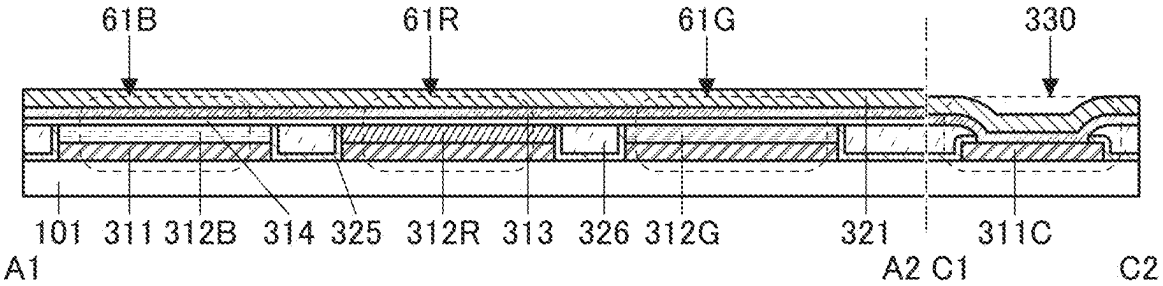


FIG. 49A

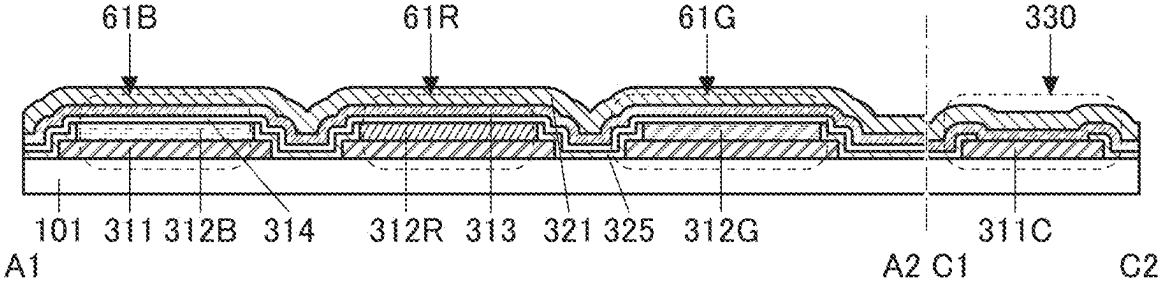


FIG. 49B

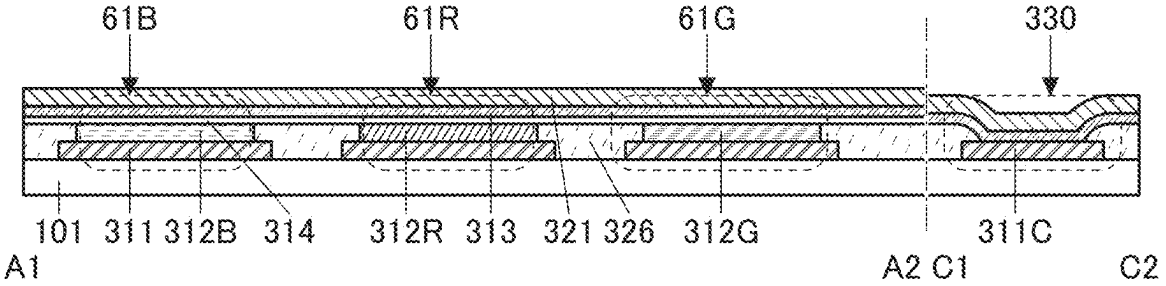


FIG. 49C

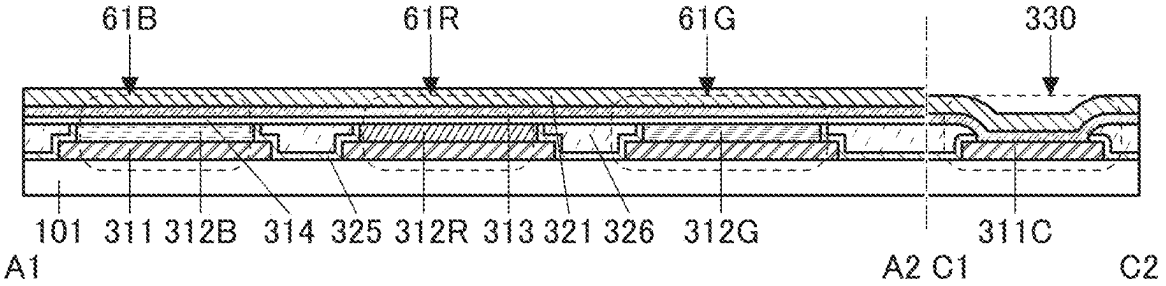


FIG. 50A

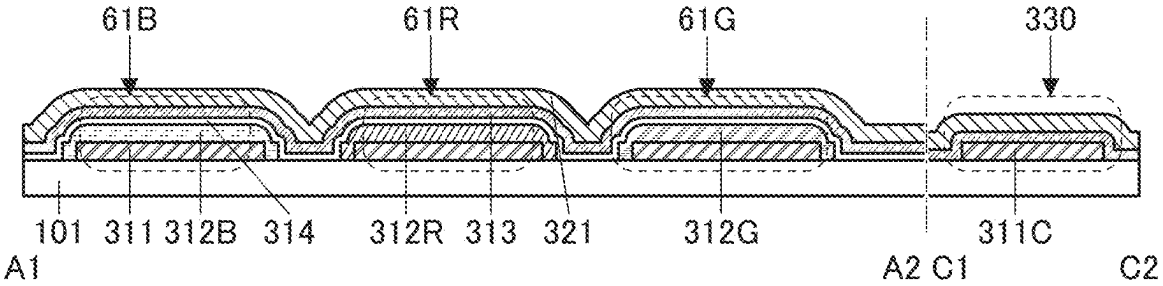


FIG. 50B

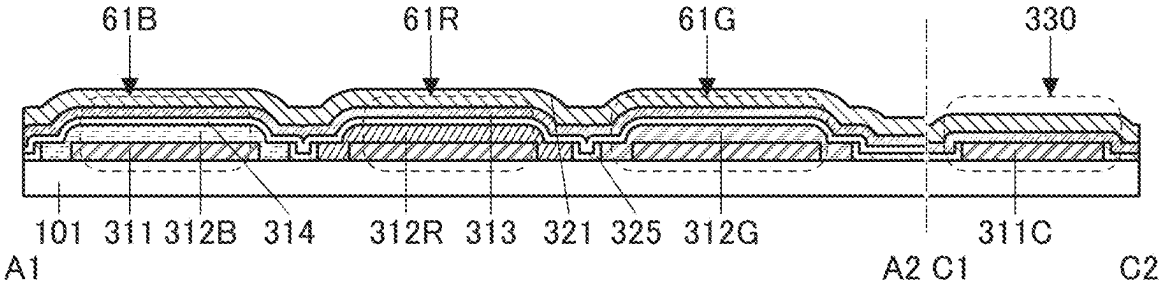


FIG. 50C

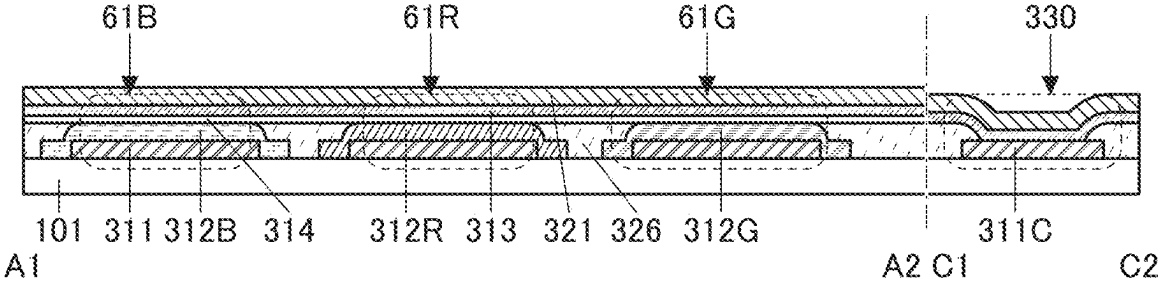


FIG. 50D

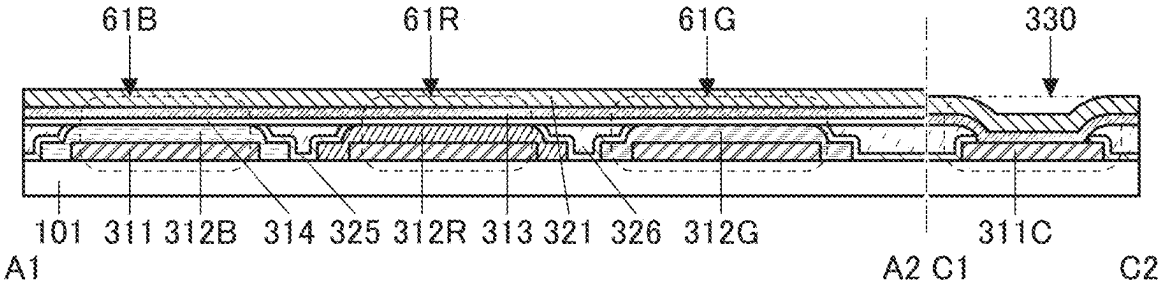


FIG. 51A

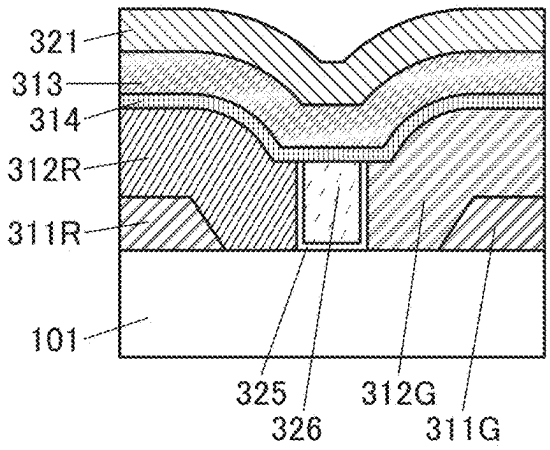


FIG. 51D

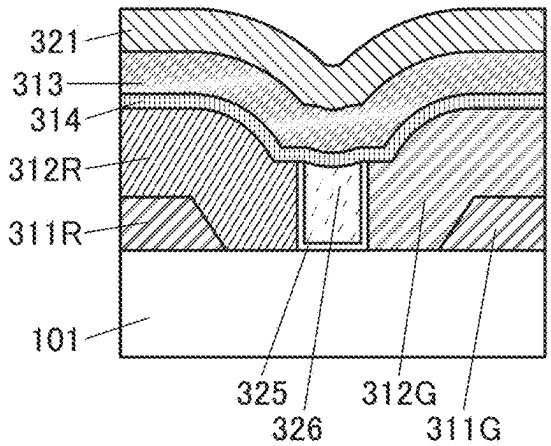


FIG. 51B

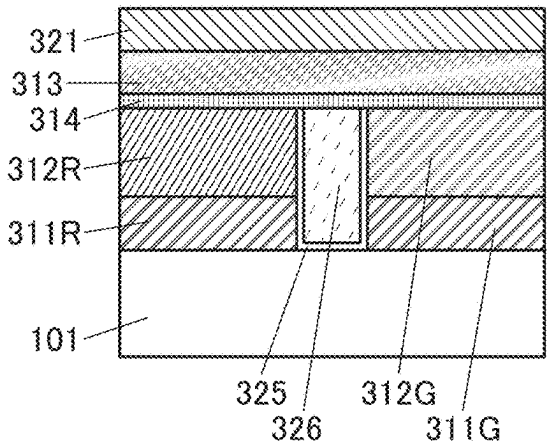


FIG. 51E

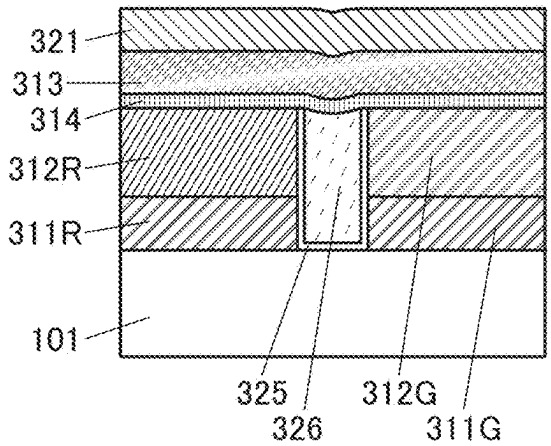


FIG. 51C

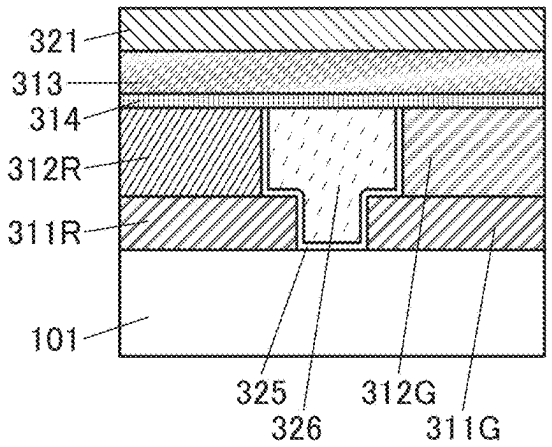


FIG. 51F

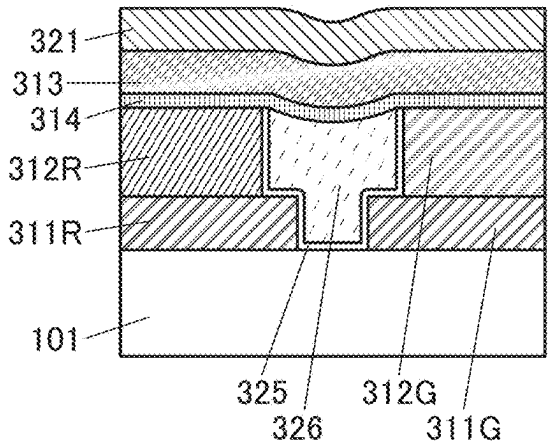


FIG. 52A

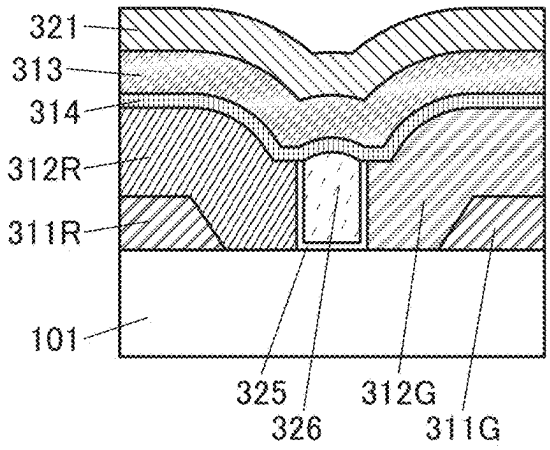


FIG. 52D

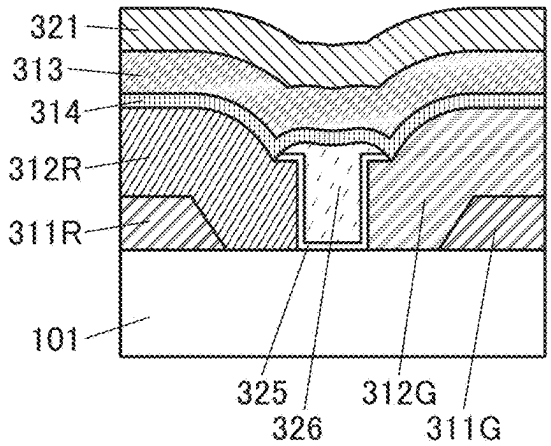


FIG. 52B

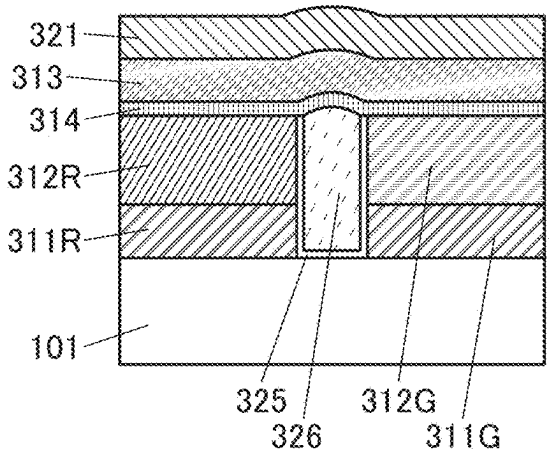


FIG. 52E

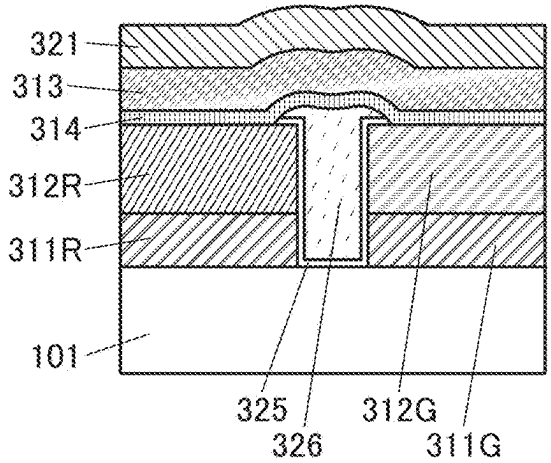


FIG. 52C

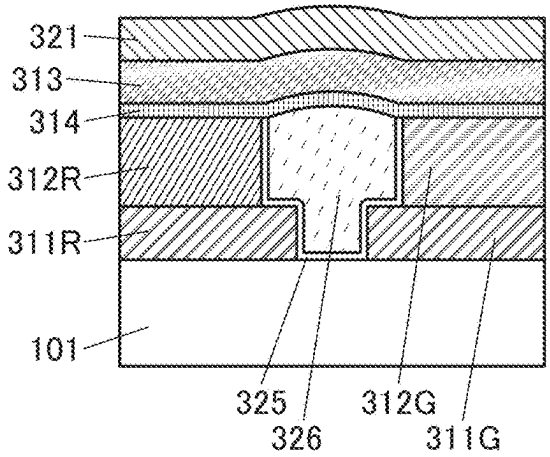


FIG. 52F

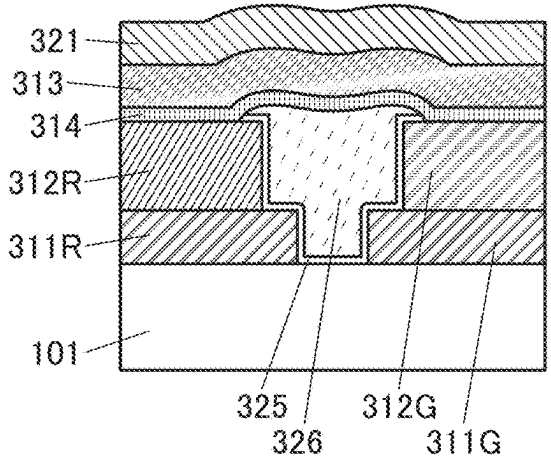


FIG. 53A

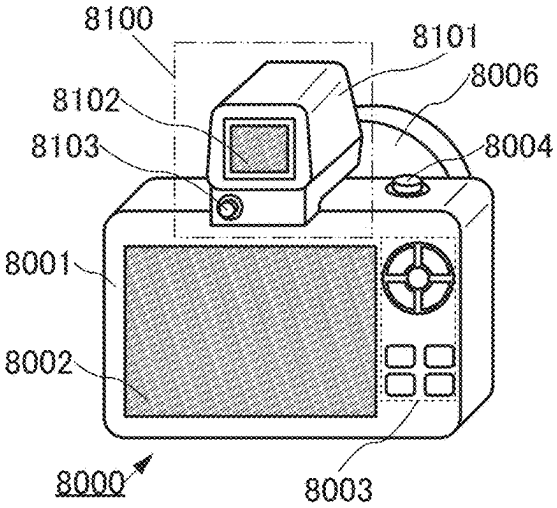


FIG. 53B

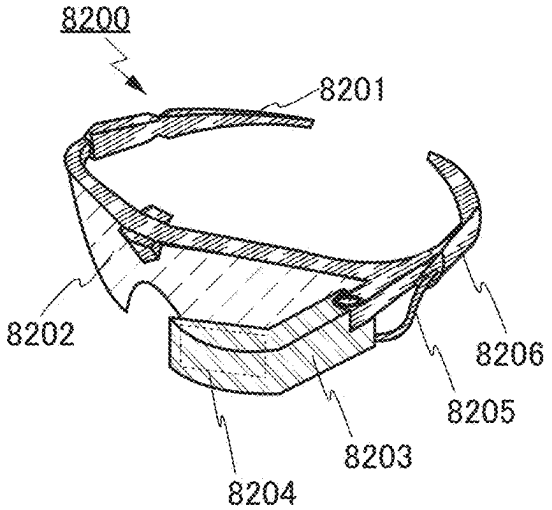


FIG. 53C

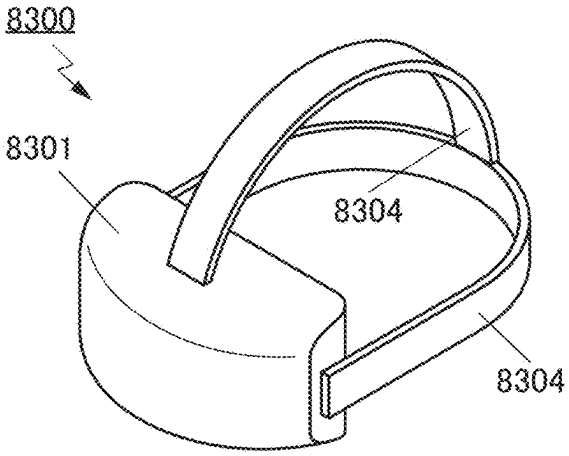


FIG. 53D

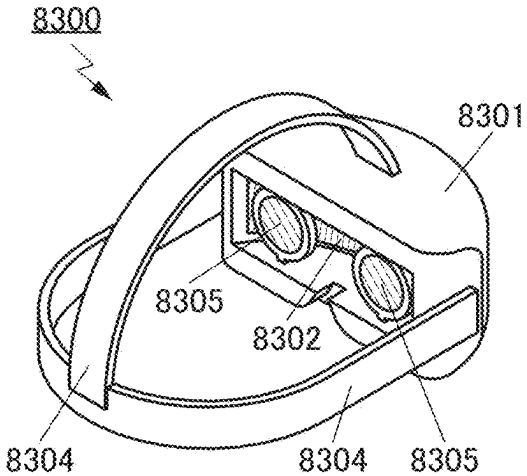


FIG. 53E

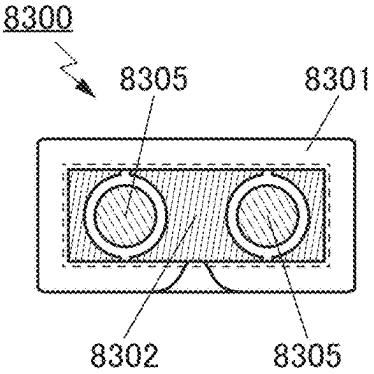


FIG. 53F

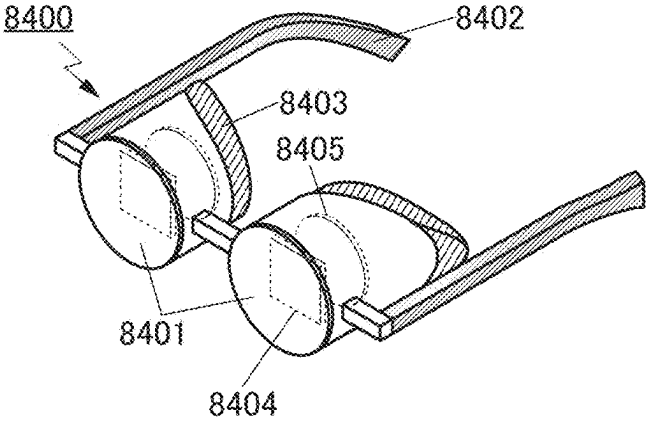


FIG. 54A

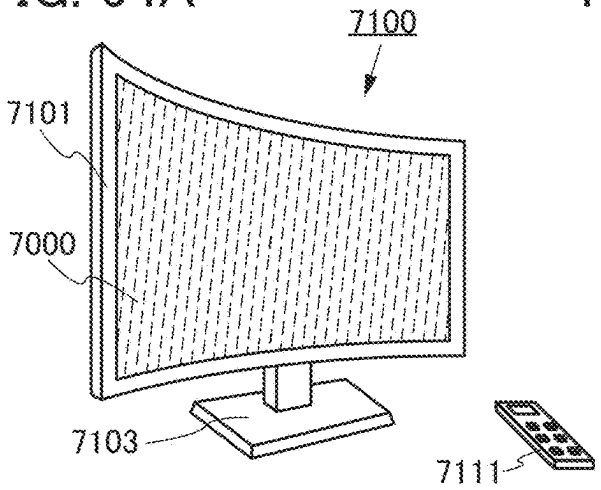


FIG. 54B

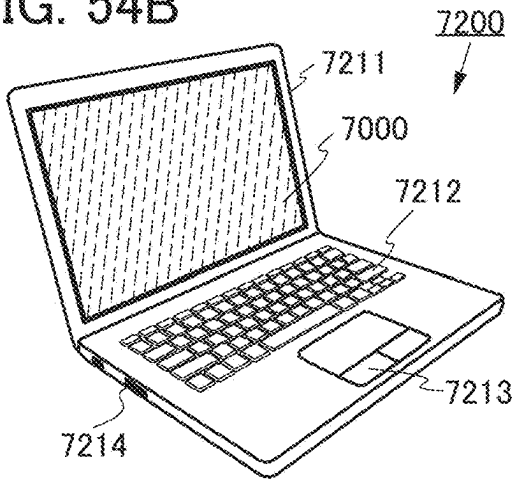


FIG. 54C

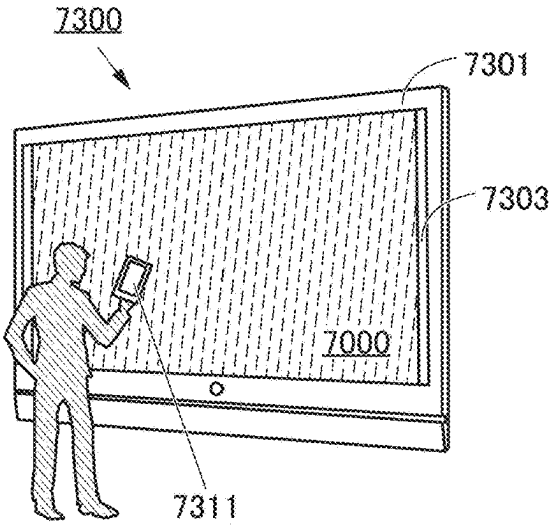


FIG. 54D

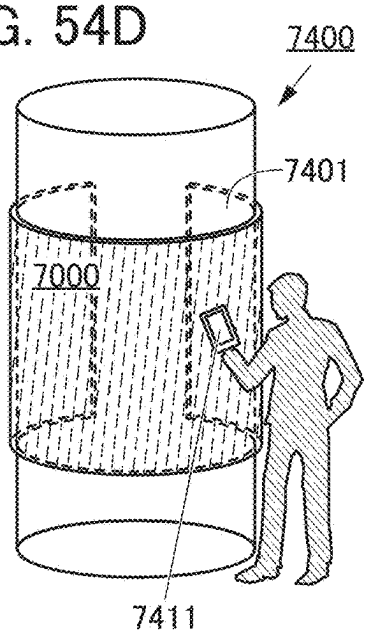


FIG. 54E

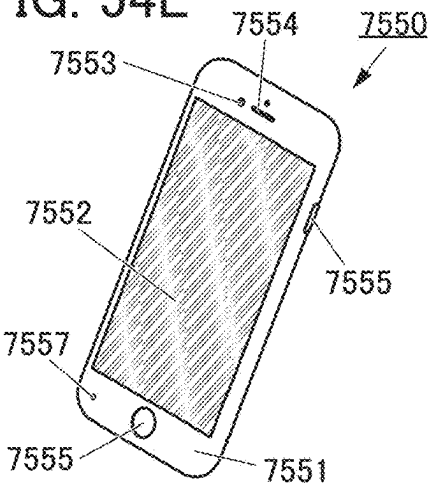
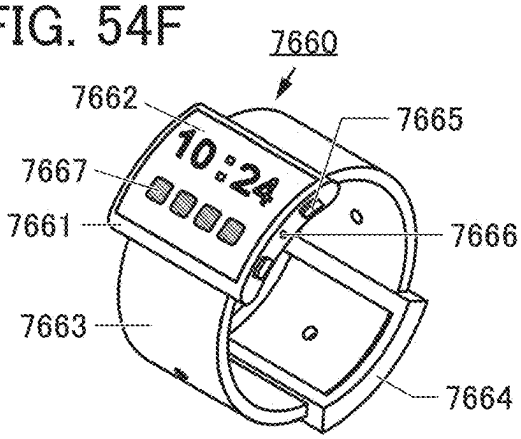


FIG. 54F



SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SEMICONDUCTOR DEVICE

TECHNICAL FIELD

[0001] One embodiment of the present invention relates to a semiconductor device, a display apparatus, a display module, and an electronic device. One embodiment of the present invention relates to a manufacturing method of a semiconductor device and a manufacturing method of a display apparatus.

[0002] Note that one embodiment of the present invention is not limited to the above technical field. Examples of the technical field of one embodiment of the present invention include a semiconductor device, a display apparatus, a light-emitting apparatus, a power storage device, a memory device, an electronic device, a lighting device, an input device (e.g., a touch sensor), an input/output device (e.g., a touch panel), a method of driving any of them, and a manufacturing method of any of them.

BACKGROUND ART

[0003] Semiconductor devices including transistors have been widely used in display apparatuses and electronic devices, and the semiconductor devices have been required increasingly to achieve high integration and high-speed operation. In the case where semiconductor devices are applied to high-definition display apparatuses, highly integrated semiconductor devices are required, for example. The development of transistors having minute sizes is ongoing as one way of increasing the degree of integration of transistors.

[0004] In recent years, display apparatuses applicable to virtual reality (VR), augmented reality (AR), substitutional reality (SR), or mixed reality (MR) have been needed. VR, AR, SR, and MR are collectively referred to as XR (Extended Reality). Display apparatuses for XR have been desired to have higher definition and higher color reproducibility so that realistic feeling and the sense of immersion can be enhanced. Examples of devices applicable to such display apparatuses include a liquid crystal display apparatus and a light-emitting apparatus including a light-emitting device (also referred to as a light-emitting element) such as an organic EL (Electro Luminescence) device or a light-emitting diode (LED). Patent Document 1 discloses a display apparatus using an organic EL device (also referred to as organic EL element) for VR.

REFERENCE

Patent Document

[0005] [Patent Document 1] PCT International Publication No. 2018/087625

SUMMARY OF THE INVENTION

Problems to be Solved by the Invention

[0006] An object of one embodiment of the present invention is to provide a semiconductor device including a transistor having a minute size and a manufacturing method thereof. Another object of one embodiment of the present invention is to provide a small semiconductor device and a manufacturing method thereof. Another object of one embodiment of the present invention is to provide a semiconductor device including a transistor with a high on-state current and a manufacturing method thereof. Another object of one embodiment of the present invention is to provide a high-performance semiconductor device and a manufacturing method thereof. Another object of one embodiment of the present invention is to provide a highly reliable semiconductor device and a manufacturing method thereof. Another object of one embodiment of the present invention is to provide a manufacturing method of a semiconductor device with high productivity. Another object of one embodiment of the present invention is to provide a novel semiconductor device and a manufacturing method thereof.

[0007] Note that the description of these objects does not preclude the existence of other objects. One embodiment of the present invention does not need to achieve all of these objects. Other objects can be derived from the description of the specification, the drawings, and the claims.

Means for Solving the Problems

[0008] One embodiment of the present invention is a semiconductor device including a first transistor and a second transistor. The first transistor includes a first conductive layer, a first insulating layer over the first conductive layer, a second insulating layer over the first insulating layer, a second conductive layer over the second insulating layer, a first semiconductor layer, a third insulating layer, and a third conductive layer. The first insulating layer, the second insulating layer, and the second conductive layer include an opening reaching the first conductive layer. The first semiconductor layer is in contact with a top surface and a side surface of the second conductive layer, a side surface of the first insulating layer, a side surface of the second insulating layer, and a top surface of the first conductive layer. The third insulating layer is provided over the first semiconductor layer. The third conductive layer is provided over the third insulating layer. The second transistor includes a second semiconductor layer over the second insulating layer, the third insulating layer over the second semiconductor layer, and a fourth conductive layer including a region overlapping with the second semiconductor layer with the third insulating layer therebetween.

[0009] One embodiment of the present invention is a semiconductor device including a first transistor, a second transistor, and a substrate. The first transistor includes a first conductive layer over the substrate, a first insulating layer over the first conductive layer, a second insulating layer over the first insulating layer, a second conductive layer over the second insulating layer, a first semiconductor layer, a third insulating layer, and a third conductive layer. The first insulating layer, the second insulating layer, and the second conductive layer include an opening reaching the first conductive layer. The first semiconductor layer is in contact with a top surface and a side surface of the second conductive layer, a side surface of the first insulating layer, a side surface of the second insulating layer, and atop surface of the first conductive layer. The third insulating layer is provided over the first semiconductor layer. The third conductive layer is provided over the third insulating layer. The second transistor includes a second semiconductor layer over the second insulating layer, the third insulating layer over the second semiconductor layer, a fourth conductive layer including a region overlapping with the second semiconductor layer with the third insulating layer therebetween,

and a fifth conductive layer over the substate. The fifth conductive layer includes a region overlapping with the fourth conductive layer with the second semiconductor layer therebetween.

[0010] One embodiment of the present invention is a semiconductor device including a first transistor and a second transistor. The first transistor includes a first conductive layer, a first insulating layer over the first conductive layer, a second insulating layer over the first insulating layer, a second conductive layer over the second insulating layer, a first semiconductor layer, a third insulating layer, and a third conductive layer. The first insulating layer, the second insulating layer, and the second conductive layer include an opening reaching the first conductive layer. The first semiconductor layer is in contact with a top surface and a side surface of the second conductive layer, a side surface of the first insulating layer, the second insulating layer, and atop surface of the first conductive layer. The third insulating layer is provided over the first semiconductor layer. The third conductive layer is provided over the third insulating layer. The second transistor includes a second semiconductor layer over the second insulating layer, the third insulating layer over the second semiconductor layer, a fourth conductive layer including a region overlapping with the second semiconductor layer with the third insulating layer therebetween, and a fifth conductive layer over the first insulating layer. The fifth conductive layer includes a region overlapping with the fourth conductive layer with the second semiconductor layer therebetween.

[0011] In the above semiconductor device, the first semiconductor layer and the second semiconductor layer each preferably contain a metal oxide.

[0012] In the above semiconductor device, the first semiconductor layer and the second semiconductor layer preferably contain the same material.

[0013] In the above semiconductor device, the third conductive layer and the fourth conductive layer preferably contain the same material.

[0014] In the above semiconductor device, the first insulating layer preferably includes a fourth insulating layer, a fifth insulating layer over the fourth insulating layer, and a sixth insulating layer over the fifth insulating layer. The fourth insulating layer preferably includes a region having a higher film density than the fifth insulating layer. The sixth insulating layer preferably includes a region having a higher film density than the fifth insulating layer.

[0015] In the above semiconductor device, the first insulating layer preferably includes a fourth insulating layer, a fifth insulating layer over the fourth insulating layer, and a sixth insulating layer over the fifth insulating layer. The fourth insulating layer preferably includes a region having a higher nitrogen content than the fifth insulating layer. The sixth insulating layer preferably includes a region having a higher nitrogen content than the fifth insulating layer.

[0016] In the above semiconductor device, the second insulating layer preferably includes a seventh insulating layer and an eighth insulating layer over the seventh insulating layer. The seventh insulating layer preferably includes a region having a higher film density than the eighth insulating layer.

[0017] In the above semiconductor device, the second insulating layer preferably includes a seventh insulating layer and an eighth insulating layer over the seventh insulating layer. The seventh insulating layer preferably includes a region having a higher nitrogen content than the eighth insulating layer.

[0018] One embodiment of the present invention is a method for manufacturing a semiconductor device including the following steps: a step of forming a first conductive film; a step of processing the first conductive film to form a first conductive layer and a second conductive layer; a step of forming a first insulating film over the first conductive layer and the second conductive layer; a step of forming a second conductive film over the first insulating film; a step of processing the first insulating film and the second conductive film to form a first insulating layer and a third conductive layer that have an opening in a region overlapping with the first conductive layer; a step of forming a first semiconductor layer in contact with a top surface of the first conductive layer, a side surface of the first insulating layer, and a top surface and a side surface of the third conductive layer and a second semiconductor layer in contact with a top surface of the first insulating layer; a step of forming a second insulating layer over the first semiconductor layer and the second semiconductor layer; and a step of forming a fourth conductive layer including a region overlapping with the first semiconductor layer and a fifth conductive layer including a region overlapping with the second semiconductor layer, over the second insulating layer.

Effect of the Invention

[0019] One embodiment of the present invention can provide a semiconductor device including a transistor having a minute size and a manufacturing method thereof. Alternatively, one embodiment of the present invention can provide a small semiconductor device and a manufacturing method thereof. Alternatively, one embodiment of the present invention can provide a semiconductor device including a transistor with a high on-state current and a manufacturing method thereof. Alternatively, one embodiment of the present invention can provide a high performance semiconductor device and a manufacturing method thereof. Alternatively, one embodiment of the present invention can provide a highly reliable semiconductor device and a manufacturing method thereof. Alternatively, one embodiment of the present invention can provide a manufacturing method of a semiconductor device with high productivity. Alternatively, one embodiment of the present invention can provide a novel semiconductor device and a manufacturing method thereof.

[0020] Note that the description of these effects does not preclude the existence of other effects. One embodiment of the present invention does not necessarily have all of these effects. Other effects can be derived from the description of the specification, the drawings, and the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021] FIG. **1**A is atop view illustrating an example of a semiconductor device. FIG. **1**B and FIG. **1**C are cross-sectional views illustrating the example of the semiconductor device.

[0022] FIG. **2**A to FIG. **2**C are perspective views illustrating an example of a semiconductor device.

[0023] FIG. **3**A and FIG. **3**B are perspective views illustrating an example of a semiconductor device.

[0024] FIG. **4**A is a top view illustrating an example of a semiconductor device. FIG. **4**B is a cross-sectional view illustrating an example of a semiconductor device.

[0025] FIG. **5**A is a top view illustrating an example of a semiconductor device. FIG. **5**B and FIG. **5**C are cross-sectional views illustrating an example of a semiconductor device.

[0026] FIG. **6**A and FIG. **6**B are cross-sectional views illustrating examples of a semiconductor device.

[0027] FIG. **7**A is a top view illustrating an example of a semiconductor device. FIG. **7**B and FIG. **7**C are cross-sectional views illustrating an example of a semiconductor device.

[0028] FIG. **8**A to FIG. **8**C are perspective views illustrating an example of a semiconductor device.

[0029] FIG. **9**A and FIG. **9**B are perspective views illustrating an example of a semiconductor device. FIG. **10**A is a top view illustrating an example of a semiconductor device. FIG. **10**B is a cross-sectional view illustrating an example of a semiconductor device.

[0030] FIG. **11**A and FIG. **11**B are cross-sectional views each illustrating an example of a semiconductor device.

[0031] FIG. **12**A and FIG. **12**B are cross-sectional views each illustrating an example of a semiconductor device.

[0032] FIG. **13**A is a top view illustrating an example of a semiconductor device. FIG. **13**B is a cross-sectional view illustrating an example of a semiconductor device.

[0033] FIG. **14** is a cross-sectional view illustrating an example of a semiconductor device.

[0034] FIG. **15**A is a top view illustrating an example of a semiconductor device. FIG. **15**B is a cross-sectional view illustrating an example of a semiconductor device.

[0035] FIG. **16**A and FIG. **16**B are cross-sectional views illustrating an example of a semiconductor device.

[0036] FIG. **17**A is a top view illustrating an example of a semiconductor device. FIG. **17**B is a cross-sectional view illustrating an example of a semiconductor device.

[0037] FIG. **18**A is a perspective view illustrating an example of a semiconductor device. FIG. **18**B and FIG. **18**C are equivalent circuit diagrams of a transistor group.

[0038] FIG. **19**A and FIG. **19**B are perspective views illustrating an example of a semiconductor device.

[0039] FIG. **20**A and FIG. **20**B are perspective views illustrating an example of a semiconductor device.

[0040] FIG. **21**A is a top view illustrating an example of a semiconductor device. FIG. **21**B is a cross-sectional view illustrating an example of a semiconductor device.

[0041] FIG. **22**A is a perspective view illustrating an example of a semiconductor device. FIG. **22**B and FIG. **22**C are equivalent circuit diagrams of a transistor group.

[0042] FIG. **23**A and FIG. **23**B are perspective views illustrating an example of a semiconductor device.

[0043] FIG. **24**A and FIG. **24**B are perspective views illustrating an example of a semiconductor device.

[0044] FIG. **25**A to FIG. **25**E are cross-sectional views illustrating an example of a method for manufacturing a semiconductor device.

[0045] FIG. **26**A to FIG. **26**D are cross-sectional views illustrating an example of a method for manufacturing a semiconductor device.

[0046] FIG. **27**A to FIG. **27**C are cross-sectional views illustrating an example of a method for manufacturing a semiconductor device.

[0047] FIG. **28**A to FIG. **28**C are cross-sectional views illustrating an example of a method for manufacturing a semiconductor device.

[0048] FIG. **29**A and FIG. **29**B are cross-sectional views illustrating an example of a method for manufacturing a semiconductor device.

[0049] FIG. **30**A and FIG. **30**B are cross-sectional views illustrating an example of a method for manufacturing a semiconductor device.

[0050] FIG. **31**A and FIG. **31**B are cross-sectional views illustrating an example of a method for manufacturing a semiconductor device.

[0051] FIG. **32**A and FIG. **32**B are cross-sectional views illustrating an example of a method for manufacturing a semiconductor device.

[0052] FIG. **33**A and FIG. **33**B are cross-sectional views illustrating an example of a method for manufacturing a semiconductor device.

[0053] FIG. **34**A and FIG. **34**B are cross-sectional views illustrating an example of a method for manufacturing a semiconductor device.

[0054] FIG. **35**A is a perspective view of the display apparatus. FIG. **35**B is a block diagram of a display apparatus.

[0055] FIG. **36**A is a circuit diagram of a latch circuit. FIG. **36**B is a circuit diagram of an inverter circuit.

[0056] FIG. **37**A and FIG. **37**B are each a circuit diagram of a pixel circuit. FIG. **37**C is a cross-sectional view illustrating an example of a pixel circuit.

[0057] FIG. **38**A and FIG. **38**B are cross-sectional views illustrating an example of a pixel circuit.

[0058] FIG. **39** is a cross-sectional view illustrating a structure example of a display apparatus.

[0059] FIG. **40** is a cross-sectional view illustrating a structure example of a display apparatus.

[0060] FIG. **41**A to FIG. **41**C are cross-sectional views illustrating a structure example of a display apparatus.

[0061] FIG. **42** is a cross-sectional view illustrating a structure example of a display apparatus.

[0062] FIG. **43**A to FIG. **43**G are diagrams each illustrating an example of a pixel.

[0063] FIG. **44**A to FIG. **44**K are diagrams each illustrating an example of a pixel.

[0064] FIG. **45**A to FIG. **45**F are diagrams each illustrating a structure example of a light-emitting device.

[0065] FIG. **46**A to FIG. **46**C are diagrams each illustrating a structure example of a light-emitting device.

[0066] FIG. **47**A and FIG. **47**B are diagrams illustrating a structure example of a display apparatus.

[0067] FIG. **48**A to FIG. **48**D are diagrams each illustrating a structure example of a display apparatus.

[0068] FIG. **49**A to FIG. **49**C are diagrams each illustrating a structure example of a display apparatus.

[0069] FIG. **50**A to FIG. **50**D are diagrams each illustrating a structure example of a display apparatus.

[0070] FIG. **51**A to FIG. **51**F are diagrams each illustrating a structure example of a display apparatus.

[0071] FIG. **52**A to FIG. **52**F are diagrams each illustrating a structure example of a display apparatus.

[0072] FIG. **53**A to FIG. **53**F are diagrams illustrating examples of electronic devices.

[0073] FIG. **54**A to FIG. **54**F are diagrams illustrating examples of electronic devices.

MODE FOR CARRYING OUT THE INVENTION

[0074] Embodiments will be described in detail with reference to the drawings. Note that the present invention is not limited to the following description, and it will be readily appreciated by those skilled in the art that modes and details of the present invention can be modified in various ways without departing from the spirit and scope of the present invention. Therefore, the present invention should not be construed as being limited to the description in the following embodiments.

[0075] Note that in structures of the invention described below, the same portions or portions having similar functions are denoted by the same reference numerals in different drawings, and the description thereof is not repeated. The same hatching pattern is used for portions having similar functions, and the portions are not especially denoted by reference numerals in some cases.

[0076] The position, size, range, or the like of each component illustrated in drawings does not represent the actual position, size, range, or the like in some cases for easy understanding. Therefore, the disclosed invention is not necessarily limited to the position, size, range, or the like disclosed in the drawings.

[0077] Note that the term "film" and the term "layer" can be used interchangeably depending on the case or the circumstances. For example, the term "conductive layer" can be replaced with the term "conductive film". As another example, the term "insulating film" can be replaced with the term "insulating layer".

[0078] In this specification and the like, a device formed using a metal mask or an FMM (fine metal mask, high-definition metal mask) may be referred to as a device having an MM (metal mask) structure. In this specification and the like, a device formed without using a metal mask or an FMM may be referred to as a device having an MML (metal maskless) structure.

[0079] In this specification and the like, a structure in which at least light-emitting layers of light-emitting devices (also referred to as light-emitting elements) having different emission wavelengths are separately formed may be referred to as a SBS (Side By Side) structure. The SBS structure can optimize materials and structures of light-emitting devices and thus can extend freedom of choice of materials and structures, whereby the luminance and the reliability can be easily improved.

[0080] In this specification and the like, a hole or an electron is sometimes referred to as a "carrier". Specifically, a hole-injection layer or an electron-injection layer may be referred to as a "carrier-injection layer", a hole-transport layer or an electron-transport layer may be referred to as a "carrier-transport layer", and a hole-blocking layer or an electron-blocking layer may be referred to as a "carrier-blocking layer". Note that the above-described carrier-injection layer, carrier-transport layer, and carrier-blocking layer cannot be clearly distinguished from each other on the basis of the cross-sectional shape, properties, or the like in some cases. One layer may have two or three functions of the carrier-injection layer, the carrier-transport layer, and the carrier-blocking layer in some cases.

[0081] In this specification and the like, a light-emitting device includes an EL layer between a pair of electrodes. The EL layer includes at least a light-emitting layer. Examples of layers (also referred to as functional layers) included in the EL layer include a light-emitting layer, carrier-injection layers (a hole-injection layer and an electron-injection layer), carrier-transport layers (a hole-transport layer and an electron-transport layer), and carrier-blocking layers (a hole-blocking layer and an electron-blocking layer).

[0082] In this specification and the like, a light-receiving device (also referred to as a light-receiving element) includes at least an active layer functioning as a photoelectric conversion layer between a pair of electrodes.

[0083] In this specification and the like, the term "island shape" refers to a state where two or more layers formed using the same material in the same step are physically separated from each other. For example, the term "island-shaped light-emitting layer" refers to a state where the light-emitting layer and its adjacent light-emitting layer are physically separated from each other.

[0084] In this specification and the like, a tapered shape refers to such a shape that at least part of the side surface of a component is inclined with respect to a substrate surface or a formation surface. For example, the tapered shape preferably includes a region where the angle formed by the inclined side surface and the substrate surface or the formation surface (such an angle is also referred to as a taper angle) is less than 90°. Note that the side surface, the substrate surface, and the formation surface of the structure are not necessarily completely flat and may be substantially flat with a slight curvature or substantially flat with slight unevenness.

[0085] Note that in this specification and the like, a mask layer (also referred to as a sacrificial layer) is positioned above at least a light-emitting layer (specifically, a layer processed into an island shape among layers included in an EL layer) and has a function of protecting the light-emitting layer in the manufacturing process.

[0086] In this specification and the like, step disconnection refers to a phenomenon in which a layer, a film, or an electrode is split because of the shape of the formation surface (e.g., a step).

[0087] In this specification and the like, the expression "having substantially the same top surface shapes" means that at least outlines of stacked layers partly overlap with each other. For example, the case of processing the upper layer and the lower layer with use of the same mask pattern or mask patterns that are partly the same is included. Note that, in some cases, the outlines do not completely overlap with each other and the upper layer is positioned inward from the lower layer or the upper layer is positioned outward from the lower layer; such cases are also represented by the expression "top surface shapes are substantially the same".

Embodiment 1

[0088] In this embodiment, a semiconductor device of one embodiment of the present invention, a manufacturing method thereof, and the like will be described with reference to FIG. **1** to FIG. **34**.

Structure Example 1

[0089] The semiconductor device of one embodiment of the present invention will be described. FIG. **1**A is a top view (also referred to as a plan view) of a semiconductor device **10**. FIG. **1**B is a cross-sectional view of a cross section along the dashed-dotted line A**1**-A**2** in FIG. **1**A, and FIG. **1**C is a cross-sectional view of cross sections along the

dashed-dotted line B**1**-B**2** and the dashed-dotted line B**3**-B**4** in FIG. **1**A. FIG. **2**A is a perspective view of the semiconductor device **10**. Note that in FIG. **1**A and FIG. **2**A, some components (e.g., an insulating layer) of the semiconductor device **10** are not illustrated. Some components are not illustrated in top views and perspective views of semiconductor devices in the following drawings, as in FIG. **1**A and FIG. **2**A.

[0090] The semiconductor device **10** includes a transistor **100** and a transistor **200**.

[0091] The transistor **100** includes a conductive layer **104**, an insulating layer **106**, a semiconductor layer **108**, a conductive layer **112***a*, and a conductive layer **112***b*. The conductive layer **104** functions as a gate electrode. Part of the insulating layer **106** functions as a gate insulating layer. The conductive layer **112***a* functions as one of a source electrode and a drain electrode, and the conductive layer **112***b* functions as the other. In the semiconductor layer **108** between the source electrode and the drain electrode, the whole region overlapping with the gate electrode with the gate insulating layer therebetween functions as a channel formation region. In the semiconductor layer **108**, a region in contact with the source electrode functions as a source region, and a region in contact with the drain electrode functions as a drain region.

[0092] The conductive layer **112***a* is provided over a substrate **102**, an insulating layer **110** is provided over the conductive layer **112***a*, an insulating layer **120** is provided over the insulating layer **110**, and the conductive layer **112***b* is provided over the insulating layer **120**. The insulating layer **110** and the insulating layer **120** each include a region interposed between the conductive layer **112***a* and the conductive layer **112***b*. The conductive layer **112***a* includes a region overlapping with the conductive layer **112***b* with the insulating layer **110** and the insulating layer **120** therebetween. The insulating layer **110** and the insulating layer **120** have an opening **141** in a region overlapping with the conductive layer **112***a*. The conductive layer **112***a* is exposed in the opening **141**. The conductive layer **112***b* has an opening **143** in a region overlapping with the conductive layer **112***a*. The opening **143** is provided in a region overlapping with the opening **141**.

[0093] The semiconductor layer **108** is provided to cover the opening **141** and the opening **143**. The semiconductor layer **108** includes a region in contact with the top surface and the side surface of the conductive layer **112***b*, the side surface of the insulating layer **110**, and the top surface of the conductive layer **112***a*. The semiconductor layer **108** is electrically connected to the conductive layer **112***a* through the opening **141** and the opening **143**. The semiconductor layer **108** has a shape along the shapes of the top surface and the side surface of the conductive layer **112***b*, the side surface of the insulating layer **110**, and the top surface of the conductive layer **112***a*.

[0094] The insulating layer **106** functioning as the gate insulating layer of the transistor **100** is provided to cover the opening **141** and the opening **143**. The insulating layer **106** is provided over the semiconductor layer **108**, the conductive layer **112***b*, and the insulating layer **110**. The insulating layer **106** includes a region in contact with the top surface and the side surface of the semiconductor layer **108**, the top surface and the side surface of the conductive layer **112***b*, and the top surface of the insulating layer **110**. The insulating layer **106** has a shape along the shapes of the top surface of the insulating layer **110**, the top surface and the side surface of the conductive layer **112***b*, the top surface and the side surface of the semiconductor layer **108**, and the top surface of the conductive layer **112***a*.

[0095] The conductive layer **104** functioning as the gate electrode of the transistor **100** is provided over the insulating layer **106** and includes a region in contact with the top surface of the insulating layer **106**. The conductive layer **104** includes a region overlapping with the semiconductor layer **108** with the insulating layer **106** therebetween. The conductive layer **104** has a shape along the shape of the top surface of the insulating layer **106**.

[0096] The transistor **100** is what is called a top-gate transistor including the gate electrode above the semiconductor layer **108**. Furthermore, since the bottom surface of the semiconductor layer **108** is in contact with the source electrode and the drain electrode, the transistor **100** can be referred to as a TGBC (Top Gate Bottom Contact) transistor. In the transistor **100**, the drain current flows in a direction perpendicular or substantially perpendicular to a surface of the substrate **102** where the transistor **100** is formed, which can also be expressed by "the drain current flows in the vertical direction or substantially in the vertical direction", and the transistor **100** can be referred to as a "vertical-channel transistor".

[0097] The channel length of the transistor **100** depends on the thickness of the insulating layer provided between the conductive layer **112***a* and the conductive layer **112***b*. Accordingly, a transistor with a channel length smaller than the resolution limit of a light exposure apparatus can be fabricated with high accuracy. Furthermore, variations in characteristics among the transistors **100** are also reduced. Accordingly, the operation of the semiconductor device including the transistor **100** can be stabilized and the reliability thereof can be improved. When the variations in characteristics is reduced, the circuit design flexibility is increased and the operation voltage of the semiconductor device can be reduced. Thus, the power consumption of the semiconductor device can be reduced.

[0098] The transistor **200** includes a conductive layer **204**, the insulating layer **106**, a semiconductor layer **208**, an insulating layer **195**, a conductive layer **212***a*, and a conductive layer **212***b*. The conductive layer **204** functions as a gate electrode. Part of the insulating layer **106** functions as a gate insulating layer. The conductive layer **212***a* functions as one of the source electrode and the drain electrode, and the conductive layer **212***b* functions as the other.

[0099] In the semiconductor layer **208** between the source electrode and the drain electrode, the whole region overlapping with the gate electrode with the gate insulating layer therebetween functions as a channel formation region. The semiconductor layer **208** includes a pair of regions **208**D between which the channel formation region is sandwiched. One of the pair of regions **208**D functions as a source region, and the other functions as a drain region. The region **208**D can also be referred to as a region having a higher carrier concentration or a lower resistance than the channel formation region.

[0100] The semiconductor layer **208** is provided over the insulating layer **120**. The semiconductor layer **208** can be formed in the same step as the semiconductor layer **108**. The insulating layer **106** is provided over the semiconductor layer **208**. The insulating layer **106** is provided in contact with the top surface and the side surface of the semicon-

ductor layer **208**. One part of the insulating layer **106** serves as the gate insulating layer of the transistor **100** and another part of the insulating layer **106** serves as the gate insulating layer of the transistor **200**. The conductive layer **204** is provided over the insulating layer **106**. The conductive layer **204** can be formed in the same step as the conductive layer **104**.

[0101] The insulating layer **195** is provided to cover the conductive layer **104**, the conductive layer **204**, and the insulating layer **106**. The insulating layer **195** functions as a protective layer protecting the transistor **100** and the transistor **200**. It is further preferable to use a material that does not easily allow diffusion of impurities for the insulating layer **195**. Providing the insulating layer **195** can effectively inhibit diffusion of impurities into the transistors from the outside and increase the reliability of the display apparatus. Examples of the impurities include water and hydrogen. The insulating layer **195** can be an insulating layer including an inorganic material or an insulating layer including an organic material. For example, an inorganic material such as an oxide, an oxynitride, a nitride oxide, or a nitride can be suitably used for the insulating layer **195**. More specifically, one or more of silicon nitride, silicon nitride oxide, silicon oxynitride, aluminum oxide, aluminum oxynitride, aluminum nitride, hafnium oxide, and hafnium aluminate can be used. As the organic material, for example, one or both of an acrylic resin and a polyimide resin can be used. As the organic material, a photosensitive material may be used. A stack including two or more of the above insulating films may also be used. The insulating layer **195** may have a stacked-layer structure of an insulating layer including an inorganic material and an insulating layer including an organic material.

[0102] The insulating layer **195** and the insulating layer **106** have an opening **147***a* and an opening **147***b* each reaching the region **208**D. The conductive layer **212***a* and the conductive layer **212***b* are provided to cover the opening **147***a* and the opening **147***b*. The conductive layer **212***a* is electrically connected to one of the pair of regions **208**D, and the conductive layer **212***b* is electrically connected to the other of the pair of regions **208**D.

[0103] The transistor **200** is what is called a top-gate transistor including the gate electrode above the semiconductor layer **208**. For example, an impurity element is added to the semiconductor layer **208** with the conductive layer **204** serving as a gate electrode used as a mask, so that the regions **208**D serving as the source region and the drain region can be formed in a self-aligned manner. The transistor **200** can be referred to as a TGSA (Top Gate Self-Aligned) transistor.

[0104] The channel length of the transistor **200** can be controlled by the length of the conductive layer **204**. Accordingly, the channel length of the transistor **200** is greater than or equal to the resolution limit of alight exposure apparatus used for fabrication of the transistor. The transistor with a long channel length can have favorable saturation.

[0105] In this specification and the like, the state where the change in current is small in the saturation region of the I_d-V_d characteristics of a transistor is sometimes described using the expression "favorable saturation".

[0106] The transistor **100** with a short channel length and the transistor **200** with a long channel length can be formed over the same substrate by the formation steps some of which are shared, as described above. For example, the transistor **100** is used as the transistor required to have a high on-state current and the transistor **200** is used as the transistor required to have favorable saturation, thereby providing a high-performance semiconductor device.

[0107] Although FIG. **1**A illustrates a structure where the top surface shapes of the opening **147***a* and the opening **147***b* are the same or substantially the same as the top surface shapes of the opening **141** and the opening **143**, one embodiment of the present invention is not limited thereto. Note that the top surface shapes of the opening **147***a* and the opening **147***b* may be different from those of the opening **141** and the opening **143**. The top surface shapes of the opening **147***a* and the opening **147***b* can be circular or elliptic, for example. Furthermore, examples of the top surface shapes of the opening **147***a* and the opening **147***b* include polygons such as a triangle, a tetragon (including a rectangle, a rhombus, and a square), and a pentagon; and polygons with rounded corners.

[0108] Next, components of the transistor **100** and the transistor **200** are described in detail.

[0109] The conductive layer **112***a* and the conductive layer **112***b* included in the transistor **100** may each have a stacked-layer structure. FIG. **1**B and the like illustrate a structure in which the conductive layer **112***a* has a stacked-layer structure of a conductive layer **112***a*_**1** and a conductive layer **112***a*_**2** over the conductive layer **112***a*_**1**. As illustrated in FIG. **1**B, the conductive layer **112***a*_**2** has an opening **145**, and the conductive layer **112***a*_**1** is exposed in the opening **145**. In the opening **145**, the conductive layer **112***a*_**1** includes a region in contact with the semiconductor layer **108**. It is preferable that the conductive layer **112***a*_**2** not include a region in contact with the semiconductor layer **108**.

[0110] FIG. **2**B is a perspective view selectively illustrating the conductive layer **112***a*. The conductive layer **112***a*_**2** has the opening **145** in a region overlapping with the conductive layer **112***a*_**1**. The conductive layer **112***a*_**1** is exposed in the opening **145**.

[0111] FIG. **2**C is a perspective view selectively illustrating the conductive layer **112***a*, the conductive layer **112***b*, the opening **141**, and the opening **143**. Note that the opening **141** provided in the insulating layer **110** and the insulating layer **120** is indicated by dashed lines. As illustrated in FIG. **2**C, the conductive layer **112***b* has the opening **143** in a region overlapping with the conductive layer **112***a*.

[0112] The top surface shapes of the opening **141** and the opening **143** can be circular or elliptic, for example. Examples of the top surface shapes of the opening **141** and the opening **143** include polygons such as a triangle, a tetragon (including a rectangle, a rhombus, and a square), and a pentagon; and polygons with rounded corners. The top surface shapes of the opening **141** and the opening **143** are preferably circular as illustrated in FIG. **1**A. In the case where the top surface shapes of the opening **141** and the opening **143** are circular, high processing accuracy to form each of the opening **141** and the opening **143** is possible and the opening **141** and the opening **143** having minute sizes can be formed. Note that in this specification and the like, a circular shape is not necessarily a perfect circular shape.

[0113] An end portion of the conductive layer **112***b* on the opening **143** side is preferably aligned or substantially aligned with an end portion of the insulating layer **120** on the opening **141** side. In other words, the top surface shape of the opening **143** is the same or substantially the same as the

top surface shape of the opening **141**. Note that in this specification and the like, the end portion of the conductive layer **112***b* on the opening **143** side refers to an end portion of the bottom surface of the conductive layer **112***b* on the opening **143** side. The bottom surface of the conductive layer **112***b* refers to the surface thereof on the insulating layer **120** side. The end portion of the insulating layer **120** on the opening **141** side refers to an end portion of the top surface of the insulating layer **120** on the opening **141** side. The top surface of the insulating layer **120** refers to the surface thereof on the conductive layer **112***b* side. The top surface shape of the opening **143** refers to the shape of the end portion of the bottom surface of the conductive layer **112***b* on the opening **143** side. The top surface shape of the opening **141** refers to the shape of the end portion of the top surface of the insulating layer **120** on the opening **141** side.

[0114] In the case where end portions are the same or substantially the same, the end portions can also be said to be aligned or substantially aligned with each other. In the case where end portions are aligned or substantially aligned with each other and the case where top surface shapes are the same or substantially the same, it can be said that outlines of stacked layers at least partly overlap with each other in a top view (also referred to as a plan view). For example, the case of processing the upper layer and the lower layer with use of the same mask pattern or mask patterns that are partly the same is included. Note that, in some cases, the outlines do not completely overlap with each other and the upper layer is positioned inward from the lower layer or the upper layer is positioned outward from the lower layer; such cases are also represented by the expression "end portions are substantially aligned with each other" or the expression "top surface shapes are substantially the same".

[0115] The opening **141** can be formed using a resist mask used for the formation of the opening **143**, for example. Specifically, a first insulating film to be the insulating layer **110**, a second insulating film to be the insulating layer **120** over the first insulating film, a conductive film to be the conductive layer **112***b* over the second insulating film, and a resist mask over the conductive film are formed. Then, the opening **143** is formed in the conductive film using the resist mask and then the opening **141** is formed in the first insulating film and the second insulating film using the resist mask, whereby the end portion of the opening **141** and the end portion of the opening **143** can be aligned or substantially aligned with each other. With such a structure, processes can be simplified.

[0116] After the opening **143** is formed, the opening **141** may be formed in a step different from that of the opening **143**. There is no particular limitation on the formation order of the opening **141** and the opening **143**. For example, after the opening **141** is formed in the first insulating film and the second insulating film, a conductive film to be the conductive layer **112***b* may be formed, and the opening **143** may be formed in the conductive film.

[0117] The end portion of the conductive layer **112***b* on the opening **143** side is not necessarily aligned with the end portion of the insulating layer **120** on the opening **141** side. That is, the top surface shape of the opening **143** is not necessarily the same as the top surface shape of the opening **141**. In the top view, the opening **143** preferably covers the opening **141** completely. The end portion of the conductive layer **112***b* on the opening **143** side may be located outward from the end portion of the insulating layer **120** on the opening **141** side. The semiconductor layer **108** includes a region in contact with the top surface and the side surface of the conductive layer **112***b*, the top surface and the side surface of the insulating layer **120**, the side surface of the insulating layer **110**, and the top surface of the conductive layer **112***a*. With such a structure, a step on the surface of a layer (e.g., the semiconductor layer **108**) over which the conductive layer **112***a*, the conductive layer **112***b*, and the insulating layer **120** are formed is reduced. Accordingly, the coverage with layers formed over the conductive layer **112***a*, the conductive layer **112***b*, the insulating layer **110**, and the insulating layer **120** can be improved, which can inhibit defects such as step disconnection or a void from being generated in the layer.

[0118] Although this embodiment describes the structure in which the opening **141** and the opening **143** are provided in the insulating layer **110**, the insulating layer **120**, and the conductive layer **112***b* and the semiconductor layer **108** is provided to cover the opening **141** and the opening **143**, one embodiment of the present invention is not limited thereto. The semiconductor device of one embodiment of the present invention may include a first region where the insulating layer **110** and the insulating layer **120** are provided over the conductive layer **112***a* and a second region where the insulating layer **110** and the insulating layer **120** are not provided over the conductive layer **112***a*. In the transistor **100**, the semiconductor layer **108** may be provided at a step generated by the first region and the second region. The insulating layer **106** may be provided over the semiconductor layer **108**, and the conductive layer **104** may be provided to overlap with the semiconductor layer **108** that is between the conductive layer **112***a* and the conductive layer **112***b*, with the insulating layer **106** therebetween.

[0119] The semiconductor layer **108** preferably covers the end portion of the conductive layer **112***b* on the opening **143** side. FIG. **1**B and the like illustrates a structure where the end portion of the semiconductor layer **108** is positioned over the conductive layer **112***b*. That is, the end portion of the semiconductor layer **108** is in contact with the top surface of the conductive layer **112***b*. Note that the semiconductor layer **108** may extend to and cover an end portion of the conductive layer **112***b* that does not face the opening **143**. The end portion of the semiconductor layer **108** may be in contact with the top surface of the insulating layer **120**.

[0120] FIG. **3**A is a perspective view selectively illustrating the conductive layer **112***a* and the semiconductor layer **108** included in the transistor **100** and the semiconductor layer **208** included in the transistor **200**. As illustrated in FIG. **3**A, the semiconductor layer **108** is provided to cover the opening **141** and the opening **143**. As illustrated in FIG. **1**B and the like, the semiconductor layer **108** includes a region in contact with the top surface of the conductive layer **112***a* in the opening **141**. Specifically, the semiconductor layer **108** preferably includes a region in contact with the top surface of the conductive layer **112***a*_**1** in the opening **141**. The semiconductor layer **208** can be formed in the same step as the semiconductor layer **108**. As illustrated in FIG. **1**B and the like, the semiconductor layer **208** is provided over the insulating layer **120**. Note that the semiconductor layer **108** and the semiconductor layer **208** may be formed in different steps. The material used for the semiconductor layer **108** may be different from the material used for the semiconductor layer **208**.

[0121] Although the semiconductor layer **108** and the semiconductor layer **208** each have a single-layer structure in FIG. **1**B and the like, one embodiment of the present invention is not limited thereto. The semiconductor layer **108** and the semiconductor layer **208** may each have a stacked-layer structure of two or more metal oxide layers.

[0122] FIG. **3**B is a perspective view selectively illustrating the conductive layer **112***a* and the conductive layer **104** included in the transistor **100** and the conductive layer **204** included in the transistor **200**. As illustrated in FIG. **3**B, the conductive layer **104** is provided to cover the opening **141** and the opening **143**. The conductive layer **204** can be formed in the same step as the conductive layer **104**. As illustrated in FIG. **1**B and the like, the conductive layer **104** and the conductive layer **204** are provided over the insulating layer **106**.

[0123] As illustrated in FIG. **1**B and the like, in the transistor **100**, the conductive layer **104** includes a region overlapping with the semiconductor layer **108** with the insulating layer **106** therebetween in the opening **141** and the opening **143**. The conductive layer **104** also includes a region overlapping with the conductive layer **112***a* and a region overlapping with the conductive layer **112***b* with the insulating layer **106** and the semiconductor layer **108** therebetween. The conductive layer **104** preferably covers the end portion of the conductive layer **112***b* on the opening **143** side. With such a structure, in the semiconductor layer **108** between the source electrode and the drain electrode, the whole region overlapping with the gate electrode with the gate insulating layer therebetween can function as a channel formation region. Note that the conductive layer **104** may extend to and cover an end portion of the conductive layer **112***b* that does not face the opening **143**. The conductive layer **104** may extend to and cover the end portion of the semiconductor layer **108**.

[0124] The conductive layer **112***a*, the conductive layer **112***b*, and the conductive layer **104** can each function as a wiring. The transistor **100** can be provided in a region where these wirings overlap with each other, and the area occupied by the transistor **100** and the wirings can be reduced in the circuit including the transistor **100** and the wirings. Accordingly, the area occupied by the circuit can be reduced, which makes it possible to provide a small semiconductor device. When the semiconductor device of one embodiment of the present invention is used for a pixel circuit of a display apparatus, the area occupied by the pixel circuit can be reduced and the display apparatus can have high definition, for example. When the semiconductor device of one embodiment of the present invention is used for a driver circuit (e.g., a gate line driver circuit and a source line driver circuit) of a display apparatus, the area occupied by the driver circuit can be reduced and the display apparatus can have a narrow bezel.

[0125] In the semiconductor device of one embodiment of the present invention, the conductive layer **112***a*, the conductive layer **112***b*, the conductive layer **104**, and the conductive layer **204** functioning as wirings are provided in different layers. Accordingly, the wirings can be placed in their respective layers, leading to high layout flexibility and a reduction in the area occupied by the circuit.

[0126] Here, the channel length and channel width of the transistor **100** are described with reference to FIG. **4**A and FIG. **4**B. FIG. **4**A is a top view of the transistor **100**. FIG. **4**B is an enlarged view of the transistor **100** in FIG. **1**B.

[0127] In the semiconductor layer **108**, a region in contact with the conductive layer **112***a* functions as one of the source region and the drain region, a region in contact with the conductive layer **112***b* functions as the other of the source region and the drain region, and a region between the source region and the drain region functions as the channel formation region.

[0128] The channel length of the transistor **100** is a distance between the source region and the drain region. In FIG. **4**B, a channel length L**100** of the transistor **100** is indicated by a dashed double-headed arrow. In the cross-sectional view, the channel length L**100** is a distance between an end portion of the region where the semiconductor layer **108** is in contact with the conductive layer **112***a* and an end portion of the region where the semiconductor layer **108** is in contact with the conductive layer **112***b*.

[0129] Here, the channel length L**100** of the transistor **100** corresponds to the sum of the length of the side surface of the insulating layer **110** on the opening **141** side and the length of the side surface of the insulating layer **120** on the opening **141** side in the cross-sectional view. That is, the channel length L**100** is determined depending on a thickness T**110** of the insulating layer **110**, a thickness T**120** of the insulating layer **120**, and an angle θ**110** formed by the side surface of the insulating layer **110** on the opening **141** side and the formation surface of the insulating layer **110** (here, the top surface of the conductive layer **112***a*), and is not affected by the performance of a light-exposure apparatus used for manufacturing the transistor. Thus, the channel length L**100** can be a value smaller than that of the resolution limit of a light-exposure apparatus, which enables a transistor having a minute size. For example, the channel length L**100** is preferably greater than or equal to 0.01 μm and less than 3 μm, further preferably greater than or equal to 0.05 μm and less than 3 μm, further preferably greater than or equal to 0.1 μm and less than 3 μm, still further preferably greater than or equal to 0.15 μm and less than 3 μm, yet still further preferably greater than or equal to 0.2 μm and less than 3 μm, yet still further preferably greater than or equal to 0.2 m and less than or equal to 2.5 μm, yet still further preferably greater than or equal to 0.2 μm and less than or equal to 2 μm, yet still further preferably greater than or equal to 0.2 μm and less than or equal to 1.5 μm, yet still further preferably greater than or equal to 0.3 μm and less than or equal to 1.5 μm, yet still further preferably greater than or equal to 0.3 μm and less than or equal to 1.2 μm, yet still further preferably greater than or equal to 0.4 μm and less than or equal to 1.2 μm, yet still further preferably greater than or equal to 0.4 μm and less than or equal to 1 μm, yet still further preferably greater than or equal to 0.5 μm and less than or equal to 1 μm. In FIG. **4**B, the thickness T**110** of the insulating layer **110** is indicated by a dashed-dotted double-headed arrow, and the thickness T**120** of the insulating layer **120** is indicated by a dashed-dotted double-headed arrow.

[0130] The reduction in the channel length L**100** can increase the on-state current of the transistor **100**. With use of the transistor **100**, a circuit capable of high-speed operation can be fabricated. Furthermore, the area occupied by the circuit can be reduced. Therefore, a small semiconductor device can be obtained. The application of the semiconductor device of one embodiment of the present invention to a large display apparatus or a high-definition display apparatus can reduce signal delay in wirings and reduce display

unevenness even if the number of wirings is increased, for example. In addition, since the area occupied by the circuit can be reduced, the bezel of the display apparatus can be narrowed.

[0131] By adjusting the thickness T**110**, the thickness T**120** of the insulating layer **120**, and the angle θ**110** of the insulating layer **110**, the channel length L**100** can be controlled.

[0132] The sum of the thickness T**110** of the insulating layer **110** and the thickness T**120** of the insulating layer **120** is preferably greater than or equal to 0.01 μm and less than 3 μm, further preferably greater than or equal to 0.05 μm and less than 3 μm, further preferably greater than or equal to 0.1 μm and less than 3 μm, still further preferably greater than or equal to 0.15 μm and less than 3 μm, yet still further preferably greater than or equal to 0.2 am and less than 3 am, yet still further preferably greater than or equal to 0.2 μm and less than or equal to 2.5 μm, yet still further preferably greater than or equal to 0.2 μm and less than or equal to 2 μm, yet still further preferably greater than or equal to 0.2 μm and less than or equal to 1.5 μm, yet still further preferably greater than or equal to 0.3 μm and less than or equal to 1.5 μm, yet still further preferably greater than or equal to 0.3 μm and less than or equal to 1.2 μm, yet still further preferably greater than or equal to 0.4 μm and less than or equal to 1.2 μm, yet still further preferably greater than or equal to 0.4 μm and less than or equal to 1 μm, yet still further preferably greater than or equal to 0.5 μm and less than or equal to 1 μm.

[0133] The side surfaces of the insulating layer **110** and the insulating layer **120** on the opening **141** side preferably have tapered shapes. The angle θ**110** formed by the side surface of the insulating layer **110** on the opening **141** side and the formation surface of the insulating layer **110** (here, the top surface of the conductive layer **112***a*) is preferably smaller than 90°. By reducing the angle θ**110**, the coverage with a layer (e.g., the semiconductor layer **108**) provided over the insulating layer **110** can be improved. However, reducing the angle θ**110** might reduce the contact area between the semiconductor layer **108** and the conductive layer **112***a* to increase the contact resistance between the semiconductor layer **108** and the conductive layer **112***a*. The angle θ**110** is preferably greater than or equal to 45° and less than 90°, further preferably greater than or equal to 50° and less than 90°, further preferably greater than or equal to 55° and less than 90°, further preferably greater than or equal to 60° and less than 90°, further preferably greater than or equal to 60° and less than or equal to 85°, still further preferably greater than or equal to 65° and less than or equal to 85°, yet further preferably greater than or equal to 65° and less than or equal to 80°, yet still further preferably greater than or equal to 70° and less than or equal to 80°. When the angle θ**110** is in the above range, the coverage with the layer (e.g., the semiconductor layer **108**) formed over the conductive layer **112***a* and the insulating layer **110** can be improved, which can inhibit defects such as step disconnection or a void from being generated in the layer. In addition, the contact resistance between the semiconductor layer **108** and the conductive layer **112***a* can be reduced.

[0134] Although FIG. **4**B and the like illustrate the structure where the side surfaces of the insulating layer **110** and the insulating layer **120** on the opening **141** side are linear in the cross-sectional view, one embodiment of the present invention is not limited thereto. In the cross-sectional view, the side surfaces of the insulating layer **110** and the insulating layer **120** on the opening **141** side may be curved, or the side surfaces may include both a linear region and a curved region.

[0135] It is preferable that the conductive layer **112***b* not be provided inside the opening **141**. Specifically, it is preferable that the conductive layer **112***b* not include a region in contact with the side surface of the insulating layer **110** on the opening **141** side and not include a region in contact with the side surface of the insulating layer **120** on the opening **141** side. If the conductive layer **112***b* is also provided inside the opening **141**, the channel length L**100** of the transistor **100** is shorter than the length of the side surfaces of the insulating layer **110** and the insulating layer **120**, and the channel length L**100** is difficult to control in some cases. Accordingly, it is preferable that the top surface shape of the opening **143** be the same as the top surface shape of the opening **141**, or the opening **143** cover the opening **141** completely in the top view.

[0136] The channel width of the transistor **100** is the width of the source region or the width of the drain region in a direction orthogonal to the channel length direction. In other words, the channel width is the width of the region where the semiconductor layer **108** is in contact with the conductive layer **112***a* or the width of the region where the semiconductor layer **108** is in contact with the conductive layer **112***b* in the direction orthogonal to the channel length direction. Here, the channel width of the transistor **100** is described as the width of the region where the semiconductor layer **108** is in contact with the conductive layer **112***b* in the direction orthogonal to the channel length direction. In FIG. **4**A and FIG. **4**B, a channel width W**100** of the transistor **100** is indicated by a solid double-headed arrow. The channel width W**100** is the length of the perimeter of the opening **143** in the top view. Specifically, the channel width W**100** is the length of the end portion of the bottom surface of the conductive layer **112***b* on the opening **143** side in the top view.

[0137] The channel width W**100** is determined depending on the top surface shape of the opening **143**. In FIG. **4**A and FIG. **4**B, a width D**143** of the opening **143** is indicated by a dashed double-dotted double-headed arrow. In the top view, the width D**143** refers to the short side of the smallest rectangle that is circumscribed around the opening **143**. In the case where the opening **143** is formed by a photolithography method, the width D**143** of the opening **143** is larger than or equal to the resolution limit of a light-exposure apparatus. For example, the width D**143** is preferably greater than or equal to 0.2 μm and less than 5 μm, further preferably greater than or equal to 0.2 μm and less than 4.5 μm, further preferably greater than or equal to 0.2 μm and less than 4 μm, still further preferably greater than or equal to 0.2 μm and less than 3.5 μm, yet still further preferably greater than or equal to 0.2 μm and less than 3 μm, yet still further preferably greater than or equal to 0.2 μm and less than or equal to 2.5 μm, yet still further preferably greater than or equal to 0.2 μm and less than or equal to 2 μm, yet still further preferably greater than or equal to 0.2 μm and less than or equal to 1.5 μm, yet still further preferably greater than or equal to 0.3 μm and less than or equal to 1.5 μm, yet still further preferably greater than or equal to 0.3 μm and less than or equal to 1.2 μm, yet still further preferably greater than or equal to 0.4 μm and less than or equal to 1.2 μm, yet still further preferably greater than or equal to 0.4 μm and less than or equal to 1 μm, yet still further preferably

greater than or equal to 0.5 μm and less than or equal to 1 μm. Note that when the top surface shape of the opening **143** is circular, the width D**143** corresponds to the diameter of the opening **143**, and the channel width W**100** can be calculated to be "D**143**×π".

[0138] Next, the channel length and the channel width of the transistor **200** will be described with reference to FIG. **5**A and FIG. **5**B. FIG. **5**A is atop view of the transistor **200**. FIG. **5**B is an enlarged view of the transistor **200** illustrated in FIG. **1**B.

[0139] In the semiconductor layer **208**, the pair of regions **208**D functions as a source region and a drain region, and the region between the source region and the drain region functions as a channel formation region. The channel formation region includes a region overlapping with the conductive layer **204** with the insulating layer **106** therebetween.

[0140] The channel length of the transistor **200** is the length of a region between the pair of regions **208**D where the semiconductor layer **208** and the conductive layer **204** overlap with each other. In FIG. **5**A and FIG. **5**B, a channel length L**200** of the transistor **200** is indicated by a dashed double-headed arrow. The channel length L**200** of the transistor **200** is determined by the length of the conductive layer **204**, which is greater than or equal to the resolution limit of a light exposure apparatus. For example, the channel length L**200** can be greater than or equal to 1.5 m. The transistor with a long channel length can have favorable saturation.

[0141] Here, the channel width of the transistor **200** is described as the width of the region where the semiconductor layer **208** overlaps with the conductive layer **204** in the direction orthogonal to the channel length direction. In FIG. **5**A and FIG. **5**C, a channel width W**200** of the transistor **200** is indicated by a solid double-headed arrow.

[0142] As described above, the channel length L**100** of the transistor **100** can have a smaller value than the resolution limit of the light exposure apparatus and the channel length L**200** of the transistor **200** can have a value larger than or equal to the resolution limit of the light exposure apparatus. For example, the transistor **100** is used as the transistor required to have a high on-state current and the transistor **200** is used as the transistor required to have favorable saturation, thereby providing the high-performance semiconductor device **10** utilizing the advantages of the transistors.

[0143] In the semiconductor device **10** of one embodiment of the present invention, some of steps can be shared for forming the transistor **100** and the transistor **200** having different structures and different channel lengths over the substrate **102**. Specifically, the semiconductor layer **108** and the semiconductor layer **208** can be formed in the same step. One part of the insulating layer **106** serves as the gate insulating layer of the transistor **100** and another part of the insulating layer **106** serves as the gate insulating layer of the transistor **200**. The conductive layer **104** and the conductive layer **204** can be formed in the same step. Thus, the manufacturing cost of the semiconductor device **10** can be made low.

[0144] Components included in the semiconductor device of this embodiment will be described below.

<Components of Semiconductor Device>

[Semiconductor Layer **108** and Semiconductor Layer **208**]

[0145] A semiconductor material that can be used for each of the semiconductor layer **108** and the semiconductor layer **208** is not particularly limited. For example, a single-element semiconductor or a compound semiconductor can be used. As the single-element semiconductor, silicon or germanium can be used, for example. Examples of the compound semiconductor include gallium arsenide and silicon germanium. As the compound semiconductor, an organic substance having semiconductor characteristics or a metal oxide having semiconductor characteristics (also referred to as an oxide semiconductor) can be used. These semiconductor materials may contain an impurity as a dopant.

[0146] There is no particular limitation on the crystallinity of a semiconductor material used for each of the semiconductor layer **108** and the semiconductor layer **208**, and any of an amorphous semiconductor and a semiconductor having crystallinity (a single crystal semiconductor, a polycrystalline semiconductor, a microcrystalline semiconductor, or a semiconductor partly including crystal regions) may be used. A semiconductor having crystallinity is preferably used, in which case deterioration of the transistor characteristics can be inhibited.

[0147] For each of the semiconductor layer **108** and the semiconductor layer **208**, silicon can be used. As silicon, single crystal silicon, polycrystalline silicon, microcrystalline silicon, and amorphous silicon can be given. As the polycrystalline silicon, low-temperature polysilicon (LTPS) can be given, for example.

[0148] The transistor including amorphous silicon in the semiconductor layer can be formed over a large glass substrate, and can be manufactured at low cost. The transistor including polycrystalline silicon in the semiconductor layer has high field-effect mobility and enables high-speed operation. The transistor including microcrystalline silicon in the semiconductor layer has higher field-effect mobility and enables higher speed operation than the transistor including amorphous silicon.

[0149] Each of the semiconductor layer **108** and the semiconductor layer **208** preferably contains a metal oxide (also referred to as an oxide semiconductor). Examples of the metal oxide that can be used for the semiconductor layer **108** and the semiconductor layer **208** include indium oxide, gallium oxide, and zinc oxide. The metal oxide preferably contains at least indium (In) or zinc (Zn). The metal oxide preferably contains two or three kinds selected from indium, an element M, and zinc. The element M is a metal element or metalloid element that has a high bonding energy with oxygen, such as a metal element or metalloid element whose bonding energy with oxygen is higher than that of indium, for example. Specific examples of the element M include aluminum, gallium, tin, yttrium, titanium, vanadium, chromium, manganese, iron, cobalt, nickel, zirconium, molybdenum, hafnium, tantalum, tungsten, lanthanum, cerium, neodymium, magnesium, calcium, strontium, barium, boron, silicon, germanium, and antimony. The element M included in the metal oxide is preferably one or more of the above elements, further preferably one or more selected from aluminum, gallium, tin, and yttrium, and still further preferably gallium. In this specification and the like, a metal element and a metalloid element may be collectively

referred to as a "metal element", and a "metal element" in this specification and the like may refer to a metalloid element.

[0150] For example, for each of the semiconductor layer **108** and the semiconductor layer **208**, indium zinc oxide (In—Zn oxide), indium tin oxide (In—Sn oxide), indium titanium oxide (In—Ti oxide), indium gallium oxide (In—Ga oxide), indium gallium aluminum oxide (In—Ga—Al oxide), indium gallium tin oxide (In—Ga—Sn oxide), gallium zinc oxide (also referred to as Ga—Zn oxide or GZO), aluminum zinc oxide (also referred to as Al—Zn oxide or AZO), indium aluminum zinc oxide (also referred to as In—Al—Zn oxide or IAZO), indium tin zinc oxide (In—Sn—Zn oxide), indium titanium zinc oxide (In—Ti—Zn oxide), indium gallium zinc oxide (also referred to as In—Ga—Zn oxide or IGZO), indium gallium tin zinc oxide (also referred to as In—Ga—Sn—Zn oxide or IGZTO), or indium gallium aluminum zinc oxide (also referred to as In—Ga—Al—Zn oxide, IGAZO, or IAGZO) can be used. Alternatively, indium tin oxide containing silicon, gallium tin oxide (Ga—Sn oxide), aluminum tin oxide (Al—Sn oxide), or the like can be used.

[0151] The compositions of the metal oxide in the semiconductor layer **108** and the semiconductor layer **208** greatly affect the electrical characteristics and reliability of the transistor **100** and the transistor **200**.

[0152] By increasing the proportion of the number of indium atoms in the total number of atoms of all the metal elements contained in the metal oxide, a transistor having a high on-state current or high field-effect mobility can be provided. By using such a transistor as a transistor requiring a high on-state current, a semiconductor device having excellent electrical characteristics can be provided.

[0153] Note that the metal oxide may contain, instead of or in addition to indium, one or more kinds selected from metal elements belonging to a period of a higher number in the periodic table. The larger the overlap between orbits of metal elements is, the more likely it is that the metal oxide will have high carrier conductivity. Thus, a transistor containing a metal element belonging to a period of a higher number in the periodic table can have high field-effect mobility in some cases. Examples of the metal element belonging to a period of a higher number in the periodic table include metal elements belonging to Period **5** and metal elements belonging to Period **6**. Specific examples of the metal element include yttrium, zirconium, silver, cadmium, tin, antimony, barium, lead, bismuth, lanthanum, cerium, praseodymium, neodymium, promethium, samarium, and europium. Note that lanthanum, cerium, praseodymium, neodymium, promethium, samarium, and europium are called light rare-earth elements.

[0154] The metal oxide may contain one or more kinds selected from nonmetallic elements. A transistor including the metal oxide including a nonmetallic element can have high field-effect mobility in some cases. Examples of the nonmetallic element include carbon, nitrogen, phosphorus, sulfur, selenium, fluorine, chlorine, bromine, and hydrogen.

[0155] As an In—Zn oxide used for the semiconductor layer, a metal oxide in which the atomic proportion of indium is higher than or equal to that of zinc is preferably used. For example, it is possible to use a metal oxide in which the atomic ratio of metal elements is In:Zn=1:1, In:Zn=2:1, In:Zn=3:1, In:Zn=4:1, In:Zn=5:1, In:Zn=7:1, or In:Zn=10:1, or in the neighborhood thereof.

[0156] In the case where an In—Sn oxide is used for the semiconductor layer, a metal oxide in which the atomic proportion of indium is higher than or equal to that of tin is preferably used. For example, it is possible to use a metal oxide in which the atomic ratio of metal elements is In:Sn=1:1, In:Sn=2:1, In:Sn=3:1, In:Sn=4:1, In:Sn=5:1, In:Sn=7:1, or In:Sn=10:1, or in the neighborhood thereof.

[0157] In the case where an In—Sn—Zn oxide is used for the semiconductor layer, it is possible to use a metal oxide in which the atomic proportion of indium is higher than that of tin. It is further preferable to use a metal oxide in which the atomic proportion of zinc is higher than the atomic proportion of tin. For example, it is possible to use a metal oxide in which the atomic ratio of metal elements is In:Sn:Zn=2:1:3, In:Sn:Zn=3:1:2, In:Sn:Zn=4:2:3, In:Sn:Zn=4:2:4.1, In:Sn:Zn=5:1:3, In:Sn:Zn=5:1:6, In:Sn:Zn=5:1:7, In:Sn:Zn=5:1:8, In:Sn:Zn=6:1:6, In:Sn:Zn=10:1:3, In:Sn:Zn=10:1:6, In:Sn:Zn=10:1:7, In:Sn:Zn=10:1:8, In:Sn:Zn=5:2:5, In:Sn:Zn=10:1:10, In:Sn:Zn=20:1:10, or In:Sn:Zn=40:1:10, or in the neighborhood thereof.

[0158] In the case where an In—Al—Zn oxide is used for the semiconductor layer, it is possible to use a metal oxide in which the atomic proportion of indium is higher than that of aluminum. It is further preferable to use a metal oxide in which the atomic proportion of zinc is higher than the atomic proportion of aluminum. For example, it is possible to use a metal oxide in which the atomic ratio of metal elements is In:Al:Zn=2:1:3, In:Al:Zn=3:1:2, In:Al:Zn=4:2:3, In:Al:Zn=4:2:4.1, In:Al:Zn=5:1:3, In:Al:Zn=5:1:6, In:Al:Zn=5:1:7, In:Al:Zn=5:1:8, In:Al:Zn=6:1:6, In:Al:Zn=10:1:3, In:Al:Zn=10:1:6, In:Al:Zn=10:1:7, In:Al:Zn=10:1:8, In:Al:Zn=5:2:5, In:Al:Zn=10:1:10, In:Al:Zn=20:1:10, or In:Al:Zn=40:1:10, or in the neighborhood thereof.

[0159] In the case of using In—Ga—Zn oxide for the semiconductor layer, a metal oxide in which the atomic proportion of indium with respect to the total number of atoms of all the contained metal elements is higher than the atomic proportion of gallium can be used. It is further preferable to use a metal oxide in which the atomic proportion of zinc is higher than the atomic proportion of gallium. For example, a metal oxide having any of the following atomic ratios of metal elements can be used in the semiconductor layer: In:Ga:Zn=2:1:3, In:Ga:Zn=3:1:2, In:Ga:Zn=4:2:3, In:Ga:Zn=4:2:4.1, In:Ga:Zn=5:1:3, In:Ga:Zn=5:1:6, In:Ga:Zn=5:1:7, In:Ga:Zn=5:1:8, In:Ga:Zn=6:1:6, In:Ga:Zn=10:1:3, In:Ga:Zn=10:1:6, In:Ga:Zn=10:1:7, In:Ga:Zn=10:1:8, In:Ga:Zn=5:2:5, In:Ga:Zn=10:1:10, In:Ga:Zn=20:1:10, In:Ga:Zn=40:1:10, and a neighborhood thereof.

[0160] In the case of using In-M-Zn oxide for the semiconductor layer, a metal oxide in which the atomic proportion of indium with respect to the total number of atoms of all the contained metal elements is higher than the atomic proportion of the element M can be used. It is further preferable to use a metal oxide in which the atomic proportion of zinc is higher than the atomic proportion of the element M. For example, a metal oxide having any of the following atomic ratios of metal elements can be used as the semiconductor layer: In:M:Zn=2:1:3, In:M:Zn=3:1:2, In:M:Zn=4:2:3, In:M:Zn=4:2:4.1, In:M:Zn=5:1:3, In:M:Zn=5:1:6, In:M:Zn=5:1:7, In:M:Zn=5:1:8, In:M:Zn=6:1:6, In:M:Zn=10:1:3, In:M:Zn=10:1:6, In:M:Zn=10:1:7, In:M:Zn=10:1:8, In:M:Zn=5:2:5, In:M:Zn=10:1:10, In:M:Zn=20:1:10, In:M:Zn=40:1:10, or a neighborhood thereof.

[0161] In the case where a plurality of metal elements are contained as the element M, the sum of the proportions of the numbers of atoms of the metal elements can be the proportion of the number of element M atoms. In the case of In—Ga—Al—Zn oxide in which gallium and aluminum are contained as the element M, for example, the sum of the proportion of the number of gallium atoms and the proportion of the number of aluminum atoms can be the atomic proportion of the element M. The atomic ratio of indium to the element M to zinc is preferably within the ranges given above. In the case of In—Ga—Sn—Zn oxide in which gallium and tin are contained as the element M, for example, the sum of the proportion of the number of gallium atoms and the proportion of the number of tin atoms can be the atomic proportion of the element M. The atomic ratio of indium to the element M to zinc is preferably within the ranges given above.

[0162] It is preferable to use a metal oxide in which the atomic proportion of indium with respect to the total number of atoms of all the metal elements contained in the metal oxide is higher than or equal to 30 atomic % and lower than or equal to 100 atomic %, preferably higher than or equal to 30 atomic % and lower than or equal to 95 atomic %, further preferably higher than or equal to 35 atomic % and lower than or equal to 95 atomic %, further preferably higher than or equal to 35 atomic % and lower than or equal to 90 atomic %, further preferably higher than or equal to 40 atomic % and lower than or equal to 90 atomic %, further preferably higher than or equal to 45 atomic % and lower than or equal to 90 atomic %, further preferably higher than or equal to 50 atomic % and lower than or equal to 80 atomic %, further preferably higher than or equal to 60 atomic % and lower than or equal to 80 atomic %, further preferably higher than or equal to 70 atomic % and lower than or equal to 80 atomic %. For example, when an In—Ga—Zn oxide is used for the semiconductor layer, the atomic ratio of indium with respect to the total number of the atoms of indium, the element M, and zinc is preferably within the ranges given above.

[0163] In this specification and the like, the atomic proportion of indium with respect to the total number of atoms of all the contained metal elements is sometimes referred to as indium content percentage. The same applies to other metal elements.

[0164] As an analysis method of the composition of a metal oxide, for example, energy dispersive X-ray spectroscopy (EDX), X-ray photoelectron spectrometry (XPS), inductively coupled plasma-mass spectrometry (ICP-MS), or inductively coupled plasma-atomic emission spectrometry (ICP-AES) can be used. Alternatively, such kinds of analysis methods may be performed in combination. Note that as for an element whose content percentage is low, the actual content percentage may be different from the content percentage obtained by analysis because of the influence of the analysis accuracy. In the case where the content percentage of the element M is low, for example, the content percentage of the element M obtained by analysis may be lower than the actual content percentage.

[0165] Note that a composition in the neighborhood in this specification and the like includes the range of ±30% of an intended atomic ratio. For example, when the atomic ratio is described as In:M:Zn=4:2:3 or a composition in the neighborhood thereof, the case is included where the atomic ratio of the element M is greater than or equal to 1 and less than or equal to 3 and the atomic ratio of zinc is greater than or equal to 2 and less than or equal to 4 with the atomic ratio of indium being 4. When the atomic ratio is described as In:M:Zn=5:1:6 or a composition in the neighborhood thereof, the case is included where the atomic ratio of the element Mis greater than 0.1 and less than or equal to 2 and the atomic ratio of zinc is greater than or equal to 5 and less than or equal to 7 with the atomic ratio of indium being 5. When the atomic ratio is described as In:M:Zn=1:1:1 or a composition in the neighborhood thereof, the case is included where the atomic ratio of the element Mis greater than 0.1 and less than or equal to 2 and the atomic ratio of zinc is greater than 0.1 and less than or equal to 2 with the atomic ratio of indium being 1.

[0166] A sputtering method or an atomic layer deposition (ALD) method can be suitably used to form the metal oxide. Note that in the case where the metal oxide is formed by a sputtering method, the atomic ratio of a target may be different from the atomic ratio of the metal oxide. In particular, the atomic ratio of zinc in the metal oxide is lower than the atomic ratio of zinc in the target in some cases. Specifically, the atomic ratio of zinc contained in the metal oxide may be approximately 40% to 90% of the atomic ratio of zinc contained in the target.

[0167] Here, the reliability of a transistor is described. One of indicators of evaluating the reliability of a transistor is a GBT (Gate Bias Temperature) stress test in which a state of applying an electric field to a gate is maintained. Among GBTs, a test in which a state where a positive potential (positive bias) relative to a source potential and a drain potential is supplied to a gate is maintained at high temperatures is referred to as a PBTS (Positive Bias Temperature Stress) test, and a test in which a state where a negative potential (negative bias) is supplied to a gate is maintained at high temperatures is referred to as an NBTS (Negative Bias Temperature Stress) test. The PBTS test and the NBTS test conducted in a state where irradiation is performed are respectively referred to as a PBTIS (Positive Bias Temperature Illumination Stress) test and an NBTIS (Negative Bias Temperature Illumination Stress) test.

[0168] In an n-channel transistor, a positive potential is supplied to a gate in putting the transistor in an on state (a state where current flows); thus, the amount of change in threshold voltage in the PBTS test is one important item to be focused on as an indicator of the reliability of the transistor.

[0169] With use of a metal oxide that does not contain gallium or has low gallium content in the semiconductor layer, the transistor can be highly reliable against positive bias application. In other words, the amount of change in the threshold voltage of the transistor in the PBTS test can be small. Meanwhile, with use of a metal oxide that contains gallium, the gallium content percentage is preferably lower than the indium content percentage. Thus, a highly reliable transistor can be achieved.

[0170] One of the factors in change in the threshold voltage in the PBTS test is a defect state at the interface between a semiconductor layer and a gate insulating layer or in the vicinity of the interface. As the density of defect states increases, degradation in the PBTS test becomes significant. Generation of the defect states can be inhibited by reducing the gallium content percentage in a region of the semiconductor layer that is in contact with the gate insulating layer.

[0171] The following can be given as an example of the reason why the amount of change in the threshold voltage in

the PBTS test can be reduced when a metal oxide that does not contain gallium or has a low gallium content percentage is used for the semiconductor layer. Gallium contained in the metal oxide has a property of attracting oxygen more easily than another metal element (e.g., indium or zinc) does. Thus, when, at the interface between a metal oxide containing a large amount of gallium and the gate insulating layer, gallium is bonded to excess oxygen in the gate insulating layer, trap sites of carriers (here, electrons) are probably generated easily. This might cause the change in the threshold voltage when a positive potential is supplied to a gate and carriers are trapped at the interface between the semiconductor layer and the gate insulating layer.

[0172] Specifically, in the case where an In—Ga—Zn oxide is used for the semiconductor layer, a metal oxide in which the atomic proportion of indium is higher than that of gallium can be used as the semiconductor layer. It is further preferable to use a metal oxide in which the atomic proportion of zinc is higher than the atomic proportion of gallium. In other words, a metal oxide in which the atomic ratios of metal elements satisfy In>Ga and Zn>Ga is preferably used as the semiconductor layer.

[0173] The semiconductor layer is preferably formed using a metal oxide having the following compositions; the atomic proportion of gallium with respect to the total number of atoms of all the contained metal elements is higher than 0 atomic % and lower than or equal to 50 atomic %, preferably higher than or equal to 0.1 atomic % and lower than or equal to 40 atomic %, further preferably higher than or equal to 0.1 atomic % and lower than or equal to 35 atomic %, further preferably higher than or equal to 0.1 atomic % and lower than or equal to 30 atomic %, further preferably higher than or equal to 0.1 atomic % and lower than or equal to 25 atomic %, further preferably higher than or equal to 0.1 atomic % and lower than or equal to 20 atomic %, further preferably higher than or equal to 0.1 atomic % and lower than or equal to 15 atomic %, further preferably higher than or equal to 0.1 atomic % and lower than or equal to 10 atomic %. The reduction in the gallium content percentage in the semiconductor layer enables the transistor to be highly resistant to the PBTS test. Note that oxygen vacancy (V_O) is less likely to be generated in the metal oxide when the metal oxide contains gallium.

[0174] A metal oxide not containing gallium may be used as the semiconductor layer. For example, an In—Zn oxide can be used for the semiconductor layer. In this case, when the atomic proportion of indium with respect to the total number of atoms of all the metal elements contained in the metal oxide is increased, the field-effect mobility of the transistor can be increased. By contrast, when the atomic proportion of zinc with respect to the total number of atoms of all the metal elements contained in the metal oxide is increased, the metal oxide has high crystallinity; thus, a change in the electrical characteristics of the transistor can be inhibited and the reliability can be increased. Alternatively, a metal oxide that contains neither gallium nor zinc, such as indium oxide, can be used as the semiconductor layer. The use of a metal oxide not containing gallium can make a change in the threshold voltage particularly in the PBTS test extremely small.

[0175] For example, an oxide containing indium and zinc can be used for the semiconductor layer. In that case, for example, a metal oxide where the atomic ratio of metal elements is In:Zn=2:3, In:Zn=4:1, or the neighborhood thereof can be used.

[0176] Although the case of using gallium is described as a typical example, the same applies to the case where the element Mis used instead of gallium. In particular, a metal oxide in which the atomic proportion of indium is higher than the atomic proportion of the element M is preferably used as the semiconductor layer. Furthermore, a metal oxide in which the atomic proportion of zinc is higher than the atomic proportion of the element M is preferably used.

[0177] The use of a metal oxide having a low content percentage of the element M for the semiconductor layer enables the transistor to be highly reliable against positive bias application. With use of the transistor as a transistor that is required to have high reliability against positive bias application, a highly reliable semiconductor device can be provided.

[0178] Next, the reliability of a transistor against light is described.

[0179] Light irradiation on a transistor may change electrical characteristics of the transistor. In particular, a transistor provided in a region on which light can be incident preferably exhibits a small variation in electrical characteristics under light irradiation and has high reliability against light. The reliability against light can be evaluated with the amount of change in threshold voltage in a NBTIS test, for example.

[0180] The high content percentage of the element M in the metal oxide enables the transistor to be highly reliable against light. In other words, the amount of change in the threshold voltage of the transistor in the NBTIS test can be small. Specifically, in a metal oxide in which the atomic proportion of the element M is higher than or equal to the atomic proportion of indium, the band gap is increased and accordingly the amount of change in the threshold voltage of the transistor in the NBTIS test can be reduced. The band gap of the metal oxide in the semiconductor layer is preferably greater than or equal to 2.0 eV, further preferably greater than or equal to 2.5 eV, further preferably greater than or equal to 3.0 eV, further preferably greater than or equal to 3.2 eV, further preferably greater than or equal to 3.3 eV, further preferably greater than or equal to 3.4 eV, further preferably greater than or equal to 3.5 eV.

[0181] For example, the semiconductor layer can include a metal oxide film having any of the following atomic ratios: In:M:Zn=1:1:1, In:M:Zn=1:1:1.2, In:M:Zn=1:3:2, In:M:Zn=1:3:3, In:M:Zn=1:3:4, and a neighborhood thereof.

[0182] For the semiconductor layer, in particular, it is preferable to use a metal oxide in which the atomic proportion of the element M with respect to the total number of atoms of all the contained metal elements is higher than or equal to 20 atomic % and lower than or equal to 70 atomic %, preferably higher than or equal to 30 atomic % and lower than or equal to 70 atomic %, further preferably higher than or equal to 30 atomic % and lower than or equal to 60 atomic %, further preferably higher than or equal to 40 atomic % and lower than or equal to 60 atomic %, further preferably higher than or equal to 50 atomic % and lower than or equal to 60 atomic %.

[0183] In the case where In—Ga—Zn oxide is used for the semiconductor layer, a metal oxide in which the atomic proportion of indium with respect to the total number of atoms of all the contained metal elements is lower than or

equal to the atomic proportion of gallium can be used. For example, it is possible to use a metal oxide having any of the following atomic ratios: In:Ga:Zn=1:1:1, In:Ga:Zn=1:1:1.2, In:Ga:Zn=1:3:2, In:Ga:Zn=1:3:3, In:Ga:Zn=1:3:4, and the neighborhood thereof.

[0184] For the semiconductor layer, in particular, it is preferable to use a metal oxide in which the atomic proportion of gallium with respect to the total number of atoms of all the contained metal elements is higher than or equal to 20 atomic % and lower than or equal to 60 atomic %, preferably higher than or equal to 20 atomic % and lower than or equal to 50 atomic %, further preferably higher than or equal to 30 atomic % and lower than or equal to 50 atomic %, further preferably higher than or equal to 40 atomic % and lower than or equal to 60 atomic %, further preferably higher than or equal to 50 atomic % and lower than or equal to 60 atomic %. The use of a metal oxide having a high content percentage of the element M for the semiconductor layer enables the transistor to be highly reliable against light. With use of the transistor as a transistor that is required to have high reliability against light, a highly reliable semiconductor device can be provided.

[0185] An increase in the content percentage of the element M can inhibit the formation of oxygen vacancies (V_O) in the metal oxide. Accordingly, when a metal oxide with a high content percentage of the element M is used for the semiconductor layer, generation of carriers due to oxygen vacancies (V_O) is inhibited, so that the transistor can have a low off-state current. Furthermore, a change in electrical characteristics of the transistor can be inhibited and the reliability of the transistor can be improved.

[0186] Furthermore, a metal oxide having a high zinc content percentage has high crystallinity, whereby diffusion of impurities can be inhibited. Accordingly, when a metal oxide with a high zinc content percentage is used for the semiconductor layer, a change in electrical characteristics of the transistor can be inhibited and the reliability can be increased.

[0187] As described above, electrical characteristics and reliability of a transistor depend on the composition of the metal oxide used for the semiconductor layer. Therefore, by determining the composition of the metal oxide in accordance with the electrical characteristics and reliability required for the transistor, the semiconductor device can have both good electrical characteristics and high reliability.

[0188] The semiconductor layer may have a stacked-layer structure including two or more metal oxide layers. The two or more metal oxide layers included in the semiconductor layer may have the same composition or substantially the same compositions. Employing a stacked-layer structure of metal oxide layers having the same composition can reduce the manufacturing cost because the metal oxide layers can be formed using the same sputtering target.

[0189] The two or more metal oxide layers included in the semiconductor layer may have different compositions. For example, a stacked-layer structure of a first metal oxide layer having In:M:Zn=1:3:4 [atomic ratio] or a composition in the neighborhood thereof and a second metal oxide layer having In:M:Zn=1:1:1 [atomic ratio] or a composition in the neighborhood thereof and being provided over the first metal oxide layer can be suitably employed. In particular, gallium or aluminum is preferably used as the element M. A stacked-layer structure of any one selected from indium oxide, indium gallium oxide, and IGZO and any one selected from IAZO, IAGZO, and ITZO (registered trademark) may be employed, for example.

[0190] It is preferable to use a metal oxide layer having crystallinity as the semiconductor layer. For example, a metal oxide layer having a CAAC (c-axis aligned crystal) structure, a polycrystalline structure, a nano-crystal (nc) structure, or the like can be used. With use of a metal oxide layer having crystallinity as the semiconductor layer, the density of defect states in the semiconductor layer can be reduced, which enables the semiconductor device to have high reliability.

[0191] The higher the crystallinity of the metal oxide layer used as the semiconductor layer is, the lower the density of defect states in the semiconductor layer can be. By contrast, the use of a metal oxide layer having low crystallinity enables a transistor to flow a large amount of current.

[0192] In the case where the metal oxide layer is formed by a sputtering method, the crystallinity of the formed metal oxide layer can be increased as the substrate temperature at the time of formation is higher. For example, the substrate temperature at the time of formation can be adjusted by the temperature of the stage on which the substrate is placed. The crystallinity of the formed metal oxide layer can be increased with a higher proportion of the flow rate of an oxygen gas to the total flow rate of the film formation gas used at the time of formation (hereinafter also referred to as a higher oxygen flow rate ratio) or with higher oxygen partial pressure in a processing chamber of a film formation apparatus.

[0193] The semiconductor layer may have a stacked-layer structure of two or more metal oxide layers having different crystallinities. For example, in a stacked-layer structure of a first metal oxide layer and a second metal oxide layer provided over the first metal oxide layer, the second metal oxide layer can include a region having higher crystallinity than the first metal oxide layer. Alternatively, the second metal oxide layer can include a region having lower crystallinity than the first metal oxide layer. The two or more metal oxide layers included in the semiconductor layer may have the same composition or substantially the same compositions. Employing a stacked-layer structure of metal oxide layers having the same composition can reduce the manufacturing cost because the metal oxide layers can be formed using the same sputtering target. For example, with use of the same sputtering target and different oxygen flow rate ratios or different oxygen partial pressures, a stacked-layer structure of two or more metal oxide layers having different crystallinities can be formed. The two or more metal oxide layers included in the semiconductor layer may have different compositions.

[0194] The thickness of each of the semiconductor layer **108** and the semiconductor layer **208** is preferably larger than or equal to 3 nm and smaller than or equal to 100 nm, further preferably larger than or equal to 5 nm and smaller than or equal to 100 nm, further preferably larger than or equal to 10 nm and smaller than or equal to 100 nm, further preferably larger than or equal to 10 nm and smaller than or equal to 70 nm, further preferably larger than or equal to 15 nm and smaller than or equal to 70 nm, further preferably larger than or equal to 15 nm and smaller than or equal to 50 nm, further preferably larger than or equal to 20 nm and smaller than or equal to 50 nm, further preferably larger than

or equal to 20 nm and smaller than or equal to 40 nm, further preferably larger than or equal to 25 nm and smaller than or equal to 40 nm.

[0195] The substrate temperature at the time of forming each of the semiconductor layer **108** and the semiconductor layer **208** is preferably higher than or equal to room temperature (25° C.) and lower than or equal to 200° C., further preferably higher than or equal to room temperature and lower than or equal to 130° C. With the substrate temperature in the above range, the bending or warpage of the substrate can be inhibited in the case where a large-area glass substrate is used.

[0196] Here, oxygen vacancies that might be formed in the semiconductor layer will be described.

[0197] In the case where an oxide semiconductor is used for the semiconductor layer, hydrogen contained in the oxide semiconductor reacts with oxygen bonded to a metal atom to be water, and thus sometimes forms oxygen vacancy (V_O) in the oxide semiconductor. In some cases, a defect where hydrogen enters oxygen vacancy (hereinafter referred to as V_OH) functions as a donor and generates an electron serving as a carrier. In other cases, bonding of part of hydrogen to oxygen bonded to a metal atom generates an electron serving as a carrier. Thus, a transistor including an oxide semiconductor that contains a large amount of hydrogen is likely to have normally-on characteristics. Moreover, hydrogen in an oxide semiconductor is easily transferred by a stress such as heat or an electric field; thus, a large amount of hydrogen contained in an oxide semiconductor might reduce the reliability of a transistor.

[0198] V_OH can function as a donor of the oxide semiconductor. However, it is difficult to evaluate the defect quantitatively. Thus, the oxide semiconductor is sometimes evaluated by not its donor concentration but its carrier concentration. Therefore, in this specification and the like, the carrier concentration on the assumption that the state where an electric field is not applied is sometimes used as the parameter of the oxide semiconductor, instead of the donor concentration. That is, "carrier concentration" described in this specification and the like can be replaced with "donor concentration" in some cases.

[0199] Accordingly, in the case where an oxide semiconductor is used as the semiconductor layer, the amount of V_OH in the semiconductor layer is preferably reduced as much as possible so that the semiconductor layer becomes a highly purified intrinsic or substantially highly purified intrinsic semiconductor layer. In order to obtain such an oxide semiconductor with sufficiently reduced V_OH, it is important to remove impurities (e.g., water and hydrogen) in the oxide semiconductor (this treatment is sometimes referred to as dehydration or dehydrogenation treatment) and supply oxygen to the oxide semiconductor to fill oxygen vacancy (V_O). When an oxide semiconductor with sufficiently reduced oxygen vacancy (V_O), V_OH, impurities is used for a channel formation region of a transistor, the transistor can have stable electrical characteristics. Supplying oxygen to the oxide semiconductor to fill oxygen vacancy (V_O) is sometimes referred to as oxygen adding treatment.

[0200] When an oxide semiconductor is used for the semiconductor layer, the carrier concentration of the oxide semiconductor in a region functioning as the channel formation region is preferably lower than or equal to 1×10^{18} cm^{-3}, further preferably lower than 1×10^{17} cm^{-3}, still further preferably lower than 1×10^{16} cm^{-3}, yet further preferably lower than 1×10^{13} cm^{-3}, yet still further preferably lower than 1×10^{12} cm^{-3}. Note that the lower limit of the carrier concentration of the oxide semiconductor in the region functioning as the channel formation region is not particularly limited and can be, for example, 1×10^{-9} cm^{-3}.

[0201] The region **208**D functioning as the source region or the drain region can also be referred to as a region having lower resistance than the channel formation region, a region having a higher carrier concentration than the channel formation region, a region having a higher oxygen defect density than the channel formation region, a region having a higher hydrogen concentration than the channel formation region, or a region having a higher impurity concentration than the channel formation region. Meanwhile, the carrier concentration in the region **208**D can be higher than or equal to 5×10^{18} cm^{-3}, preferably higher than or equal to 1×10^{19} cm^{-3}, further preferably higher than or equal to 5×10^{19} cm^{-3}, for example. The upper limit of the carrier concentration of the region **208**D is not particularly limited and can be, for example, 5×10^{21} cm^{-3} or 1×10^{22} cm^{-3}.

[0202] The electric resistance of the channel formation region in a state where the channel is not formed is preferably as high as possible. For example, the sheet resistance of the channel formation region is preferably higher than or equal to 1×10^{9} Ω/square, further preferably higher than or equal to 5×10^{9} Ω/square, still further preferably higher than or equal to 1×10^{10} Ω/square.

[0203] Since the electric resistance of the channel formation region in a state where the channel is not formed is preferably as high as possible, it is not necessary to set its upper limit. If the upper limit is set, the sheet resistance of the channel formation region is preferably higher than or equal to 1×10^{9} Ω/square and lower than or equal to 1×10^{12} Ω/square, further preferably higher than or equal to 5×10^{9} Ω/square and lower than or equal to 1×10^{12} Ω/square, still further preferably higher than or equal to 1×10^{10} Ω/square and lower than or equal to 1×10^{12} Ω/square, for example.

[0204] The electric resistance of the region **208**D is preferably as low as possible. For example, the sheet resistance of the region **208**D is preferably higher than or equal to 1 Ω/square and lower than 1×10^{3} Ω/square, further preferably higher than or equal to 1 Ω/square and lower than or equal to 8×10^{2} Ω/square.

[0205] The electric resistance of the channel formation region in a state where the channel is not formed can be higher than or equal to 1×10^{6} times and lower than or equal to 1×10^{12} times that of the region **208**D, preferably higher than or equal to 1×10^{6} times and lower than or equal to 1×10^{11} times that of the region **208**D, further preferably higher than or equal to 1×10^{6} times and lower than or equal to 1×10^{10} times that of the region **280**D.

[0206] The region **208**D is a region containing an impurity element. Examples of the impurity element include one or more of hydrogen, boron, carbon, nitrogen, fluorine, phosphorus, sulfur, arsenic, aluminum, magnesium, silicon, and a noble gas. Note that typical examples of a noble gas include helium, neon, argon, krypton, and xenon. It is particularly preferable to use one or more of boron, phosphorus, aluminum, magnesium, and silicon as the impurity element.

[0207] For example, the region **208**D can be formed by supplying the impurity element to the semiconductor layer **208** through the insulating layer **106** with the conductive layer **204** as a mask.

[0208] The semiconductor layer **108** can be formed in the same step as the semiconductor layer **208**. In other words, the semiconductor layer **208**, the same material as the semiconductor layer **108** can be used. For example, the semiconductor layer **108** and the semiconductor layer **208** can be formed using the same sputtering target, reducing the manufacturing cost.

[0209] When the region **208**D is formed, the impurity element may be supplied to the semiconductor layer **108** through the insulating layer **106** with use of the conductive layer **104** as a mask. Consequently, a region **108**D is formed in the region of the semiconductor layer **108** not overlapping with the conductive layer **104**. Note that in the transistor **100**, a region of the semiconductor layer **108** in contact with the conductive layer **112***b* serves as the source region or the drain region. The region **108**D is formed in part of the source region or the drain region. The region **108**D is not necessarily formed. For example, in the case where the conductive layer **104** is extended to cover the end portion of the semiconductor layer **108**, the conductive layer **104** masks the whole semiconductor layer **108** to preclude the supply of the impurity element to the semiconductor layer **108**, and the region **108**D is not formed.

[0210] A transistor including an oxide semiconductor (hereinafter referred to as an OS transistor) has much higher field-effect mobility than a transistor including amorphous silicon. In addition, the OS transistor has an extremely low leakage current between a source and a drain in an off state (hereinafter also referred to as off-state current), and charge accumulated in a capacitor that is connected in series with the transistor can be held for along period. Furthermore, the power consumption of the semiconductor device can be reduced with the OS transistor.

[0211] The semiconductor device of one embodiment of the present invention can be used for a display apparatus, for example. To increase the emission luminance of a light-emitting device included in a pixel circuit in the display apparatus, it is necessary to increase the amount of current flowing through the light-emitting device. To increase the amount of current, the source-drain voltage of a driving transistor included in the pixel circuit needs to be increased. Since the OS transistor has higher breakdown voltage between a source and a drain than a transistor including silicon (hereinafter referred to as a Si transistor), high voltage can be applied between the source and the drain of the OS transistor. Accordingly, when an OS transistor is used as the driving transistor included in the pixel circuit, the amount of current flowing through the light-emitting device can be increased, so that the emission luminance of the light-emitting device can be increased.

[0212] When a transistor operates in a saturation region, a change in source-drain current relative to a change in gate-source voltage can be smaller in an OS transistor than in a Si transistor. Accordingly, when an OS transistor is used as the driving transistor included in the pixel circuit, the amount of current flowing between the source and the drain can be finely set by a change in gate-source voltage; thus, the amount of current flowing through the light-emitting device can be controlled. Therefore, the number of gray levels in the pixel circuit can be increased.

[0213] Regarding saturation characteristics of current flowing when a transistor operates in a saturation region, even in the case where the source-drain voltage of an OS transistor increases gradually, more stable current (saturation current) can be made flow through the OS transistor than through a Si transistor. Thus, with use of an OS transistor as a driving transistor, current can be made flow stably to the light-emitting device, for example, even when a variation in current-voltage characteristics of the light-emitting device occurs. In other words, when the OS transistor operates in the saturation region, the source-drain current hardly changes even with an increase in the source-drain voltage; thus, the emission luminance of the light-emitting device can be stable.

[0214] As described above, with use of an OS transistor as the driving transistor included in the pixel circuit, it is possible to achieve "inhibition of black floating", "increase in emission luminance", "increase in the number of gray levels", "inhibition of variation in light-emitting devices", and the like.

[0215] A change in electrical characteristics of an OS transistor due to irradiation with radiation is small, i.e., an OS transistor has high tolerance to radiation; thus, an OS transistor can be suitably used even in an environment where radiation can enter. It can also be said that an OS transistor has high reliability against radiation. For example, an OS transistor can be suitably used for a pixel circuit of an X-ray flat panel detector. Moreover, an OS transistor can be suitably used for a semiconductor device used in space. Examples of radiation include electromagnetic radiation (e.g., X-rays and gamma rays) and particle radiation (e.g., alpha rays, beta rays, a proton beam, and a neutron beam).

[Insulating Layer **110** and Insulating Layer **120**]

[0216] For the insulating layer **110**, an inorganic insulating material or an organic insulating material can be used. The insulating layer **110** may have a stacked-layer structure of an inorganic insulating material and an organic insulating material.

[0217] For the insulating layer **110**, an inorganic insulating material can be suitably used. As the inorganic insulating material, one or more of an oxide, an oxynitride, a nitride oxide, and a nitride can be used. For the insulating layer **110**, for example, one or more of silicon oxide, silicon oxynitride, aluminum oxide, hafnium oxide, yttrium oxide, zirconium oxide, gallium oxide, tantalum oxide, magnesium oxide, lanthanum oxide, cerium oxide, neodymium oxide, silicon nitride, silicon nitride oxide, and aluminum nitride can be used.

[0218] Note that in this specification and the like, an oxynitride refers to a material that contains more oxygen than nitrogen in its composition. A nitride oxide refers to a material that contains more nitrogen than oxygen in its composition. For example, silicon oxynitride refers to a material that contains more oxygen than nitrogen in its composition, and silicon nitride oxide refers to a material that contains more nitrogen than oxygen in its composition.

[0219] The oxygen content and the nitrogen content can be analyzed by secondary ion mass spectrometry (SIMS) or X-ray photoelectron spectroscopy (XPS). When the content percentage of a target element is high (e.g., higher than or equal to 0.5 atomic %, or higher than or equal to 1 atomic %), XPS is suitable. In contrast, when the content percentage of a target element is low (e.g., lower than 0.5 atomic %, or

lower than 1 atomic %), SIMS is suitable. To compare the contents of elements, analysis with a combination of SIMS and XPS is preferably used.

[0220] The insulating layer **110** may have a stacked-layer structure of two or more layers. FIG. **1**B and the like illustrate a structure in which the insulating layer **110** has a stacked-layer structure of an insulating layer **110***a*, an insulating layer **110***b* over the insulating layer **110***a*, and an insulating layer **110***c* over the insulating layer **110***b*. For each of the insulating layer **110***a*, the insulating layer **110***b*, and the insulating layer **110***c*, the material that can be used for the insulating layer **110** can be used. For the insulating layer **110***a*, the insulating layer **110***b*, and the insulating layer **110***c*, the same material or different materials may be used. Note that the insulating layer **110***a*, the insulating layer **110***b*, and the insulating layer **110***c* may each have a stacked-layer structure of two or more layers.

[0221] The thickness of the insulating layer **110***b* can be larger than the thickness of the insulating layer **110***a*. The thickness of the insulating layer **110***b* can be larger than the thickness of the insulating layer **110***c*. The formation speed of the insulating layer **110***b* is preferably high. In particular, the formation speed of the insulating layer **110***b* is preferably high in the case where the thickness of the insulating layer **110***b* is large. By increasing the formation speed of the insulating layer **110***b*, the productivity can be increased. For example, by increasing power at the time of forming the insulating layer **110***b*, the formation speed can be increased.

[0222] The insulating layer **110***b* may have a stacked-layer structure of two or more layers. For example, the insulating layer **110***b* has high stress when the insulating layer **110***b* has a large thickness, which might cause warpage of the substrate. In some cases, the formation of the insulating layer **110***b* in a plurality of steps can inhibit occurrence of problems during the process caused by stress. Note that in a cross-sectional transmission electron microscopy (TEM) image or the like, a boundary between the layers included in the insulating layer **110***b* is unclear in some cases.

[0223] The stress of the insulating layer **110***b* is preferably low. The insulating layer **110***b* has high stress when the insulating layer **110***b* has a large thickness, which might cause warpage of the substrate. The low stress of the insulating layer **110***b* can inhibit occurrence of problems during the process caused by stress such as warpage of the substrate.

[0224] The insulating layer **110***a* and the insulating layer **110***c* function as blocking films that inhibit release of gas from the insulating layer **110***b*. For each of the insulating layer **110***a* and the insulating layer **110***c*, a material in which gas is hardly diffused is preferably used. The insulating layer **110***a* and the insulating layer **110***c* each preferably include a region having a higher film density than the insulating layer **110***b*. The insulating layer **110***a* and the insulating layer **110***c* having high film densities can have a high blocking property. Note that the insulating layer **110***a* and the insulating layer **110***c* may have different film densities. For each of the insulating layer **110***a* and the insulating layer **110***c*, a material containing more nitrogen than the insulating layer **110***b* can be used, for example. The insulating layer **110***a* and the insulating layer **110***c* in each of which the nitrogen content is high can have a high blocking property. Note that the insulating layer **110***a* and the insulating layer **110***c* may have different nitrogen contents.

[0225] The insulating layer **110***a* and the insulating layer **110***c* have thicknesses with which the insulating layers function as blocking films that inhibit release of gas from the insulating layer **110***b*, and can be thinner than the insulating layer **110***b*. Note that the insulating layer **110***a* and the insulating layer **110***c* may have different thicknesses. The formation speeds of the insulating layer **110***a* and the insulating layer **110***c* are preferably lower than the formation speed of the insulating layer **110***b*. Note that each of the insulating layer **110***a* and the insulating layer **110***c* formed at a low speed has a high film density and can have a high blocking property. Similarly, each of the insulating layer **110***a* and the insulating layer **110***c* formed at a high substrate temperature has a high film density and can have a high blocking property.

[0226] The film density can be evaluated by Rutherford backscattering spectrometry (RBS) or X-ray reflection (XRR), for example. A difference in film density can be evaluated using a transmission electron microscopy (TEM) image of a cross section in some cases. In TEM observation, a transmission electron (TE) image is dark-colored (dark) when the film density is high, and a transmission electron (TE) image is pale (bright) when the film density is low. Therefore, in a transmission electron (TE) image, the insulating layer **110***a* and the insulating layer **110***c* are each sometimes shown as a dark-colored (dark) image compared to the insulating layer **110***b*. Note that since the insulating layer **110***a*, the insulating layer **110***b*, and the insulating layer **110***c* have different film densities even when including the same materials, it is sometimes possible to identify the boundary between the insulating layers by a difference in contrast in a TEM image of a cross section.

[0227] A difference in nitrogen content between the insulating layer **110***a*, the insulating layer **110***b*, and the insulating layer **110***c* can be confirmed by EDX, for example. In the case where silicon nitride is used for the insulating layer **110***a* and silicon oxynitride is used for the insulating layer **110***b*, for example, the ratio of the peak intensity of nitrogen to the peak intensity of silicon in the insulating layer **110***a* is higher than the ratio of the peak intensity of nitrogen to the peak intensity of silicon in the insulating layer **110***b*. In the case where silicon nitride is used for the insulating layer **110***c* and silicon oxynitride is used for the insulating layer **110***b*, the ratio of the peak intensity of nitrogen to the peak intensity of silicon in the insulating layer **110***c* is higher than the ratio of the peak intensity of nitrogen to the peak intensity of silicon in the insulating layer **110***b*. Note that in EDX, the peak of a certain element refers to a point at which the number of counts of the element reaches a local maximum value in a spectrum where the horizontal axis represents the energy of characteristic X-rays and the vertical axis represents the number of counts (the detected value) of characteristic X-rays. Alternatively, the number of counts at an energy of a characteristic X-ray unique to the element may be used to confirm a difference in nitrogen content with the ratio of the number of counts of nitrogen to the number of counts of silicon. For example, the number of counts at 1.739 keV (Si-Kα) can be used for silicon, and the number of counts at 0.392 keV (N-Kα) can be used for nitrogen. The ratio of the number of counts of nitrogen to the number of counts of silicon in the insulating layer **110***a* is higher than the ratio of the number of counts of nitrogen to the number of counts of silicon in the insulating layer **110***b*. The ratio of the number of counts of nitrogen to the number of counts of

silicon in the insulating layer **110***c* is higher than the ratio of the number of counts of nitrogen to the number of counts of silicon in the insulating layer **110***b*.

[0228] The insulating layer **110***a* and the insulating layer **110***c* may each include a region having a lower hydrogen concentration in the film than the insulating layer **110***b*. The difference in hydrogen concentration between the insulating layer **110***a*, the insulating layer **110***b*, and the insulating layer **110***c* can be examined by secondary ion mass spectrometry (SIMS), for example.

[0229] Here, the insulating layer **110** will be described in detail with use of a structure in which a metal oxide is used for the semiconductor layer **108** as an example.

[0230] In the case where an oxide semiconductor is used for the semiconductor layer **108**, an inorganic insulating material can be suitably used for each of the insulating layer **110***a*, the insulating layer **110***b*, and the insulating layer **110***c*.

[0231] It is preferable to use an oxide or an oxynitride for the insulating layer **110***b*. A film from which oxygen is released by heating is preferably used as the insulating layer **110***b*. For example, silicon oxide or silicon oxynitride can be suitably used for the insulating layer **110***b*.

[0232] Oxygen released from the insulating layer **110***b* can be supplied to the semiconductor layer **108**. Supplying oxygen from the insulating layer **110***b* to the semiconductor layer **108**, particularly to the channel formation region in the semiconductor layer **108**, can allow the amount of oxygen vacancy (V_O) and V_OH to be reduced in the semiconductor layer **108**, so that a highly reliable transistor having favorable electrical characteristics can be obtained. The insulating layer **110***b* preferably has a high oxygen diffusion coefficient. When the insulating layer **110***b* has a high oxygen diffusion coefficient, oxygen easily diffuses in the insulating layer **110***b*, so that oxygen can be efficiently supplied from the insulating layer **110***b* to the semiconductor layer **108**. Examples of treatment for supplying oxygen to the semiconductor layer **108** include heat treatment in an oxygen-containing atmosphere and plasma treatment in an oxygen-containing atmosphere.

[0233] It is preferable that the amount of oxygen vacancy (V_O) and V_OH be small in the channel formation region of the transistor **100**. Particularly in the case where the channel length L**100** is short, oxygen vacancy (V_O) and V_OH in the channel formation region greatly affect electrical characteristics and reliability. For example, diffusion of V_OH from the source region or the drain region into the channel formation region increases the carrier concentration in the channel formation region, which might cause a change in the threshold voltage or a reduction in the reliability in the transistor **100**. As the channel length L**100** of the transistor **100** is shorter, such diffusion of V_OH greatly affects electrical characteristics and reliability. Supplying oxygen from the insulating layer **110***b* to the semiconductor layer **108**, particularly to the channel formation region in the semiconductor layer **108**, can allow the amount of oxygen vacancy (V_O) and V_OH to be reduced. Thus, the transistor with a short channel length can have favorable electrical characteristics and high reliability.

[0234] The amount of impurities (e.g., water and hydrogen) released from the insulating layer **110***b* itself is preferably small. With the insulating layer **110***b* from which a small amount of impurities is released, diffusion of impurities into the semiconductor layer **108** is inhibited, and the transistor can have favorable electrical characteristics and high reliability.

[0235] For example, silicon oxide or silicon oxynitride formed by a PECVD method can be suitably used for the insulating layer **110***b*. In that case, a mixed gas including a gas containing silicon and a gas containing oxygen is preferably used as a source gas. As the gas containing silicon, one or more of silane, disilane, trisilane, and silane fluoride can be used, for example. As the gas containing oxygen, one or more of oxygen (O_2), ozone (O_3), nitrous oxide (N_2O), nitric oxide (NO), and nitrogen dioxide (NO_2) can be used, for example. Note that by increasing power at the time of forming the insulating layer **110***b*, the amount of impurities (e.g., water and hydrogen) released from the insulating layer **110***b* can be reduced.

[0236] The insulating layer **110***a* and the insulating layer **110***c* are preferably less likely to transmit oxygen. The insulating layer **110***a* and the insulating layer **110***c* function as blocking films that inhibit release of oxygen from the insulating layer **110***b*. Moreover, the insulating layer **110***a* and the insulating layer **110***c* are preferably less likely to transmit hydrogen. The insulating layer **110***a* and the insulating layer **110***c* function as blocking films that inhibit diffusion of hydrogen into the semiconductor layer **108** from the outside of the transistor through the insulating layer **110**. The insulating layer **110***a* and the insulating layer **110***c* preferably have high film densities. The insulating layer **110***a* and the insulating layer **110***c* having high film densities can have a high blocking property against oxygen and hydrogen. The film densities of the insulating layer **110***a* and the insulating layer **110***c* are preferably higher than the film density of the insulating layer **110***b*. In the case where silicon oxide or silicon oxynitride is used for the insulating layer **110***b*, silicon nitride, silicon nitride oxide, or aluminum oxide can be suitably used for each of the insulating layer **110***a* and the insulating layer **110***c*, for example. The insulating layer **110***a* and the insulating layer **110***c* each preferably include a region containing more nitrogen than the insulating layer **110***b*. For each of the insulating layer **110***a* and the insulating layer **110***c*, a material containing more nitrogen than the insulating layer **110***b* can be used, for example. A nitride or a nitride oxide is preferably used for each of the insulating layer **110***a* and the insulating layer **110***c*. For example, silicon nitride or silicon nitride oxide can be suitably used for each of the insulating layer **110***a* and the insulating layer **110***c*.

[0237] When oxygen contained in the insulating layer **110***b* diffuses upward from a region of the insulating layer **110***b* that is not in contact with the semiconductor layer **108** (e.g., the top surface of the insulating layer **110***b*), the amount of oxygen supplied from the insulating layer **110***b* to the semiconductor layer **108** might be reduced. Provision of the insulating layer **110***c* over the insulating layer **110***b* can inhibit diffusion of oxygen contained in the insulating layer **110***b* from the region of the insulating layer **110** that is not in contact with the semiconductor layer **108**. Similarly, provision of the insulating layer **110***a* under the insulating layer **110***b* can inhibit downward diffusion of oxygen from the region of the insulating layer **110** that is not in contact with the semiconductor layer **108**. Accordingly, the amount of oxygen supplied from the insulating layer **110***b* to the semiconductor layer **108** is increased, whereby the amount of oxygen vacancy (V_O) and V_OH in the semiconductor

layer **108** can be reduced. Consequently, the transistor can have favorable electrical characteristics and high reliability.

[0238] The conductive layer **112***a* and the conductive layer **112***b* are oxidized by oxygen contained in the insulating layer **110***b* and have high resistance in some cases. Moreover, when the conductive layer **112***a* and the conductive layer **112***b* are oxidized by oxygen contained in the insulating layer **110***b*, the amount of oxygen supplied from the insulating layer **110***b* to the semiconductor layer **108** might be reduced. Provision of the insulating layer **110***a* between the insulating layer **110***b* and the conductive layer **112***a* can inhibit the conductive layer **112***a* from being oxidized and having high resistance. Similarly, provision of the insulating layer **110***c* between the insulating layer **110***b* and the conductive layer **112***b* can inhibit the conductive layer **112***b* from being oxidized and having high resistance. In addition, the amount of oxygen supplied from the insulating layer **110***b* to the semiconductor layer **108** is increased and the amount of oxygen vacancy (V_O) and V_OH in the semiconductor layer **108** can be reduced, whereby the transistor can have favorable electric characteristics and high reliability.

[0239] Hydrogen diffused in the semiconductor layer **108** reacts with an oxygen atom contained in an oxide semiconductor to be water, and thus sometimes forms oxygen vacancy (V_O). Furthermore, V_OH is formed and the carrier concentration is increased in some cases. Provision of the insulating layer **110***a* and the insulating layer **110***c* can allow the amount of oxygen vacancy (V_O) and V_OH to be reduced in the semiconductor layer **108**, whereby the transistor can have favorable electric characteristics and high reliability.

[0240] The insulating layer **110***a* and the insulating layer **110***c* preferably have thicknesses with which the insulating layers function as blocking films against oxygen and hydrogen. When the insulating layer **110***a* and the insulating layer **110***c* are thin, the function of a blocking film might deteriorate. Meanwhile, when the insulating layer **110***a* and the insulating layer **110***c* are thick, a region where the semiconductor layer **108** is in contact with the insulating layer **110***b* is narrowed and the amount of oxygen supplied from the insulating layer **110***b* to the semiconductor layer **108** might be reduced. The insulating layer **110***a* and the insulating layer **110***c* may each be thinner than the insulating layer **110***b*. The thicknesses of the insulating layer **110***a* and the insulating layer **110***c* are each preferably larger than or equal to 5 nm and smaller than or equal to 100 nm, further preferably larger than or equal to 5 nm and smaller than or equal to 70 nm, further preferably larger than or equal to 10 nm and smaller than or equal to 70 nm, further preferably larger than or equal to 10 nm and smaller than or equal to 50 nm, further preferably larger than or equal to 20 nm and smaller than or equal to 50 nm, further preferably larger than or equal to 20 nm and smaller than or equal to 40 nm. The thicknesses of the insulating layer **110***a* and the insulating layer **110***c* in the above range can allow the amount of oxygen vacancy (V_O) and V_OH to be reduced in the semiconductor layer **108**, particularly in the channel formation region, whereby the transistor can have favorable electric characteristics and high reliability.

[0241] The amount of impurities (e.g., water and hydrogen) released from the insulating layer **110***a* and the insulating layer **110***c* themselves is preferably small. With the insulating layer **110***a* and the insulating layer **110***c* from which a small amount of impurities is released, diffusion of impurities into the semiconductor layer **108** is inhibited, and the transistor can have favorable electrical characteristics and high reliability.

[0242] By reducing the amount of impurities (e.g., water and hydrogen) released from the insulating layer **110***a* and the insulating layer **110***c*, the semiconductor layer **108** in a region in contact with the insulating layer **110***a* and the semiconductor layer **108** in a region in contact with the insulating layer **110***c* can each also function as the channel formation region. Note that when a material that releases impurities (e.g., water and hydrogen) is used for the insulating layer **110***a*, the semiconductor layer **108** in the region in contact with the insulating layer **110***a* can function as the source region or the drain region. The same applies to the insulating layer **110***c*.

[0243] In the transistor **100**, oxygen is supplied from the insulating layer **110** to the semiconductor layer **108**, whereby the amount of oxygen vacancy (V_O) and V_OH in the channel formation region is reduced. Consequently, the transistor can have favorable electrical characteristics and high reliability.

[0244] Due to heat applied in a step after the formation of the semiconductor layer **108**, oxygen might be released from the semiconductor layer **108**. However, supply of oxygen from the insulating layer **110** to the semiconductor layer **108** can inhibit an increase in the amount of oxygen vacancy (V_O) and V_OH. Furthermore, in a step after the formation of the semiconductor layer **108**, the flexibility of the treatment temperature can be increased. Specifically, also in a step after the formation of the semiconductor layer **108**, the treatment temperature can be high. Consequently, the transistor **100** can have favorable electrical characteristics and high reliability.

[0245] Note that one or both of the insulating layer **110***a* and the insulating layer **110***c* are not necessarily provided. A structure in which neither the insulating layer **110***a* nor the insulating layer **110***c* is provided may be employed.

[0246] For the insulating layer **120**, a material that can be used for the insulating layer **110** can be used. Although the insulating layer **120** has a single-layer structure in FIG. **1**B and the like, one embodiment of the present invention is not limited thereto. The insulating layer **120** may have a stacked-layer structure of two or more layers.

[0247] In the case where a metal oxide is used for the semiconductor layer **108** and the semiconductor layer **208**, an insulating layer containing oxygen is preferably used as the insulating layer **120** in contact with the semiconductor layer **108** and the semiconductor layer **208**. It is preferable to use an oxide or an oxynitride for the insulating layer **120**. A film from which oxygen is released by heating is preferably used as the insulating layer **120**. For example, silicon oxide or silicon oxynitride can be suitably used for the insulating layer **120**.

[0248] Note that a structure in which no insulating layer **120** is provided may be employed.

[Conductive Layer **112***a*, Conductive Layer **112***b*, Conductive Layer **104**, Conductive Layer **212***a*, Conductive Layer **212***b*, and Conductive Layer **204**]

[0249] The conductive layer **112***a*, the conductive layer **112***b*, the conductive layer **104**, the conductive layer **212***a*, the conductive layer **212***b*, and the conductive layer **204** each functioning as a source electrode, a drain electrode, or a gate electrode can each be formed using one or more of

chromium, copper, aluminum, gold, silver, zinc, tantalum, titanium, tungsten, manganese, nickel, iron, cobalt, molybdenum, and niobium; or an alloy including one or more of these metals as its components. For each of the conductive layer **112***a*, the conductive layer **112***b*, the conductive layer **104**, the conductive layer **212***a*, the conductive layer **212***b*, and the conductive layer **204**, a conductive material with low electrical resistivity that contains one or more of copper, silver, gold, and aluminum can be suitably used. Copper or aluminum is particularly preferable because of its high mass-productivity.

[0250] As the conductive layer **112***a*, the conductive layer **112***b*, the conductive layer **104**, the conductive layer **212***a*, the conductive layer **212***b*, and the conductive layer **204**, metal oxide films (also referred to as oxide conductors) can be used. Examples of the oxide conductor (OC) include In—Sn oxide (ITO), In—W oxide, In—W—Zn oxide, In—Ti oxide, In—Ti—Sn oxide, In—Zn oxide, In—Sn—Si oxide (ITSO), and In—Ga—Zn oxide.

[0251] Here, an oxide conductor (OC) is described. For example, when oxygen vacancy is formed in a metal oxide having semiconductor characteristics and hydrogen is added to the oxygen vacancy, a donor level is formed in the vicinity of the conduction band. As a result, the conductivity of the metal oxide is increased, so that the metal oxide becomes a conductor. The metal oxide having become a conductor can be referred to as an oxide conductor.

[0252] Each of the conductive layer **112***a*, the conductive layer **112***b*, the conductive layer **104**, the conductive layer **212***a*, the conductive layer **212***b*, and the conductive layer **204** may have a stacked-layer structure of a conductive film containing the oxide conductor (the metal oxide) and a conductive film containing a metal or an alloy. The use of the conductive film containing a metal or an alloy can reduce the wiring resistance.

[0253] A Cu—X alloy film (X is Mn, Ni, Cr, Fe, Co, Mo, Ta, or Ti) may be used for each of the conductive layer **112***a*, the conductive layer **112***b*, the conductive layer **104**, the conductive layer **212***a*, the conductive layer **212***b*, and the conductive layer **204**. The use of a Cu—X alloy film enables the manufacturing cost to be reduced because a wet etching method can be used in the processing.

[0254] Note that the conductive layer **112***a*, the conductive layer **112***b*, the conductive layer **104**, the conductive layer **212***a*, the conductive layer **212***b*, and the conductive layer **204** may be formed using the same material or different materials.

[0255] Here, the conductive layer **112***a* and the conductive layer **112***b* will be described in detail with use of a structure in which a metal oxide is used for each of the semiconductor layer **108** and the semiconductor layer **208** as an example.

[0256] When an oxide semiconductor is used for the semiconductor layer **108**, the conductive layer **112***a* and the conductive layer **112***b* are oxidized by oxygen contained in the semiconductor layer **108** and have high resistance in some cases. The conductive layer **112***a* and the conductive layer **112***b* are oxidized by oxygen contained in the insulating layer **110***b* and have high resistance in some cases. Moreover, when the conductive layer **112***a* and the conductive layer **112***b* are oxidized by oxygen contained in the semiconductor layer **108**, the amount of oxygen vacancy (V_O) in the semiconductor layer **108** is increased in some cases. When the conductive layer **112***a* and the conductive layer **112***b* are oxidized by oxygen contained in the insulating layer **110***b*, the amount of oxygen supplied from the insulating layer **110***b* to the semiconductor layer **108** might be reduced.

[0257] Since the channel length L**100** of the transistor **100** is shorter than that of the transistor **200**, oxygen vacancies (V_O) and V_OH in the channel formation region greatly affect the electrical characteristics and reliability of the transistor **100**. For example, diffusion of V_OH from the source region or the drain region into the channel formation region increases the carrier concentration in the channel formation region, which might cause a change in the threshold voltage or a reduction in the reliability of the transistor **100**. The shorter the channel length is, the more the electrical characteristics and reliability are affected by such diffusion of V_OH. Thus, a material that is less likely to be oxidized is preferably used for each of the conductive layer **112***a* and the conductive layer **112***b* in contact with the semiconductor layer **108**. An oxide conductor is preferably used for each of the conductive layer **112***a* and the conductive layer **112***b*. For example, In—Sn oxide (ITO) or In—Sn—Si oxide (ITSO) can be suitably used. For the conductive layer **112***a* and the conductive layer **112***b*, a nitride conductor may be used. Examples of the nitride conductor include tantalum nitride and titanium nitride. The conductive layer **112***a* and the conductive layer **112***b* may have a stacked-layer structure of the above-described materials. Note that the conductive layer **112***a* and the conductive layer **112***b* may be formed using the same material or different materials.

[0258] The conductive layer **112***a* and the conductive layer **112***b* each containing a material that is less likely to be oxidized can be inhibited from being oxidized by oxygen contained in the semiconductor layer **108** or oxygen contained in the insulating layer **110***b* and having high resistance. Furthermore, it is possible to increase the amount of oxygen supplied from the insulating layer **110***b* to the semiconductor layer **108** while an increase in the amount of oxygen vacancy (V_O) in the semiconductor layer **108** is inhibited. Accordingly, the amount of oxygen vacancy (V_O) and V_OH in the semiconductor layer **108** can be reduced, whereby the transistor **100** can have favorable electric characteristics and high reliability.

[0259] Note that a material that is less likely to be oxidized may be used for the conductive layer **212***a* and the conductive layer **212***b*. The conductive layer **212***a* and the conductive layer **212***b* can be formed using a material that can be used for the conductive layer **112***a* and the conductive layer **112***b*.

[0260] As described above, a material that is less likely to be oxidized is preferably used for each of the conductive layer **112***a* and the conductive layer **112***b* in contact with the semiconductor layer **108**. However, the use of a material that is less likely to be oxidized might increase resistance. The conductive layer **112***a* and the conductive layer **112***b* function as wirings and thus preferably have low resistance. In view of this, a material that is less likely to be oxidized is used for the conductive layer **112***a*_**1** including a region in contact with the semiconductor layer **108**, and a material with low electrical resistivity is used for the conductive layer **112***a*_**2** not including a region in contact with the semiconductor layer **108**, whereby the resistance of the conductive layer **112***a* can be reduced. Furthermore, the amount of oxygen vacancy (V_O) and V_OH in the semiconductor layer **108** can be reduced, whereby the transistor can have favorable electric characteristics and high reliability.

[0261] In particular, in the case where the channel length L**100** is short, oxygen vacancy (V_O) and V_OH in the channel formation region greatly affect electrical characteristics and reliability, as described above. When a material that is less likely to be oxidized is used for the conductive layer **112***a*_**1**, an increase in the amount of oxygen vacancy (V_O) and V_OH in the semiconductor layer **108** can be inhibited. Thus, the transistor with a short channel length can have favorable electrical characteristics and high reliability.

[0262] One or more of an oxide conductor and a nitride conductor can be suitably used for the conductive layer **112***a*_**1**. For the conductive layer **112***a*_**2**, a material having lower electrical resistivity than the conductive layer **112***a*_**1** is preferably used. For the conductive layer **112***a*_**2**, one or more of copper, aluminum, titanium, tungsten, and molybdenum or an alloy containing one or more of these metals as its components can be suitably used, for example. Specifically, In—Sn—Si oxide (ITSO) and tungsten can be suitably used for the conductive layer **112***a*_**1** and the conductive layer **112***a*_**2**, respectively.

[0263] Note that the structure of the conductive layer **112***a* is determined in accordance with wiring resistance required for the conductive layer **112***a*. For example, when the wiring (the conductive layer **112***a*) is short and requires relatively high wiring resistance, the conductive layer **112***a* may have a single-layer structure using a material that is less likely to be oxidized. Meanwhile, when the wiring (the conductive layer **112***a*) is long and requires relatively low wiring resistance, the conductive layer **112***a* preferably has a stacked-layer structure using a material that is less likely to be oxidized and a material with low electrical resistivity.

[0264] The structure of the conductive layer **112***a* can be employed for another conductive layer. For example, the conductive layer **112***b* has a stacked-layer structure of a first conductive layer and a second conductive layer over the first conductive layer, and part of the second conductive layer is removed so that a region where the first conductive layer is exposed is provided. In the region, the first conductive layer and the semiconductor layer **108** may be in contact with each other.

[Insulating Layer **106**]

[0265] The insulating layer **106** functioning as a gate insulating layer of each of the transistor **100** and the transistor **200** preferably has low defect density. With the insulating layer **106** having low defect density, the transistor **100** and the transistor **200** can have favorable electrical characteristics. In addition, the insulating layer **106** preferably has high breakdown voltage. With the insulating layer **106** having high breakdown voltage, the transistor **100** and the transistor **200** can have high reliability.

[0266] For the insulating layer **106**, one or more of an insulating oxide, an insulating oxynitride, an insulating nitride oxide, and an insulating nitride can be used, for example. For the insulating layer **106**, one or more of silicon oxide, silicon oxynitride, silicon nitride oxide, silicon nitride, aluminum oxide, aluminum oxynitride, aluminum nitride oxide, aluminum nitride, hafnium oxide, hafnium oxynitride, gallium oxide, gallium oxynitride, yttrium oxide, yttrium oxynitride, and Ga—Zn oxide can be used. The insulating layer **106** may be either a single layer or a stacked layer. The insulating layer **106** may have a stacked-layer structure of an oxide and a nitride.

[0267] A transistor having a minute size and including a thin gate insulating layer may have a large leakage current. When a high dielectric constant material (also referred to as a high-k material) is used for the gate insulating layer, the voltage at the time of operation of the transistor can be reduced while the physical thickness is maintained. Examples of the high-k material include gallium oxide, hafnium oxide, zirconium oxide, an oxide containing aluminum and hafnium, an oxynitride containing aluminum and hafnium, an oxide containing silicon and hafnium, an oxynitride containing silicon and hafnium, and a nitride containing silicon and hafnium.

[0268] The amount of impurities (e.g., water and hydrogen) released from the insulating layer **106** itself is preferably small. With the insulating layer **106** from which a small amount of impurities is released, diffusion of impurities into the semiconductor layer **108** and the semiconductor layer **208** is inhibited, and the transistor can have favorable electrical characteristics and high reliability.

[0269] The insulating layer **106** is formed over the semiconductor layer **108** and the semiconductor layer **208**, and thus is preferably a film formed under conditions where damage to the semiconductor layer **108** and the semiconductor layer **208** is small. For example, the insulating layer **106** is preferably formed under conditions where the film formation speed (also referred to as film formation rate) is sufficiently low. For example, when the insulating layer **106** is formed by a plasma CVD method under a low-power condition, damage to the semiconductor layer **108** and the semiconductor layer **208** can be extremely small.

[0270] Here, the insulating layer **106** will be described in detail with use of a structure in which a metal oxide is used for each of the semiconductor layer **108** and the semiconductor layer **208** as an example.

[0271] In order to improve properties of the interface between the insulating layer **106** and the semiconductor layer **108** and the interface between the insulating layer **106** and the semiconductor layer **208**, an oxide or an oxynitride is preferably used at least for the side of the insulating layer **106** that is in contact with the semiconductor layer **108** and the semiconductor layer **208**. For example, one or more of silicon oxide and silicon oxynitride can be suitably used for the insulating layer **106**. A film from which oxygen is released by heating is further preferably used for the insulating layer **106**.

[0272] Note that the insulating layer **106** may have a stacked-layer structure. The insulating layer **106** can have a stacked-layer structure of an oxide film on the side in contact with the semiconductor layer **108** and the semiconductor layer **208** and a nitride film on the side in contact with the conductive layer **104** and the conductive layer **204**. For example, one or more of silicon oxide and silicon oxynitride can be suitably used for the oxide film. Silicon nitride can be suitably used for the nitride film.

[Substrate **102**]

[0273] Although there is no great limitation on a material of the substrate **102**, it is necessary that the substrate have heat resistance high enough to withstand at least heat treatment performed later. For example, a single crystal semiconductor substrate or a polycrystalline semiconductor substrate of silicon or silicon carbide, a compound semiconductor substrate of silicon germanium or the like, an SOI substrate, a glass substrate, a quartz substrate, a sapphire

substrate, a ceramic substrate, or an organic resin substrate may be used as the substrate **102**. Alternatively, any of these substrates over which a semiconductor element is provided may be used as the substrate **102**. Note that the shape of the semiconductor substrate and an insulating substrate may be a circular shape or a shape with corners.

[0274] A flexible substrate may be used as the substrate **102**, and the transistor **100** and the like may be formed directly on the flexible substrate. Alternatively, a separation layer may be provided between the substrate **102** and the transistor **100** and the like. The separation layer can be used when part or the whole of a semiconductor device completed thereover is separated from the substrate **102** and transferred onto another substrate. In such a case, the transistor **100** and the like can be transferred to a substrate having low heat resistance or a flexible substrate as well.

[0275] Note that FIG. **1**B and the like illustrate the structure of the transistor **100** in which the thickness of the region in contact with the semiconductor layer **108** and the thickness of the region not in contact with the semiconductor layer **108** are equal to or substantially equal to each other in the conductive layer **112***a* (specifically, the conductive layer **112***a*_**1**); however, one embodiment of the present invention is not limited thereto. The thickness of the region in contact with the semiconductor layer **108** and the thickness of the region not in contact with the semiconductor layer **108** may be different from each other in the conductive layer **112***a*_**1**. As illustrated in FIG. **6**A, the thickness of the region in contact with the semiconductor layer **108** is preferably smaller than the thickness of the region not in contact with the semiconductor layer **108** in the conductive layer **112***a*_**1**.

[0276] FIG. **6**A illustrates a height H**104** from the formation surface of the conductive layer **112***a*_**1** (here, the top surface of the substrate **102**) to the lowest position of the bottom surface of the conductive layer **104**. FIG. **6**A also illustrates a height H**112***a* from the formation surface of the conductive layer **112***a*_**1** (here, the top surface of the substrate **102**) to the highest position of the region where the conductive layer **112***a*_**1** and the semiconductor layer **108** are in contact with each other. As illustrated in FIG. **6**A, the height H**104** to the lowest position of the bottom surface of the conductive layer **104** is preferably equal to or substantially equal to the height H**112***a* to the highest position of the region where the conductive layer **112***a*_**1** and the semiconductor layer **108** are in contact with each other. Alternatively, as illustrated in FIG. **6**B, the height H**104** is preferably smaller than the height H**112***a*. When the height H**104** to the lowest position of the bottom surface of the conductive layer **104** is equal to the height H**112***a* to the highest position of the region where the conductive layer **112***a*_**1** and the semiconductor layer **108** are in contact with each other or smaller than the height H**112***a*, the electric field of the gate electrode that is applied to the channel formation region in the vicinity of the conductive layer **112***a* can be increased and the on-state current of the transistor **100** can be increased.

[0277] When the height H**104** to the lowest position of the bottom surface of the conductive layer **104** is equal to the height H**112***a* to the highest position of the region where the conductive layer **112***a*_**1** and the semiconductor layer **108** are in contact with each other or smaller than the height H**112***a*, the electric field of the gate electrode applied to the channel formation region can be more uniform. Here, in the case where the electric field of the gate electrode applied to the channel formation region is not uniform, the electrical characteristics in the case where the conductive layer **112***a* is the source electrode and the conductive layer **112***b* is the drain electrode and the electrical characteristics in the case where the conductive layer **112***a* is the drain electrode and the conductive layer **112***b* is the source electrode might be different from each other. By making the electric field of the gate electrode applied to the channel formation region of the transistor **100** more uniform, the electrical characteristics in the both cases can be made equivalent to each other. Thus, the transistor **100** can be suitably used in a circuit structure in which a source and a drain are interchanged with each other.

[0278] Note that the thickness of the conductive layer **112***a* (specifically, the conductive layer **112***a*_**1**) is adjusted as appropriate so that the height H**104** is equal to the height H**112***a* or smaller than the height H**112***a*.

[0279] The above is the description of the components.

[0280] A structure example of a semiconductor device whose structure is partly different from that of Structure example 1 shown above will be described below. Note that description of the same portions as those in Structure example 1 shown above is omitted below in some cases. Furthermore, in drawings that are referred to later, the same hatching pattern is applied to portions having functions similar to those in Structure example 1 shown above, and the portions are not denoted by reference numerals in some cases.

Structure Example 2

[0281] FIG. **7**A is a top view of a semiconductor device **10**A. FIG. **7**B is a cross-sectional view of a cross section along the dashed-dotted line A**1**-A**2** in FIG. **7**A, and FIG. **7**C is a cross-sectional view of a cross section along the dashed-dotted line B**3**-B**4** in FIG. **7**A. FIG. **8**A is a perspective view of the semiconductor device **10**A.

[0282] The semiconductor device **10**A includes the transistor **100** and a transistor **200**A. A main difference in the transistor **200**A from the transistor **200** included in the semiconductor device **10** described in Structure example 1 above is including a conductive layer **202**.

[0283] The conductive layer **202** is provided between the substrate **102** and the insulating layer **110**. In the transistor **200**A, the conductive layer **204** has a function of a first gate electrode (also referred to as a top gate electrode), and the conductive layer **202** has a function of a second gate electrode (also referred to as a bottom gate electrode or a back gate electrode). Part of the insulating layer **106** functions as a first gate insulating layer, and part of each of the insulating layer **110** and the insulating layer **120** functions as a second gate insulating layer.

[0284] A portion of the semiconductor layer **208** that overlaps with at least one of the conductive layer **204** and the conductive layer **202** functions as a channel formation region. Note that for easy explanation, a portion of the semiconductor layer **208** that overlaps with the conductive layer **204** is sometimes referred to as a channel formation region; however, a channel can also be actually formed in a portion not overlapping with the conductive layer **204** and overlapping with the conductive layer **202** (a portion including the regions **208**D).

[0285] FIG. **8**B is a perspective view selectively illustrating the conductive layer **112***a* included in the transistor **100** and the conductive layer **202** included in the transistor **200**A.

FIG. **8**C is a perspective view selectively illustrating the conductive layer **112***a* and the conductive layer **112***b* included in the transistor **100** and the conductive layer **202** included in the transistor **200**A. For the conductive layer **202**, a material that can be used for the conductive layer **112***a* can be used. In other words, the conductive layer **202** can be formed through the same step as the conductive layer **112***a*. The conductive layer **202** can have a stacked-layer structure of a conductive layer **202_1** and a conductive layer **202_2** over the conductive layer **202_1**. The conductive layer **202_1** can be formed in the same step as the conductive layer **112***a*_**1**, and the conductive layer **202_2** can be formed in the same step as the conductive layer **112***a*_**2**. Since the conductive layer **202** does not include a region in contact with the semiconductor layer **208**, an opening corresponding to the opening **145** in the conductive layer **112***a*_**2** is not necessarily provided in the conductive layer **2022**.

[0286] FIG. **9**A is a perspective view selectively illustrating the conductive layer **112***a* and the semiconductor layer **108** included in the transistor **100** and the conductive layer **202** and the semiconductor layer **208** included in the transistor **200**A. The semiconductor layer **208** is provided over the conductive layer **202**. The semiconductor layer **208** has a region overlapping with the conductive layer **202**.

[0287] As illustrated in FIG. **7**A and FIG. **7**C, the conductive layer **204** may be electrically connected to the conductive layer **202** through an opening **149** provided in the insulating layer **106**, the insulating layer **110**, and the insulating layer **120**. In that case, the conductive layer **204** and the conductive layer **202** can be supplied with the same potential. When the same potential is applied to the conductive layer **204** and the conductive layer **202**, the amount of current that can flow in the transistor **200**A in an on state can be increased. FIG. **9**B is a perspective view selectively illustrating the conductive layer **112***a* and the conductive layer **104** included in the transistor **100** and the conductive layer **202** and the conductive layer **204** included in the transistor **200**A. The conductive layer **204** is provided to cover the opening **149** and includes a region in contact with the conductive layer **202**.

[0288] Although FIG. **7**A illustrates the structure where the top surface shape of the opening **149** is the same or substantially the same as the top surface shapes of the opening **141** and the opening **143**, one embodiment of the present invention is not limited thereto. Note that the top surface shape of the opening **149** may be different from those of the opening **141** and the opening **143**. The top surface shape of the opening **149** can be circular or elliptic, for example. Examples of the top surface shape of the opening **149** include polygons such as a triangle, a tetragon (including a rectangle, a rhombus, and a square), and a pentagon; and polygons with rounded corners.

[0289] As illustrated in FIG. **7**A and FIG. **7**C, the conductive layer **204** and the conductive layer **202** preferably extend beyond the end portion of the semiconductor layer **208** in the channel width direction of the transistor **200**A. In that case, as shown in FIG. **7**C, the whole of the semiconductor layer **208** in the channel width direction is covered with the conductive layer **204** with the insulating layer **106** therebetween and also covered with the conductive layer **202** with the insulating layer **110** and the insulating layer **120** therebetween. In such a structure, the semiconductor layer **208** can be electrically surrounded by electric fields generated by the pair of gate electrodes. In that case, it is particularly preferable that the same potential be supplied to the conductive layer **204** and the conductive layer **202**. In that case, electric fields for inducing a channel can be effectively applied to the semiconductor layer **208**, whereby the on-state current of the transistor **200**A can be increased. Thus, the transistor **200**A can also be miniaturized.

[0290] Note that a structure where the conductive layer **204** and the conductive layer **202** are not connected to each other may be employed. In that case, a constant potential may be applied to one of the pair of gate electrodes, and a signal for driving the transistor **200**A may be applied to the other of the pair of gate electrodes. In this case, the potential applied to one of the gate electrodes can control the threshold voltage at the time of driving the transistor **200**A with the other gate electrode.

[0291] The conductive layer **202** may be electrically connected to the conductive layer **212***a* or the conductive layer **212***b*. In that case, the conductive layer **212***a* or the conductive layer **212***b* and the conductive layer **202** may be electrically connected to each other through an opening provided in the insulating layer **195**, the insulating layer **106**, the insulating layer **120**, and the insulating layer **110**.

[0292] The insulating layer **110** is provided over the conductive layer **202**. FIG. **7**B and FIG. **7**C illustrate a structure where the insulating layer **110***a* is provided in contact with the top surface and the side surface of the conductive layer **202**. It is preferable that the insulating layer **110***a* in contact with the conductive layer **202** be less likely to diffuse a metal element contained in the conductive layer **202**. The insulating layer **110***a* preferably functions as a blocking film that inhibits release of a gas from the insulating layer **110***b* and also functions as a blocking film that inhibits diffusion of a metal element from the conductive layer **202**. For the insulating layer **110***a*, the above-described material can be suitably used.

[0293] Note that the conductive layer **202** illustrated in FIG. **7**B and the like can also be employed in another structure example.

[0294] The description of Structure example 1 can be referred to for the transistor **100**; thus, the detailed description thereof is omitted.

Structure Example 3

[0295] FIG. **10**A is a top view of a semiconductor device **10**B. FIG. **10**B is a cross-sectional view of a cross section along the dashed-dotted line A**1**-A**2** in FIG. **10**A, and FIG. **7**C can be referred to for a cross-sectional view of cross sections along the dashed-dotted line B**1**-B**2** and the dashed-dotted line B**3**-B**4** in FIG. **10**A.

[0296] The semiconductor device **10**B includes the transistor **100** and a transistor **200**B. The transistor **200**B is different from the transistor **200**A included in the semiconductor device TOA described in Structure example 2 above, mainly in that the end portion of the conductive layer **202** is positioned outward from the end portion of the semiconductor layer **208**.

[0297] The structure in which the end portion of the conductive layer **202** is positioned outward from the end portion of the semiconductor layer **208** can improve the coverage with a layer (e.g., the semiconductor layer **208** and the insulating layer **106**) formed over the conductive layer **202**, thereby inhibiting generation of defects such as disconnection or voids in the layer. The conductive layer **202**

can function as a light-blocking layer that blocks light entering the semiconductor device **10**B from the outside thereof. Accordingly, a semiconductor device with high reliability against light can be provided. When the area of a region where the conductive layer **202** functioning as the back gate electrode and the semiconductor layer **208** overlap with each other is increased, the intensity of the electric field of the back gate electrode can be further increased.

[0298] Note that the conductive layer **202** illustrated in FIG. **10**B and the like can also be employed in another structure example.

[0299] The description of Structure example 1 can be referred to for the transistor **100**; thus, the detailed description thereof is omitted.

Structure Example 4

[0300] FIG. **7**A can be referred to for a top view of a semiconductor device **10**C. FIG. **11**A is a cross-sectional view of a cross section along the dashed-dotted line A**1**-A**2** in FIG. **7**A, and FIG. **11**B is a cross-sectional view of cross sections along the dashed-dotted line B**1**-B**2** and the dashed-dotted line B**3**-B**4** in FIG. **7**A.

[0301] The semiconductor device **10**C includes a transistor **100**A and a transistor **200**C. The transistor **100**A and the transistor **200**C are different respectively from the transistor **100** and the transistor **200**A included in the semiconductor device **10**A described in Structure example 2 above, in including an insulating layer **106**A in the transistor **100**A instead of the insulating layer **106** and including an insulating layer **106**B in the transistor **200**C instead of the insulating layer **106**.

[0302] The insulating layer **106**A is processed to have substantially the same top surface shape as the conductive layer **104**. That is, the insulating layer **106**B is processed to have substantially the same top surface shape as the conductive layer **204**. The insulating layer **106**A and the insulating layer **106**B can be formed, for example, by forming an insulating film to be the insulating layer **106**A and the insulating layer **106**B and processing the insulating film with use of a resist mask for processing the conductive layer **104** and the conductive layer **204**.

[0303] The insulating layer **195** includes a region in contact with the top surface and the side surface of the conductive layer **104**, the side surface of the insulating layer **106**A, the top surface and the side surface of the semiconductor layer **108**, the top surface and the side surface of the conductive layer **112***b*, the top surface and the side surface of the conductive layer **204**, the side surface of the insulating layer **106**B, the top surface and the side surface of the semiconductor layer **208**, and the top surface of the insulating layer **120**. The insulating layer **195** has the opening **147***a* and the opening **147***b* in regions overlapping with the regions **208**D.

[0304] Note that the insulating layer **106**A and the insulating layer **106**B illustrated in FIG. **11**A and the like can also be employed in another structure example.

Structure Example 5

[0305] FIG. **7**A can be referred to for atop view of a semiconductor device **10**D. FIG. **12**A is a cross-sectional view of a cross section along the dashed-dotted line A**1**-A**2** in FIG. **7**A, and FIG. **12**B is a cross-sectional view of cross sections along the dashed-dotted line B**1**-B**2** and the dashed-dotted line B**3**-B**4** in FIG. **7**A.

[0306] The semiconductor device **10**D includes a transistor **100**B and a transistor **200**D. The transistor **100**B and the transistor **200**D are different from the transistor **100**A and the transistor **200**C in the semiconductor device **10**C described in Structure example 4 above, mainly in the structure of the insulating layer **106**A and the structure of the insulating layer **106**B.

[0307] The end portion of the conductive layer **204** is positioned inward from the end portion of the insulating layer **106**B. In other words, the insulating layer **106**B includes a portion extending beyond the end portion of the conductive layer **204** over at least the semiconductor layer **208**.

[0308] The semiconductor layer **208** includes a pair of regions **208**L between which a channel formation region is sandwiched and a pair of regions **208**D outside the pair of regions **208**L. The regions **208**L are each a region of the semiconductor layer **208** that overlaps with the insulating layer **106**B and does not overlap with the conductive layer **204**.

[0309] The region **208**L functions as a buffer region that relieves a drain electric field. The region **208**L is a region not overlapping with the conductive layer **204** and thus is a region where a channel is hardly formed by application of gate voltage to the conductive layer **204**. The region **208**L preferably has a higher carrier concentration than the channel formation region. Thus, the region **208**L can function as an LDD (Lightly Doped Drain) region.

[0310] The region **208**L can be referred to as a region whose resistance is substantially equal to or lower than that of the channel formation region, a region whose carrier concentration is substantially equal to or higher than that of the channel formation region, a region whose oxygen vacancy density is substantially equal to or higher than that of the channel formation region, or a region whose impurity concentration is substantially equal to or higher than that of the channel formation region.

[0311] The region **208**L can be referred to as a region whose resistance is substantially equal to or higher than the resistance of the region **208**D, a region whose carrier concentration is substantially equal to or lower than the carrier concentration of the region **208**D, a region whose oxygen vacancy density is substantially equal to or lower than the oxygen vacancy density of the region **208**D, or a region whose impurity concentration is substantially equal to or lower than the impurity concentration of the region **208**D.

[0312] In this manner, the region **208**L functioning as the LDD region is provided between the channel formation region and the region **208**D functioning as a source region or a drain region, whereby the transistor **200**D can have high reliability and achieve both a high drain breakdown voltage and a high on-state current.

[0313] The region **208**D functions as a source region or a drain region and has lower resistance than any of the other regions of the semiconductor layer **208**. Alternatively, the region **208**D can be referred to as a region having the highest carrier concentration, a region having the highest oxygen vacancy density, or a region having the highest impurity concentration in the regions of the semiconductor layer **208**.

[0314] The electric resistance of the region **208**D is preferably as low as possible. For example, the sheet resistance of the region **208**D is preferably higher than or equal to 1

Ω/square and less than 1×10^3 Ω/square, further preferably higher than or equal to 1 Ω/square and lower than or equal to 8×10^2 Ω/square.

[0315] The electric resistance of the channel formation region in a state where the channel is not formed is preferably as high as possible. For example, the sheet resistance of the channel formation region is preferably higher than or equal to 1×10^9 Ω/square, further preferably higher than or equal to 5×10^9 Ω/square, still further preferably higher than or equal to 1×10^{10} square.

[0316] Since the electric resistance of the channel formation region in a state where the channel is not formed is preferably as high as possible, it is not necessary to set its upper limit. If the upper limit is set, the sheet resistance of the channel formation region is preferably higher than or equal to 1×10^9 Ω/square and lower than or equal to 1×10^{12} Ω/square, further preferably higher than or equal to 5×10^9 Ω/square and lower than or equal to 1×10^{12} Ω/square, still further preferably higher than or equal to 1×10^{10} Ω/square and lower than or equal to 1×10^{12} Ω/square, for example.

[0317] The sheet resistance of the region **208**L can be, for example, higher than or equal to 1×10^3 Ω/square and lower than or equal to 1×10^9 Ω/square, preferably higher than or equal to 1×10^3 Ω/square and lower than or equal to 1×10^8 Ω/square, further preferably higher than or equal to 1×10^3 Ω/square and lower than or equal to 1×10^7 Ω/square. When the resistance is within the above range, a transistor that has favorable electrical characteristics and high reliability can be provided. Note that the sheet resistance can be calculated from a resistance value. Providing such regions **208**L between the channel formation region and the regions **208**D can increase the source-drain breakdown voltage of the transistor **200**D.

[0318] The electric resistance of the channel formation region in a state where the channel is not formed can be more than or equal to 1×10^6 times and less than or equal to 1×10^{12} times that of the region **208**D, preferably more than or equal to 1×10^6 times and less than or equal to 1×10^{11} times that of the region **208**D, further preferably more than or equal to 1×10^6 times and less than or equal to 1×10^{10} times that of the region **208**D.

[0319] The electric resistance of the channel formation region in a state where the channel is not formed can be more than or equal to 1×10^0 times and less than or equal to 1×10^9 times that of the region **208**L, preferably more than or equal to 1×10^1 times and less than or equal to 1×10^8 times that of the region **208**L, further preferably more than or equal to 1×10^2 times and less than or equal to 1×10^7 times that of the region **208**L.

[0320] The electric resistance of the region **208**L can be more than or equal to 1×10^0 times and less than or equal to 1×10^9 times that of the region **208**D, preferably more than or equal to 1×10^1 times and less than or equal to 1×10^8 times that of the region **208**D, further preferably more than or equal to 1×10^1 times and less than or equal to 1×10^7 times that of the region **208**D.

[0321] The carrier concentration in the semiconductor layer **208** preferably has a distribution such that the concentration is the lowest in the channel formation region and increases in the order of the region **208**L and the region **280**D. Providing the region **208**L between the channel formation region and the region **208**D can keep the carrier concentration of the channel formation region extremely low even when impurities such as hydrogen diffuse from the region **208**D during the manufacturing process, for example.

[0322] The carrier concentration in the channel formation region is preferably as low as possible and is preferably lower than or equal to 1×10^{18} cm^{-3}, further preferably lower than or equal to 1×10^{17} cm^{-3}, still further preferably lower than or equal to 1×10^{16} cm^{-3}, yet further preferably lower than or equal to 1×10^{13} cm^{-3}, yet still further preferably lower than or equal to 1×10^{12} cm^{-3}. Note that the lower limit of the carrier concentration of the channel formation region is not particularly limited and can be, for example, 1×10^{-9} cm^{-3}.

[0323] Meanwhile, the carrier concentration in the region **208**D can be higher than or equal to 5×10^{18} cm^{-3}, preferably higher than or equal to 1×10^{19} cm^{-3}, further preferably higher than or equal to 5×10^{19} cm^{-3}, for example. The upper limit of the carrier concentration of the region **208**D is not particularly limited and can be, for example, 5×10^{21} cm^{-3} or 1×10^{22} cm^{-3}.

[0324] The carrier concentration of the region **208**L can be a value between that of the channel formation region and that of the region **208**D. For example, the carrier concentration of the region **208**L may be higher than or equal to 1×10^{14} cm^{-3} and lower than 1×10^{20} cm^{-3}.

[0325] Note that the carrier concentration is not necessarily uniform in the region **208**L; the region **208**L sometimes has a carrier concentration gradient that decreases from the region **208**D side to the channel formation region side. For example, one or both of the hydrogen concentration and the oxygen vacancy concentration of the region **208**L may have a gradient that decreases from the region **208**D side to the channel formation region side.

[0326] Part of the end portion of the insulating layer **106**B is positioned over the semiconductor layer **208**. The insulating layer **106**B includes a region overlapping with the conductive layer **204** and functioning as the gate insulating layer and a region not overlapping with the conductive layer **104** (i.e., a region overlapping with the region **208**L).

[0327] The end portions of the conductive layer **104** is positioned inward from the end portion of the insulating layer **106**A. In other words, the insulating layer **106**A includes a portion extending beyond the end portion of the conductive layer **104** over at least the semiconductor layer **108**.

[0328] The semiconductor layer **108** includes a region **108**L on the inner side of the region **108**D. The region **108**L is a region of the semiconductor layer **108** that overlaps with the insulating layer **106**A and does not overlap with the conductive layer **104**. The region **108**L is formed in the step of forming the region **208**L. Note that in the transistor **100**B, a region of the semiconductor layer **108** in contact with the conductive layer **112***b* serves as the source region or the drain region. The region **108**L and the region **108**D are each formed in part of the source region or the drain region.

[0329] Note that the insulating layer **106**A and the insulating layer **106**B illustrated in FIG. **12**A and the like can also be employed in another structure example.

Structure Example 6

[0330] FIG. **13**A is a top view of a semiconductor device TOE. FIG. **13**B is a cross-sectional view along the dashed-dotted line A**1**-A**2** in FIG. **13**A. FIG. **12**B can be referred to for a cross-sectional view along the dashed-dotted line B**1**-B**2** and the dashed-dotted line B**3**-B**4** in FIG. **13**A.

[0331] The semiconductor device TOE includes the transistor **100**B and a transistor **200**E. The transistor **200**E is different from the transistor **200**D included in the semiconductor device **10**D described in Structure example 5 above, mainly in that the insulating layer **195** is not provided between the semiconductor layer **208** and each of the conductive layer **212***a* and the conductive layer **212***b*.

[0332] Each of the conductive layer **212***a* and the conductive layer **212***b* includes a region in contact with a top surface and a side surface of the semiconductor layer **208**.

[0333] The conductive layer **212***a* and the conductive layer **212***b* can be formed in the same step as the conductive layer **104** and the conductive layer **204**. For example, after the insulating layer **106**A and the insulating layer **106**B are formed, a conductive film is formed and then processed, so that the conductive layer **104**, the conductive layer **204**, the conductive layer **212***a*, and the conductive layer **212***b* can be formed. When the conductive layer **104**, the conductive layer **204**, the conductive layer **212***a*, and the conductive layer **212***b* are formed in the same step, the manufacturing cost of the semiconductor device TOE can be made low. Note that the opening **147***a* and the opening **147***b* illustrated in FIG. **12**A and the like are not provided.

[0334] FIG. **13**B illustrates a structure where neither the region **208**L nor the region **208**D is provided in regions of the semiconductor layer **208** that are in contact with the conductive layer **212***a* and in contact with the conductive layer **212***b*. For example, after the conductive layer **104**, the conductive layer **204**, the conductive layer **212***a*, and the conductive layer **212***b* are formed, an impurity element can be added to the semiconductor layer **208** using these conductive layers as masks. In the semiconductor layer **208**, a region in contact with the conductive layer **212***a* and the region **208**D adjacent to the region serve as one of the source region and the drain region. In the semiconductor layer **208**, a region in contact with the conductive layer **212***b* and the region **208**D adjacent to the region serve as the other of the source region and the drain region.

[0335] Although FIG. **13**B illustrates the structure where neither the region **208**L nor the region **208**D is provided in regions of the semiconductor layer **208** that are in contact with the conductive layer **212***a* and in contact with the conductive layer **212***b*, one embodiment of the present invention is not limited thereto. For example, the region **208**D may be provided in regions of the semiconductor layer **208** that are in contact with the conductive layer **212***a* and in contact with the conductive layer **212***b*.

[0336] Note that the conductive layer **212***a* and the conductive layer **212***b* illustrated in FIG. **13**B and the like can also be employed in another structure example.

[0337] The description of Structure example 5 can be referred to for the transistor **100**B; thus, the detailed description thereof is omitted.

Structure Example 7

[0338] FIG. **13**A can be referred to for a top view of a semiconductor device **10**F. FIG. **14** is a cross-sectional view along the dashed-dotted line A**1**-A**2** in FIG. **13**A. FIG. **7**B can be referred to for a cross-sectional view along the dashed-dotted line B**1**-B**2** and the dashed-dotted line B**3**-B**4** in FIG. **13**A.

[0339] The semiconductor device **10**F includes the transistor **100**A and a transistor **200**F. The transistor **200**F is different from the transistor **200**E included in the semiconductor device **10**E described in Structure example 5 above mainly in including an insulating layer **106**C and an insulating layer **106**D.

[0340] The insulating layer **106**C and the insulating layer **106**D are formed in the same step as the insulating layer **106**A and the insulating layer **106**B. The insulating layer **106**C is provided in a region overlapping with the conductive layer **212***a* and includes a region in contact with part of the bottom surface of the conductive layer **212***a*. The insulating layer **106**D is provided in a region overlapping with the conductive layer **212***b* and includes a region in contact with part of the bottom surface of the conductive layer **212***b*. The insulating layer **106**C and the insulating layer **106**D may cover the respective end portions of the semiconductor layer **108**. The insulating layer **106**C is provided between the insulating layer **120** and the conductive layer **212***a* and between the semiconductor layer **208** and the conductive layer **212***a*. The insulating layer **106**D is provided between the insulating layer **120** and the conductive layer **212***b* and between the semiconductor layer **208** and the conductive layer **212***b*.

[0341] FIG. **14** illustrates a structure where the end portion of the conductive layer **204** is aligned or substantially aligned with the end portion of the insulating layer **106**B. The insulating layer **106**B can be formed using a resist mask used for forming the conductive layer **204**, for example. With such a structure, processes can be simplified.

[0342] The region **208**D is formed in a region overlapping with none of the conductive layer **204**, the conductive layer **212***a*, and the conductive layer **212***b*. Note that the region **208**L may be formed in a region overlapping with the insulating layer **106**B and not overlapping with the conductive layer **204** by processing the conductive layer **204** to have the end portion positioned inward from the end portion of the insulating layer **106**B (see FIG. **13**B).

[0343] Note that the insulating layer **106**C and the insulating layer **106**D illustrated in FIG. **14** can also be employed in another structure example.

[0344] The description of Structure example 4 can be referred to for the transistor **100**A; thus, the detailed description thereof is omitted.

Structure Example 8

[0345] FIG. **15**A is a top view of a semiconductor device **10**G. FIG. **15**B is a cross-sectional view along the dashed-dotted line A**1**-A**2** in FIG. **15**A. FIG. **7**B can be referred to for a cross-sectional view along the dashed-dotted line B**1**-B**2** and the dashed-dotted line B**3**-B**4** in FIG. **15**A.

[0346] The semiconductor device **10**G includes the transistor **100** and a transistor **200**G. The transistor **200**G is different from the transistor **200**F included in the semiconductor device **10**F described in Structure example 7 above mainly in that an opening **137***a* and an opening **137***b* are provided in the insulating layer **106**.

[0347] The opening **137***a* and the opening **137***b* are each provided in a region of the insulating layer **106** that overlaps with the semiconductor layer **208**. In the opening **137***a*, the conductive layer **212***a* includes a region in contact with the semiconductor layer **208**, and in the opening **137***b*, the conductive layer **212***b* includes a region in contact with the semiconductor layer **208**. The opening **137***a* is preferably provided to have a region protruding toward the channel formation region from the end portion of the conductive layer **212***a* on the channel formation region side. Similarly,

the opening **137***b* is preferably provided to have a region toward the channel formation region from the end portion of the conductive layer **212***b* on the channel formation region side. Accordingly, in the opening **137***a*, part of the end portion of the conductive layer **212***a* is in contact with the top surface of the semiconductor layer **208**. In the opening **137***b*, part of the end portion of the conductive layer **212***b* is in contact with the top surface of the semiconductor layer **208**. The region **208**D is formed in a region overlapping with none of the conductive layer **204**, the conductive layer **212***a*, and the conductive layer **212***b*. The region **208**L is formed in a region overlapping with the insulating layer **106** and not overlapping with the conductive layer **204**. Thus, the region of the semiconductor layer **208** that is in contact with the conductive layer **212***a* can be adjacent to the region **208**D. Similarly, a region of the semiconductor layer **208** that is in contact with the conductive layer **212***b* can be adjacent to the region **208**D.

[0348] The insulating layer **106** includes a region in contact with part of the bottom surface of the conductive layer **212***a* and a region in contact with part of the bottom surface of the conductive layer **212***b*. The insulating layer **106** may cover the end portion of the semiconductor layer **208**. The insulating layer **106** is provided between the insulating layer **120** and the conductive layer **212***a*, between the insulating layer **120** and the conductive layer **212***b*, between the semiconductor layer **208** and the conductive layer **212***a*, and between the semiconductor layer **208** and the conductive layer **212***b*.

[0349] The above description of Structure example 1 can be referred to for the transistor **100**; thus, the detailed description thereof is omitted.

Structure Example 9

[0350] FIG. **7**A can be referred to for atop view of a semiconductor device **10**H. FIG. **16**A is a cross-sectional view of a cross section along the dashed-dotted line A**1**-A**2** in FIG. **7**A, and FIG. **16**B is a cross-sectional view of cross sections along the dashed-dotted line B**1**-B**2** and the dashed-dotted line B**3**-B**4** in FIG. **7**A.

[0351] The semiconductor device **10**H includes a transistor **100**C and a transistor **200**H. The transistor **100**C is different from the transistor **100** included in the semiconductor device **10**A described in Structure example 2 above mainly in that the insulating layer **120** has a stacked-layer structure. The transistor **200**H is different from the transistor **200**A included in the semiconductor device **10**A described in Structure example 2 above mainly in that the insulating layer **120** has a stacked-layer structure and the conductive layer **202** is provided between the insulating layer **110** and the insulating layer **120**.

[0352] The conductive layer **202** is provided over the insulating layer **110**. The conductive layer **202** is formed in a step different from that of the conductive layer **112***a*. When the conductive layer **202** is provided over the insulating layer **110**, the distance between the conductive layer **202** functioning as the second gate electrode and the semiconductor layer **208** is shortened, so that the intensity of agate electric field applied to the semiconductor layer **208** can be increased.

[0353] FIG. **16**A and FIG. **16**B each illustrate a structure where the conductive layer **202** is provided in contact with the top surface of the insulating layer **110***c*. It is preferable that the insulating layer **110***c* that is in contact with the conductive layer **202** be less likely to diffuse a metal element included in the conductive layer **202**. The insulating layer **110***c* preferably functions as a blocking film that inhibits release of gas from the insulating layer **110***b* and also functions as a blocking film that inhibits diffusion of a metal element from the conductive layer **202**. For the insulating layer **110***c*, the above-described material can be suitably used.

[0354] The insulating layer **120** is provided in contact with the top surface and the side surface of the conductive layer **202**. The insulating layer **120** preferably has a stacked-layer structure. In each structure in FIG. **16**A and FIG. **16**B, the insulating layer **120** has a stacked structure of an insulating layer **120***a* and an insulating layer **120***b* over the insulating layer **120***a*. It is preferable that the insulating layer **120***a* in contact with the conductive layer **202** be less likely to diffuse a metal element included in the conductive layer **202**. The insulating layer **120***a* preferably functions as a blocking film that inhibits diffusion of a metal element from the conductive layer **202**. For the insulating layer **120***a*, a material that can be used for the insulating layer **110***a* and the insulating layer **110***c* can be used. The insulating layer **120***a* includes a region in contact with the insulating layer **110***c*. For the insulating layer **120***a*, the insulating layer **110***a*, and the insulating layer **110***c*, the same material or different materials may be used. For the insulating layer **120***b* in contact with the semiconductor layer **208**, an oxide or an oxynitride is preferably used. A film from which oxygen is released by heating is preferably used as the insulating layer **120***b*. For the insulating layer **120***b*, a material that can be used for the insulating layer **110***b* can be used. Note that the insulating layer **120***b* and the insulating layer **110***b* may be formed using the same material or different materials.

[0355] Although the structure in each of FIG. **16**A and FIG. **16**B illustrates the insulating layer **120** that has a stacked-layer structure of two layers, the insulating layer **120***a* and the insulating layer **120***b*, one embodiment of the present invention is not limited thereto. The insulating layer **120** may have a single-layer structure or a stacked-layer structure of three or more layers.

[0356] Note that the conductive layer **202** and the insulating layer **120** illustrated in FIG. **16**B and the like can also be employed in another structure example.

Structure Example 10

[0357] Instead of the transistor **100**, the transistor **100**A, the transistor **100**B, and the transistor **100**C described above, a transistor group including a plurality of transistors can be used. FIG. **17**A is a top view of a semiconductor device **10**J including a transistor group. FIG. **17**B is a cross-sectional view of a cross section along the dashed-dotted line A**3**-A**4** in FIG. **17**A. FIG. **18**A is a perspective view of the semiconductor device **10**J.

[0358] The semiconductor device **10**J includes a transistor group **100**D and the transistor **200**A. The semiconductor device **10**J is different from the semiconductor device TOA described in Structure example 2 above mainly in including the transistor group **100**D instead of the transistor **100**.

[0359] FIG. **18**B is an equivalent circuit diagram of the transistor group **100**D. The transistor group **100**D includes a transistor **100_1** to a transistor **100_4**. The transistor group **100**D can be regarded as one transistor, in which the transistor **100_1** to the transistor **100_4** are connected in parallel. Gate electrodes of the transistor **100_1** to the

transistor **100_4** are electrically connected to each other. Source electrodes of the transistor **100_1** to the transistor **100_4** are electrically connected to each other. Drain electrodes of the transistor **100_1** to the transistor **100_4** are electrically connected to each other.

[0360] Although four transistors are connected in parallel here, one embodiment of the present invention is not limited thereto. Note that the number of transistors which are connected in parallel is not particularly limited. As illustrated in FIG. **18**C, the transistor group **100**D can have a structure including a transistor **100_1** to a transistor **100_*p*** (p is an integer greater than or equal to 2). The transistor group **100**D can be regarded as one transistor, in which the transistor **100_1** to the transistor **100_*p*** are connected in parallel.

[0361] Gate electrodes of the transistor **100_1** to the transistor **100_*p*** are electrically connected to each other. Source electrodes of the transistor **100_1** to the transistor **100_*p*** are electrically connected to each other. Drain electrodes of the transistor **100_1** to the transistor **100_*p*** are electrically connected to each other.

[0362] Although the transistors in FIG. **18**B and FIG. **18**C are shown as n-channel transistors, one embodiment of the present invention is not limited thereto. Each of the transistors may be a p-channel transistor.

[0363] Any of the above-described structures of the transistor **100** to the transistor **100**C can be used for the transistors included in the transistor group **100**D. FIG. **17**B illustrates an example in which the structure of the transistor **100** illustrated in FIG. **1**B and the like is employed for the transistor **100_1** to the transistor **100_4**. The transistor group **100**D includes the conductive layer **104**, the insulating layer **106**, the semiconductor layer **108**, the conductive layer **112***a*, and the conductive layer **112***b*. The conductive layer **104** functions as a gate electrode of each of the transistor **100_1** to the transistor **100_4**. Part of the insulating layer **106** functions as a gate insulating layer of each of the transistor **100_1** to the transistor **100_4**. The conductive layer **112***a* functions as one of a source electrode and a drain electrode, and the conductive layer **112***b* functions as the other thereof in each of the transistor **100_1** to the transistor **100_4**. The above description can be referred to for the transistor **200**A; thus, the detailed description thereof is omitted.

[0364] FIG. **19**A is a perspective view selectively illustrating the conductive layer **112***a* included in the transistor group **100**D and the conductive layer **202** included in the transistor **200**A. The conductive layer **112***a* has an opening **145_1** to an opening **145_4** in regions in contact with the semiconductor layer **108**. The conductive layer **112***a*_**1** is exposed in the opening **145_1** to the opening **145_4**.

[0365] FIG. **19**B is a perspective view selectively illustrating the conductive layer **112***a*, the conductive layer **112***b*, an opening **141_1** to an opening **141_4**, an opening **143_1** to an opening **143_4**, and the conductive layer **202** included in the transistor **200**A that are included in the transistor group **100**D. Note that the opening **141_1** to an opening **141_4** provided in the insulating layer **110** and the insulating layer **120** are indicated by dashed lines. The opening **141_1** to the opening **141_4** are preferably provided in regions overlapping with the opening **145_1** to the opening **145_4**. The conductive layer **112***a*_**1** is preferably exposed in the opening **141_1** to the opening **1414**. As illustrated in FIG. **19**B, the conductive layer **112***b* has the opening **143_1** to the opening **143_4** in regions overlapping with the conductive layer **112***a*.

[0366] The top surface shapes of the opening **141_1** to the opening **141_4** and the opening **143_1** to the opening **143_4** are preferably circular. Furthermore, the widths of the opening **141_1** to the opening **141_4** are preferably equal to or substantially equal to each other. Similarly, the widths of the opening **143_1** to the opening **143_4** are preferably equal to or substantially equal to each other. When the widths of the opening **141_1** to the opening **141_4** are equal to or substantially equal to each other and the widths of the opening **143_1** to the opening **143_4** are equal to or substantially equal to each other, the processing accuracy at the time of forming the opening **141_1** to the opening **141_4** and the opening **143_1** to the opening **143_4** can be increased.

[0367] In the case where the transistor group **100**D is regarded as one transistor, the channel width of the transistor is the sum of the channel widths of the transistor **100_1** to the transistor **100_4**. For example, in the case where the top surface shapes of the opening **143_1** to the opening **143_4** are circular and the width D**143** corresponds to the width of each of the opening **143_1** to the opening **143_4**, the transistor group **100**D can be regarded as a transistor having a channel width of "D**143**×π×4" (see FIG. **4**A and FIG. **4**B). The transistor group **100**D composed of p transistors can be regarded as a transistor having a channel width of "D**143**×π×p". Note that the transistor group **100**D can be regarded as a transistor having the channel length L**100** (see FIG. **4**B). A plurality of transistors connected in parallel can have a larger channel width and a higher on-state current. By adjusting the number (p) of transistors connected in parallel, the channel width can be changed. The number (p) of transistors connected in parallel is determined so that a desired on-state current is obtained.

[0368] FIG. **20**A is a perspective view selectively illustrating the conductive layer **112***a* and the semiconductor layer **108** included in the transistor group **100**D and the conductive layer **202** and the semiconductor layer **208** included in the transistor **200**A. As illustrated in FIG. **20**A, the semiconductor layer **108** is provided to cover the opening **141_1** to the opening **141_4** and the opening **143_1** to the opening **143_4**. The semiconductor layer **108** includes regions in contact with the top surface of the conductive layer **112***a* in the opening **141_1** to the opening **1414**. Specifically, the semiconductor layer **108** preferably includes regions in contact with the top surface of the conductive layer **112***a*_**1** in the opening **141_1** to the opening **141_4**. Although FIG. **20**A illustrates the structure in which the transistor **100_1** to the transistor **100_4** share the semiconductor layer **108**, one embodiment of the present invention is not limited thereto. The semiconductor layer **108** may be separated for each of the transistor **100_1** to the transistor **100_4**.

[0369] Although FIG. **19**A and the like illustrate the structure where the conductive layer **112***a* has four openings **145** (the opening **145_1** to the opening **145_4**), one embodiment of the present invention is not limited thereto. The conductive layer **112***a* may include one or more openings covering the opening **141_1** to the opening **141_4** completely. For example, the conductive layer **112***a* can include one opening covering the opening **141_1** to the opening **141_4** completely. In the opening, the semiconductor layers

108 of the transistor **100_1** to the transistor **1004** may be in contact with the conductive layer **112***a*_**1**.

[0370] FIG. **20**B is a perspective view selectively illustrating the conductive layer **112***a* and the conductive layer **104** included in the transistor group **100**D and the conductive layer **202** and the conductive layer **204** included in the transistor **200**A. As illustrated in FIG. **20**B, the conductive layer **104** is provided to cover the opening **141_1** to the opening **141_4** and the opening **143_1** to the opening **143_4**.

[0371] Although FIG. **17**B and the like illustrate the structure where the above transistors **100** are connected in parallel, one embodiment of the present invention is not limited thereto. A transistor group in which transistors having any of the structures of the transistor **100**, the transistor **100**A, the transistor **100**B, and the transistor **100**C are connected in parallel can be used.

[0372] Although the top view in FIG. **17**A and the perspective view in FIG. **18**A and the like illustrate the structure where the transistor **100_1** to a transistor **100_4** are arranged in two rows and two columns, the arrangement of transistors included in the transistor group **100**D is not particularly limited. For example, the transistor **100_1** to the transistor **1004** may be arranged in one row and four columns.

[0373] Note that the transistor group **100**D illustrated in FIG. **17**A and the like can also be employed in another structure example.

Structure Example 11

[0374] FIG. **21**A is a top view of a semiconductor device **10**K. FIG. **21**B is a cross-sectional view of a cross section along the dashed-dotted line A**5**-A**6** in FIG. **21**A. FIG. **22**A is a perspective view of the semiconductor device **10**K.

[0375] The semiconductor device **10**K includes a transistor group **100**E and the transistor **200**A. The semiconductor device **10**K is different from the semiconductor device **10**J described in Structure example 10 above mainly in including the transistor group **100**E instead of the transistor group **100**D.

[0376] In the transistor group **100**E, the above-described transistor **100** is connected in series. FIG. **22**B is an equivalent circuit diagram of the transistor group **100**E. The transistor group **100**E includes the transistor **100_1** to the transistor **100_4**. The transistor group **100**E can be regarded as one transistor, in which the transistor **100_1** to the transistor **100_4** are connected in series.

[0377] Although four transistors are connected in series here, one embodiment of the present invention is not limited thereto. Note that the number of transistors which are connected in series is not particularly limited. As illustrated in FIG. **22**C, the transistor group **100**E can have a structure including the transistor **100_1** to a transistor **100**_*q* (q is an integer greater than or equal to 2). The transistor group **100**E in which the transistor **100_1** to the transistor **100**_*q* are connected in series can be regarded as one transistor.

[0378] Although the transistors in FIG. **22**B and FIG. **22**C are shown as n-channel transistors, one embodiment of the present invention is not limited thereto. Each of the transistors may be a p-channel transistor.

[0379] The transistor **100_1** includes the conductive layer **104**, the insulating layer **106**, a semiconductor layer **1081**, the conductive layer **112***a*, and the conductive layer **112***b*. The conductive layer **112***a* functions as one of the source electrode and the drain electrode and the conductive layer **112***b* functions as the other thereof in the transistor **100_1**.

[0380] The transistor **100_2** includes the conductive layer **104**, the insulating layer **106**, a semiconductor layer **108_2**, the conductive layer **112***b*, and a conductive layer **112***c*. The conductive layer **112***b* functions as one of the source electrode and the drain electrode and the conductive layer **112***c* functions as the other thereof in the transistor **100_2**. The conductive layer **112***b* is shared by the transistor **100_1** and the transistor **100_2**.

[0381] The transistor **100_3** includes the conductive layer **104**, the insulating layer **106**, a semiconductor layer **1083**, the conductive layer **112***c*, and a conductive layer **112***d*. The conductive layer **112***c* functions as one of the source electrode and the drain electrode and the conductive layer **112***d* functions as the other thereof in the transistor **100_3**. The conductive layer **112***c* is shared by the transistor **100_2** and the transistor **100_3**.

[0382] The transistor **100_4** includes the conductive layer **104**, the insulating layer **106**, a semiconductor layer **108_4**, the conductive layer **112***d*, and a conductive layer **112***e*. The conductive layer **112***d* functions as one of the source electrode and the drain electrode and the conductive layer **112***e* functions as the other thereof in the transistor **100_4**. The conductive layer **112***d* is shared by the transistor **100_3** and the transistor **100_4**.

[0383] FIG. **23**A is a perspective view selectively illustrating the conductive layer **112***a*, the conductive layer **112***c*, and the conductive layer **112***e* included in the transistor group **100**E and the conductive layer **202** included in the transistor **200**A. The conductive layer **112***a*, the conductive layer **112***c*, the conductive layer **112***e*, and the conductive layer **202** can be formed in the same step. A structure can be employed in which the conductive layer **112***a*_**2** has the opening **145_1** and the semiconductor layer **108_1** is in contact with the conductive layer **112***a*_**1** through the opening **145_1**. A structure can be employed in which a conductive layer **112***c*_**2** has the opening **145_2** and the opening **145_3** and the semiconductor layer **108_2** and the semiconductor layer **108_3** are in contact with the conductive layer **112***c*_**1** through the opening **145_2** and the opening **145_3**. A structure can be employed in which the conductive layer **112***e*_**2** has the opening **145_4** and the semiconductor layer **1084** is in contact with the conductive layer **112***e*_**1** through the opening **145_4**.

[0384] FIG. **23**B is a perspective view selectively illustrating the conductive layer **112***a* to the conductive layer **112***e*, the opening **141_1** to the opening **1414**, and the opening **143_1** to the opening **143_4** included in the transistor group **100**E, and the conductive layer **202** included in the transistor **200**A. The opening **143_1** and the opening **143_2** are provided in the conductive layer **112***b*, and the opening **143_3** and the opening **143_4** are provided in the conductive layer **112***d*.

[0385] FIG. **24**A is a perspective view selectively illustrating the conductive layer **112***a*, the conductive layer **112***c*, the conductive layer **112***e*, and the semiconductor layer **108_1** to the semiconductor layer **108_4** included in the transistor group **100**E, and the conductive layer **202** and the semiconductor layer **208** included in the transistor **200**A. The semiconductor layer **1081** to the semiconductor layer **1084** and the semiconductor layer **208** can be formed in the same step.

[0386] FIG. **24**B is a perspective view selectively illustrating the conductive layer **112***a*, the conductive layer **112***c*, the conductive layer **112***e*, and the conductive layer **104**

included in the transistor group **100**E, and the conductive layer **202** and the conductive layer **204** included in the transistor **200**A. The conductive layer **104** functions as a gate electrode of each of the transistor **100_1** to the transistor **100_4**.

[0387] The other of the source electrode and the drain electrode of the transistor **100_1** is electrically connected to one of the source electrode and the drain electrode of the transistor **100_2**. The other of the source electrode and the drain electrode of the transistor **100_2** is electrically connected to one of the source electrode and the drain electrode of the transistor **100_3**. The other of the source electrode and the drain electrode of the transistor **100_3** is electrically connected to one of the source electrode and the drain electrode of the transistor **100_4**.

[0388] In the case where the transistor group **100**E is regarded as one transistor, the channel width of the transistor is the sum of the channel lengths of the transistor **100_1** to the transistor **100_4**. For example, in the case where the channel length L**100** corresponds to the channel length of each of the transistor **100_1** to the transistor **100_4**, the transistor group **100**E can be regarded as a transistor having a channel length of "L**100**×4" (see FIG. **4**B). The transistor group **100**E composed of q transistors can be regarded as a transistor having a channel length of "L**100**×q". Note that the transistor group **100**E can be regarded as a transistor having the channel width W**100** (see FIG. **4**A and FIG. **4**B). A plurality of transistors connected in series can have a larger channel length and favorable saturation. By adjusting the number (q) of transistors connected in series, the channel length can be changed. The number (q) of transistors connected in series is determined so that desired saturation is obtained.

[0389] Although FIG. **21**B and the like illustrate the structure where the transistors **100** described above are connected in series, one embodiment of the present invention is not limited thereto. A transistor group in which transistors having any of the structures of the transistor **100**, the transistor **100**A, the transistor **100**B, and the transistor **100**C are connected in series can be used.

[0390] Although the top view in FIG. **21**A and the perspective view in FIG. **22**A and the like illustrate a structure in which the transistor **100_1** to the transistor **100_4** are arranged in two rows and two columns, the arrangement of transistors included in the transistor group **100**E is not particularly limited. For example, the transistor **100_1** to the transistor **1004** may be arranged in one row and four columns.

[0391] Note that the transistor group **100**E illustrated in FIG. **21**A and the like can also be employed in another structure example.

Manufacturing Method Example 1

[0392] A method for manufacturing the semiconductor device of one embodiment of the present invention will be described below with reference to drawings. Here, for describing the manufacturing method, a structure in which an oxide semiconductor is used for each of the semiconductor layer **108** and the semiconductor layer **208** of the semiconductor device **10**A illustrated in FIG. **7**B and the like is used as an example.

[0393] Note that thin films that form the semiconductor device (insulating films, semiconductor films, conductive films, and the like) can be formed by a sputtering method, a chemical vapor deposition (CVD) method, a vacuum evaporation method, a pulsed laser deposition (PLD) method, an atomic layer deposition (ALD) method, or the like. Examples of the CVD method include a plasma-enhanced chemical vapor deposition (PECVD) method and a thermal CVD method. An example of the thermal CVD method is a metal organic chemical vapor deposition (MOCVD: Metal Organic CVD) method.

[0394] The thin films that form the semiconductor device (insulating films, semiconductor films, conductive films, and the like) can be formed by a method such as spin coating, dipping, spray coating, ink-jetting, dispensing, screen printing, offset printing, a doctor knife, slit coating, roll coating, curtain coating, or knife coating.

[0395] When the thin films that form the semiconductor device are processed, a photolithography method or the like can be used for the processing. Alternatively, a nanoimprinting method, a sandblasting method, a lift-off method, or the like may be used for the processing of the thin films. Island-shaped thin films may be directly formed by a film formation method using a blocking mask such as a metal mask.

[0396] There are the following two typical examples of a photolithography method. In one of the methods, a resist mask is formed over a thin film that is to be processed, the thin film is processed by etching or the like, and the resist mask is removed. In the other method, a photosensitive thin film is formed and then the thin film is processed into a desired shape by light exposure and development.

[0397] As the light used for light exposure in the photolithography method, for example, an i-line (with a wavelength of 365 nm), a g-line (with a wavelength of 436 nm), an h-line (with a wavelength of 405 nm), or combined light of any of them can be used. Besides, ultraviolet light, KrF laser light, ArF laser light, or the like can be used. In addition, light exposure may be performed by liquid immersion exposure technique. As the light used for the light exposure, extreme ultraviolet (EUV) light, X-rays, or the like may be used. Instead of the light used for light exposure, an electron beam can be used. It is preferable to use extreme ultraviolet light, X-rays, or an electron beam because extremely minute processing can be performed. Note that in the case of performing light exposure by scanning of a beam such as an electron beam, a photomask is not needed.

[0398] For etching of the thin film, a dry etching method, a wet etching method, or a sandblasting method can be used, for example.

[0399] Each of FIG. **25**A to FIG. **28**C is a drawing illustrating the method for manufacturing the semiconductor device **10**A. Each drawing is a cross-sectional view taken along the dashed-dotted line A**1**-A**2**.

[Formation of Conductive Layer **112***a* and Conductive Layer **202**]

[0400] A conductive film **112***a*_if to be the conductive layer **112***a*_**1** and the conductive layer **202_1** and a conductive film **112***a*_**2***f* to be the conductive layer **112***a*_**2** and the conductive layer **202_2** are formed over the substrate **102** (FIG. **25**A). For the formation of the conductive film **112***a*_if and the conductive film **112***a*_**2***f*, a sputtering method can be suitably used, for example.

[0401] Next, a resist mask is formed over the conductive film **112***a*_if and the conductive film **112***a*_**2***f* by a photolithography process, and then the conductive film **112***a*_if and

the conductive film **112***a*_**2***f* are processed, whereby the conductive layer **112***a*_**1**, a conductive layer **112***a*_**2**A over the conductive layer **112***a*_**1**, the conductive layer **202**_**1**, and the conductive layer **2022** over the conductive layer **2021** are formed (FIG. **25**B). For processing of the conductive film **112***a*_if and the conductive film **112***a*_**2***f*, one or both of a wet etching method and a dry etching method may be used. Thus, the conductive layer **202** functioning as a second gate electrode of the transistor **200**A is formed.

[0402] Next, part of the conductive layer **112***a*_**2**A is removed, so that the conductive layer **112***a*_**2** having the opening **145** is formed (FIG. **25**C). Accordingly, the conductive layer **112***a* functioning as one of the source electrode and the drain electrode of the transistor **100** is formed.

[Formation of Insulating Film **110***af* and Insulating Film **110***bf*]

[0403] Next, an insulating film **110***af* to be the insulating layer **110***a* and an insulating film **110***bf* to be the insulating layer **110***b* are formed over the substrate **102**, the conductive layer **112***a*, and the conductive layer **202**.

[0404] For the formation of the insulating film **110***af* and the insulating film **110***bf*, a PECVD method can be suitably used. It is preferable that the insulating film **110***bf* be formed in a vacuum successively after the formation of the insulating film **110***af*, without exposure of a surface of the insulating film **110***af* to the air. By forming the insulating film **110***af* and the insulating film **110***bf* successively, attachment of impurities derived from the air to the surface of the insulating layer **110***af* can be inhibited. Examples of the impurities include water and organic substances.

[0405] The substrate temperatures at the time of forming the insulating film **110***af* and the insulating film **110***bf* are each preferably higher than or equal to 180° C. and lower than or equal to 450° C., further preferably higher than or equal to 200° C. and lower than or equal to 450° C., still further preferably higher than or equal to 250° C. and lower than or equal to 450° C., yet still further preferably higher than or equal to 300° C. and lower than or equal to 450° C., yet still further preferably higher than or equal to 300° C. and lower than or equal to 400° C., yet still further preferably higher than or equal to 350° C. and lower than or equal to 400° C. When the substrate temperatures at the time of forming the insulating film **110***af* and the insulating film **110***bf* are in the above range, impurities (e.g., water and hydrogen) released from the insulating films themselves can be reduced, which inhibits diffusion of the impurities to the semiconductor layer **108**. Consequently, the transistor can have favorable electrical characteristics and high reliability.

[0406] Note that since the insulating film **110***af* and the insulating film **110***bf* are formed earlier than the semiconductor layer **108** and the semiconductor layer **208**, there is no need to consider the probability of oxygen release from the semiconductor layer **108** and the semiconductor layer **208** due to heat applied thereto at the time of forming the insulating film **110***af* and the insulating film **110***bf*.

[0407] After the insulating film **110***af* and the insulating film **110***bf* are formed, heat treatment may be performed. By performing the heat treatment, water and hydrogen can be released from the surface and inside of each of the insulating film **110***af* and the insulating film **110***bf*.

[0408] The heat treatment temperature is preferably higher than or equal to 150° C. and lower than the strain point of the substrate, further preferably higher than or equal to 200° C. and lower than or equal to 450° C., still further preferably higher than or equal to 250° C. and lower than or equal to 450° C., yet still further preferably higher than or equal to 300° C. and lower than or equal to 450° C., yet still further preferably higher than or equal to 300° C. and lower than or equal to 400° C., yet still further preferably higher than or equal to 350° C. and lower than or equal to 400° C. The heat treatment can be performed in an atmosphere containing one or more of a noble gas, nitrogen, and oxygen. As a nitrogen-containing atmosphere or an oxygen-containing atmosphere, clean dry air (CDA) may be used. Note that the content of hydrogen, water, or the like in the atmosphere is preferably as low as possible. As the atmosphere, a high-purity gas with a dew point of −60° C. or lower, preferably −100° C. or lower is preferably used. With use of an atmosphere where the content of hydrogen, water, or the like is as low as possible, entry of hydrogen, water, or the like into the insulating film **110***af* and the insulating film **110***bf* can be prevented as much as possible. An oven or a rapid thermal annealing (RTA) apparatus can be used for the heat treatment, for example. The use of the RTA apparatus can shorten the heat treatment time.

[0409] Next, a metal oxide layer **180** is formed over the insulating film **110***bf* (FIG. **25**D).

[0410] The metal oxide layer **180** may be an insulating layer or a conductive layer. For the metal oxide layer **180**, aluminum oxide, hafnium oxide, hafnium aluminate, indium oxide, indium tin oxide (ITO), or indium tin oxide containing silicon (ITSO) can be used, for example.

[0411] An oxide material containing one or more kinds of elements that are the same as those in the semiconductor layer **108** or the semiconductor layer **208** is preferably used for the metal oxide layer **180**. It is particularly preferable to use an oxide semiconductor material that can be used for the semiconductor layer **108** or the semiconductor layer **208**.

[0412] A metal oxide film formed using a sputtering target having the same composition as the semiconductor layer **108** or the semiconductor layer **208** can be used as the metal oxide layer **180**. The sputtering target having the same composition as the semiconductor layer **108** or the semiconductor layer **208** is preferably used, in which case the same manufacturing apparatus and the same sputtering target can be used.

[0413] When a metal oxide material containing indium and gallium is used for each of the semiconductor layer **108**, the semiconductor layer **208**, and the metal oxide layer **180**, a material whose content percentage of gallium is higher than that in the semiconductor layer **108** and the semiconductor layer **208** can be used for the metal oxide layer **180**. It is preferable to use a material whose content percentage of gallium is high for the metal oxide layer **180**, in which case an oxygen blocking property can be further increased.

[0414] The metal oxide layer **180** is preferably formed in, for example, an oxygen-containing atmosphere. It is particularly preferable that the metal oxide layer **180** be formed by a sputtering method in an oxygen-containing atmosphere. In that case, oxygen can be suitably supplied to the insulating film **110***bf* at the time of forming the metal oxide layer **180**.

[0415] For example, the metal oxide layer **180** may be formed by a reactive sputtering method using oxygen as a deposition gas and a metal target. When aluminum is used for the metal target, for example, an aluminum oxide film can be formed.

[0416] At the time of forming the metal oxide layer **180**, the amount of oxygen supplied into the insulating film **110***bf* can be increased with a higher flow rate ratio of an oxygen gas of the film formation gas introduced into a processing chamber of a film formation apparatus or with higher oxygen partial pressure in the processing chamber. The oxygen flow rate ratio or oxygen partial pressure is, for example, set to higher than or equal to 50% and lower than or equal to 100%, preferably higher than or equal to 65% and lower than or equal to 100%, further preferably higher than or equal to 80% and lower than or equal to 100%, still further preferably higher than or equal to 90% and lower than or equal to 100%. It is particularly preferable that the oxygen flow rate ratio be 100% and the oxygen partial pressure be as close to 100% as possible.

[0417] When the metal oxide layer **180** is formed by a sputtering method in an oxygen-containing atmosphere in the above manner, oxygen can be supplied to the insulating film **110***bf* and release of oxygen from the insulating film **110***bf* can be prevented during the formation of the metal oxide layer **180**. As a result, a large amount of oxygen can be enclosed in the insulating film **110***bf*. Moreover, a large amount of oxygen can be supplied to the semiconductor layer **108** by heat treatment performed later. As a result, the amount of oxygen vacancy (V_O) and V_OH in the semiconductor layer **108** can be reduced, so that a highly reliable transistor exhibiting favorable electrical characteristics can be obtained.

[0418] After the metal oxide layer **180** is formed, heat treatment may be performed. The above description can be referred to for the heat treatment; thus, the detailed description thereof is omitted. By the heat treatment performed after the formation of the metal oxide layer **180**, oxygen can be effectively supplied from the metal oxide layer **180** to the insulating film **110***bf*.

[0419] After the formation of the metal oxide layer **180** or after the above-described heat treatment, oxygen may be further supplied to the insulating film **110***bf* through the metal oxide layer **180**. As a method for supplying oxygen, an ion implantation method, an ion doping method, a plasma immersion ion implantation method, or plasma treatment can be used, for example. For the plasma treatment, an apparatus in which an oxygen gas is made to be plasma by high-frequency power can be suitably used. Examples of the apparatus in which a gas is made to be plasma by high-frequency power include a plasma etching apparatus and a plasma ashing apparatus.

[0420] Then, the metal oxide layer **180** is removed.

[0421] There is no particular limitation on a method for removing the metal oxide layer **180**, and wet etching can be suitably used. With use of a wet etching method, the insulating film **110***bf* can be inhibited from being etched during the removal of the metal oxide layer **180**. This can inhibit a reduction in the thickness of the insulating film **110***bf* and the thickness of the insulating layer **110***b* can be uniform.

[0422] The treatment for supplying oxygen to the insulating film **110***bf* is not necessarily performed in the above-described manner. An oxygen radical, an oxygen atom, an oxygen atomic ion, an oxygen molecular ion, or the like is supplied to the insulating film **110***bf* by an ion doping method, an ion implantation method, plasma treatment, or the like. Alternatively, a film that inhibits oxygen release may be formed over the insulating film **110***bf*, and then oxygen may be supplied to the insulating film **110***bf* through the film. It is preferable to remove the film after supply of oxygen. As the above film that inhibits oxygen release, a conductive film or a semiconductor film containing one or more of indium, zinc, gallium, tin, aluminum, chromium, tantalum, titanium, molybdenum, nickel, iron, cobalt, and tungsten can be used.

[Formation of Insulating Film **110***Cf* and Formation of Insulating Film **120***f*]

[0423] Next, an insulating film **110***cf* to be the insulating layer **110***c* and an insulating film **120***f* to be the insulating layer **120** are formed over the insulating film **110***bf* (FIG. **25**E). The description of the formation of the insulating film **110***af* and the insulating film **110***bf* can be referred to for the formation of the insulating film **110***cf* and the insulating film **120***f*; thus, the detailed description thereof is omitted.

[Formation of Conductive Film **112***f*]

[0424] Then, a conductive film **112***f* to be a conductive layer **112***b* is formed over the insulating film **120***f* (FIG. **26**A). For the formation of the conductive film **112***f*, a sputtering method can be suitably used, for example.

[Formation of Opening **141** and Formation of Opening **143**]

[0425] Next, the conductive film **112***f* is processed to form the conductive layer **112**B (FIG. **26**B). For the formation of the conductive layer **112**B, one or both of a wet etching method and a dry etching method can be used. For the formation of the conductive layer **112**B, a wet etching method can be suitably used, for example.

[0426] Next, the conductive layer **112**B in a region overlapping with the opening **145** is removed, whereby the conductive layer **112***b* having the opening **143** is formed. For the formation of the opening **143**, one or both of a wet etching method and a dry etching method can be used. For the formation of the opening **143**, a wet etching method can be suitably used, for example.

[0427] Next, the insulating film **120***f* and the insulating film **110***f* (the insulating film **110***af*, the insulating film **110***bf*, and the insulating film **110***cf*) in a region overlapping with the opening **143** are removed, whereby the insulating layer **120** and the insulating layer **110** each having the opening **141** are formed (FIG. **26**C). For the formation of the opening **141**, one or both of a wet etching method and a dry etching method can be used. For the formation of the opening **141**, a dry etching method can be suitably used, for example. The opening **141** is provided in a region overlapping with the opening **145**. The conductive layer **112***a*_**1** is exposed in the opening **145**.

[0428] The opening **141** can be formed using a resist mask used for the formation of the opening **143**, for example. Specifically, a resist mask is formed over the conductive film **112***f*, the conductive film **112***f* is removed with use of the resist mask to form the opening **143**, and the insulating film **120***f* and the insulating film **110***f* are removed with use of the resist mask, whereby the opening **141** can be formed. The opening **143** may be formed using a resist mask that is different from the resist mask used for the formation of the opening **141**.

[0429] Note that in the formation of the opening **141** or after the formation of the opening **141**, part of the conductive layer **112***a* (specifically, the conductive layer **112***a*_**1**) in a region overlapping with the opening **141** may be removed. By removing part of the conductive layer **112***a*_**1**, the structure illustrated in FIG. **6**A and FIG. **6**B can be obtained.

[Formation of Semiconductor Layer **108** and Semiconductor Layer **208**]

[0430] Next, a metal oxide film **108***f* to be the semiconductor layer **108** and the semiconductor layer **208** is formed to cover the opening **141** and the opening **143** (FIG. **26**D). The metal oxide film **108***f* is provided in contact with the top surface of the insulating layer **120**, the top surface and the side surface of the conductive layer **112***b*, the top surface and the side surface of the insulating layer **110**, and the top surface of the conductive layer **112***a*_**1**.

[0431] The metal oxide film **108***f* is preferably formed by a sputtering method using a metal oxide target.

[0432] The metal oxide film **108***f* is preferably a dense film with as few defects as possible. The metal oxide film **108***f* is preferably a highly purified film in which impurities including a hydrogen element are reduced as much as possible. It is particularly preferable to use a metal oxide film having crystallinity as the metal oxide film **108***f*.

[0433] In forming the metal oxide film **108***f*, an oxygen gas is preferably used. In the case of using an oxygen gas at the time of forming the metal oxide film **108***f*, oxygen can be suitably supplied into the insulating layer **120** and the insulating layer **110**. For example, in the case of using an oxide or an oxynitride for the insulating layer **120**, oxygen can be suitably supplied into the insulating layer **120**. Similarly, in the case of using an oxide or an oxynitride for the insulating layer **110***b*, oxygen can be suitably supplied into the insulating layer **110***b*.

[0434] By the supply of oxygen to the insulating layer **120** and the insulating layer **110***b*, oxygen is supplied to the semiconductor layer **108** and the semiconductor layer **208** in a later step, so that oxygen vacancies (V_O) and V_OH in the semiconductor layer **108** and the semiconductor layer **208** can be reduced.

[0435] In forming the metal oxide film **108***f*, an inert gas (e.g., a helium gas, an argon gas, or a xenon gas) may be mixed in addition to the oxygen gas. Note that when the oxygen flow rate ratio or the oxygen partial pressure at the time of forming the metal oxide film **108***f* is higher, the crystallinity of the metal oxide film **108***f* can be higher and a transistor with higher reliability can be obtained. On the other hand, when the oxygen flow rate ratio or the oxygen partial pressure is lower, the crystallinity of the metal oxide film **108***f* is lower and a transistor with a high on-state current can be obtained.

[0436] In forming the metal oxide film **108***f*, as the substrate temperature is higher, a denser metal oxide film having higher crystallinity can be formed. On the other hand, as the substrate temperature is lower, the metal oxide film **108***f* having lower crystallinity and higher electric conductivity can be formed.

[0437] The substrate temperature at the time of forming the metal oxide film **108***f* is higher than or equal to room temperature and lower than or equal to 250° C., preferably higher than or equal to room temperature and lower than or equal to 200° C., further preferably higher than or equal to room temperature and lower than or equal to 140° C. For example, when the substrate temperature is higher than or equal to room temperature and lower than 140° C., high productivity is achieved, which is preferable. Furthermore, when the metal oxide film **108***f* is formed with the substrate temperature set at room temperature or without heating the substrate, the crystallinity can be made low.

[0438] It is preferable to perform at least one of treatment for desorbing impurities (e.g., water, hydrogen, an organic substance) adsorbed onto the surface of the insulating layer **120** and the surface of the insulating layer **110** and treatment for supplying oxygen into the insulating layer **120** and the insulating layer **110** before the formation of the metal oxide film **108***f*. For example, heat treatment can be performed at a temperature higher than or equal to 70° C. and lower than or equal to 200° C. in a reduced-pressure atmosphere. Alternatively, plasma treatment may be performed in an oxygen-containing atmosphere. Alternatively, oxygen may be supplied to the insulating layer **120** and the insulating layer **110** by plasma treatment in an atmosphere containing an oxidizing gas such as dinitrogen monoxide (N_2O). Performing plasma treatment containing a dinitrogen monoxide gas can supply oxygen while suitably removing the impurities on the surface of the insulating layer **110** and the surface of the insulating layer **120**.

[0439] Note that in the case where each of the semiconductor layer **108** and the semiconductor layer **208** has a stacked-layer structure, an upper metal oxide film is preferably formed successively after the formation of a lower metal oxide film without exposure of the surface of the lower metal oxide layer to the air.

[0440] Next, the metal oxide film **108***f* is processed into an island shape, so that the semiconductor layer **108** and the semiconductor layer **208** are formed (FIG. **27**A).

[0441] For each of the formation of the semiconductor layer **108** and the semiconductor layer **208**, one or both of a wet etching method and a dry etching method can be used. For the formation of each of the semiconductor layer **108** and the semiconductor layer **208**, a wet etching method can be suitably used, for example. At this time, part of the insulating layer **112***b* in a region not overlapping with the semiconductor layer **108** is etched and thinned in some cases. In a similar manner, part of the insulating layer **120** in a region overlapping with none of the semiconductor layer **108**, the conductive layer **112***b*, and the semiconductor layer **208** is etched and thinned in some cases. For example, in some cases, the insulating layer **120** in a region overlapping with none of the semiconductor layer **108**, the conductive layer **112***b*, and the semiconductor layer **208** is removed by etching, whereby a surface of the insulating layer **110** (specifically, the insulating layer **110***c*) is exposed. Note that in etching of the metal oxide film **108***f*, a reduction in the thickness of the insulating layer **110***c* can be inhibited when a material having high selectivity is used for the insulating layer **110***c*.

[0442] It is preferable that heat treatment be performed after the metal oxide film **108***f* is formed or the metal oxide film **108***f* is processed into the semiconductor layer **108** and the semiconductor layer **208**. By the heat treatment, hydrogen and water contained in the metal oxide film **108***f* or the semiconductor layer **108** and the semiconductor layer **208** or adsorbed onto a surface thereof can be removed. Furthermore, the film quality of the metal oxide film **108***f* or the semiconductor layer **108** and the semiconductor layer **208** is improved (e.g., the number of defects is reduced or crystallinity is increased) by the heat treatment in some cases.

[0443] Oxygen can be supplied from the insulating layer **110***b* and the insulating layer **120** to the metal oxide film **108***f* or the semiconductor layer **108** and the semiconductor layer **208** by heat treatment. In this case, it is further preferable that the heat treatment be performed before

processing into the semiconductor layer **108** and the semiconductor layer **208**. The above description can be referred to for the heat treatment; thus, the detailed description thereof is omitted.

[0444] Note that the heat treatment is not necessarily performed. The heat treatment in this step may be omitted, and heat treatment performed in a later step may also serve as the heat treatment in this step. In some cases, treatment at a high temperature in a later step (e.g., a film formation step) or the like can serve as the heat treatment in this step.

[Formation of Insulating Layer **106**]

[0445] Next, the insulating layer **106** is formed to cover the semiconductor layer **108**, the conductive layer **112***b*, the semiconductor layer **208**, and the insulating layer **120** (FIG. **27**B). For the formation of the insulating layer **106**, a PECVD method can be favorably used.

[0446] In the case of using an oxide semiconductor for the insulating layer **108** and the semiconductor layer **208**, the insulating layer **106** preferably functions as a barrier film that inhibits diffusion of oxygen. When the insulating layer **106** has a function of inhibiting diffusion of oxygen, oxygen contained in the semiconductor layer **108** and the semiconductor layer **208** is inhibited from diffusing to above the insulating layer **106**, and an increase in oxygen vacancies (V_O) in the semiconductor layer **108** and the semiconductor layer **208** can be inhibited. Consequently, the transistor can have favorable electrical characteristics and high reliability.

[0447] By increasing the temperature at the time of forming the insulating layer **106** functioning as the gate insulating layer of each of the transistor **100** and the transistor **200**A, the insulating layer including a small number of defects can be obtained. However, the high temperature at the time of forming the insulating layer **106** sometimes allows release of oxygen from the semiconductor layer **108** and the semiconductor layer **208**, which increases the amount of oxygen vacancy (V_O) and V_OH in the semiconductor layer **108** and the semiconductor layer **208** in some cases. The substrate temperature at the time of forming the insulating layer **106** is preferably higher than or equal to 180° C. and lower than or equal to 450° C., further preferably higher than or equal to 200° C. and lower than or equal to 450° C., still further preferably higher than or equal to 250° C. and lower than or equal to 450° C., yet still further preferably higher than or equal to 300° C. and lower than or equal to 450° C., yet still further preferably higher than or equal to 300° C. and lower than or equal to 400° C. When the substrate temperature at the time of forming the insulating layer **106** is in the above range, release of oxygen from the semiconductor layer **108** and the semiconductor layer **208** can be inhibited while the defects in the insulating layer **106** can be reduced. Consequently, the transistor can have favorable electrical characteristics and high reliability.

[0448] It is preferable to perform plasma treatment on the surface of the semiconductor layer **108** and the surface of the semiconductor layer **208** before the formation of the insulating layer **106**. By the plasma treatment, impurities (e.g., water) adsorbed onto the surfaces of the semiconductor layer **108** and the semiconductor layer **208** can be reduced. Therefore, impurities at the interface between the semiconductor layer **108** and the insulating layer **106** and the interface between the semiconductor layer **208** and the insulating layer **106** can be reduced, achieving a highly reliable transistor. The plasma treatment is particularly suitable in the case where the surfaces of the semiconductor layer **108** and the semiconductor layer **208** are exposed to the air after the formation of the semiconductor layer **108** and the semiconductor layer **208** and before the formation of the insulating layer **106**. For example, plasma treatment can be performed in an atmosphere containing one or more of oxygen, ozone, nitrogen, dinitrogen monoxide, and argon. The plasma treatment and the formation of the insulating layer **106** are preferably performed successively without exposure to the air.

[Formation of Conductive Layer **104** and Conductive Layer **204**]

[0449] Next, a conductive film **104***f* to be the conductive layer **104** and the conductive layer **204** is formed over the insulating layer **106** (FIG. **27**C). For the formation of the conductive film **104***f*, a sputtering method can be suitably used, for example.

[0450] Next, a resist mask is formed over the conductive film **104***f* by a photolithography process, and then the conductive film **104***f* is processed, whereby the conductive layer **104** functioning as the gate electrode of the transistor **100** and the conductive layer **204** functioning as the first gate electrode of the transistor **200**A are formed (FIG. **28**A). For processing of the conductive film **104***f*, one or both of a wet etching method and a dry etching method may be used.

[0451] Through the above process, the transistor **100** can be manufactured.

[Formation of Region **208**D]

[0452] Next, an impurity **190** is supplied (added or injected) to the semiconductor layer **208** through the insulating layer **106** with use of the conductive layer **204** as a mask (FIG. **28**B). In FIG. **28**B, the supplied impurities **190** are indicated by arrows. Thus, the region **208**D can be formed in a region of the semiconductor layer **208** not overlapping with the conductive layer **204**. At this time, the conditions of the treatment for supplying the impurity **190** are preferably determined in consideration of the material and thickness of the conductive layer **204** serving as the mask and the like so that the impurity **190** is supplied as little as possible to the region of the semiconductor layer **208** overlapping with the conductive layer **204**. Thus, a channel formation region with a sufficiently reduced impurity concentration can be formed in the region of the semiconductor layer **208** overlapping with the conductive layer **204**. In this manner, the region **108**D is formed in a region of the semiconductor layer **108** not overlapping with the conductive layer **104**.

[0453] A plasma ion doping method or an ion implantation method can be suitably used for the supply of the impurity **190**. In these methods, the concentration profile in the depth direction can be controlled with high accuracy by the acceleration voltage and the dosage of ions, or the like. The use of a plasma ion doping method can increase productivity. In addition, the use of an ion implantation method with mass separation can increase the purity of an impurity to be supplied.

[0454] In the treatment for supplying the impurity **190**, treatment conditions are preferably controlled such that the concentration is the highest at an interface between the semiconductor layer **208** and the insulating layer **106**, a portion in the semiconductor layer **208** near the interface, or

a portion in the insulating layer **106** near the interface. Accordingly, the impurity **190** at an optimal concentration can be supplied to both the semiconductor layer **208** and the insulating layer **106** in one treatment.

[0455] As a source material used for supplying the impurity **190**, a gas containing the above impurity element can be used, for example. In the case where boron is supplied, typically, one or more of a B_2H_6 gas and a BF_3 gas can be used. In the case where phosphorus is supplied, typically, a PH_3 gas can be used. A mixed gas in which any of these source gases is diluted with a noble gas may be used.

[0456] For example, any of CH_4, N_2, NH_3, AlH_3, $AlCl_3$, SiH_4, Si_2H_6, F_2, HF, H_2, $(C_5H_5)_2Mg$, a noble gas, and the like can be used as the source gas for supplying the impurity **190**. Note that the source material is not limited to a gas, and a solid or liquid may be heated and vaporized.

[0457] Addition of the impurity **190** can be controlled by setting the conditions such as the acceleration voltage and the dosage in consideration of the compositions, densities, thicknesses, and the like of the insulating layer **106** and the semiconductor layer **208**.

[0458] For example, in the case where boron is added by an ion implantation method or a plasma ion doping method, the acceleration voltage can be, for example, higher than or equal to 5 kV and lower than or equal to 100 kV, preferably higher than or equal to 7 kV and lower than or equal to 70 kV, further preferably higher than or equal to 10 kV and lower than or equal to 50 kV. The dosage can be, for example, greater than or equal to 1×10^{13} ions/cm^2 and less than or equal to 1×10^{17} ions/cm^2, preferably greater than or equal to 1×10^{14} ions/cm^2 and less than or equal to 5×10^{16} ions/cm^2, further preferably greater than or equal to 1×10^{15} ions/cm^2 and less than or equal to 3×10^{16} ions/cm^2.

[0459] In the case where phosphorus ions are added by an ion implantation method or a plasma ion doping method, the acceleration voltage can be, for example, higher than or equal to 10 kV and lower than or equal to 100 kV, preferably higher than or equal to 30 kV and lower than or equal to 90 kV, further preferably higher than or equal to 40 kV and lower than or equal to 80 kV. The dosage can be, for example, greater than or equal to 1×10^{13} ions/cm^2 and less than or equal to 1×10^{17} ions/cm^2, preferably greater than or equal to 1×10^{14} ions/cm^2 and less than or equal to 5×10^{16} ions/cm^2, further preferably greater than or equal to 1×10^{15} ions/cm^2 and less than or equal to 3×10^{16} ions/cm^2.

[0460] Note that a method for supplying the impurity **190** is not limited thereto; plasma treatment, treatment using thermal diffusion by heating, or the like may be used, for example. In a plasma treatment method, plasma is generated in a gas atmosphere containing an impurity element to be added and plasma treatment is performed, so that the impurity can be added. A dry etching apparatus, an ashing apparatus, a plasma CVD apparatus, a high-density plasma CVD apparatus, or the like can be used as an apparatus for generating the plasma.

[0461] For example, when plasma treatment is performed with a plasma CVD apparatus in an atmosphere containing a hydrogen gas, hydrogen can be supplied as the impurity **190** to a region of the semiconductor layer **208** not overlapping with the conductive layer **204** and a region of the semiconductor layer **108** not overlapping with the conductive layer **104**. With use of a plasma CVD apparatus for the treatment for supplying the impurity **190** and the formation of the insulating layer **106**, the treatment for supplying the impurity **190** and the formation of the insulating layer **106** can be successively performed in the apparatus, so that the productivity can be increased.

[0462] In one embodiment of the present invention, the impurity **190** can be supplied to the semiconductor layer **208** through the insulating layer **106**. Thus, even in the case where the semiconductor layer **208** has crystallinity, damage to the semiconductor layer **208** is reduced at the time of supplying the impurity **190**, and degradation of crystallinity can be inhibited. Therefore, this is suitable for the case where a reduction in crystallinity increases electrical resistance. Similarly, damage to the semiconductor layer **108** can be reduced.

[Formation of Insulating Layer **195**]

[0463] Next, the insulating layer **195** is formed to cover the conductive layer **104**, the conductive layer **204**, and the insulating layer **106** (FIG. **28**C). For the formation of the insulating layer **195**, a PECVD method can be favorably used.

[0464] If the deposition temperature of the insulating layer **195** is too high, impurities contained in the region **108**D and the region **208**D might diffuse into peripheral portions of the semiconductor layer **108** and the semiconductor layer **208**, which include the channel formation regions. Furthermore, electrical resistance of the region **108**D and the region **208**D might be increased. Thus, the deposition temperature of the insulating layer **195** may be determined in consideration of the impurity diffusion.

[0465] The deposition temperature of the insulating layer **195** is higher than or equal to 150° C. and lower than or equal to 400° C., preferably higher than or equal to 180° C. and lower than or equal to 360° C., further preferably higher than or equal to 200° C. and lower than or equal to 250° C., for example. Deposition of the insulating layer **195** at low temperatures enables the transistor to have favorable electrical characteristics even when it has a short channel length.

[0466] Heat treatment may be performed after the formation of the insulating layer **195**. The heat treatment can allow the region **108**D and the region **208**D to have lower resistance, in some cases. For example, by the heat treatment, the impurity **190** diffuses moderately, so that the region **108**D and the region **208**D each having an ideal concentration gradient of the impurity **190** can be formed. The above description can be referred to for the heat treatment; thus, the detailed description thereof is omitted. Note that when the temperature of the heat treatment is too high (e.g., higher than or equal to 500° C.), the impurity **190** is also diffused into the channel formation region, so that the electrical characteristics or reliability of the transistor might be degraded.

[0467] Note that the heat treatment is not necessarily performed. The heat treatment in this step may be omitted, and heat treatment performed in a later step may also serve as the heat treatment in this step. In the case where treatment at a high temperature (e.g., deposition step) is performed in a later step, such treatment can serve as the heat treatment in this step in some cases.

[0468] Next, the insulating layer **106** and the insulating layer **195** are partly etched, whereby the opening **147***a* and the opening **147***b* that reach the regions **208**D are formed.

[0469] Subsequently, a conductive film is formed over the insulating layer **195** to cover the opening **147***a* and the opening **147***b* and then processed, whereby the conductive

layer **212***a* and the conductive layer **212***b* functioning as the source electrode and the drain electrode of the transistor **200** are formed (FIG. **7**B).

[0470] Through the above steps, the transistor **200**A can be manufactured.

[0471] Through the above process, the semiconductor device **10**A can be manufactured.

Manufacturing Method Example 2

[0472] A manufacturing method will be described with use of a structure where an oxide semiconductor is used for each of the semiconductor layer **108** and the semiconductor layer **208** of the semiconductor device **10**E illustrated in FIG. **13**A and the like as an example. Each of FIG. **29**A to FIG. **30**B is a diagram illustrating the method for manufacturing the semiconductor device **10**E. Each drawing is a cross-sectional view taken along the dashed-dotted line A**1**-A**2**.

[0473] The steps up to the formation of the insulating layer **106** are similar to those in the manufacturing method described in <Manufacturing method example 1>. Thus, the method for manufacturing the semiconductor device in FIG. **25**A to FIG. **27**B can be referred to.

[Formation of Insulating Layer **106**A and Insulating Layer **106**B]

[0474] Next, a resist mask is formed over the insulating layer **106** by a photolithography process, and then the insulating layer **106** is processed, whereby the insulating layer **106**A functioning as a gate insulating layer of the transistor **100**B and the insulating layer **106**B functioning as a first gate insulating layer of the transistor **200**E are formed (FIG. **29**A). The insulating layer **106**A is provided in a region overlapping with the semiconductor layer **108**. The insulating layer **106**B is provided in a region overlapping with the semiconductor layer **208**. For processing of the insulating layer **106**, one or both of a wet etching method and a dry etching method may be used. A dry etching method can be suitably used for the processing of the insulating layer **106**.

[Formation of Conductive Layer **104** and Conductive Layer **204**]

[0475] Next, the conductive film **104***f* to be the conductive layer **104**, the conductive layer **204**, the conductive layer **212***a*, and the conductive layer **212***b* is formed over the insulating layer **120**, the conductive layer **112***b*, the semiconductor layer **108**, the semiconductor layer **208**, the insulating layer **106**A, and the insulating layer **106**B (FIG. **29**B). For the formation of the conductive film **104***f*, a sputtering method can be suitably used, for example.

[0476] Next, a resist mask is formed over the conductive film **104***f* by a photolithography process, and then the conductive film **104***f* is processed to form the conductive layer **104** functioning as the gate electrode of the transistor **100**B, the conductive layer **204** functioning as the first gate electrode of the transistor **200**A, and the conductive layer **212***a* and the conductive layer **212***b* functioning as the source electrode and the drain electrode (FIG. **30**A). The conductive layer **104** is provided in a region overlapping with the semiconductor layer **108** with the insulating layer **106**A therebetween. The conductive layer **204** is provided in a region overlapping with the semiconductor layer **208** with the insulating layer **106**B therebetween. For processing of the conductive film **104***f*, one or both of a wet etching method and a dry etching method may be used.

[0477] Through the above steps, the transistor **100**B can be manufactured.

[Formation of Region **208**L and Region **208**D]

[0478] Next, with the conductive layer **204**, the conductive layer **212***a*, and the conductive layer **212***b* used as masks, the impurity **190** is supplied to the semiconductor layer **208** through the insulating layer **106**B (FIG. **30**B). In FIG. **30**B, the supplied impurities **190** are indicated by arrows. In this manner, the region **208**L and the region **208**D can be formed in the semiconductor layer **208**. The region **208**L is formed in a region overlapping with the insulating layer **106**B and not overlapping with the conductive layer **204**. The region **208**D is formed in a region overlapping with none of the insulating layer **106**B, the conductive layer **204**, the conductive layer **212***a*, and the conductive layer **212***b*. The region **108**L and the region **108**D in the semiconductor layer **108** are formed in a manner similar to the above. The above description can be referred to for supplying the impurity **190**; thus, the detailed description thereof is omitted.

[0479] The above description in <Manufacturing method example 1> can be referred to for the formation of the insulating layer **195**; thus, the detailed description thereof is omitted.

[0480] Through the above steps, the transistor **200**E can be manufactured.

[0481] Through the above process, the semiconductor device **10**E can be manufactured.

Manufacturing Method Example 3

[0482] A manufacturing method will be described with use of a structure where an oxide semiconductor is used for each of the semiconductor layer **108** and the semiconductor layer **208** of the semiconductor device **10**F illustrated in FIG. **14**A as an example.

[0483] Each of FIG. **31**A to FIG. **32**B is a diagram illustrating the method for manufacturing the semiconductor device **10**F. Each drawing is across-sectional view taken along the dashed-dotted line A**1**-A**2**.

[0484] The steps up to the formation of the insulating layer **106** are similar to those in the manufacturing method described in <Manufacturing method example 1>. Thus, the method for manufacturing the semiconductor device in FIG. **25**A to FIG. **27**B can be referred to.

[Formation of Insulating Layer **106**A and Insulating Layer **106**B]

[0485] Next, the insulating layer **106** is processed to form an opening **139***a* and an opening **139***b* in a region overlapping with the semiconductor layer **208** (FIG. **31**A). For processing of the insulating layer **106**, one or both of a wet etching method and a dry etching method may be used. A dry etching method can be suitably used for the processing of the insulating layer **106**.

[Formation of Conductive Layer **104**, Conductive Layer **204**, Conductive Layer **212***a*, and Conductive Layer **212***b*]

[0486] Next, the conductive film **104***f* to be the conductive layer **104**, the conductive layer **204**, the conductive layer **212***a*, and the conductive layer **212***b* is formed over the insulating layer **120**, the conductive layer **112***b*, the semiconductor layer **108**, the semiconductor layer **208**, and the

insulating layer **106** (FIG. **31**B). For the formation of the conductive film **104***f*, a sputtering method can be suitably used, for example.

[0487] Next, a resist mask is formed over the conductive film **104***f* by a photolithography process, and then the conductive film **104***f* and the insulating layer **106** are processed to form the conductive layer **104**, the conductive layer **204**, the conductive layer **212***a*, and the conductive layer **212***b*, the insulating layer **106**A, the insulating layer **106**B, the insulating layer **106**C, and the insulating layer **106**D (FIG. **32**A). For processing of the conductive film **104***f* and the insulating layer **106**, one or both of a wet etching method and a dry etching method may be used.

[0488] Through the above steps, the transistor **100**A can be manufactured.

[Formation of Region **208**D]

[0489] Next, the impurity **190** is supplied to the semiconductor layer **208** using the conductive layer **204**, the conductive layer **212***a*, and the conductive layer **212***b* as masks (FIG. **32**B). In FIG. **32**B, the supplied impurities **190** are indicated by arrows. In this manner, the region **208**D can be formed in the semiconductor layer **208**. The region **108**D in the semiconductor layer **108** is also formed in a manner similar to the above. The above description can be referred to for supplying the impurity **190**; thus, the detailed description thereof is omitted.

[0490] The above description in <Manufacturing method example 1> can be referred to for the formation of the insulating layer **195**; thus, the detailed description thereof is omitted.

[0491] Through the above steps, the transistor **200**F can be manufactured.

[0492] Through the above process, the semiconductor device **10**F can be manufactured.

Manufacturing Method Example 4

[0493] A manufacturing method will be described with use of a structure where an oxide semiconductor is used for each of the semiconductor layer **108** and the semiconductor layer **208** of the semiconductor device **10**G illustrated in FIG. **15**B as an example.

[0494] Each of FIG. **33**A to FIG. **34**B is a diagram illustrating a method for manufacturing the semiconductor device **10**G. Each drawing is a cross-sectional view taken along the dashed-dotted line A**1**-A**2**.

[0495] The steps up to the formation of the insulating layer **106** are similar to those in the manufacturing method described in <Manufacturing method example 1>. Thus, the method for manufacturing the semiconductor device in FIG. **25**A to FIG. **27**B can be referred to.

[Formation of Opening **137***a* and Opening **137***b*]

[0496] Next, the insulating layer **106** is processed to form the opening **137***a* and the opening **137***b* in a region overlapping with the semiconductor layer **208** (FIG. **33**A). For processing of the insulating layer **106**, one or both of a wet etching method and a dry etching method may be used. A dry etching method can be suitably used for the processing of the insulating layer **106**.

[Formation of Conductive Layer **104**, Conductive Layer **204**, Conductive Layer **212***a*, and Conductive Layer **212***b*]

[0497] Next, the conductive film **104***f* to be the conductive layer **104**, the conductive layer **204**, the conductive layer **212***a*, and the conductive layer **212***b* is formed over the insulating layer **120**, the conductive layer **112***b*, the semiconductor layer **108**, the semiconductor layer **208**, and the insulating layer **106** (FIG. **33**B). For the formation of the conductive film **104***f*, a sputtering method can be suitably used, for example.

[0498] Next, a resist mask is formed over the conductive film **104***f* by a photolithography process, and then the conductive film **104***f* is processed to form the conductive layer **104**, the conductive layer **204**, the conductive layer **212***a*, and the conductive layer **212***b* (FIG. **34**A). For processing of the conductive film **104***f*, one or both of a wet etching method and a dry etching method may be used.

[0499] Through the above steps, the transistor **100** can be manufactured.

[Formation of Region **208**L and Region **208**D]

[0500] Next, with the conductive layer **204**, the conductive layer **212***a*, and the conductive layer **212***b* as masks, the impurity **190** is supplied to the semiconductor layer **208** through the insulating layer **106** (FIG. **34**B). In FIG. **34**B, the supplied impurities **190** are indicated by arrows. In this manner, the region **208**L and the region **208**D can be formed in the semiconductor layer **208**. The region **208**L is formed in a region overlapping with the insulating layer **106** and not overlapping with the conductive layer **204**. The region **208**D is formed in a region overlapping with none of the insulating layer **106**, the conductive layer **204**, the conductive layer **212***a*, and the conductive layer **212***b*. Also in the semiconductor layer **108**, the region **108**D is formed in a region overlapping with the conductive layer **104**, in a manner similar to the above. Note that the amount of the impurities **190** supplied to the region **108**D may be approximately the same as the amount of the impurities supplied to the region **208**L. The above description can be referred to for supplying the impurity **190**; thus, the detailed description thereof is omitted.

[0501] The above description in <Manufacturing method example 1> can be referred to for the formation of the insulating layer **195**; thus, the detailed description thereof is omitted.

[0502] Through the above steps, the transistor **200**G can be manufactured.

[0503] Through the above process, the semiconductor device **10**G can be manufactured.

[0504] This embodiment can be combined with the other embodiments as appropriate. In this specification, in the case where a plurality of structure examples are shown in one embodiment, the structure examples can be combined as appropriate.

Embodiment 2

[0505] In this embodiment, a structure example of a display apparatus for which the semiconductor device of one embodiment of the present invention can be used will be described.

[0506] FIG. **35**A is a schematic view of a display apparatus **50** of one embodiment of the present invention. In the display apparatus **50**, a substrate **152** and the substrate **101** are bonded to each other. In FIG. **35**A, the substrate **152** is denoted by a dashed line.

[0507] The display apparatus **50** includes a display portion **235**, a connection portion **140**, a first driver circuit portion

231, a second driver circuit portion **232**, and a wiring **165**. FIG. **35**A illustrates an example in which an IC **173** and an FPC **172** are mounted on the display apparatus **50**. Thus, the structure illustrated in FIG. **35**A can also be regarded as a display module including the display apparatus **50**, the IC (integrated circuit), and the FPC.

[0508] The connection portion **140** is provided outside the display portion **235**. The connection portion **140** can be provided along one or more sides of the display portion **235**. The number of the connection portions **140** can be one or more. FIG. **35**A illustrates an example in which the connection portion **140** is provided to surround the four sides of the display portion **235**. A common electrode of a light-emitting device is electrically connected to a conductive layer in the connection portion **140**, so that a potential can be supplied to the common electrode.

[0509] The wiring **165** has a function of supplying a signal and electric power to the display portion **235**, the first driver circuit portion **231**, and the second driver circuit portion **232**. The signal and electric power are input to the wiring **165** from the outside through the FPC **172** or input to the wiring **165** from the IC **173**.

[0510] FIG. **35**A illustrates an example in which the IC **173** is provided over the substrate **101** by a COG (Chip On Glass) method, a COF (Chip On Film) method, or the like. The IC **173** may include a scan line driver circuit or a signal line driver circuit, for example. Note that the display apparatus **50** and the display module are not necessarily provided with an IC. The IC may be mounted on the FPC by a COF method or the like.

[0511] The display portion **235** includes a plurality of pixels **230** arranged in a matrix. As the pixels **230**, three types of pixels, a pixel **230***a*, a pixel **230***b*, and a pixel **230***c*, can be used, for example. The pixel **230***a*, the pixel **230***b*, and the pixel **230***c* each include a display device (also referred to as a display element). Examples of the display device include a liquid crystal device (also referred to as a liquid crystal element) and a light-emitting device. As the light-emitting device, an OLED (Organic Light Emitting Diode) or a QLED (Quantum-dot Light Emitting Diode) is preferably used, for example. Examples of a light-emitting substance included in the light-emitting device include a substance that emits fluorescent light (a fluorescent material), a substance that emits phosphorescent light (a phosphorescent material), a substance exhibiting thermally activated delayed fluorescence (a thermally activated delayed fluorescent (TADF) material), and an inorganic compound (e.g., a quantum dot material). In addition, an LED such as a micro-LED can be also used as the light-emitting device.

[0512] The pixel **230***a*, the pixel **230***b*, and the pixel **230***c* have a function of emitting light of different colors. For example, the pixel **230***a* may have a function of emitting red (R) light, the pixel **230***b* may have a function of emitting green (G) light, and the pixel **230***c* may have a function of emitting blue (B) light. Alternatively, for example, the pixel **230***a* may have a function of emitting yellow (Y) light, the pixel **230***b* may have a function of emitting cyan (C) light, and the pixel **230***c* may have a function of emitting magenta (M) light.

[0513] One pixel **230***a*, one pixel **230***b*, and one pixel **230***c* form one pixel **240**, which achieves full-color display. Thus, the pixel **230** functions as a subpixel. The display apparatus **50** illustrated in FIG. **35**A shows an example in which the pixels **230** each functioning as a subpixel are arranged in a stripe pattern. The number of subpixels for forming one pixel **240** is not limited to three, and may be four or more. For example, four subpixels which emit light of R, G, B, and white (W) may be included. Alternatively, four subpixels which emit light of four colors, R, G, B, and Y, may be included.

[0514] FIG. **35**B is a block diagram illustrating the display apparatus **50**. The display apparatus **50** includes the display portion **235**, the first driver circuit portion **231**, and the second driver circuit portion **232**. The display portion **235** includes a plurality of pixels **230** arranged in a matrix of m rows and n columns (m and n are each an integer of 1 or more). In FIG. **35**B, the pixel **230** in the first row and the n-th column is denoted as a pixel **230**[**1**,*n*], the pixel **230** in the m-th row and the first column is denoted as a pixel **230**[*m*,**1**], and the pixel **230** in the m-th row and the n-th column is denoted as a pixel **230**[*m,n*]. A given pixel **230** included in the display portion **235** is denoted as a pixel **230**[*r,s*] in some cases. Note that r is an integer greater than or equal to 1 and less than or equal to m, and s is an integer greater than or equal to 1 and less than or equal to n.

[0515] A circuit included in the first driver circuit portion **231** functions as, for example, a scan line driver circuit. A circuit included in the second driver circuit portion **232** functions as, for example, a signal line driver circuit. Note that some sort of circuit may be provided at a position facing the first driver circuit portion **231** with the display portion **235** positioned therebetween. Some sort of circuit may be provided at a position facing the second driver circuit portion **232** with the display portion **235** positioned therebetween. Note that circuits included in the first driver circuit portion **231** and the second driver circuit portion **232** are collectively referred to as a peripheral driver circuit.

[0516] Any of various circuits such as a shift register circuit, a level shifter circuit, an inverter circuit, a latch circuit, an analog switch circuit, a demultiplexer circuit, and a logic circuit can be used as a peripheral driver circuit **233**. In the peripheral driver circuit **233**, a transistor, a capacitor, and the like can be used. Transistors included in the peripheral driver circuit **233** may be formed in the same step as the transistors included in the pixels **230**.

[0517] The display apparatus **50** includes m wirings **236** which are arranged substantially parallel to each other and whose potentials are controlled by the circuits included in the first driver circuit portion **231**, and n wirings **237** which are arranged substantially parallel to each other and whose potentials are controlled by the circuits included in the second driver circuit portion **232**.

[0518] FIG. **35**B illustrates an example in which the wiring **236** and the wiring **237** are connected to the pixel **230**. Note that the wiring **236** and the wiring **237** are examples, and the wirings connected to the pixel **230** are not limited to the wiring **236** and the wiring **237**.

<Structure Example of Peripheral Driver Circuit>

[0519] Using a latch circuit as an example, a structure example of a circuit that can be used as a peripheral driver circuit will be described.

[0520] FIG. **36**A is a circuit diagram illustrating a structure example of a latch circuit LAT. The latch circuit LAT illustrated in FIG. **36**A includes a transistor Tr**31**, a transistor Tr**33**, a transistor Tr**35**, a transistor Tr**36**, a capacitor C**31**, and an inverter circuit INV. In FIG. **36**A, a node that is electrically connected to one of a source and a drain of the

transistor Tr**33**, a gate of the transistor Tr**35**, and one electrode of the capacitor C**31** is referred to as a node N.

[0521] In the latch circuit LAT illustrated in FIG. **36**A, when a high-potential signal is input to a terminal SMP, the transistor Tr**33** is turned on. Thus, the potential of the node N becomes a potential corresponding to the potential of a terminal ROUT, and data corresponding to a signal input from the terminal ROUT to the latch circuit LAT is written to the latch circuit LAT. After data is written to the latch circuit LAT, the potential of the terminal SMP is set to a low potential, so that the transistor Tr**33** is turned off Thus, the potential of the node N is held and the data written to the latch circuit LAT is held. Specifically, when the potential of the node N is a low potential, data "0" is held in the latch circuit LAT and when the potential of the node N is a high potential, data "1" is held in the latch circuit LAT, for example.

[0522] A transistor with a low off-state current is preferably used as the transistor Tr**33**. An OS transistor can be suitably used as the transistor Tr**33**. Thus, the latch circuit LAT can hold data for a long period. Thus, the frequency of rewriting data in the latch circuit LAT can be lowered.

[0523] In this specification and the like, data that allows a signal input from a terminal SP**2** to be output to a terminal LIN is written to the latch circuit LAT, which is referred to simply as "writing data to the latch circuit LAT" in some cases. That is, for example, data "1" is written to the latch circuit LAT, which is referred to simply as "writing data to the latch circuit LAT" in some cases.

[0524] The semiconductor device of one embodiment of the present invention can be suitably used for the latch circuit LAT. For example, the transistor **100** or the transistor **200** illustrated in FIG. **1**B or the like can be used as one or more of the transistor Tr**31**, the transistor Tr**33**, the transistor Tr**35**, and the transistor Tr**36**.

[0525] FIG. **36**B illustrates a structure example of the inverter circuit INV. The inverter circuit INV includes a transistor Tr**41**, a transistor Tr**43**, a transistor Tr**45**, a transistor Tr**47**, and a capacitor C**41**.

[0526] The latch circuit LAT has the structure illustrated in FIG. **36**A and the inverter circuit INV has the structure illustrated in FIG. **36**B, in which case all the transistors included in the latch circuit LAT can be transistors having the same polarity, for example, n-channel transistors. Thus, the transistor Tr**31**, the transistor Tr**35**, the transistor Tr**36**, the transistor Tr**41**, the transistor Tr**43**, the transistor Tr**45**, and the transistor Tr**47** as well as the transistor Tr**33** can be OS transistors, for example. Accordingly, all the transistors included in the latch circuit LAT can be formed in the same step.

[0527] The semiconductor device of one embodiment of the present invention can be suitably used for the inverter circuit INV. For example, the transistor **100** or the transistor **200** illustrated in FIG. **1**B or the like can be used as one or more of the transistor Tr**41**, the transistor Tr**43**, the transistor Tr**45**, and the transistor Tr**47**.

<Structure Example of Pixel Circuit>

[0528] FIG. **37**A illustrates a structure example of the pixel **230**. The pixel **230** includes a pixel circuit **51** and a light-emitting device **61**.

[0529] The pixel circuit **51** illustrated in FIG. **37**A is a 2Tr1C-type pixel circuit including a transistor **52**A, a transistor **52**B, and a capacitor **53**.

[0530] One of a source and a drain of the transistor **52**A is electrically connected to a gate of the transistor **52**B and one terminal of the capacitor **53**, and the other of the source and the drain of the transistor **52**A is electrically connected to a wiring SL. A gate of the transistor **52**A is electrically connected to a wiring GL. One of a source electrode and a drain electrode of the transistor **52**B and the other terminal of the capacitor **53** are electrically connected to an anode of the light-emitting device **61**. The other of the source electrode and the drain electrode of the transistor **52**B is electrically connected to a wiring ANO. A cathode of the light-emitting device **61** is electrically connected to a wiring VCOM.

[0531] The wiring GL corresponds to the wiring **236**, and the wiring SL corresponds to the wiring **237**. The wiring VCOM is a wiring for supplying a potential for supplying current to the light-emitting device **61**. The transistor **52**A has a function of controlling the on/off state between the wiring SL and the gate of the transistor **52**B in accordance with the potential of the wiring GL. For example, VDD is supplied to the wiring ANO, and VSS is supplied to the wiring VCOM.

[0532] The transistor **52**B has a function of controlling the amount of current flowing through the light-emitting device **61**. The capacitor **53** has a function of holding a gate potential of the transistor **52**B. The intensity of light emitted by the light-emitting device **61** is controlled in accordance with an image signal supplied to the gate of the transistor **52**B.

[0533] Some or all of the transistors included in the pixel circuit **51** may be provided with a back gate electrode. In the pixel circuit **51** illustrated in FIG. **37**A, the transistor **52**B includes a back gate electrode, and the back gate electrode is electrically connected to one of a source electrode and a drain electrode of the transistor **52**B. Note that the back gate electrode of the transistor **52**B may be electrically connected to a gate electrode of the transistor **52**B.

[0534] The above-described semiconductor device can be suitably used for the pixel circuit **51**. For example, the transistor **100** illustrated in FIG. **7**B or the like can be used as the transistor **52**A, and the transistor **200**A can be used as the transistor **52**B.

[0535] FIG. **37**B shows a structure example different from that of the pixel **230** shown in FIG. **37**A. The pixel **230** includes a pixel circuit **51**A and the light-emitting device **61**.

[0536] The pixel circuit **51**A illustrated in FIG. **37**B is different from the pixel circuit **51** illustrated in FIG. **37**A mainly in including a transistor **52**C. The pixel circuit **51**A is a 3Tr1C-type pixel circuit including the transistor **52**A, the transistor **52**B, the transistor **52**C, and the capacitor **53**.

[0537] One of a source electrode and a drain electrode of the transistor **52**C is electrically connected to one of a source electrode and a drain electrode of the transistor **52**B. The other of the source electrode and the drain electrode of the transistor **52**C is electrically connected to a wiring V**0**. For example, a reference potential is supplied to the wiring V**0**.

[0538] The transistor **52**C has a function of controlling the on/off state between the wiring V**0** and the one of the source electrode and the drain electrode of the transistor **52**B in accordance with the potential of the wiring GL. Furthermore, variations in the gate-source potential of the transistor **52**B can be inhibited by the reference potential of the wiring V**0** supplied through the transistor **52**C.

[0539] A current value that can be used for setting of pixel parameters can be obtained with use of the wiring V**0**. Specifically, the wiring V**0** can function as a monitor line for outputting current flowing through the transistor **52**B or current flowing through the light-emitting device **61** to the outside. A current output to the wiring V**0** is converted into a voltage by a source follower circuit or the like and can be output to the outside. For another example, the current is converted into a digital signal by an A/D converter, and can be output to the outside.

[0540] The above-described semiconductor device can be suitably used for the pixel circuit **51**A. For example, the transistor **100** illustrated in FIG. **7**B or the like can be used as each of the transistor **52**A and the transistor **52**C, and the transistor **200**A can be used as the transistor **52**B.

[0541] Note that there is no particular limitation on the pixel circuit that can be used for the display apparatus of one embodiment of the present invention.

[0542] A structure example of the pixel circuit **51**A is illustrated in FIG. **37**C. FIG. **37**C is a cross-sectional view of the pixel circuit **51**A.

[0543] In a structure illustrated in FIG. **37**C, the pixel circuit **51**A employs the semiconductor device **10**E illustrated in FIG. **13**B or the like. Specifically, the transistor **100**B is used as each of the transistor **52**A and the transistor **52**C, and the transistor **200**E is used as the transistor **52**B.

[0544] The transistor **52**B functioning as a driving transistor that controls a current flowing through the light-emitting device **61** preferably has a higher saturation point than the transistor **52**A functioning as a selection transistor for controlling a selection state of the pixel **230**. The use of the transistor **200**E having a long channel length as the transistor **52**B enables the display apparatus to have high reliability. Furthermore, when the transistor **100**B is used as each of the transistor **52**A and the transistor **52**C, the area occupied by the pixel circuit **51**A can be reduced, so that a high-resolution display apparatus can be obtained.

[0545] Note that the transistor **100**B may also be used as the transistor **52**B. The use of the transistor **100**B having a short channel length as the transistor **52**B enables the display apparatus to have high luminance. Furthermore, the area occupied by the pixel circuit **51**A can be reduced, so that a high-resolution display apparatus can be obtained.

[0546] The conductive layer **212***a* included in the transistor **52**B is electrically connected to the conductive layer **202** through an opening **133** provided in the insulating layer **120** and the insulating layer **110**. The conductive layer **212***a* is electrically connected to the conductive layer **112***b* included in the transistor **52**C. Note that the electrical connection between the transistor **52**A and the transistor **52**B is omitted in FIG. **37**C. For example, a first opening reaching the conductive layer **112***b* included in the transistor **52**A and a second opening reaching the conductive layer **204** included in the transistor **52**B are provided in the insulating layer **195**. A first wiring is provided over the insulating layer **195** to cover the first opening and the second opening, whereby the conductive layer **112***b* included in the transistor **52**A and the conductive layer **204** included in the transistor **52**B can be electrically connected to each other through the first wiring.

[0547] In FIG. **37**C, the capacitor **53** is omitted. The capacitor **53** can be formed in a region where the insulating layer **106** is sandwiched between the conductive layer **204** functioning as the gate electrode of the transistor **52**B and the conductive layer **112***b* functioning as the gate electrode/one of the source electrode and the drain electrode of the transistor **52**C, for example. Note that there is no particular limitation on the structure of the capacitor **53**.

[0548] The insulating layer **195** is provided to cover the transistor **52**A, the transistor **52**B, the transistor **52**C, and the capacitor **53**, and an insulating layer **197** is provided to cover the insulating layer **195**. The light-emitting device **61** can be provided over the insulating layer **197**. FIG. **37**C illustrates a pixel electrode **111** functioning as one electrode of the light-emitting device **61**. The pixel electrode **111** is electrically connected to the conductive layer **112***b* of the transistor **52**C through an opening **135** formed in the insulating layer **195** and the insulating layer **197**. The above description can be referred to for the insulating layer **195**; thus, the detailed description thereof is omitted. The insulating layer **197** has a function of reducing unevenness due to the transistor **52**A, the transistor **52**B, and the transistor **52**C and making the formation surface of the light-emitting device **61** flatter. Note that in this specification and the like, the insulating layer **197** is referred to as a planarization layer in some cases.

[0549] As the insulating layer **197**, an insulating layer including an organic material can be favorably used. As the organic material, a photosensitive organic resin is preferably used, and for example, a photosensitive resin composite containing an acrylic resin is preferably used. Note that in this specification and the like, an acrylic resin refers to not only a polymethacrylic acid ester or a methacrylic resin, but also all the acrylic-based polymers in a broad sense in some cases.

[0550] For the insulating layer **197**, it is possible to use an acrylic resin, a polyimide resin, an epoxy resin, an imide resin, a polyamide resin, a polyimide-amide resin, a silicone resin, a siloxane resin, a benzocyclobutene-based resin, a phenol resin, precursors of these resins, or the like. Alternatively, for the insulating layer **197**, it is possible to use an organic material such as polyvinyl alcohol (PVA), polyvinyl butyral, polyvinylpyrrolidone, polyethylene glycol, polyglycerin, pullulan, water-soluble cellulose, or an alcohol-soluble polyamide resin. A photoresist may be used as the photosensitive resin. As the photosensitive organic resin, either a positive material or a negative material may be used.

[0551] The insulating layer **197** may have a stacked-layer structure of an organic insulating layer and an inorganic insulating layer. For example, the insulating layer **197** can have a stacked-layer structure of an organic insulating layer and an inorganic insulating layer over the organic insulating layer. An inorganic insulating layer provided on the outermost surface of the insulating layer **197** can function as an etching protective layer. This can inhibit a decrease in the flatness of the insulating layer **197**, which is caused by etching of part of the insulating layer **197** in the formation of the pixel electrode **111**.

[0552] The pixel electrode **111** is electrically connected to the conductive layer **112***b* through an opening provided in the insulating layer **197** and the insulating layer **195**.

[0553] The display apparatus of one embodiment of the present invention can have any of a top-emission structure in which light is emitted in a direction opposite to the substrate where the light-emitting device is formed, a bottom-emission structure in which light is emitted toward the substrate where the light-emitting device is formed, and a dual-emission structure in which light is emitted toward both surfaces.

[0554] Different structure examples from that of the pixel circuit **51**A in FIG. **37**C are illustrated in FIG. **38**A and FIG. **38**B. FIG. **38**A illustrates a structure where the semiconductor device **10**F illustrated in FIG. **14**A is used for the pixel circuit **51**A. Specifically, the transistor **100**A is used for each of the transistor **52**A and the transistor **52**C and the transistor **200**F is used for the transistor **52**B. FIG. **38**B illustrates a structure in which the semiconductor device **10**G illustrated in FIG. **14**B is used for the pixel circuit **51**A. Specifically, the transistor **100** is used as each of the transistor **52**A and the transistor **52**C and the transistor **200**G is used as the transistor **52**B. The above description can be referred to for each of the transistors; thus, the detailed description thereof is omitted.

[0555] FIG. **39** illustrates a structure example different from that of the pixel circuit **51**A illustrated in FIG. **37**C, FIG. **38**A, and FIG. **38**B. FIG. **39** illustrates a structure where the semiconductor device **10**H illustrated in FIG. **16**A is used for the pixel circuit **51**A. Specifically, the transistor **100**C is used as the transistor **52**C and the transistor **200**H is used as the transistor **52**B. The above description can be referred to for the transistor **52**B and the transistor **52**C; thus, the detailed description is omitted.

[0556] The transistor **52**A can be provided over the transistor **52**B. FIG. **39** illustrates an example in which the transistor **52**A employs the structure of the transistor **100** illustrated in FIG. **1**B or the like. The transistor **52**A includes a conductive layer **203**, an insulating layer **107**, a semiconductor layer **109**, a conductive layer **116***a*, and a conductive layer **116***b*. The conductive layer **203** functions as a gate electrode. The conductive layer **203** can be formed using a material that can be used for the conductive layer **104** and the conductive layer **204**. Part of the insulating layer **107** functions as a gate insulating layer. For the insulating layer **107**, a material that can be used for the insulating layer **106** can be used. The conductive layer **116***a* functions as one of a source electrode and a drain electrode, and the conductive layer **116***b* functions as the other. For the conductive layer **116***a* and the conductive layer **116***b*, a material that can be used for the conductive layer **112***a* and the conductive layer **112***b* can be used. For the semiconductor layer **109**, a material that can be used for the semiconductor layer **108** and the semiconductor layer **208** can be used.

[0557] An insulating layer **150** is provided over the insulating layer **195**, the conductive layer **212***a*, and the conductive layer **212***b*. For the insulating layer **150**, a material that can be used for the insulating layer **195** can be used. An opening reaching the conductive layer **104** is provided in the insulating layer **195** and the insulating layer **150**, and the conductive layer **116***a* is provided to cover the opening. Thus, the conductive layer **116***a* functioning as one of the source electrode and the drain electrode of the transistor **52**A and the conductive layer **204** functioning as the gate electrode of the transistor **52**B are electrically connected to each other. An insulating layer **210** is provided over the insulating layer **150** and the conductive layer **116***a*. For the insulating layer **210**, a material that can be used for the insulating layer **110** can be used. The insulating layer **210** preferably has a stacked-layer structure. FIG. **39** illustrates an example in which the insulating layer **210** has a stacked-layer structure of an insulating layer **210***a*, an insulating layer **210***b* over the insulating layer **210***a*, and an insulating layer **210***c* over the insulating layer **210***b*. The description of the insulating layer **110***a* can be referred to for the insulating layer **210***a*, the description of the insulating layer **110***b* can be referred to for the insulating layer **210***b*, and the description of the insulating layer **110***c* can be referred to for the insulating layer **210***c*. The conductive layer **116***b* is provided over the insulating layer **110**. The conductive layer **116***b* and the insulating layer **110** have an opening reaching the conductive layer **116***a*. The semiconductor layer **109** is provided to cover the opening. The insulating layer **107** is provided over the semiconductor layer **109**, and the conductive layer **203** is provided over the insulating layer **107**.

[0558] An insulating layer **199** is provided over the transistor **52**A. For the insulating layer **199**, a material that can be used for the insulating layer **195** can be used. The insulating layer **197** is provided over the insulating layer **199**.

[0559] An opening reaching the conductive layer **212***a* included in the transistor **52**B is provided in the insulating layer **150**, the insulating layer **210**, and the insulating layer **107**, and a conductive layer **206** is provided to cover the opening. The conductive layer **206** can be formed in the same step as the conductive layer **203**, for example. An opening reaching the conductive layer **206** is provided in the insulating layer **199** and the insulating layer **197**, and the pixel electrode **111** functioning as one electrode of the light-emitting device **61** is provided to cover the opening. Thus, the pixel electrode **111** functioning as one electrode of the light-emitting device **61** and the conductive layer **212***a* functioning as one of the source electrode and the drain electrode of the transistor **52**B are electrically connected through the conductive layer **206**. The conductive layer **212***a* is electrically connected to the conductive layer **112***b* included in the transistor **52**C.

[0560] FIG. **39** illustrates an example in which the insulating layer **150** is interposed between the conductive layer **116***a* functioning as one of the source electrode and the drain electrode of the transistor **52**A and the conductive layer **212***b* functioning as one of the source electrode and the drain electrode of the transistor **52**B, whereby the capacitor **53** is formed. Note that there is no particular limitation on the structure of the capacitor **53**.

<Structure Example of Display Apparatus>

[0561] FIG. **40** illustrates an example of cross sections of part of a region including the FPC **172**, part of the peripheral driver circuit **233**, part of the display portion **235**, part of the connection portion **140**, and part of a region including an end portion of the display apparatus **50**.

[0562] In the display apparatus **50**, transistors are provided over the substrate **102**; an insulating layer is provided over the transistors; a light-emitting device **130**R, a light-emitting device **130**G, and a light-emitting device **130**B are provided over the insulating layer; and a protective layer **131** is provided to cover these light-emitting devices. The substrate **152** is attached onto the protective layer **131** with an adhesive layer **142**.

[0563] Note that in the case of describing matters common to the light-emitting device **130**R, the light-emitting device **130**G, and the light-emitting device **130**B, these light-emitting devices are sometimes referred to as a light-emitting device **130** by omitting the alphabets that distinguish them from each other. In the same manner, in the description common to the components that are distinguished by alphabets, reference numerals without alphabets are sometimes used.

[0564] Transistors that control the light-emitting device **130**R, the light-emitting device **130**G, and the light-emitting device **130**B can be provided in the display portion **235**. FIG. **40** illustrates a transistor **205**R that controls the light-emitting device **130**R and a transistor **205**G that controls the light-emitting device **130**G. FIG. **40** also illustrates a transistor **201** provided in the peripheral driver circuit **233**. The transistor or the transistor group described in Embodiment 1 can be suitably used as each of the transistor **205**R, the transistor **205**G, and the transistor **201**. Note that FIG. **40** does not illustrate electrical connection between the transistors.

[0565] The transistor provided in the peripheral driver circuit **233** is sometimes required to have a higher on-state current than the transistor provided in the display portion **235**. The transistor provided in the peripheral driver circuit **233** preferably has a short channel length. For example, one or more of the transistor **100** to the transistor **100**C and the transistor group **100**D can be suitably used for the transistor provided in the peripheral driver circuit **233**. One or more of the transistor **200** to the transistor **200**H can be suitably used for the transistor provided in the display portion **235**. Note that one or more of the transistor **100** to the transistor **100**C and the transistor group **100**D may be used in the display portion **235**, and one or more of the transistor **200** to the transistor **200**H may be used in the peripheral driver circuit **233**.

[0566] A structure can be employed in which the light-emitting device **130**R emits red (R) light, the light-emitting device **130**G emits green (G) light, and the light-emitting device **130**B emits blue (B) light.

[0567] One of pair of electrodes included in the light-emitting device functions as an anode, and the other electrode functions as a cathode. The case where the pixel electrode functions as an anode and the common electrode functions as a cathode is described below as an example in some cases.

[0568] The light-emitting device **130**R includes a pixel electrode **111**R, an island-shaped layer **113**R over the pixel electrode **111**R, a common layer **114** over the island-shaped layer **113**R, and a common electrode **115** over the common layer **114**. In the light-emitting device **130**R, the layer **113**R and the common layer **114** can be collectively referred to as an EL layer.

[0569] The light-emitting device **130**G includes a pixel electrode **111**G, an island-shaped layer **113**G over the pixel electrode **111**G, the common layer **114** over the island-shaped layer **113**G, and the common electrode **115** over the common layer **114**. In the light-emitting device **130**G, the layer **113**G and the common layer **114** can be collectively referred to as an EL layer.

[0570] The light-emitting device **130**B includes a pixel electrode **111**B, an island-shaped layer **113**B over the pixel electrode **111**B, the common layer **114** over the island-shaped layer **113**B, and the common electrode **115** over the common layer **114**. In the light-emitting device **130**B, the layer **113**B and the common layer **114** can be collectively referred to as an EL layer.

[0571] In this specification and the like, in the EL layers included in the light-emitting devices, the island-shaped layer provided in each light-emitting device is referred to as the layer **113**B, the layer **113**G, or the layer **113**R, and the layer shared by the plurality of light-emitting devices is referred to as the common layer **114**. Note that in this specification and the like, the layer **113**R, the layer **113**G, and the layer **113**B are sometimes referred to as island-shaped EL layers, EL layers formed in an island shape, or the like, in which case the common layer **114** is not included.

[0572] The layer **113**R, the layer **113**G, and the layer **113**B are separated from one another. When the EL layer is provided in an island shape for each light-emitting device, a leakage current between adjacent light-emitting devices can be inhibited. This can prevent unintended light emission due to crosstalk, so that a display apparatus with extremely high contrast can be obtained. Specifically, a display apparatus having high current efficiency at low luminance can be obtained. Note that the layer **113**R, the layer **113**G, and the layer **113**B are hereinafter collectively referred as a layer **113** in some cases.

[0573] In FIG. **40**, an insulating layer (also referred to as an embankment, a partition wall, a bank, or a spacer) covering an end portion of the top surface of the pixel electrode **111**R is not provided between the pixel electrode **111**R and the layer **113**R. An insulating layer covering an end portion of the top surface of the pixel electrode **111**G is not provided between the pixel electrode **111**G and the layer **113**G. Thus, the distance between adjacent light-emitting devices can be extremely short. Accordingly, the display apparatus can have a high definition or a high resolution. In addition, a mask for forming the insulating layer is not needed, which leads to a reduction in manufacturing cost of the display apparatus. With a structure in which an insulating layer covering the end portion of the pixel electrode is not provided, light emitted from the EL layer can be extracted efficiently. Therefore, the display apparatus of one embodiment of the present invention can significantly reduce the viewing angle dependence.

[0574] The layer **113**R, the layer **113**G, and the layer **113**B each include at least a light-emitting layer. The layer **113**R includes a light-emitting layer emitting red light, the layer **113**G includes a light-emitting layer emitting green light, and the layer **113**B includes a light-emitting layer emitting blue light. In other words, the layer **113**R contains a light-emitting material emitting red light, the layer **113**G contains alight-emitting material emitting green light, and the layer **113**B contains a light-emitting material emitting blue light. The layer **113**R, the layer **113**G, and the layer **113**B may each include one or more of a hole-injection layer, a hole-transport layer, a hole-blocking layer, a charge-generation layer, an electron-blocking layer, an electron-transport layer, and an electron-injection layer.

[0575] As illustrated in FIG. **40**, an end portion of the layer **113**G is preferably positioned outward from an end portion of the pixel electrode **111**G. Note that although description is made using the pixel electrode **111**G and the layer **113**G as an example, the same applies to the pixel electrode **111**R and the layer **113**R, and the pixel electrode **111**B and the layer **113**B.

[0576] In FIG. **40**, the layer **113**G is formed to cover the end portion of the pixel electrode **111**G. Such a structure enables the entire top surface of the pixel electrode to be a light-emitting region, and the aperture ratio can be easily increased as compared with the structure in which the end portion of the island-shaped EL layer is positioned inward from the end portion of the pixel electrode.

[0577] Covering the side surface of the pixel electrode **111** with the EL layer can inhibit contact between the pixel electrode **111** and the common electrode **115**, thereby inhib-

iting a short circuit of the light-emitting device. Furthermore, the distance between the light-emitting region (i.e., the region overlapping with the pixel electrode) in the EL layer and the end portion of the EL layer can be increased. Since the end portion of the EL layer might be damaged by processing, the use of a region away from the end portion of the EL layer as a light-emitting region can improve the reliability of the light-emitting device in some cases.

[0578] Although FIG. **40** illustrates the layer **113**R, the layer **113**G, and the layer **113**B that have the same thickness, one embodiment of the present invention is not limited thereto. The layer **113**R, the layer **113**G, and the layer **113**B may have different thicknesses. For example, the thickness is preferably set to match an optical path length that intensifies light emitted from the layer **113**R, the layer **113**G, and the layer **113**B. A microcavity structure can be achieved in this manner, and the color purity of light from each light-emitting device can be increased.

[0579] The common layer **114** includes, for example, an electron-injection layer or a hole-injection layer. Alternatively, the common layer **114** may include a stack of an electron-transport layer and an electron-injection layer, or may include a stack of a hole-transport layer and a hole-injection layer. The common layer **114** is shared by the light-emitting device **130**R, the light-emitting device **130**G, and the light-emitting device **130**B.

[0580] The common electrode **115** is shared by the light-emitting device **130**R, the light-emitting device **130**G, and the light-emitting device **130**B. The common electrode **115** shared by the plurality of light-emitting devices is electrically connected to a conductive layer **123** provided in the connection portion **140**. The conductive layer **123** can be formed in the same step as the pixel electrode **111**R, the pixel electrode **111**G, and the pixel electrode **111**B.

[0581] The display apparatus **50** illustrated in FIG. **40** has a top-emission structure. Light emitted by the light-emitting device is emitted toward the substrate **152**. For the substrate **152**, a material having a high visible-light-transmitting property is preferably used. The pixel electrode **111** contains a material reflecting visible light, and the common electrode **115** contains a material transmitting visible light. In FIG. **40**, arrows with broken lines indicate light R, light G, and light B, which are emitted toward the substrate **152** from the light-emitting device **130**R, the light-emitting device **130**G, and the light-emitting device **130**B, respectively.

[0582] The protective layer **131** is provided over the light-emitting device **130**R, the light-emitting device **130**G, and the light-emitting device **130**B. The protective layer **131** and the substrate **152** are bonded to each other with the adhesive layer **142**. The substrate **152** is provided with a light-blocking layer **117**. A solid sealing structure, a hollow sealing structure, or the like can be employed to seal the light-emitting devices. In FIG. **40**, a solid sealing structure is employed in which a space between the substrate **152** and the substrate **101** is filled with the adhesive layer **142**. Alternatively, a hollow sealing structure may be employed, in which the space is filled with an inert gas (e.g., nitrogen or argon). Here, the adhesive layer **142** may be provided not to overlap with the light-emitting device. The space may be filled with a resin different from that of the frame-like adhesive layer **142**.

[0583] The protective layer **131** is preferably provided over the light-emitting device **130**R, the light-emitting device **130**G, and the light-emitting device **130**B. Provision of the protective layer **131** can inhibit oxidation of the common electrode **115** and entry of impurities (e.g., water and oxygen) into the light-emitting device. Accordingly, deterioration of the light-emitting device can be inhibited, and the reliability of the display apparatus can be increased. The protective layer **131** may have a single-layer structure or a stacked-layer structure including two or more layers. There is no limitation on the conductivity of the protective layer **131**. As the protective layer **131**, at least one of an insulating layer, a semiconductor layer, and a conductive layer can be used.

[0584] An inorganic substance can be used for the protective layer **131**. For example, one or more of an oxide, an oxynitride, a nitride oxide, and a nitride can be used for the protective layer **131**. Specific examples include silicon oxide, silicon oxynitride, silicon nitride oxide, silicon nitride, aluminum oxide, aluminum oxynitride, and hafnium oxide. In particular, the protective layer **131** preferably includes a nitride or a nitride oxide, and further preferably includes a nitride.

[0585] As the protective layer **131**, a layer containing In—Sn oxide (ITO), In—Zn oxide, Ga—Zn oxide, Al—Zn oxide, or In—Ga—Zn oxide (IGZO) can also be used. The layer preferably has high resistance, specifically, higher resistance than the common electrode **115**. The layer may further contain nitrogen.

[0586] When light emitted from the light-emitting device **130** is extracted through the protective layer **131**, the protective layer **131** preferably has a high visible-light-transmitting property. For example, In—Sn oxide, In—Ga—Zn oxide, and aluminum oxide are preferable because they have a high visible-light-transmitting property.

[0587] Furthermore, the protective layer **131** may include an organic film. For example, the protective layer **131** may include both an organic film and an inorganic film.

[0588] Examples of methods for forming the protective layer **131** include a vacuum evaporation method, a sputtering method, a CVD method, and an ALD method. The protective layer **131** may have a stacked-layer structure of layers which are formed by different film formation methods.

[0589] The protective layer **131** is provided at least in the display portion **235**, and preferably provided to cover the entire display portion **235**. The protective layer **131** is preferably provided to cover not only the display portion **235** but also the connection portion **140** and the peripheral driver circuit **233**. It is also preferable that the protective layer **131** be provided to extend to the end portion of the display apparatus **50**.

[0590] FIG. **41**A is an enlarged view of the light-emitting device **130**G, the transistor **205**G, and the vicinity thereof.

[0591] The pixel electrode **111**G included in the light-emitting device **130**G includes a conductive layer **124**G, a conductive layer **126**G over the conductive layer **124**G, and a conductive layer **129**G over the conductive layer **126**G.

[0592] The conductive layer **124**G is electrically connected to the conductive layer **212***a* included in the transistor **205**G through the opening provided in the insulating layer **199**, the insulating layer **197**, and an insulating layer **239**.

[0593] The end portion of the conductive layer **124**G is positioned outward from the end portion of the conductive layer **126**G. The end portion of the conductive layer **126**G is positioned inward from an end portion of the conductive layer **129**G. The end portion of the conductive layer **124**G is

positioned inward from the end portion of the conductive layer **129**G. In other words, the end portion of the conductive layer **126**G is positioned over the conductive layer **124**G. The end portion of the conductive layer **129**G is positioned over the conductive layer **124**G. The top surface and the side surface of the conductive layer **126**G are covered with the conductive layer **129**G.

[0594] For the conductive layer **124**G, no particular limitations are imposed on the properties of transmitting and reflecting visible light. As the conductive layer **124**G, a conductive layer having a visible-light-transmitting property or a conductive layer having a visible-light-reflecting property can be used. As the conductive layer having a visible-light-transmitting property, a conductive layer including an oxide conductor (also referred to as an oxide conductive layer) can be used, for example. Specifically, In—Si—Sn oxide (also referred to as ITSO) can be suitably used for the conductive layer **124**G. Examples of the conductive layer having a property of reflecting visible light include metal such as aluminum, titanium, chromium, nickel, copper, yttrium, zirconium, silver, tin, zinc, platinum, gold, molybdenum, tantalum, and tungsten, and an alloy containing the metal as its main component (e.g., an alloy of silver, palladium, and copper (APC: Ag—Pd—Cu)). The conductive layer **124**G may have a stacked-layer structure of a conductive layer having a visible-light-transmitting property and a conductive layer having visible-light-reflecting property over the conductive layer. For the conductive layer **124**G, a material with high adhesion to the formation surface of the conductive layer **124**G (here, the insulating layer **239**) is preferably used. Accordingly, film separation of the conductive layer **124**G can be inhibited.

[0595] As the conductive layer **126**G, a conductive layer having a visible-light-reflecting property can be used. The conductive layer **126**G may have a stacked-layer structure of a conductive layer having a visible-light-transmitting property and a conductive layer having a visible-light-reflecting property over the conductive layer. For the conductive layer **126**G, a material that can be used for the conductive layer **124**G can be used. Specifically, a stacked-layer structure of In—Si—Sn oxide (ITSO) and an alloy of silver, palladium, and copper (APC) over the In—Si—Sn oxide (ITSO) can be suitably used for the conductive layer **126**G.

[0596] For the conductive layer **129**G, a material that can be used for the conductive layer **124**G can be used. As the conductive layer **129**G, a conductive layer having a visible-light-transmitting property can be used. Specifically, In—Si—Sn oxide (ITSO) can be used for the conductive layer **129**G.

[0597] In the case where a material that is easily oxidized is used for the conductive layer **126**G, a material that is not easily oxidized is used for the conductive layer **129**G and the conductive layer **126**G is covered with the conductive layer **129**G, whereby oxidation of the conductive layer **126**G can be inhibited. In addition, precipitation of a metal component included in the conductive layer **126**G can be inhibited. For example, in the case where a material containing silver is used for the conductive layer **126**G, In—Si—Sn oxide (ITSO) can be suitably used for the conductive layer **129**G. Thus, oxidation of the conductive layer **126**G can be inhibited, and precipitation of silver can be inhibited.

[0598] The end portions of the conductive layer **129**G, the conductive layer **126**G, and the conductive layer **124**G may be aligned or substantially aligned with one another. The layer **113**G may be in contact with the side surface of the conductive layer **129**G, the side surface of the conductive layer **126**G, and the side surface of the conductive layer **124**G.

[0599] For example, a first conductive film to be the conductive layer **124**G, a layer **128**, a second conductive film to be the conductive layer **126**G, and a third conductive film to be the conductive layer **129**G are formed; after that, a resist mask is formed over the third conductive film, and the first conductive film, the second conductive film, and the third conductive film are processed using the resist mask, whereby the conductive layer **124**G, the conductive layer **126**G, and the conductive layer **129**G can be formed. The first conductive film, the second conductive film, and the third conductive film are processed in the same step to form the conductive layer **124**G, the conductive layer **126**G, and the conductive layer **129**G, whereby the process can be simplified.

[0600] Alternatively, the side surface of the conductive layer **124**G and the top surface and the side surface of the conductive layer **126**G may be covered with the conductive layer **129**G. The layer **113**G includes a region in contact with the top surface and the side surface of the conductive layer **129**G, and does not necessarily include a region in contact with the conductive layer **124**G and the conductive layer **126**G.

[0601] For example, the first conductive film to be the conductive layer **124**G and the second conductive film to be the conductive layer **126**G are formed; after that, a resist mask is formed over the second conductive film, and the first conductive film and the second conductive film are processed using the resist mask, whereby the conductive layer **124**G and the conductive layer **126**G are formed. After that, the third conductive film to be the conductive layer **129**G is formed to cover the conductive layer **124**G and the conductive layer **126**G, and the third conductive film is processed, whereby the conductive layer **129**G can be formed. The first conductive film and the second conductive film are processed in the same step to form the conductive layer **124**G and the conductive layer **126**G, whereby the process can be simplified. Even when a material that is easily diffused, such as silver, is used for the conductive layer **124**G or the conductive layer **126**G, diffusion can be inhibited by covering the top surfaces and the side surfaces of the conductive layer **124**G and the conductive layer **126**G with the conductive layer **129**G.

[0602] The pixel electrode **111**R in the light-emitting device **130**R and the pixel electrode **111**B in the light-emitting device **130**B can each have a structure similar to that of the pixel electrode **111**G.

[0603] Depressed portions are formed in the conductive layer **124**R, the conductive layer **124**G, and the conductive layer **124**B so as to cover the openings provided in the insulating layer **199**, the insulating layer **197**, the insulating layer **239**. The layer **128** is embedded in the depressed portions.

[0604] The layer **128** has a planarization function for the depressed portions of the conductive layer **124**R, the conductive layer **124**G, and the conductive layer **124**B. A conductive layer **126**R, the conductive layer **126**G, and a conductive layer **126**B electrically connected to the conductive layer **124**R, the conductive layer **124**G, and the conductive layer **124**B, respectively, are provided over the conductive layer **124**R, the conductive layer **124**G, the

conductive layer **124**B, and the layer **128**. Thus, regions overlapping with the depressed portions of the conductive layer **124**R, the conductive layer **124**G, and the conductive layer **124**B can also function as the light-emitting regions, increasing the aperture ratio of the pixels.

[0605] The layer **128** has a planarization function for the concave portions formed in the conductive layer **124**R, the conductive layer **124**G, and the conductive layer **124**B. Provision of the layer **128** can improve the planarity of the top surfaces of the pixel electrode **111**R, the pixel electrode **111**G, and the pixel electrode **111**B that are formation surfaces of the layer **113**R, the layer **113**G, and the layer **113**B, respectively.

[0606] The layer **128** may be an insulating layer or a conductive layer. Any of a variety of inorganic insulating materials, organic insulating materials, and conductive materials can be used for the layer **128** as appropriate.

[0607] As the layer **128**, an insulating layer including an organic material can be favorably used. As the organic material, a photosensitive organic resin is preferably used, and for example, a photosensitive resin composite containing an acrylic resin is preferably used. Note that in this specification and the like, an acrylic resin refers to not only a polymethacrylic acid ester or a methacrylic resin, but also all the acrylic-based polymers in a broad sense in some cases.

[0608] For the layer **128**, an acrylic resin, a polyimide resin, an epoxy resin, an imide resin, a polyamide resin, a polyimide-amide resin, a silicone resin, a siloxane resin, a benzocyclobutene-based resin, a phenol resin, precursors of these resins, or the like may be used. Alternatively, for an insulating layer **127**, an organic material such as polyvinyl alcohol (PVA), polyvinyl butyral, polyvinylpyrrolidone, polyethylene glycol, polyglycerin, pullulan, water-soluble cellulose, or an alcohol-soluble polyamide resin may be used. A photoresist may be used as the photosensitive resin. As the photosensitive organic resin, either a positive material or a negative material may be used.

[0609] When the layer **128** is a conductive layer, the layer **128** can function as part of a pixel electrode. For the layer **128**, for example, an organic resin in which metal particles are dispersed can be used.

[0610] Although FIG. **41**A and the like illustrate a structure where the top surface of the layer **128** has a shape in which the center and the vicinity thereof are bulged, i.e., a shape including a convex surface, in the cross-sectional view, the shape of the layer **128** is not particularly limited. The top surface of the layer **128** can have a shape in which its center and the vicinity thereof are depressed, i.e., a shape including a concave surface, in a cross-sectional view. The top surface of the layer **128** may include one or both of a convex surface and a concave surface. The number of convex surfaces and the number of concave surfaces included in the top surface of the layer **128** are not limited and can each be one or more.

[0611] The level of the top surface of the layer **128** and the level of the top surface of the conductive layer **124**G may be equal to or substantially equal to each other, or may be different from each other. For example, the level of the top surface of the layer **128** may be either lower or higher than the level of the top surface of the conductive layer **124**G.

[0612] FIG. **41**B is an enlarged view of the connection portion **140**. For example, the conductive layer **123** can have a stacked-layer structure of a conductive layer **124***p*, a conductive layer **126***p* over the conductive layer **124***p*, and a conductive layer **129***p* over the conductive layer **126***p*. The conductive layer **124***p* can be formed in the same step as the conductive layer **124**R, the conductive layer **124**G, and the conductive layer **124**B. The conductive layer **126***p* can be formed in the same step as the conductive layer **126**R, the conductive layer **126**G, and the conductive layer **126**B. The conductive layer **129***p* can be formed in the same step as a conductive layer **129**R, the conductive layer **129**G, and a conductive layer **129**B.

[0613] FIG. **41**B and the like illustrate an example in which the common layer **114** is not provided in the connection portion **140** and the common electrode **115** is provided over the conductive layer **123**. Note that an example in which the common layer **114** is provided over the conductive layer **123** and the conductive layer **123** and the common electrode **115** are electrically connected to each other through the common layer **114** may be employed. For example, by using a mask for specifying a film formation area (also referred to as an area mask, a rough metal mask, or the like to be distinguished from a fine metal mask), the common layer **114** and the common electrode **115** can be formed in different regions.

[0614] A connection portion **214** is provided in a region of the substrate **101** that does not overlap with the substrate **152**. In the connection portion **214**, the wiring **165** is electrically connected to the FPC **172** through a conductive layer **166** and a connection layer **242**. The conductive layer **166** is exposed from the top surface of the connection portion **214**. Thus, the connection portion **214** and the FPC **172** can be electrically connected to each other through the connection layer **242**. Note that FIG. **40** and the like illustrate a structure where the wiring **165** functions as a source electrode or a drain electrode of the transistor **201**. Note that the conductive layer **112***a* of the transistor **201** may be electrically connected to the FPC **172** through the conductive layer **166** and the connection layer **242**.

[0615] As the connection layer **242**, an anisotropic conductive film (ACF) or an anisotropic conductive paste (ACP) can be used, for example.

[0616] Note that the connection portion **214** has a portion not provided with the protective layer **131** so that the FPC **172** and the conductive layer **166** are electrically connected to each other. For example, the protective layer **131** is formed over the entire surface of the display apparatus **50** and then a region of the protective layer **131** overlapping with the conductive layer **166** is removed, so that the conductive layer **166** can be exposed.

[0617] FIG. **41**C is an enlarged view of the connection portion **214**. For example, the conductive layer **166** can have a stacked-layer structure of a conductive layer **124***q*, a conductive layer **126***q* over the conductive layer **124***q*, and a conductive layer **129***q* over the conductive layer **126***q*. The conductive layer **124***q* can be formed in the same step as the conductive layer **124**R, the conductive layer **124**G, and the conductive layer **124**B. The conductive layer **126***q* can be formed in the same step as the conductive layer **126**R, the conductive layer **126**G, and the conductive layer **126**B. The conductive layer **129***q* can be formed in the same step as the conductive layer **129**R, the conductive layer **129**G, and the conductive layer **129**B.

[0618] FIG. **40** and the like illustrate a structure where the thicknesses of the conductive layer **129***p* and the conductive layer **129***q* are different from the thicknesses of the conduc-

tive layer **129**R, the conductive layer **129**G, and the conductive layer **129**B. These thicknesses of the conductive layer **129***p*, the conductive layer **129***q*, the conductive layer **129**R, the conductive layer **129**G, and the conductive layer **129**B may be different depending on the resistivities of materials used for these layers. In the case of making the thicknesses different, the conductive layer **129***p* and the conductive layer **129***q* may be formed in a step different from a step of forming the conductive layer **129**R, the conductive layer **129**G, and the conductive layer **129**B. Alternatively, formation of the conductive layer **129***p* and the conductive layer **129***q* and formation of the conductive layer **129**R, the conductive layer **129**G, and the conductive layer **129**B may share some steps. Alternatively, the conductive layer **129***p* and the conductive layer **129***q* may have different thicknesses.

[0619] The pixel electrode **111**R, the pixel electrode **111**G, the pixel electrode **111**B, the conductive layer **123**, and the conductive layer **166** illustrated in FIG. **40** and the like can also be applied to other structure examples.

[0620] In a region between the adjacent light-emitting devices, an insulating layer **125** and the insulating layer **127** over the insulating layer **125** are provided. Although FIG. **40** illustrates a plurality of cross sections of the insulating layer **125** and the insulating layer **127**, the insulating layer **125** and the insulating layer **127** are each one continuous layer in a top view of the display apparatus **50**. In other words, the display apparatus **50** can have a structure including one insulating layer **125** and one insulating layer **127**, for example. Note that the display apparatus **50** may include a plurality of insulating layers **125** that are separated from each other, and may include a plurality of insulating layers **127** that are separated from each other.

[0621] A mask layer **118**R and a mask layer **119**R are positioned over the layer **113**R, a mask layer **118**G and a mask layer **119**G are positioned over the layer **113**G, and a mask layer **118**B and a mask layer **119**B are positioned over the layer **113**B. The mask layer **118**R, the mask layer **119**R, the mask layer **118**G, the mask layer **119**G, the mask layer **118**B, and the mask layer **119**B have openings in portions overlapping with the light-emitting region. The mask layer **118**R and the mask layer **119**R are remaining parts of the mask layers provided in contact with the top surface of the layer **113**R at the time of processing the layer **113**R. In a similar manner, the mask layer **118**G and the mask layer **119**G are remaining parts of the mask layers provided at the time of forming the layer **113**G, and the mask layer **118**B and the mask layer **119**B are remaining parts of the mask layers provided at the time of forming the layer **113**B. Thus, the mask layer used to protect the EL layer in manufacture of the display apparatus may partly remain in the display apparatus of one embodiment of the present invention. For any two or all of the mask layer **118**R, the mask layer **118**G, and the mask layer **118**B, the same material may be used or different materials may be used. For any two or all of the mask layer **119**R, the mask layer **119**G, and the mask layer **119**B, the same material may be used or different materials may be used. Note that in the following description, in some cases, the mask layer **118**R, the mask layer **118**G, and the mask layer **118**B are collectively referred to as a mask layer **118**, and the mask layer **119**R, the mask layer **119**G, and the mask layer **119**B are collectively referred to as a mask layer **119**.

[0622] As each of the mask layer **118** and the mask layer **119**, it is possible to use one or more of a metal film, an alloy film, a metal oxide film, a semiconductor film, an organic insulating film, and an inorganic insulating film, for example.

[0623] For each of the mask layer **118** and the mask layer **119**, it is possible to use a metal material such as gold, silver, platinum, magnesium, nickel, tungsten, chromium, molybdenum, iron, cobalt, copper, palladium, titanium, aluminum, yttrium, zirconium, or tantalum or an alloy material containing any of the metal materials, for example. It is particularly preferable to use a low-melting-point material such as aluminum or silver. When a metal material capable of blocking ultraviolet rays is used for one or both of the mask layer **118** and the mask layer **119**, the layer **113** can be inhibited from being irradiated with ultraviolet rays and deterioration of the layer **113** can be inhibited.

[0624] As each of the mask layer **118** and the mask layer **119**, a metal oxide can be used. Examples of the metal oxide include In—Ga—Zn oxide, indium oxide, In—Zn oxide, In—Sn oxide, indium titanium oxide (In—Ti oxide), indium tin zinc oxide (In—Sn—Zn oxide), indium titanium zinc oxide (In—Ti—Zn oxide), indium gallium tin zinc oxide (In—Ga—Sn—Zn oxide), and indium tin oxide containing silicon.

[0625] Different materials can be used for the mask layer **118** and the mask layer **119**. Note that a structure in which the mask layer **119** is not provided may be employed.

[0626] As illustrated in FIG. **40**, one end portion of the mask layer **118**R and one end portion of the mask layer **119**R (outer end portions which are opposite to the light-emitting region side) are aligned or substantially aligned with the end portion of the layer **113**R, and the other end portion of the mask layer **118**R and the other end portion of the mask layer **119**R are positioned over the layer **113**R. Here, the other end portion of the mask layer **118**R and the other end portion of the mask layer **119**R (inner end portions which are on the light-emitting region side) preferably overlap with the layer **113**R and the pixel electrode **111**R. In this case, the other end portion of the mask layer **118**R and the other end portion of the mask layer **119**R are easily formed over a substantially flat surface of the layer **113**R. Note that the same applies to the mask layer **118**G, the mask layer **118**B, the mask layer **118**G, and the mask layer **119**G. The mask layer **118** and the mask layer **118** remain between the top surface of the EL layer processed into an island shape (the layer **113**R, the layer **113**G, or the layer **113**B) and the insulating layer **125**.

[0627] In the case where end portions are aligned or substantially aligned with each other and the case where top surface shapes are the same or substantially the same, it can be said that outlines of stacked layers at least partly overlap with each other in a top view. For example, the case of processing the upper layer and the lower layer with use of the same mask pattern or mask patterns that are partly the same is included. Note that, in some cases, the outlines do not completely overlap with each other and the upper layer is positioned inward from the lower layer or the upper layer is positioned outward from the lower layer; such cases are also represented by the expression "end portions are substantially aligned with each other" or the expression "top surface shapes are substantially the same".

[0628] The side surfaces of the layer **113**R, the layer **113**G, and the layer **113**B are each covered with the insulating layer **125**. The insulating layer **127** overlaps with the side surfaces of the layer **113**R, the layer **113**G, and the layer **113**B with the insulating layer **125** therebetween.

[0629] The side surface and part of the top surface of each of the layer **113**R, the layer **113**G, and the layer **113**B are covered with at least one of the insulating layer **125**, the insulating layer **127**, the mask layer **118**, and the mask layer **119**, so that the common layer **114** (or the common electrode **115**) can be inhibited from being in contact with the side surfaces of the pixel electrode **111**R, the pixel electrode **111**G, the pixel electrode **111**B, the layer **113**R, the layer **113**G, and the layer **113**B, leading to inhibition of a short circuit of the light-emitting device. Accordingly, the reliability of the light-emitting device can be improved.

[0630] The insulating layer **125** is preferably in contact with the side surfaces of the layer **113**R, the layer **113**G, and the layer **113**B. The insulating layer **125** is configured to be in contact with the layer **113**R, the layer **113**G, and the layer **113**B, whereby film separation of the layer **113**R, the layer **113**G, and the layer **113**B can be prevented. When the insulating layer is in close contact with the layer **113**B, the layer **113**G, or the layer **113**R, the layer **113**B and the like that are adjacent each other can be fixed or bonded to each other by the insulating layer. Accordingly, the reliability of the light-emitting device can be improved. The manufacturing yield of the light-emitting device can also be improved.

[0631] Note that the insulating layer **125** and the insulating layer **127** may cover the side surface and part of the top surface of each of the layer **113**R, the layer **113**G, and the layer **113**B. With such a structure, film separation of the EL layers can further be prevented and the reliability of the light-emitting device can be improved. The manufacturing yield of the light-emitting device can also be improved.

[0632] The insulating layer **127** is provided over the insulating layer **125** to fill a depressed portion defined by the insulating layer **125**. The insulating layer **127** can be configured to overlap with the side surface and part of the top surface of each of the layer **113**R, the layer **113**G, and the layer **113**B with the insulating layer **125** therebetween. The insulating layer **127** preferably covers at least part of the side surface of the insulating layer **125**.

[0633] The insulating layer **125** and the insulating layer **127** can fill a space between adjacent island-shaped layers, whereby the formation surface of the layers (e.g., the carrier-injection layer and the common electrode) provided over the island-shaped layers can have higher flatness with a small level of unevenness. Consequently, coverage with the carrier-injection layer, the common electrode, and the like can be improved.

[0634] The common layer **114** and the common electrode **115** are provided over the layer **113**R, the layer **113**G, the layer **113**B, the mask layer **118**, the mask layer **119**, the insulating layer **125**, and the insulating layer **127**. Before the insulating layer **125** and the insulating layer **127** are provided, a step is generated due to a difference between a region where the pixel electrode and the island-shaped EL layer are provided and a region where neither the pixel electrode nor the island-shaped EL layer is provided (region between the light-emitting devices). In the display apparatus of one embodiment of the present invention, the step can be reduced with the insulating layer **125** and the insulating layer **127**, and the coverage with the common layer **114** and the common electrode **115** can be improved. Thus, connection defects caused by step disconnection can be inhibited. In addition, an increase in electric resistance, which is caused by local thinning of the common electrode **115** due to the step, can be inhibited.

[0635] The top surface of the insulating layer **127** preferably has a shape with higher flatness, but may include a projection portion, a convex surface, a concave surface, or a depressed portion. For example, the top surface of the insulating layer **127** preferably has a convex shape with a large radius of curvature.

[0636] The insulating layer **125** can be an insulating layer including an inorganic material. As the insulating layer **125**, an inorganic insulating film such as an oxide insulating film, a nitride insulating film, an oxynitride insulating film, or a nitride oxide insulating film can be used, for example. The insulating layer **125** may have a single-layer structure or a stacked-layer structure. Examples of the oxide insulating film include a silicon oxide film, an aluminum oxide film, a magnesium oxide film, an indium-gallium-zinc oxide film, a gallium oxide film, a germanium oxide film, an yttrium oxide film, a zirconium oxide film, a lanthanum oxide film, a neodymium oxide film, a hafnium oxide film, and a tantalum oxide film. Examples of the nitride insulating film include a silicon nitride film and an aluminum nitride film. Examples of the oxynitride insulating film include a silicon oxynitride film and an aluminum oxynitride film. Examples of the nitride oxide insulating film include a silicon nitride oxide film and an aluminum nitride oxide film. In particular, aluminum oxide is preferable because it has high selectivity with respect to the EL layer in etching and has a function of protecting the EL layer in forming the insulating layer **127** which is to be described later. In particular, when an inorganic insulating film such as an aluminum oxide film, a hafnium oxide film, or a silicon oxide film formed by an atomic layer deposition (ALD) method is used as the insulating layer **125**, the insulating layer **125** having few pinholes and an excellent function of protecting the EL layer can be formed. The insulating layer **125** may have a stacked-layer structure of a film formed by an ALD method and a film formed by a sputtering method. The insulating layer **125** may have a stacked-layer structure of an aluminum oxide film formed by an ALD method and a silicon nitride film formed by a sputtering method, for example.

[0637] The insulating layer **125** preferably has a function of a barrier insulating layer against at least one of water and oxygen. Alternatively, the insulating layer **125** preferably has a function of inhibiting diffusion of at least one of water and oxygen. Alternatively, the insulating layer **125** preferably has a function of capturing or fixing (also referred to as gettering) at least one of water and oxygen.

[0638] Note that in this specification and the like, a barrier insulating layer refers to an insulating layer having a barrier property. A barrier property in this specification and the like means a function of inhibiting diffusion of a targeted substance (also referred to as having low permeability). Alternatively, a barrier property refers to a function of capturing or fixing (also referred to as gettering) a targeted substance.

[0639] When the insulating layer **125** has a function of a barrier insulating layer or a gettering function, entry of impurities (typically, at least one of water and oxygen) that would diffuse into the light-emitting devices from the outside can be inhibited. With this structure, a highly reliable light-emitting device and a highly reliable display apparatus can be provided.

[0640] The insulating layer **125** preferably has a low impurity concentration. Accordingly, degradation of the EL layer, which is caused by entry of impurities into the EL layer from the insulating layer **125**, can be inhibited. In

addition, when the impurity concentration is reduced in the insulating layer **125**, a barrier property against at least one of water and oxygen can be increased. For example, the insulating layer **125** preferably has one of a sufficiently low hydrogen concentration and a sufficiently low carbon concentration, desirably has both of them.

[0641] The insulating layer **127** provided over the insulating layer **125** has a planarization function for unevenness with a large level difference on the insulating layer **125** formed between adjacent light-emitting devices. In other words, the insulating layer **127** has an effect of improving the flatness of the formation surface of the common electrode **115**.

[0642] For the insulating layer **127**, a material that can be used for the layer **128** can be used.

[0643] For the insulating layer **127**, a material absorbing visible light may be used. When the insulating layer **127** absorbs light from the light-emitting device, leakage of light (stray light) from the light-emitting device to the adjacent light-emitting device through the insulating layer **127** can be inhibited. Thus, the display quality of the display apparatus can be improved. Since no polarizing plate is required to improve the display quality, the weight and thickness of the display apparatus can be reduced.

[0644] Examples of the material absorbing visible light include materials containing pigment of black or the like, materials containing dye, light-absorbing resin materials (e.g., polyimide), and resin materials that can be used for color filters (color filter materials). Using a resin material obtained by stacking or mixing color filter materials of two colors or three or more colors is particularly preferred, in which case the effect of blocking visible light can be enhanced. In particular, mixing color filter materials of three or more colors enables the formation of a black or nearly black resin layer.

[0645] The insulating layer **239** is provided over the insulating layer **197** and can function as an etching protective film when the layer **113**, the mask layer **118**, and the mask layer **119** are formed. Provision of the insulating layer **239** can prevent generation of unevenness in the insulating layer **197** caused by etching of part of the insulating layer **197** at the time when the layer **113**, the mask layer **118**, and the mask layer **119** are formed. Thus, steps in the formation surface of the insulating layer **125** become small, whereby the coverage with the insulating layer **125** can be increased. Consequently, the side surface of the layer **113** is covered with the insulating layer **125**, which inhibits film separation of the layer **113**.

[0646] The insulating layer **239** can be an insulating layer including an inorganic material. As the insulating layer **239**, an inorganic insulating film such as an oxide insulating film, a nitride insulating film, an oxynitride insulating film, or a nitride oxide insulating film can be used, for example. The insulating layer **239** may have a single-layer structure or a stacked-layer structure. Examples of the oxide insulating film include a silicon oxide film, an aluminum oxide film, a magnesium oxide film, an indium gallium zinc oxide film, a gallium oxide film, a germanium oxide film, an yttrium oxide film, a zirconium oxide film, a lanthanum oxide film, a neodymium oxide film, a hafnium oxide film, and a tantalum oxide film. Examples of the nitride insulating film include a silicon nitride film and an aluminum nitride film. Examples of the oxynitride insulating film include a silicon oxynitride film and an aluminum oxynitride film. Examples of the nitride oxide insulating film include a silicon nitride oxide film and an aluminum nitride oxide film. A silicon oxide film or a silicon oxynitride film can be suitably used as the insulating layer **239**, for example.

[0647] For the insulating layer **239**, it is preferable to select a material having a high etching rate (also referred to as high selectivity) with respect to films to be the layer **113**, the mask layer **118**, and the mask layer **119** in etching of the films.

[0648] Here, the low flatness of the formation surface of the light-emitting device **130** might cause a defect such as a connection defect due to disconnection of the common electrode **115** or an increase in electric resistance due to the locally thinned regions of the common electrode **115**. In addition, the processing accuracy of the layer to be formed over the formation surface might be lowered.

[0649] In the display apparatus of one embodiment of the present invention, by providing the insulating layer **239**, the formation surface of the light-emitting device **130** can be flat. Accordingly, the processing accuracy of the light-emitting device **130** and the like provided over the insulating layer **239** is increased, whereby the display apparatus can have high definition. Furthermore, since a connection defect due to disconnection of the common electrode **115** and an increase in electric resistance due to the locally thinned regions of the common electrode **115** can be prevented, the display apparatus can have high display quality.

[0650] In the region that does not overlap with any of the layer **113**R, the layer **113**G, and the layer **113**B, part of the insulating layer **239** may be removed. The thickness of the insulating layer **239** in the region that does not overlap with any of the layer **113**R, the layer **113**G, and the layer **113**B may be smaller than the thickness of the insulating layer **239** in the region that overlaps with the layer **113**R, the layer **113**G, or the layer **113**B.

[0651] Although the insulating layer **239** has a single-layer structure in FIG. **40** and the like, one embodiment of the present invention is not limited thereto. The insulating layer **239** may have a stacked-layer structure. Note that a structure in which the insulating layer **239** is not provided may be employed.

[0652] Note that the insulating layer **239** can be applied to other structure examples.

[0653] FIG. **42** illustrates a structure example of a bottom-emission display apparatus. In a display apparatus **50**A illustrated in FIG. **42**, light emitted by the light-emitting device **130** is emitted toward the substrate **102**. For the substrate **102**, a material having a high visible-light-transmitting property is preferably used. In contrast, there is no limitation on the light-transmitting property of a material used for the substrate **152**.

[0654] The light-blocking layer **117** is preferably formed between the substrate **102** and each of the transistor **201**, the transistor **205**R, and the transistor **205**G. FIG. **42** illustrates an example in which the light-blocking layer **117** is provided over the substrate **102**, an insulating layer **153** is provided over the light-blocking layer **117**, and the transistor **201**, the transistor **205**R, and the transistor **205**G are provided over the insulating layer **153**.

[0655] A material having a high visible-light-transmitting property is used for each of the layers included in the pixel electrode **111**. A material reflecting visible light is preferably used for the common electrode **115**.

<Pixel Layout>

[0656] Pixel layouts different from that in FIG. **35**A will be mainly described with reference to FIG. **43**A to FIG. **43**G and FIG. **44**A to FIG. **44**K. There is no particular limitation on the arrangement of subpixels, and any of a variety of pixel layouts can be employed. Examples of the arrangement of subpixels include stripe arrangement, S-stripe arrangement, matrix arrangement, delta arrangement, Bayer arrangement, and PenTile arrangement.

[0657] The top surface shapes of the subpixels illustrated in FIG. **35**A, FIG. **43**A to FIG. **43**G, and FIG. **44**A to FIG. **44**K correspond to the top surface shapes of the light-emitting regions of the light-emitting devices.

[0658] Examples of a top surface shape of the subpixel include polygons such as a triangle, a tetragon (including a rectangle and a square), and a pentagon; polygons with rounded corners; an ellipse; and a circle.

[0659] The pixel circuit **51** included in the subpixel (the pixel **230**) may be placed to overlap with a light-emitting region or may be placed outside the light-emitting region.

[0660] The pixel **240** illustrated in FIG. **43**A employs S-stripe arrangement. The pixel **240** illustrated in FIG. **43**A is composed of three types of subpixels that are the pixel **230***a*, the pixel **230***b*, and the pixel **230***c*.

[0661] The pixel **240** illustrated in FIG. **43**B includes the pixel **230***a* whose top surface has a rough trapezoidal shape with rounded corners, the pixel **230***b* whose top surface has a rough triangle shape with rounded corners, and the pixel **230***c* whose top surface has a rough tetragonal or rough hexagonal shape with rounded corners. The pixel **230***b* has a larger light-emitting area than the pixel **230***a*. In this manner, the shapes and sizes of the subpixels can be determined independently. For example, the size of a subpixel including a light-emitting device with higher reliability can be smaller.

[0662] A pixel **240**A and a pixel **240**B illustrated in FIG. **43**C employ PenTile arrangement. FIG. **43**C illustrates an example in which the pixels **240**A including the pixel **230***a* and the pixel **230***b* and the pixels **240**B including the pixel **230***b* and the pixel **230***c* are alternately arranged.

[0663] The pixel **240**A and the pixel **240**B illustrated in FIG. **43**D to FIG. **43**F employ delta arrangement. The pixel **240**A includes two subpixels (the pixel **230***a* and the pixel **230***b*) in the upper row (first row) and one subpixel (the pixel **230***c*) in the lower row (second row). The pixel **240**B includes one subpixel (the pixel **230***c*) in the upper row (first row) and two subpixels (the pixel **230***a* and the pixel **230***b*) in the lower row (second row).

[0664] FIG. **43**D illustrates an example in which each subpixel has a rough tetragonal top surface shape with rounded corners, FIG. **43**E illustrates an example in which each subpixel has a circular top surface shape, and FIG. **43**F illustrates an example in which each subpixel has a rough hexagonal top surface shape with rounded corners.

[0665] In FIG. **43**F, subpixels are placed in respective hexagonal regions that are arranged densely. Focusing on one of the subpixels, the subpixel is placed so as to be surrounded by six subpixels. The subpixels are arranged such that subpixels that emit light of the same color are not adjacent to each other. For example, focusing on the pixel **230***a*, three pixels **230***b* and three pixels **230***c* are arranged to surround the pixel **230***a*, so that the pixel **230***a*, the pixel **230***b*, and the pixel **230***c* are alternately arranged.

[0666] FIG. **43**G illustrates an example in which subpixels of different colors are arranged in a zigzag manner. Specifically, the positions of the top sides of two subpixels arranged in the row direction (e.g., the pixel **230***a* and the pixel **230***b* or the pixel **230***b* and the pixel **230***c*) are not aligned in a top view.

[0667] For example, in each pixel illustrated in FIG. **43**A to FIG. **43**G, it is preferable that the pixel **230***a* be a subpixel R emitting red light, the pixel **230***b* be a subpixel G emitting green light, and the pixel **230***c* be a subpixel B emitting blue light. Note that the structure of the subpixels is not limited to this, and the colors and arrangement order of the subpixels can be determined as appropriate. For example, the pixel **230***b* may be the subpixel R emitting red light and the pixel **230***a* may be the subpixel G emitting green light.

[0668] In a photolithography method, as a pattern to be processed becomes finer, the influence of light diffraction becomes more difficult to ignore; therefore, the fidelity in transferring a photomask pattern by light exposure is degraded, and it becomes difficult to process a resist mask into a desired shape. Thus, a pattern with rounded corners is likely to be formed even with a rectangular photomask pattern. Consequently, the top surface of a subpixel has a polygonal shape with rounded corners, an elliptical shape, a circular shape, or the like, in some cases.

[0669] In the case where the EL layer is processed into an island shape using a resist mask, a resist film formed over the EL layer needs to be cured at a temperature lower than the upper temperature limit of the EL layer. Therefore, the resist film is insufficiently cured in some cases depending on the upper temperature limit of the material of the EL layer and the curing temperature of the resist material. An insufficiently cured resist film may have a shape different from a desired shape after being processed. As a result, the top surface of the EL layer may have a polygonal shape with rounded corners, an elliptical shape, a circular shape, or the like. For example, when a resist mask whose top surface has a square shape is intended to be formed, a resist mask whose top surface has a circular shape may be formed, and the top surface of the EL layer may have a circular shape.

[0670] Note that to obtain a desired top surface shape of the EL layer, a technique of correcting a mask pattern in advance so that a transferred pattern agrees with a design pattern (OPC (Optical Proximity Correction) technique) may be used. Specifically, with the OPC technique, a pattern for correction is added to a corner portion or the like of a figure on a mask pattern.

[0671] As illustrated in FIG. **44**A to FIG. **44**I, the pixel can include four types of subpixels.

[0672] The pixels **240** illustrated in FIG. **44**A to FIG. **44**C employ stripe arrangement.

[0673] FIG. **44**A illustrates an example in which each subpixel has a rectangular top surface shape, FIG. **44**B illustrates an example in which each subpixel has a top surface shape formed by combining two half circles and a rectangle, and FIG. **44**C illustrates an example in which each subpixel has an elliptical top surface shape.

[0674] The pixels **240** illustrated in FIG. **44**D to FIG. **44**F employ matrix arrangement.

[0675] FIG. **44**D illustrates an example in which each subpixel has a square top surface shape, FIG. **44**E illustrates an example in which each subpixel has a rough square top

surface shape with rounded corners, and FIG. **44**F illustrates an example in which each subpixel has a circular top surface shape.

[0676] FIG. **44**G and FIG. **44**H each illustrate an example in which one pixel **240** is composed of subpixels arranged in two rows and three columns.

[0677] The pixel **240** illustrated in FIG. **44**G includes three subpixels (the pixel **230***a*, the pixel **230***b*, and the pixel **230***c*) in the upper row (first row) of the pixel **240** and one subpixel (a pixel **230***d*) in the lower row (second row) thereof. In other words, the pixel **240** includes the pixel **230***a* in the left column (first column), the pixel **230***b* in the center column (second column), the pixel **230***c* in the right column (third column), and the pixel **230***d* across these three columns.

[0678] The pixel **240** illustrated in FIG. **44**H includes three subpixels (the pixel **230***a*, the pixel **230***b*, and the pixel **230***c*) in the upper row (first row) and three pixels **230***d* in the lower row (second row). In other words, the pixel **240** includes the pixel **230***a* and the pixel **230***d* in the left column (first column) of the pixel **240**, the pixel **230***b* and the pixel **230***d* in the center column (second column) thereof, and the pixel **230***c* and the pixel **230***d* in the right column (third column) thereof. Matching the positions of the subpixels in the upper row and the lower row as illustrated in FIG. **44**H enables efficient removal of dust and the like that would be produced in the manufacturing process. Thus, a display apparatus with high display quality can be provided.

[0679] FIG. **44**I illustrates an example in which one pixel **240** is composed of subpixels arranged in three rows and two columns.

[0680] The pixel **240** illustrated in FIG. **44**I includes the pixel **230***a* in the upper row (first row) of the pixel **240**, the pixel **230***b* in the center row (second row) thereof, the pixel **230***c* across the first row and the second row, and one subpixel (the pixel **230***d*) in the lower row (third row) thereof. In other words, the pixel **240** includes the pixel **230***a* and the pixel **230***b* in the left column (first column) of the pixel **240**, the pixel **230***c* in the right column (second column) thereof, and the pixel **230***d* across these two columns thereof.

[0681] The pixels **240** illustrated in FIG. **44**A to FIG. **44**I are each composed of four subpixels: the pixel **230***a*, the pixel **230***b*, the pixel **230***c*, and the pixel **230***d*.

[0682] The pixel **230***a*, the pixel **230***b*, the pixel **230***c*, and the pixel **230***d* can include light-emitting devices whose emission colors are different. The pixel **230***a*, the pixel **230***b*, the pixel **230***c*, and the pixel **230***d* are subpixels of four colors of R, G, B, and white (W), subpixels of four colors of R, G, B, and Y, or subpixels of R, G, B, and infrared light (IR).

[0683] In the pixels **240** illustrated in FIG. **44**A to FIG. **44**I, the pixel **230***a* may be the subpixel R emitting red light, the pixel **230***b* may be the subpixel G emitting green light, the pixel **230***c* may be the subpixel B emitting blue light, and the pixel **230***d* may be any of a subpixel W emitting white light, a subpixel Y emitting yellow light, and a subpixel IR emitting near-infrared light, for example. In the case of such a structure, stripe arrangement is employed as the layout of R, G, and B in the pixels **240** illustrated in FIG. **44**G and FIG. **44**H, leading to higher display quality. In addition, what is called S-stripe arrangement is employed as the layout of R, G, and B in the pixel **240** illustrated in FIG. **44**I, leading to higher display quality.

[0684] Note that the pixel **240** may include a subpixel including a light-receiving device.

[0685] In the pixels **240** illustrated in FIG. **44**A to FIG. **44**I, any one of the pixel **230***a* to the pixel **230***d* may be a subpixel including a light-receiving device.

[0686] In the pixels **240** illustrated in FIG. **44**A to FIG. **44**I, the pixel **230***a* may be the subpixel R emitting red light, the pixel **230***b* may be the subpixel G emitting green light, the pixel **230***c* may be the subpixel B emitting blue light, and the pixel **230***d* may be a subpixel S including a light-receiving device, for example. In the case of such a structure, stripe arrangement is employed as the layout of R, G, and B in the pixels **240** illustrated in FIG. **44**G and FIG. **44**H, leading to higher display quality. In addition, what is called S-stripe arrangement is employed as the layout of R, G, and B in the pixel **240** illustrated in FIG. **44**I, leading to higher display quality.

[0687] There is no particular limitation on the wavelength of light detected by the subpixel S including a light-receiving device. The subpixel S can have a structure in which one or both of visible light and infrared light are detected.

[0688] As illustrated in FIG. **44**J and FIG. **44**K, one pixel **240** may include five types of subpixels.

[0689] FIG. **44**J illustrates an example in which one pixel **240** is composed of subpixels arranged in two rows and three columns.

[0690] The pixel **240** illustrated in FIG. **44**J includes three subpixels (the pixel **230***a*, the pixel **230***b*, and the pixel **230***c*) in the upper row (first row) of the pixel **240** and two subpixels (the pixel **230***d* and a pixel **230***e*) in the lower row (second row) thereof. In other words, the pixel **240** includes the pixel **230***a* and the pixel **230***d* in the left column (first column) of the pixel **240**, the pixel **230***b* in the center column (second column) thereof, the pixel **230***c* in the right column (third column) thereof, and the pixel **230***e* across the second column and the third column thereof.

[0691] FIG. **44**K illustrates an example in which one pixel **240** is composed of subpixels arranged in three rows and two columns.

[0692] The pixel **240** illustrated in FIG. **44**K includes the pixel **230***a* in the upper row (first row) of the pixel **240**, the pixel **230***b* in the center row (second row) thereof, the pixel **230***c* across the first row and the second row, and two subpixels (the pixel **230***d* and the pixel **230***e*) in the lower row (third row) thereof. In other words, the pixel **240** includes the pixel **230***a*, the pixel **230***b*, and the pixel **230***d* in the left column (first column) and the pixel **230***c* and the pixel **230***e* in the right column (second column).

[0693] In the pixels **240** illustrated in FIG. **44**J and FIG. **44**K, it is preferable that the pixel **230***a* be the subpixel R emitting red light, the pixel **230***b* be the subpixel G emitting green light, and the pixel **230***c* be the subpixel B emitting blue light, for example. In the case of such a structure, stripe arrangement is employed as the layout of subpixels in the pixels **240** illustrated in FIG. **44**J, leading to higher display quality. In addition, what is called S-stripe arrangement is employed as the layout of subpixels in the pixel **240** illustrated in FIG. **44**K, leading to higher display quality.

[0694] In the pixels **240** illustrated in FIG. **44**J and FIG. **44**K, for example, the subpixel S including a light-receiving device may be used as at least one of the pixel **230***d* and the pixel **230***e*. In the case where light-receiving devices are used in both the pixel **230***d* and the pixel **230***e*, the light-receiving devices may have different structures. For

example, the wavelength ranges of detected light may be different at least partly. Specifically, one of the pixel **230***d* and the pixel **230***e* may include a light-receiving device mainly detecting visible light and the other may include a light-receiving device mainly detecting infrared light.

[0695] In the pixels **240** illustrated in FIG. **44**J and FIG. **44**K, for example, the subpixel S including a light-receiving device may be used as one of the pixel **230***d* and the pixel **230***e* and a subpixel including a light-emitting device that can be used as a light source may be used as the other. For example, one of the pixel **230***d* and the pixel **230***e* may be the subpixel IR emitting infrared light and the other may be the subpixel S including a light-receiving device detecting infrared light.

[0696] In a pixel including the subpixels R, G, B, IR, and S, while an image is displayed using the subpixels R, G, and B, reflected light of infrared light emitted by the subpixel IR that is used as a light source can be detected by the subpixel S.

[0697] As described above, in the display apparatus of one embodiment of the present invention, various layouts of the subpixels (the pixels **230**) can be employed for the pixel **240**. Furthermore, the pixel **240** may be configured to include both a light-emitting device and a light-receiving device. Also in this case, any of various layouts can be employed.

[0698] The structure described in this embodiment can be used in an appropriate combination with any of the structures described in the other embodiments.

Embodiment 3

[0699] In this embodiment, a light-emitting device that can be used as the light-emitting device **61** is described.

[0700] As illustrated in FIG. **45**A, the light-emitting device includes an EL layer **763** between a pair of electrodes (a lower electrode **761** and an upper electrode **762**). The EL layer **763** can be formed with a plurality of layers such as a layer **780**, a light-emitting layer **771**, and a layer **790**.

[0701] The light-emitting layer **771** includes at least a light-emitting substance (also referred to as a light-emitting material).

[0702] In the case where the lower electrode **761** is an anode and the upper electrode **762** is a cathode, the layer **780** includes one or more of a layer including a substance having a high hole-injection property (hole-injection layer), a layer including a substance having a high hole-transport property (hole-transport layer), and a layer including a substance having a high electron-blocking property (electron-blocking layer). Furthermore, the layer **790** includes one or more of a layer including a substance having a high electron-injection property (electron-injection layer), a layer including a substance having a high electron-transport property (electron-transport layer), and a layer including a substance having a high hole-blocking property (hole-blocking layer). In the case where the lower electrode **761** is a cathode and the upper electrode **762** is an anode, the structures of the layer **780** and the layer **790** are interchanged.

[0703] The structure including the layer **780**, the light-emitting layer **771**, and the layer **790**, which is provided between the pair of electrodes, can function as a single light-emitting unit, and the structure in FIG. **45**A is referred to as a single structure in this specification.

[0704] FIG. **45**B is a variation example of the EL layer **763** included in the light-emitting device illustrated in FIG. **45**A. Specifically, the light-emitting device illustrated in FIG. **45**B includes a layer **781** over the lower electrode **761**, a layer **782** over the layer **781**, the light-emitting layer **771** over the layer **782**, a layer **791** over the light-emitting layer **771**, a layer **792** over the layer **791**, and the upper electrode **762** over the layer **792**.

[0705] In the case where the lower electrode **761** is an anode and the upper electrode **762** is a cathode, the layer **781** can be a hole-injection layer, the layer **782** can be a hole-transport layer, the layer **791** can be an electron-transport layer, and the layer **792** can be an electron-injection layer, for example. In the case where the lower electrode **761** is a cathode and the upper electrode **762** is an anode, the layer **781** can be an electron-injection layer, the layer **782** can be an electron-transport layer, the layer **791** can be a hole-transport layer, and the layer **792** can be a hole-injection layer. With such a layered structure, carriers can be efficiently injected to the light-emitting layer **771**, and the efficiency of the recombination of carriers in the light-emitting layer **771** can be enhanced.

[0706] Note that structures in which a plurality of light-emitting layers (the light-emitting layer **771**, a light-emitting layer **772**, and a light-emitting layer **773**) are provided between the layer **780** and the layer **790** as illustrated in FIG. **45**C and FIG. **45**D are other variations of the single structure. Although FIG. **45**C and FIG. **45**D illustrate the examples where three light-emitting layers are included, the light-emitting device with a single structure may include two or four or more light-emitting layers. A light-emitting device having a single structure may include a buffer layer between two light-emitting layers. A carrier-transport layer (a hole-transport layer or an electron-transport layer) can be used as the buffer layer, for example.

[0707] A structure in which a plurality of light-emitting units (a light-emitting unit **763***a* and a light-emitting unit **763***b*) are connected in series with a charge-generation layer (also referred to as an intermediate layer) **785** therebetween as illustrated in FIG. **45**E and FIG. **45**F is referred to as a tandem structure in this specification. The tandem structure may be referred to as a stack structure. The tandem structure enables a light-emitting device capable of high-luminance light emission. Furthermore, the tandem structure allows the amount of current needed for obtaining the same luminance to be reduced as compared with the case of using a single structure, and thus can improve the reliability.

[0708] Note that FIG. **45**D and FIG. **45**F illustrate examples where the display apparatus includes a layer **764** overlapping with the light-emitting device. FIG. **45**D illustrates an example in which the layer **764** overlaps with the light-emitting device illustrated in FIG. **45**C, and FIG. **45**F illustrates an example in which the layer **764** overlaps with the light-emitting device illustrated in FIG. **45**E. In FIG. **45**D and FIG. **45**F, a conductive film transmitting visible light is used for the upper electrode **762** to extract light to the upper electrode **762** side.

[0709] One or both of a color conversion layer and a color filter (coloring layer) can be used as the layer **764**.

[0710] In FIG. **45**C and FIG. **45**D, light-emitting substances emitting light of the same color, or moreover, the same light-emitting substance may be used for the light-emitting layer **771**, the light-emitting layer **772**, and the light-emitting layer **773**. For example, alight-emitting substance that emits blue light may be used for the light-emitting layer **771**, the light-emitting layer **772**, and the light-emitting layer **773**. In a subpixel that emits blue light,

blue light emitted from the light-emitting device can be extracted. In each of a subpixel that emits red light and a subpixel that emits green light, a color conversion layer is provided as the layer **764** illustrated in FIG. **45**D for converting blue light emitted from the light-emitting device into light with a longer wavelength, so that red light or green light can be extracted. As the layer **764**, both a color conversion layer and a coloring layer are preferably used. In some cases, part of light emitted from the light-emitting device is transmitted through the color conversion layer without being converted. When light transmitted through the color conversion layer is extracted through the coloring layer, light other than light of the intended color can be absorbed by the coloring layer, and color purity of light exhibited by a subpixel can be improved.

[0711] In FIG. **45**C and FIG. **45**D, light-emitting substances that emit light of different colors may be used for the light-emitting layer **771**, the light-emitting layer **772**, and the light-emitting layer **773**. White light emission can be obtained by mixing of light emitted from the light-emitting layer **771**, the light-emitting layer **772**, and the light-emitting layer **773**. The light-emitting device having a single structure preferably includes a light-emitting layer including a light-emitting substance that emits blue light and a light-emitting layer including a light-emitting substance that emits visible light with a longer wavelength than blue light, for example.

[0712] A color filter may be provided as the layer **764** illustrated in FIG. **45**D. When white light passes through the color filter, light of a desired color can be obtained.

[0713] In the case where the light-emitting device having a single structure includes three light-emitting layers, for example, a light-emitting layer including a light-emitting substance that emits red (R) light, a light-emitting layer including a light-emitting substance that emits green (G) light, and a light-emitting layer including a light-emitting substance that emits blue (B) light are preferably included. The stacking order of the light-emitting layers can be RGB or RBG from an anode side, for example. In that case, a buffer layer may be provided between R and G or between R and B.

[0714] In the case where the light-emitting device having a single structure includes two light-emitting layers, for example, a light-emitting layer including a light-emitting substance that emits blue (B) light and a light-emitting layer including a light-emitting substance that emits yellow (Y) light are preferably included. Such a structure may be referred to as a BY single structure.

[0715] In the light-emitting device that emits white light, two or more kinds of light-emitting substances are preferably included. To obtain white light emission, the two or more kinds of light-emitting substances are selected so as to emit light of complementary colors. In the case of including three or more kinds of light-emitting substances, the light-emitting substances are selected such that white light emission can be obtained by mixing of light emitted from the light-emitting substances. For example, when emission colors of a first light-emitting layer and a second light-emitting layer are complementary colors, the light-emitting device can emit white light as a whole. The same applies to a light-emitting device including three or more light-emitting layers.

[0716] Also in FIG. **45**C and FIG. **45**D, the layer **780** and the layer **790** may each independently have a stacked-layer structure of two or more layers as illustrated in FIG. **45**B.

[0717] In FIG. **45**E and FIG. **45**F, light-emitting substances emitting light of the same color, or moreover, the same light-emitting substance may be used for the light-emitting layer **771** and the light-emitting layer **772**. For example, in light-emitting devices included in subpixels emitting light of different colors, a light-emitting substance that emits blue light may be used for each of the light-emitting layer **771** and the light-emitting layer **772**. In a subpixel that emits blue light, blue light emitted from the light-emitting device can be extracted. In each of the subpixel that emits red light and the subpixel that emits green light, a color conversion layer is provided as the layer **764** illustrated in FIG. **45**F for converting blue light emitted from the light-emitting device into light with a longer wavelength, so that red light or green light can be extracted. As the layer **764**, both a color conversion layer and a coloring layer are preferably used.

[0718] In the case where light-emitting devices with the structure illustrated in FIG. **45**E or FIG. **45**F are used in subpixels emitting light of different colors, light-emitting substances may be different between the subpixels. Specifically, in the light-emitting device included in the subpixel that emits red light, a light-emitting substance that emits red light may be used for each of the light-emitting layer **771** and the light-emitting layer **772**. Similarly, in the light-emitting device included in the subpixel that emits green light, a light-emitting substance that emits green light may be used for each of the light-emitting layer **771** and the light-emitting layer **772**. In the light-emitting device included in the subpixel that emits blue light, a light-emitting substance that emits blue light may be used for each of the light-emitting layer **771** and the light-emitting layer **772**. A display apparatus with such a structure includes a light-emitting device with a tandem structure and can be regarded to have an SBS structure. Thus, the display apparatus can have advantages of both of a tandem structure and an SBS structure. Accordingly, a highly reliable light-emitting device capable of high-luminance light emission can be obtained.

[0719] In FIG. **45**E and FIG. **45**F, light-emitting substances that emit light of different colors may be used for the light-emitting layer **771** and the light-emitting layer **772**. When the light-emitting layer **771** and the light-emitting layer **772** emit light of complementary colors, white light emission can be obtained. A color filter may be provided as the layer **764** illustrated in FIG. **45**F. When white light passes through the color filter, light of a desired color can be obtained.

[0720] Although FIG. **45**E and FIG. **45**F illustrate examples where the light-emitting unit **763***a* includes one light-emitting layer **771** and the light-emitting unit **763***b* includes one light-emitting layer **772**, one embodiment of the present invention is not limited thereto. Each of the light-emitting unit **763***a* and the light-emitting unit **763***b* may include two or more light-emitting layers.

[0721] In addition, although FIG. **45**E and FIG. **45**F illustrate the light-emitting device including two light-emitting units, one embodiment of the present invention is not limited thereto. The light-emitting device may include three or more light-emitting units. Note that a structure including two light-emitting units and a structure including three

light-emitting units may be referred to as a two-unit tandem structure and a three-unit tandem structure, respectively.

[0722] In each of FIG. **45**E and FIG. **45**F, the light-emitting unit **763***a* includes a layer **780***a*, the light-emitting layer **771**, and a layer **790***a*, and the light-emitting unit **763***b* includes a layer **780***b*, the light-emitting layer **772**, and a layer **790***b*.

[0723] In the case where the lower electrode **761** is an anode and the upper electrode **762** is a cathode, the layer **780***a* and the layer **780***b* each include one or more of a hole-injection layer, a hole-transport layer, and an electron-blocking layer. Furthermore, the layer **790***a* and the layer **790***b* each include one or more of an electron-injection layer, an electron-transport layer, and a hole-blocking layer. In the case where the lower electrode **761** is a cathode and the upper electrode **762** is an anode, the structures of the layer **780***a* and the layer **790***a* are interchanged and the structures of the layer **780***b* and the layer **790***b* are interchanged.

[0724] In the case where the lower electrode **761** is an anode and the upper electrode **762** is a cathode, the layer **780***a* includes a hole-injection layer and a hole-transport layer over the hole-injection layer, and may further include an electron-blocking layer over the hole-transport layer, for example. The layer **790***a* includes an electron-transport layer, and may further include a hole-blocking layer between the light-emitting layer **771** and the electron-transport layer. The layer **780***b* includes a hole-transport layer, and may further include an electron-blocking layer over the hole-transport layer. The layer **790***b* includes an electron-transport layer and an electron-injection layer over the electron-transport layer, and may further include a hole-blocking layer between the light-emitting layer **772** and the electron-transport layer. In the case where the lower electrode **761** is a cathode and the upper electrode **762** is an anode, the layer **780***a* includes an electron-injection layer and an electron-transport layer over the electron-injection layer, and may further include a hole-blocking layer over the electron-transport layer, for example. The layer **790***a* includes a hole-transport layer, and may further include an electron-blocking layer between the light-emitting layer **771** and the hole-transport layer. The layer **780***b* includes an electron-transport layer, and may further include a hole-blocking layer over the electron-transport layer. The layer **790***b* includes a hole-transport layer and a hole-injection layer over the hole-transport layer, and may further include an electron-blocking layer between the light-emitting layer **772** and the hole-transport layer.

[0725] In the case of fabricating the light-emitting device with a tandem structure, two light-emitting units are stacked with the charge-generation layer **785** therebetween. The charge-generation layer **785** includes at least a charge-generation region. The charge-generation layer **785** has a function of injecting electrons into one of the two light-emitting units and injecting holes to the other when voltage is applied between the pair of electrodes.

[0726] Structures illustrated in FIG. **46**A to FIG. **46**C can be given as examples of the light-emitting device with a tandem structure.

[0727] FIG. **46**A illustrates a structure including three light-emitting units. In FIG. **46**A, a plurality of light-emitting units (the light-emitting unit **763***a*, the light-emitting unit **763***b*, and a light-emitting unit **763***c*) are connected in series with the charge-generation layer **785** provided between each two light-emitting units. The light-emitting unit **763***a* includes the layer **780***a*, the light-emitting layer **771**, and the layer **790***a*. The light-emitting unit **763***b* includes the layer **780***b*, the light-emitting layer **772**, and the layer **790***b*. The light-emitting unit **763***c* includes a layer **780***c*, the light-emitting layer **773**, and a layer **790***c*. Note that the layer **780***c* can have a structure applicable to the layer **780***a* and the layer **780***b*, and the layer **790***c* can have a structure applicable to the layer **790***a* and the layer **790***b*.

[0728] In FIG. **46**A, the light-emitting layer **771**, the light-emitting layer **772**, and the light-emitting layer **773** preferably include light-emitting substances that emit light of the same color. Specifically, the light-emitting layer **771**, the light-emitting layer **772**, and the light-emitting layer **773** can each include a light-emitting substance that emits red (R) light (what is called an R\R\R three-unit tandem structure), the light-emitting layer **771**, the light-emitting layer **772**, and the light-emitting layer **773** can each include a light-emitting substance that emits green (G) light (what is called a G\G\G three-unit tandem structure), or the light-emitting layer **771**, the light-emitting layer **772**, and the light-emitting layer **773** can each include a light-emitting substance that emits blue (B) light (what is called a B\B\B three-unit tandem structure). Note that "a\b" means that a light-emitting unit including a light-emitting substance that emits light of a color "b" is provided over a light-emitting unit including a light-emitting substance that emits light of a color "a" with a charge-generation layer therebetween, and "a" and "b" each mean a color.

[0729] In FIG. **46**A, light-emitting substances that emit light of different colors may be used for some or all of the light-emitting layer **771**, the light-emitting layer **772**, and the light-emitting layer **773**. Examples of the combination of emission colors for the light-emitting layer **771**, the light-emitting layer **772**, and the light-emitting layer **773** include a combination of blue (B) for two of them and yellow (Y) for the other; and a combination of red (R) for one of them, green (G) for another, and blue (B) for the other.

[0730] Note that the light-emitting substances that emit light of the same color is not limited to the above structure. For example, a light-emitting device with a tandem structure may be employed in which light-emitting units each including a plurality of light-emitting layers are stacked as illustrated in FIG. **46**B. FIG. **46**B illustrates a structure in which two light-emitting units (the light-emitting unit **763***a* and the light-emitting unit **763***b*) are connected in series with the charge-generation layer **785** therebetween. The light-emitting unit **763***a* includes the layer **780***a*, a light-emitting layer **771***a*, a light-emitting layer **771***b*, a light-emitting layer **771***c*, and the layer **790***a*. The light-emitting unit **763***b* includes the layer **780***b*, a light-emitting layer **772***a*, a light-emitting layer **772***b*, a light-emitting layer **772***c*, and the layer **790***b*.

[0731] In FIG. **46**B, by selecting light-emitting substances for the light-emitting layer **771***a*, the light-emitting layer **771***b*, and the light-emitting layer **771***c* such that white light emission is obtained when light emitted from the light-emitting layers is mixed, the light-emitting unit **763***a* enables white (W) light emission. Furthermore, by selecting light-emitting substances for the light-emitting layer **772***a*, the light-emitting layer **772***b*, and the light-emitting layer **772***c* such that white light emission is obtained when light emitted from the light-emitting layers is mixed, the light-emitting unit **763***b* enables white (W) light emission. That is, the structure illustrated in FIG. **46**B is a two-unit tandem

structure of W\W. Note that there is no particular limitation on the stacking order of the light-emitting substances. A practitioner can select an optimum stacking order as appropriate. Although not illustrated, a three-unit tandem structure of W\W\W or a tandem structure with four or more units may be employed.

[0732] In the case of a light-emitting device with a tandem structure, any of the following structures may be employed: a two-unit tandem structure of B\Y or Y\B including a light-emitting unit that emits yellow (Y) light and a light-emitting unit that emits blue (B) light; a two-unit tandem structure of R·G\B or B\R·G including a light-emitting unit that emits red (R) and green (G) light and a light-emitting unit that emits blue (B) light; a three-unit tandem structure of B\Y\B including a light-emitting unit that emits blue (B) light, a light-emitting unit that emits yellow (Y) light, and a light-emitting unit that emits blue (B) light in this order; a three-unit tandem structure of B\YG\B including a light-emitting unit that emits blue (B) light, a light-emitting unit that emits yellow-green (YG) light, and a light-emitting unit that emits blue (B) light in this order; and a three-unit tandem structure of B\G\B including a light-emitting unit that emits blue (B) light, a light-emitting unit that emits green (G) light, and a light-emitting unit that emits blue (B) light in this order. Note that "a·b" means that one light-emitting unit contains a light-emitting substance that emits light of a color "a" and a light-emitting substance that emits light of a color "b".

[0733] Alternatively, a light-emitting unit including one light-emitting layer and a light-emitting unit including a plurality of light-emitting layers may be used in combination as illustrated in FIG. **46**C.

[0734] Specifically, in the structure illustrated in FIG. **46**C, a plurality of light-emitting units (the light-emitting unit **763***a*, the light-emitting unit **763***b*, and the light-emitting unit **763***c*) are connected in series with the charge-generation layer **785** provided between each two light-emitting units. The light-emitting unit **763***a* includes the layer **780***a*, the light-emitting layer **771**, and the layer **790***a*. The light-emitting unit **763***b* includes the layer **780***b*, the light-emitting layer **772***a*, the light-emitting layer **772***b*, the light-emitting layer **772***c*, and the layer **790***b*. The light-emitting unit **763***c* includes the layer **780***c*, the light-emitting layer **773**, and the layer **790***c*.

[0735] The structure illustrated in FIG. **46**C can be, for example, a three-unit tandem structure of B\R·G·YG\B in which the light-emitting unit **763***a* is a light-emitting unit that emits blue (B) light, the light-emitting unit **763***b* is a light-emitting unit that emits red (R), green (G), and yellow-green (YG) light, and the light-emitting unit **763***c* is a light-emitting unit that emits blue (B) light.

[0736] Examples of the number of stacked light-emitting units and the order of colors from the anode side include a two-unit structure of B and Y; a two-unit structure of B and a light-emitting unit X; a three-unit structure of B, Y, and B; and a three-unit structure of B, X, and B. Examples of the number of light-emitting layers stacked in the light-emitting unit X and the order of colors from an anode side include a two-layer structure of R and Y; a two-layer structure of R and G; a two-layer structure of G and R; a three-layer structure of G, R, and G; and a three-layer structure of R, G, and R. Another layer may be provided between two light-emitting layers.

[0737] Next, materials that can be used for the light-emitting device will be described.

[0738] A conductive film transmitting visible light is used for the electrode through which light is extracted, which is either the lower electrode **761** or the upper electrode **762**. A conductive film reflecting visible light is preferably used for the electrode through which light is not extracted. In the case where the display apparatus includes a light-emitting device emitting infrared light, a conductive film transmitting visible light and infrared light is preferably used for the electrode through which light is extracted, and a conductive film reflecting visible light and infrared light is preferably used for the electrode through which light is not extracted.

[0739] A conductive film transmitting visible light may be used also for the electrode through which light is not extracted. In that case, the electrode is preferably placed between a reflective layer and the EL layer **763**. In other words, light emitted from the EL layer **763** may be reflected by the reflective layer to be extracted from the display apparatus.

[0740] As a material for the pair of electrodes of the light-emitting device, a metal, an alloy, an electrically conductive compound, a mixture thereof, or the like can be used as appropriate. Specific examples of the material include metals such as aluminum, magnesium, titanium, chromium, manganese, iron, cobalt, nickel, copper, gallium, zinc, indium, tin, molybdenum, tantalum, tungsten, palladium, gold, platinum, silver, yttrium, and neodymium, and an alloy containing appropriate combination of any of these metals. Other examples of the material include indium tin oxide (In—Sn oxide, also referred to as ITO), In—Si—Sn oxide (also referred to as ITSO), indium zinc oxide (In—Zn oxide), and In—W—Zn oxide. Other examples of the material include an alloy containing aluminum (aluminum alloy), such as an alloy of aluminum, nickel, and lanthanum (Al—Ni—La), and an alloy containing silver, such as an alloy of silver and magnesium and an alloy of silver, palladium, and copper (Ag—Pd—Cu, also referred to as APC). Other examples of the material include an element belonging to Group 1 or Group 2 of the periodic table that is not exemplified above (e.g., lithium, cesium, calcium, or strontium), a rare earth metal such as europium or ytterbium, an alloy containing an appropriate combination of any of these elements, and graphene.

[0741] The light-emitting device preferably employs a microcavity structure. Therefore, one of the pair of electrodes of the light-emitting device is preferably an electrode having properties of transmitting and reflecting visible light (transflective electrode), and the other is preferably an electrode having a visible-light-reflecting property (reflective electrode). When the light-emitting device has a microcavity structure, light obtained from the light-emitting layer can be resonated between the electrodes, whereby light emitted from the light-emitting device can be intensified.

[0742] The transmittance of light of the electrode having a visible-light-transmitting property is greater than or equal to 40%. For example, in the case of using an electrode having a visible-light-transmitting property in the light-emitting device, an electrode having a visible light (light at a wavelength greater than or equal to 400 nm and less than 750 nm) transmittance higher than or equal to 40% is preferably used. The transflective electrode has a visible light reflectance higher than or equal to 10% and lower than or equal to 95%, preferably higher than or equal to 30% and

lower than or equal to 80%. The reflective electrode has a visible light reflectance higher than or equal to 40% and lower than or equal to 100%, preferably higher than or equal to 70% and lower than or equal to 100%. These electrodes preferably have a resistivity lower than or equal to 1×10^{-2} Ωcm.

[0743] The light-emitting device includes at least a light-emitting layer. In addition to the light-emitting layer, the light-emitting device may further include a layer including any of a substance having a high hole-injection property, a substance having a high hole-transport property, a hole-blocking material, a substance having a high electron-transport property, an electron-blocking material, a substance having a high electron-injection property, a substance having a bipolar property (a substance with a high electron- and hole-transport property), and the like. For example, the light-emitting device can include one or more of a hole-injection layer, a hole-transport layer, a hole-blocking layer, a charge-generation layer, an electron-blocking layer, an electron-transport layer, and an electron-injection layer in addition to the light-emitting layer.

[0744] Either a low molecular compound or a high molecular compound can be used in the light-emitting device, and an inorganic compound may also be included. Each layer included in the light-emitting device can be formed by any of the following methods: an evaporation method (including a vacuum evaporation method), a transfer method, a printing method, an inkjet method, a coating method, and the like.

[0745] The light-emitting layer includes one or more kinds of light-emitting substances. As the light-emitting substance, a substance whose emission color is blue, violet, bluish violet, green, yellow green, yellow, orange, red, or the like is appropriately used. Alternatively, as the light-emitting substance, a substance that emits near-infrared light can be used.

[0746] Examples of the light-emitting substance include a fluorescent material, a phosphorescent material, a TADF material, and a quantum dot material.

[0747] Examples of a fluorescent material include a pyrene derivative, an anthracene derivative, a triphenylene derivative, a fluorene derivative, a carbazole derivative, a dibenzothiophene derivative, a dibenzofuran derivative, a dibenzoquinoxaline derivative, a quinoxaline derivative, a pyridine derivative, a pyrimidine derivative, a phenanthrene derivative, and a naphthalene derivative.

[0748] Examples of a phosphorescent material include an organometallic complex (particularly an iridium complex) having a 4H-triazole skeleton, a 1H-triazole skeleton, an imidazole skeleton, a pyrimidine skeleton, a pyrazine skeleton, or a pyridine skeleton; an organometallic complex (particularly an iridium complex) having a phenylpyridine derivative including an electron-withdrawing group as a ligand; a platinum complex; and a rare earth metal complex.

[0749] The light-emitting layer may include one or more kinds of organic compounds (e.g., a host material or an assist material) in addition to the light-emitting substance (a guest material). As one or more kinds of organic compounds, one or both of a substance with a high hole-transport property (a hole-transport material) and a substance with a high electron-transport property (an electron-transport material) can be used. As the hole-transport material, it is possible to use any of after-mentioned substances each having a high hole-transport property that can be used for the hole-transport layer. As the electron-transport material, it is possible to use any of after-mentioned substances each having a high electron-transport property that can be used for the electron-transport layer. Alternatively, as one or more kinds of organic compounds, a bipolar material or a TADF material may be used.

[0750] The light-emitting layer preferably includes a phosphorescent material and a combination of a hole-transport material and an electron-transport material that easily forms an exciplex, for example. With such a structure, light emission can be efficiently obtained by ExTET (Exciplex-Triplet Energy Transfer), which is energy transfer from the exciplex to the light-emitting substance (phosphorescent material). When a combination of materials is selected so as to form an exciplex that emits light whose wavelength overlaps with the wavelength of a lowest-energy-side absorption band of the light-emitting substance, energy can be transferred smoothly and light emission can be obtained efficiently. With the above structure, high efficiency, low-voltage driving, and a long lifetime of a light-emitting device can be achieved at the same time.

[0751] The hole-injection layer injects holes from the anode to the hole-transport layer and includes a substance having a high hole-injection property. Examples of a substance having a high hole-injection property include an aromatic amine compound and a composite material including a hole-transport material and an acceptor material (electron-accepting material).

[0752] As the hole-transport material, it is possible to use any of after-mentioned substances each having a high hole-transport property that can be used for the hole-transport layer.

[0753] As the acceptor material, for example, an oxide of a metal belonging to any of Group 4 to Group 8 of the periodic table can be used. Specific examples include molybdenum oxide, vanadium oxide, niobium oxide, tantalum oxide, chromium oxide, tungsten oxide, manganese oxide, and rhenium oxide. Among these, molybdenum oxide is especially preferred because it is stable in the air, has a low hygroscopic property, and is easy to handle. Alternatively, an organic acceptor material containing fluorine can be used. Alternatively, organic acceptor materials such as a quinodimethane derivative, a chloranil derivative, and a hexaazatriphenylene derivative can be used.

[0754] As the substance having a high hole-injection property, a material containing a hole-transport material and the above-described oxide of a metal belonging to Group 4 to Group 8 of the periodic table (typically, molybdenum oxide) may be used, for example.

[0755] The hole-transport layer transports holes injected from the anode by the hole-injection layer, to the light-emitting layer. The hole-transport layer includes a hole-transport material. The hole-transport material is preferably a substance having a hole mobility higher than or equal to 1×10^{-6} cm^2/Vs. Note that other substances can also be used as long as the substances have a hole-transport property higher than an electron-transport property. As the hole-transport material, substances having a high hole-transport property, such as a π-electron rich heteroaromatic compound (e.g., a carbazole derivative, a thiophene derivative, and a furan derivative) and an aromatic amine (a compound having an aromatic amine skeleton), are preferred.

[0756] The electron-blocking layer is provided in contact with the light-emitting layer. The electron-blocking layer is

a layer having a hole-transport property and including a material that can block an electron. Among the above-described hole-transport materials, a material having an electron-blocking property can be used for the electron-blocking layer.

[0757] The electron-blocking layer has a hole-transport property, and thus can also be referred to as a hole-transport layer. Among hole-transport layers, a layer having an electron-blocking property can also be referred to as an electron-blocking layer.

[0758] The electron-transport layer transports electrons injected from the cathode by the electron-injection layer, to the light-emitting layer. The electron-transport layer includes an electron-transport material. The electron-transport material is preferably a substance having an electron mobility higher than or equal to 1×10^{-6} cm^2/Vs. Note that other substances can also be used as long as the substances have an electron-transport property higher than a hole-transport property. As the electron-transport material, any of the following substances having a high electron-transport property can be used, for example: a metal complex having a quinoline skeleton, a metal complex having a benzoquinoline skeleton, a metal complex having an oxazole skeleton, a metal complex having a thiazole skeleton, an oxadiazole derivative, a triazole derivative, an imidazole derivative, an oxazole derivative, a thiazole derivative, a phenanthroline derivative, a quinoline derivative having a quinoline ligand, a benzoquinoline derivative, a quinoxaline derivative, a dibenzoquinoxaline derivative, a pyridine derivative, a bipyridine derivative, a pyrimidine derivative, and a π-electron deficient heteroaromatic compound such as a nitrogen-containing heteroaromatic compound.

[0759] The hole-blocking layer is provided in contact with the light-emitting layer. The hole-blocking layer is a layer having an electron-transport property and including a material that can block a hole. Among the above-described electron-transport materials, a material having a hole-blocking property can be used for the hole-blocking layer.

[0760] The hole-blocking layer has an electron-transport property, and thus can also be referred to as an electron-transport layer. Among electron-transport layers, a layer having a hole-blocking property can also be referred to as a hole-blocking layer.

[0761] The electron-injection layer injects electrons from the cathode to the electron-transport layer and includes a substance having a high electron-injection property. As the substance having a high electron-injection property, an alkali metal, an alkaline earth metal, or a compound thereof can be used. As the substance having a high electron-injection property, a composite material including an electron-transport material and a donor material (electron-donating material) can also be used.

[0762] The lowest unoccupied molecular orbital (LUMO) level of the substance having a high electron-injection property preferably has a small difference (specifically, 0.5 eV or less) from the work function of a material used for the cathode.

[0763] The electron-injection layer can be formed using an alkali metal, an alkaline earth metal, or a compound thereof, such as lithium, cesium, ytterbium, lithium fluoride (LiF), cesium fluoride (CsF), calcium fluoride (CaF_x, where X is a given number), 8-(quinolinolato)lithium (abbreviation: Liq), 2-(2-pyridyl)phenolatolithium (abbreviation: LiPP), 2-(2-pyridyl)-3-pyridinolatolithium (abbreviation: LiPPy), 4-phenyl-2-(2-pyridyl)phenolatolithium (abbreviation: LiPPP), lithium oxide (LiO_x), or cesium carbonate, for example. The electron-injection layer may have a stacked-layer structure of two or more layers. As an example of the stacked-layer structure, a structure in which lithium fluoride is used for the first layer and ytterbium is used for the second layer is given.

[0764] The electron-injection layer may include an electron-transport material. For example, a compound having an unshared electron pair and an electron deficient heteroaromatic ring can be used as the electron-transport material. Specifically, it is possible to use a compound having at least one of a pyridine ring, a diazine ring (a pyrimidine ring, a pyrazine ring, or a pyridazine ring), and a triazine ring.

[0765] Note that the LUMO level of the organic compound having an unshared electron pair is preferably greater than or equal to −3.6 eV and less than or equal to −2.3 eV. In general, the highest occupied molecular orbital (HOMO) level and the LUMO level of an organic compound can be estimated by CV (cyclic voltammetry), photoelectron spectroscopy, optical absorption spectroscopy, inverse photoelectron spectroscopy, or the like.

[0766] For example, 4,7-diphenyl-1,10-phenanthroline (abbreviation: BPhen), 2,9-di(naphthalen-2-yl)-4,7-diphenyl-1,10-phenanthroline (abbreviation: NBPhen), diquinoxalino[2,3-a:2',3'-c]phenazine (abbreviation: HATNA), 2,4,6-tris[3'-(pyridin-3-yl)biphenyl-3-yl]-1,3,5-triazine (abbreviation: TmPPPyTz), or the like can be used as the organic compound having an unshared electron pair. Note that NBPhen has a higher glass transition point (Tg) than BPhen and thus has high heat resistance.

[0767] As described above, the charge-generation layer includes at least a charge-generation region. The charge-generation region preferably includes an acceptor material. For example, the charge-generation region preferably includes the above-described hole-transport material and acceptor material that can be used for the hole-injection layer.

[0768] The charge-generation layer preferably includes a layer including a substance having a high electron-injection property. The layer can also be referred to as an electron-injection buffer layer. The electron-injection buffer layer is preferably provided between the charge-generation region and the electron-transport layer. The electron-injection buffer layer can reduce an injection barrier between the charge-generation region and the electron-transport layer; thus, electrons generated in the charge-generation region can be easily injected into the electron-transport layer.

[0769] The electron-injection buffer layer preferably contains an alkali metal or an alkaline earth metal, and can contain an alkali metal compound or an alkaline earth metal compound, for example. Specifically, the electron-injection buffer layer preferably includes an inorganic compound containing an alkali metal and oxygen or an inorganic compound containing an alkaline earth metal and oxygen, and further preferably includes an inorganic compound containing lithium and oxygen (e.g., lithium oxide (Li_2O)). Alternatively, a material that can be used for the electron-injection layer can be favorably used for the electron-injection buffer layer.

[0770] The charge-generation layer preferably includes a layer including a substance having a high electron-transport property. The layer can also be referred to as an electron-relay layer. The electron-relay layer is preferably provided

between the charge-generation region and the electron-injection buffer layer. In the case where the charge-generation layer does not include an electron-injection buffer layer, the electron-relay layer is preferably provided between the charge-generation region and the electron-transport layer. The electron-relay layer has a function of preventing an interaction between the charge-generation region and the electron-injection buffer layer (or the electron-transport layer) to transfer electrons smoothly.

[0771] For the electron-relay layer, a phthalocyanine-based material such as copper(II) phthalocyanine (abbreviation: CuPc), or a metal complex having a metal-oxygen bond and an aromatic ligand is preferably used.

[0772] Note that the charge-generation region, the electron-injection buffer layer, and the electron-relay layer cannot be clearly distinguished from one another on the basis of the cross-sectional shape or properties in some cases.

[0773] The charge-generation layer may contain a donor material instead of an acceptor material. For example, the charge-generation layer may include a layer including the above-described electron-transport material and donor material that can be used for the electron-injection layer.

[0774] When the charge-generation layer is provided between two light-emitting units to be stacked, an increase in driving voltage can be inhibited.

[0775] The structure described in this embodiment can be used in an appropriate combination with any of the structures described in the other embodiments.

Embodiment 4

[0776] In this embodiment, a structure example of the light-emitting device **61** that achieves full-color display in the display apparatus **50** will be described.

[0777] A plurality of light-emitting devices **61** provided in the display portion **235** of the display apparatus **50** can be obtained by a photolithography method without a shadow mask such as a metal mask. Accordingly, a high-definition display apparatus with a high aperture ratio, which had been difficult to achieve, can be fabricated. Moreover, a leakage current between adjacent EL layers is reduced; thus, a display apparatus with a high contrast and high display quality can be fabricated.

[0778] Although it is difficult to set the distance between adjacent light-emitting devices **61** to be less than 10 μm by a formation method using a metal mask, for example, a photolithography method can shorten the distance to be less than or equal to 8 μm, less than or equal to 3 μm, less than or equal to 2 μm, or less than or equal to 1 μm. Here, the distance between adjacent light-emitting devices **61** can be determined by the distance between end portions of two adjacent pixel electrodes. Alternatively, the distance between adjacent light-emitting devices **61** can be determined by the distance between end portions of two adjacent EL layers.

[0779] In this specification and the like, a display apparatus formed using a metal mask or an FMM (fine metal mask, high-definition metal mask) may be referred to as a display apparatus having an MM (metal mask) structure. In this specification and the like, a display apparatus formed without using a metal mask or an FMM may be referred to as a display apparatus having an MML (metal maskless) structure.

[0780] By shortening the distance between adjacent light-emitting devices **61** in the above manner, the area of a non-light-emitting region that may exist between two light-emitting devices can be significantly reduced, and the aperture ratio can be close to 100%. For example, the aperture ratio is higher than or equal to 50%, higher than or equal to 60%, higher than or equal to 70%, higher than or equal to 80%, or higher than or equal to 90%; that is, an aperture ratio lower than 100% can be achieved.

[0781] Furthermore, a pattern (also referred to as a processing size) of the EL layer itself can be made much smaller than that in the case of using a metal mask. For example, in the case of using a metal mask for forming EL layers separately, a variation in the thickness occurs between the center and the edge of the EL layer. This causes a reduction in an effective area that can be used as a light-emitting region with respect to the area of the EL layer. In contrast, in the above manufacturing method, an EL layer is formed by processing a film formed to have a uniform thickness, which enables a uniform thickness in the EL layer. Thus, even in a fine pattern, almost the whole area can be used as a light-emitting region. Therefore, the above manufacturing method makes it possible to achieve high definition and a high aperture ratio.

[0782] In many cases, an organic film formed using an FMM (Fine Metal Mask) has an extremely small taper angle (e.g., a taper angle of greater than 0° and less than 30°) so that the thickness of the film becomes smaller in a portion closer to an end portion. Therefore, it is difficult to clearly observe the side surface of an organic film formed using an FMM because the side surface and the top surface are continuously connected. In contrast, an EL layer included in one embodiment of the present invention is processed without using an FMM, and has a clear side surface. In particular, part of the taper angle of the EL layer included in one embodiment of the present invention is preferably greater than or equal to 30° and less than or equal to 120°, further preferably greater than or equal to 60° and less than or equal to 120°.

[0783] Note that in this specification and the like, an end portion of an object having a tapered shape indicates that the end portion of the object has a cross-sectional shape in which the angle between the side surface (the surface) of the object and the formation surface (the bottom surface) of the object is greater than 0° and less than 90° in a region of the end portion, and the thickness continuously increases from the end portion. A taper angle refers to an angle between a bottom surface (a formation surface) and a side surface (a surface) at an end portion of the object.

[0784] A more specific structure example is described below.

[0785] FIG. **47**A is a schematic top view of part of the display portion **235** included in the display apparatus **50**. The display apparatus **50** includes a plurality of light-emitting devices **61**R that emit red light, a plurality of light-emitting devices **61**G that emit green light, and a plurality of light-emitting devices **61**B that emit blue light over the substrate **101** provided with a semiconductor circuit. In FIG. **47**A, light-emitting regions of the light-emitting devices are denoted by R, G, and B to easily differentiate the light-emitting devices. Note that the substrate **101** is a substrate over which the semiconductor device described in the above embodiment is formed and the description of the above embodiment can be referred to for the details. Note that FIG. **47** does not illustrate the semiconductor device provided over the substrate **101**.

[0786] The light-emitting devices **61**R, the light-emitting devices **61**G, and the light-emitting devices **61**B are arranged in a stripe pattern. In FIG. **47**A, two elements are alternately arranged in one direction. Note that the arrangement method of the light-emitting devices is not limited thereto; another method such as S-stripe arrangement, delta arrangement, Bayer arrangement, or zigzag arrangement may be employed, or PenTile arrangement, diamond arrangement, or the like can also be employed.

[0787] FIG. **47**A illustrates a connection electrode **311**C that is electrically connected to a common electrode **313**. The connection electrode **311**C is supplied with a potential (e.g., an anode potential or a cathode potential) that is to be supplied to the common electrode **313**. The connection electrode **311**C is provided outside a display region where the light-emitting devices **61**R and the like are arranged. In FIG. **47**A, the common electrode **313** is denoted by a dashed line.

[0788] The connection electrode **311**C can be provided along the outer periphery of the display region. For example, the connection electrode **311**C may be provided along one side of the outer periphery of the display region or two or more sides of the outer periphery of the display region. That is, in the case where the display region has a rectangular top surface, the top surface of the connection electrode **311**C can have a band shape, an L shape, a square bracket shape, a quadrangular shape, or the like.

[0789] FIG. **47**B is a schematic cross-sectional view taken along the dashed-dotted line A**1**-A**2** and the dashed-dotted line C**1**-C**2** in FIG. **47**A. FIG. **47**B is a schematic cross-sectional view of the light-emitting device **61**B, the light-emitting device **61**R, the light-emitting device **61**G, and the connection electrode **311**C.

[0790] The light-emitting device **61**B includes a pixel electrode **311**, an organic layer **312**B, an organic layer **314**, and the common electrode **313**. The light-emitting device **61**R includes the pixel electrode **311**, an organic layer **312**R, the organic layer **314**, and the common electrode **313**. The light-emitting device **61**G includes the pixel electrode **311**, an organic layer **312**G, the organic layer **314**, and the common electrode **313**. The organic layer **314** and the common electrode **313** are shared by the light-emitting device **61**B, the light-emitting device **61**R, and the light-emitting device **61**G. The organic layer **314** can also be referred to as a common layer. The pixel electrodes **311** are provided apart from each other between the light-emitting devices and between the light-emitting device and the light-receiving device.

[0791] The organic layer **312**R, the organic layer **312**G, and the organic layer **312**B each correspond to the EL layer **763** of the above embodiment.

[0792] The organic layer **312**R contains at least a light-emitting organic compound that emits red light. The organic layer **312**G contains at least a light-emitting organic compound that emits green light. The organic layer **312**B contains at least a light-emitting organic compound that emits blue light. Each of the organic layer **312**R, the organic layer **312**G, and the organic layer **312**B can also be referred to as an EL layer.

[0793] The organic layer **312**R, the organic layer **312**B, and the organic layer **312**G may each include one or more of an electron-injection layer, an electron-transport layer, a hole-injection layer, and a hole-transport layer. The organic layer **314** does not necessarily include the light-emitting layer. For example, the organic layer **314** includes one or more of an electron-injection layer, an electron-transport layer, a hole-injection layer, and a hole-transport layer.

[0794] Here, the uppermost layer in the stacked-layer structure of each of the organic layer **312**R, the organic layer **312**B, and the organic layer **312**G, i.e., the layer in contact with the organic layer **314** is preferably a layer other than the light-emitting layer. For example, a structure is preferable in which an electron-injection layer, an electron-transport layer, a hole-injection layer, a hole-transport layer, or a layer other than those covers the light-emitting layer so as to be in contact with the organic layer **314**. When the top surface of the light-emitting layer is protected by another layer in manufacturing each light-emitting device, the reliability of the light-emitting device can be improved.

[0795] By processing the EL layers by a photolithography method, the distance between pixels can be shortened to less than or equal to 8 μm, less than or equal to 3 μm, less than or equal to 2 m, or less than or equal to 1 μm. Here, the distance between pixels can be determined by the distance between opposite end portions of the organic layer **312**B and the organic layer **312**R, the distance between opposite end portions of the organic layer **312**B and the organic layer **312**G, and the distance between opposite end portions of the organic layer **312**R and the organic layer **312**G, for example. Alternatively, the distance between pixels can be determined by the distance between opposite end portions of adjacent EL layers for the same color. Alternatively, the distance between pixels can be determined by the distance between opposite end portions of the adjacent pixel electrodes **311**. The distance between pixels is shortened in this manner, whereby a display apparatus with high definition and a high aperture ratio can be provided.

[0796] The pixel electrode **311** is provided for each element. The common electrode **313** and the organic layer **314** are provided as continuous layers common to the light-emitting devices. A conductive film that transmits visible light is used for either the respective pixel electrodes or the common electrode **313**, and a reflective conductive film is used for the other. When the respective pixel electrodes transmit light and the common electrode **313** reflects light, a bottom-emission display apparatus is obtained. When the respective pixel electrodes reflect light and the common electrode **313** transmits light, a top-emission display apparatus is obtained. Note that when both the respective pixel electrodes and the common electrode **313** transmit light, a dual-emission display apparatus can be obtained.

[0797] The pixel electrode **311** is electrically connected to a transistor provided in a semiconductor circuit of the substrate **101**. The transistor provided on the substrate **101** has a reduced channel length and is miniaturized as described in the above embodiment. For this reason, even when the display apparatus has high definition and the pixel area is reduced, the pixel circuit can be disposed in the reduced pixel area.

[0798] The insulating layer **331** is provided to cover end portions of the pixel electrode **311**. The end portions of the insulating layer **331** preferably have tapered shapes. Note that in this specification and the like, an end portion of an object having a tapered shape indicates that the end portion of the object has a cross-sectional shape in which the angle between a surface of the object and a formation surface of

the object is greater than 0° and less than 90° in a region of the end portion, and the thickness continuously increases from the end portion.

[0799] When an organic resin is used for the insulating layer **331**, a surface of the insulating layer **331** can be moderately curved. Thus, coverage with a film formed over the insulating layer **331** can be improved.

[0800] Examples of materials that can be used for the insulating layer **331** include an acrylic resin, a polyimide resin, an epoxy resin, a polyamide resin, a polyimide-amide resin, a siloxane resin, a benzocyclobutene-based resin, a phenol resin, and precursors of these resins.

[0801] Alternatively, an inorganic insulating material may be used for the insulating layer **331**. As the insulating layer **331**, for example, as an oxide, an oxynitride, a nitride oxide, or a nitride can be used. As the insulating layer **331**, for example, one or more kinds of a silicon oxide film, a silicon oxynitride film, a silicon nitride oxide film, a silicon nitride film, an aluminum oxide film, an aluminum oxynitride film, a hafnium oxide film, an yttrium oxide film, a zirconium oxide film, a gallium oxide film, a tantalum oxide film, a magnesium oxide film, a lanthanum oxide film, a cerium oxide film, and a neodymium oxide film can be used.

[0802] As illustrated in FIG. **47**B, there are gaps between two organic layers of light-emitting devices that emit light of different colors and between two organic layers of the light-emitting device and the light-receiving device, and the two organic layers are provided apart from each other. The organic layer **312**R, the organic layer **312**B, and the organic layer **312**G are thus preferably provided so as not to be in contact with each other. This favorably prevents unintentional light emission from being caused by a current flowing through adjacent two organic layers. As a result, the contrast can be increased to achieve a display apparatus with high display quality.

[0803] The organic layer **312**R, the organic layer **312**B, and the organic layer **312**G each preferably have a taper angle greater than or equal to 30°. In an end portion of each of the organic layer **312**R, the organic layer **312**G, and the organic layer **312**B, the angle between the side surface (the surface) of the layer and the bottom surface (the formation surface) of the layer is preferably greater than or equal to 30° and less than or equal to 120°, further preferably greater than or equal to 45° and less than or equal to 120°, still further preferably greater than or equal to 60° and 120°. Alternatively, the organic layer **312**R, the organic layer **312**G, and the organic layer **312**B each preferably have a taper angle of 90° or the neighborhood thereof (greater than or equal to 80° and less than or equal to 100°, for example).

[0804] A protective layer **321** is provided over the common electrode **313**. The protective layer **321** has a function of preventing diffusion of impurities such as water into each light-emitting device from the above.

[0805] The protective layer **321** can have, for example, a single-layer structure or a stacked-layer structure including at least an inorganic insulating film. As the inorganic insulating film, one or more of an oxide film, an oxynitride film, a nitride oxide film, and a nitride film can be used. For example, as the protective layer **321**, it is possible to use one or more of a silicon oxide film, a silicon oxynitride film, a silicon nitride oxide film, a silicon nitride film, an aluminum oxide film, an aluminum oxynitride film, or a hafnium oxide film. Alternatively, a semiconductor material may be used for the protective layer **321**. For example, one or more of an indium gallium oxide or an indium gallium zinc oxide may be used for the protective layer **321**.

[0806] As the protective layer **321**, a stacked film of an inorganic insulating film and an organic insulating film can be used. For example, a structure in which an organic insulating film is sandwiched between a pair of inorganic insulating films is preferable. Furthermore, it is preferable that the organic insulating film function as a planarization film. With this structure, the top surface of the organic insulating film can be flat, and accordingly, coverage with the inorganic insulating film over the organic insulating film is improved, leading to an improvement in a barrier property. Moreover, since the top surface of the protective layer **321** is flat, a preferable effect can be obtained; when a component (e.g., a color filter, an electrode of a touch sensor, or a lens array) is provided above the protective layer **321**, the component is less affected by an uneven shape caused by the lower structure.

[0807] In the connection portion **330**, the common electrode **313** is provided on and in contact with the connection electrode **311**C, and the protective layer **321** is provided to cover the common electrode **313**. In addition, the insulating layer **331** is provided to cover end portions of the connection electrode **311**C.

[0808] Structure examples of display apparatuses whose structures are partly different from that in FIG. **47**B are described below. Specifically, an example in which the insulating layer **331** is not provided is described.

[0809] FIG. **48**A to FIG. **48**C show examples of the case where the side surface of the pixel electrode **311** is substantially aligned with the side surfaces of the organic layer **312**R, the organic layer **312**B, or the organic layer **312**G.

[0810] In FIG. **48**A, the organic layer **314** is provided to cover the top surfaces and the side surfaces of the organic layer **312**R, the organic layer **312**B, and the organic layer **312**G. The organic layer **314** can prevent the pixel electrode **311** and the common electrode **313** from being in contact with each other and being electrically short-circuited.

[0811] FIG. **48**B shows an example in which an insulating layer **325** is provided in contact with the side surfaces of the organic layer **312**R, the organic layer **312**B, the organic layer **312**G, and the pixel electrode **311**. The insulating layer **325** can prevent the pixel electrode **311** and the common electrode **313** from being electrically short-circuited and effectively inhibit a leakage current therebetween.

[0812] The insulating layer **325** can be an insulating layer including an inorganic material. As the insulating layer **325**, an inorganic insulating film such as an oxide insulating film, a nitride insulating film, an oxynitride insulating film, or a nitride oxide insulating film can be used, for example. The insulating layer **325** may have a single-layer structure or a stacked-layer structure. Examples of the oxide insulating film include a silicon oxide film, an aluminum oxide film, a magnesium oxide film, an indium-gallium-zinc oxide film, a gallium oxide film, a germanium oxide film, an yttrium oxide film, a zirconium oxide film, a lanthanum oxide film, a neodymium oxide film, a hafnium oxide film, and a tantalum oxide film. Examples of the nitride insulating film include a silicon nitride film and an aluminum nitride film. Examples of the oxynitride insulating film include a silicon oxynitride film and an aluminum oxynitride film. Examples of the nitride oxide insulating film include a silicon nitride oxide film and an aluminum nitride oxide film. In particular, when an inorganic insulating film such as an aluminum

oxide film, a hafnium oxide film, or a silicon oxide film formed by an ALD method is used as the insulating layer **325**, the insulating layer **325** can have a small number of pin holes and excel in a function of protecting the organic layer.

[0813] The insulating layer **325** can be formed by a sputtering method, a CVD method, a PLD method, an ALD method, or the like. The insulating layer **325** is preferably formed by an ALD method achieving good coverage.

[0814] In FIG. **48**C, resin layers **326** are provided between two adjacent light-emitting devices and between the light-emitting device and the light-receiving device so as to fill the gap between two facing pixel electrodes and the gap between two facing organic layers. The resin layer **326** can planarize the formation surface of the organic layer **314**, the common electrode **313**, and the like, which prevents disconnection of the common electrode **313** due to poor coverage in a step between adjacent light-emitting devices.

[0815] An insulating layer containing an organic material can be suitably used as the resin layer **326**. For the resin layer **326**, for example, it is possible to use an acrylic resin, a polyimide resin, an epoxy resin, an imide resin, a polyamide resin, a polyimide-amide resin, a silicone resin, a siloxane resin, a benzocyclobutene-based resin, a phenol resin, precursors of these resins, or the like. Alternatively, for the resin layer **326**, an organic material such as polyvinyl alcohol (PVA), polyvinyl butyral, polyvinylpyrrolidone, polyethylene glycol, polyglycerin, pullulan, water-soluble cellulose, or an alcohol-soluble polyamide resin may be used. Moreover, for the resin layer **326**, a photosensitive resin can be used. A photoresist may be used for the photosensitive resin. As the photosensitive resin, a positive photosensitive material or a negative photosensitive material can be used.

[0816] A colored material (e.g., a material containing a black pigment) may be used for the resin layer **326** so that the resin layer **326** has a function of blocking stray light from an adjacent pixel and inhibiting color mixture.

[0817] In FIG. **48**D, the insulating layer **325** and the resin layer **326** over the insulating layer **325** are provided. Since the insulating layer **325** prevents the organic layer **312**R or the like from being in contact with the resin layer **326**, impurities (e.g., water) included in the resin layer **326** can be prevented from being diffused into the organic layer **312**R or the like, whereby a highly reliable display apparatus can be provided.

[0818] A reflective film (e.g., a metal film containing one or more of silver, palladium, copper, titanium, aluminum, and the like) may be provided between the insulating layer **325** and the resin layer **326** so that light emitted from the light-emitting layer is reflected by the reflective film; hence, the display apparatus may be provided with a function of increasing the light extraction efficiency.

[0819] FIG. **49**A to FIG. **49**C show examples in which the width of the pixel electrode **311** is larger than the width of the organic layer **312**R, the organic layer **312**B, or the organic layer **312**G. The organic layer **312**R or the like is provided on the inner side than end portions of the pixel electrode **311**.

[0820] FIG. **49**A shows an example in which the insulating layer **325** is provided. The insulating layer **325** is provided to cover the side surfaces of the organic layers included in the light-emitting device and the light-receiving device and part of the top surface and the side surfaces of the pixel electrode **311**.

[0821] FIG. **49**B shows an example in which the resin layer **326** is provided. The resin layer **326** is positioned between two adjacent light-emitting devices or between the light-emitting device and the light-receiving device, and covers the side surfaces of the organic layers and the top surface and the side surfaces of the pixel electrode **311**.

[0822] FIG. **49**C shows an example in which both the insulating layer **325** and the resin layer **326** are provided. The insulating layer **325** is provided between the organic layer **312**R or the like and the resin layer **326**.

[0823] FIG. **50**A to FIG. **50**D show examples in which the width of the pixel electrode **311** is smaller than the width of the organic layer **312**R, the organic layer **312**B, or the organic layer **312**G. The organic layer **312**R or the like extends to an outer side beyond the end portions of the pixel electrode **311**.

[0824] FIG. **50**B shows an example in which the insulating layer **325** is provided. The insulating layer **325** is provided in contact with the side surfaces of the organic layers of two adjacent light-emitting devices. The insulating layer **325** may be provided to cover not only the side surface but also part of the top surface of the organic layer **312**R or the like.

[0825] FIG. **50**C shows an example in which the resin layer **326** is provided. The resin layer **326** is positioned between two adjacent light-emitting devices and covers the side surface and part of the top surface of the organic layer **312**R or the like. The resin layer **326** may be formed to be in contact with the side surface of the organic layer **312**R or the like and not to cover the top surface thereof.

[0826] FIG. **50**D shows an example in which both the insulating layer **325** and the resin layer **326** are provided. The insulating layer **325** is provided between the organic layer **312**R or the like and the resin layer **326**.

[0827] Here, a structure example of the resin layer **326** is described.

[0828] The top surface of the resin layer **326** is preferably as flat as possible; however, the surface of the resin layer **326** may be depressed or projecting depending on an uneven shape of the formation surface of the resin layer **326**, the formation conditions of the resin layer **326**, or the like.

[0829] FIG. **51**A to FIG. **52**F are each an enlarged view of an end portion of a pixel electrode **311**R included in the light-emitting device **61**R, an end portion of a pixel electrode **311**G included in the light-emitting device **61**G, and the vicinity thereof.

[0830] FIG. **51**A, FIG. **51**B, and FIG. **51**C are each an enlarged view of the resin layer **326** having a flat top surface and the vicinity thereof. FIG. **51**A shows an example of the case where the organic layer **312**R or the like has a larger width than the pixel electrode **311**. FIG. **51**B shows an example in which these widths are substantially the same. FIG. **51**C shows an example of the case where the organic layer **312**R or the like has a smaller width than the pixel electrode **311**.

[0831] The organic layer **312**R or the like is provided to cover the end portions of the pixel electrode **311** as illustrated in FIG. **51**A, so that the end portion of the pixel electrode **311** preferably has a tapered shape. Accordingly, the step coverage with the organic layer **312**R or the like is improved and a highly reliable display apparatus can be provided.

[0832] FIG. **51**D, FIG. **51**E, and FIG. **51**F illustrate examples of the case where the top surface of the resin layer

326 has a depressed portion. Here, FIG. **51**D, FIG. **51**E and FIG. **51**F correspond to FIG. **51**A, FIG. **51**B, and FIG. **51**C, respectively. In this case, a depressed portion that reflects the depressed top surface of the resin layer **326** is formed on each of the top surfaces of the organic layer **314**, the common electrode **313**, and the protective layer **321**.

[0833] FIG. **52**A, FIG. **52**B, and FIG. **52**C illustrate examples of the case where the top surface of the resin layer **326** is projecting. Here, FIG. **52**A, FIG. **52**B, and FIG. **52**C correspond to FIG. **51**A, FIG. **51**B, and FIG. **51**C, respectively. In this case, a projecting portion that reflects the projecting top surface of the resin layer **326** is formed on each of the top surfaces of the organic layer **314**, the common electrode **313**, and the protective layer **321**.

[0834] FIG. **52**D, FIG. **52**E, and FIG. **52**F illustrate examples of the case where part of the resin layer **326** covers an upper end portion and part of the top surface of the organic layer **312**R and an upper end portion and part of atop surface of the organic layer **312**G. Here, FIG. **52**D, FIG. **52**E, and FIG. **52**F correspond to FIG. **51**A, FIG. **51**B, and FIG. **51**C, respectively. Here, the insulating layer **325** is provided between the resin layer **326** and the top surfaces of the organic layer **312**R and the organic layer **312**G.

[0835] FIG. **52**D, FIG. **52**E, and FIG. **52**F illustrate examples of the case where the top surface of the resin layer **326** is partly depressed. In this case, unevenness that reflects the shape of the resin layer **326** is formed on each of the organic layer **314**, the common electrode **313**, and the protective layer **321**.

[0836] The above is the description of the structure example of the resin layer.

[0837] The structure described in this embodiment can be used in an appropriate combination with any of the structures described in the other embodiments.

Embodiment 5

[0838] In this embodiment, electronic devices in which the semiconductor device of one embodiment of the present invention can be used will be described.

[0839] The semiconductor device of one embodiment of the present invention can be used in a display portion of an electronic device. Thus, an electronic device with high display quality can be obtained. An electronic device with an extremely high definition can be obtained. A highly reliable electronic device can be obtained.

[0840] Examples of electronic devices including the semiconductor device or the like of one embodiment of the present invention include display apparatuses such as televisions and monitors, lighting devices, desktop or laptop personal computers, word processors, image reproduction devices which reproduce still images or moving images stored in recording media such as DVDs (Digital Versatile Discs), portable CD players, radios, tape recorders, headphone stereos, stereos, table clocks, wall clocks, cordless phone handsets, transceivers, car phones, cellular phones, portable information terminals, tablet terminals, portable game machines, stationary game machines such as pachinko machines, calculators, electronic notebooks, e-book readers, electronic translators, audio input devices, video cameras, digital still cameras, electric shavers, high-frequency heating appliances such as microwave ovens, electric rice cookers, electric washing machines, electric vacuum cleaners, water heaters, electric fans, hair dryers, air-conditioning systems such as air conditioners, humidifiers, and dehumidifiers, dishwashers, dish dryers, clothes dryers, futon dryers, electric refrigerators, electric freezers, electric refrigerator-freezers, freezers for preserving DNA, flashlights, tools such as chain saws, smoke detectors, and medical equipment such as dialyzers. Other examples include industrial equipment such as guide lights, traffic lights, conveyor belts, elevators, escalators, industrial robots, power storage systems, and power storage devices for leveling the amount of power supply and smart grid. In addition, moving objects and the like driven by fuel engines or electric motors using electric power from power storage units may also be included in the category of electronic devices. Examples of the moving objects include electric vehicles (EVs), hybrid electric vehicles (HVs) that include both an internal-combustion engine and a motor, plug-in hybrid electric vehicles (PHVs), tracked vehicles in which caterpillar tracks are substituted for wheels of these vehicles, motorized bicycles including motor-assisted bicycles, motorcycles, electric wheelchairs, golf carts, boats, ships, submarines, helicopters, aircraft, rockets, artificial satellites, space probes, planetary probes, and spacecraft.

[0841] The electronic device of one embodiment of the present invention may include a secondary battery (battery), and it is preferable that the secondary battery be capable of being charged by contactless power transmission.

[0842] Examples of the secondary battery include a lithium ion secondary battery, a nickel-hydride battery, a nickel-cadmium battery, an organic radical battery, a lead-acid battery, an air secondary battery, a nickel-zinc battery, and a silver-zinc battery.

[0843] The electronic device of one embodiment of the present invention may include an antenna. With the antenna receiving a signal, the electronic device can display an image, information, and the like on the display portion. When the electronic device includes an antenna and a secondary battery, the antenna may be used for contactless power transmission.

[0844] The electronic device of one embodiment of the present invention may include a sensor (a sensor having a function of measuring force, displacement, position, speed, acceleration, angular velocity, rotational frequency, distance, light, liquid, magnetism, temperature, a chemical substance, sound, time, hardness, an electric field, current, voltage, electric power, radioactive rays, flow rate, humidity, a gradient, oscillation, odor, or infrared rays).

[0845] The electronic device of one embodiment of the present invention can have a variety of functions. For example, the electronic device can have a function of displaying a variety of information (a still image, a moving image, a text image, and the like) on the display portion, a touch panel function, a function of displaying a calendar, date, time, and the like, a function of executing a variety of software (programs), a wireless communication function, and a function of reading out a program or data stored in a recording medium.

[0846] Furthermore, an electronic device including a plurality of display portions can have a function of displaying image information mainly on one display portion while displaying text information mainly on another display portion, a function of displaying a three-dimensional image made up of images with parallax taken into account displayed on a plurality of display portions, or the like. Furthermore, an electronic device including an image receiving portion can have a function of taking a still image or a

moving image, a function of automatically or manually correcting a taken image, a function of storing a taken image in a recording medium (an external recording medium or a recording medium incorporated in the electronic device), a function of displaying a taken image on a display portion, or the like. Note that functions of the electronic device of one embodiment of the present invention are not limited thereto, and the electronic devices can have a variety of functions.

[0847] The semiconductor device of one embodiment of the present invention can display high-definition images. Thus, the semiconductor device of one embodiment of the present invention can be suitably used especially for a portable electronic device, a wearable electronic device (wearable device), an e-book reader, and the like. For example, the semiconductor device can be suitably used for xR devices such as a VR device and an AR device.

[0848] FIG. **53**A is an external view of a camera **8000** to which a finder **8100** is attached.

[0849] The camera **8000** includes a housing **8001**, a display portion **8002**, operation buttons **8003**, a shutter button **8004**, and the like. In addition, a detachable lens **8006** is attached to the camera **8000**. Note that the lens **8006** and the housing may be integrated with each other in the camera **8000**.

[0850] Images can be taken with the camera **8000** at the press of the shutter button **8004** or the touch of the display portion **8002** serving as a touch panel.

[0851] The housing **8001** includes a mount including an electrode, so that the finder **8100**, a stroboscope, or the like can be connected to the housing **8001**.

[0852] The finder **8100** includes a housing **8101**, a display portion **8102**, a button **8103**, and the like.

[0853] The housing **8101** is attached to the camera **8000** with the mount engaging with a mount of the camera **8000**. The finder **8100** can display, for example, a video received from the camera **8000** on the display portion **8102**.

[0854] The button **8103** has a function of a power supply button or the like.

[0855] The semiconductor device of one embodiment of the present invention can be used in the display portion **8002** of the camera **8000** and the display portion **8102** of the finder **8100**. Note that the finder **8100** may be incorporated in the camera **8000**.

[0856] FIG. **53**B is an external view of a head-mounted display **8200**.

[0857] The head-mounted display **8200** includes a wearing portion **8201**, a lens **8202**, a main body **8203**, a display portion **8204**, a cable **8205**, and the like. A battery **8206** is incorporated in the mounting portion **8201**.

[0858] The cable **8205** supplies electric power from the battery **8206** to the main body **8203**. The main body **8203** includes a wireless receiver or the like to receive image data and display it on the display portion **8204**. The main body **8203** includes a camera, and data on the movement of eyeballs or eyelids of a user can be used as an input means.

[0859] The mounting portion **8201** may be provided with a plurality of electrodes capable of sensing a current flowing in response to the movement of the user's eyeball in a position in contact with the user to have a function of recognizing the user's sight line. Furthermore, the mounting portion **8201** may have a function of monitoring the user's pulse with use of the current flowing through the electrodes. The mounting portion **8201** may include sensors such as a temperature sensor, a pressure sensor, and an acceleration sensor so that the user's biological information can be displayed on the display portion **8204** and an image displayed on the display portion **8204** can be changed in accordance with the movement of the user's head.

[0860] The semiconductor device of one embodiment of the present invention can be used in the display portion **8204**.

[0861] FIG. **53**C to FIG. **53**E are external views of a head-mounted display **8300**. The head-mounted display **8300** includes a housing **8301**, a display portion **8302**, a band-like fixing member **8304**, and a pair of lenses **8305**.

[0862] A user can perceive display on the display portion **8302** through the lenses **8305**. Note that the display portion **8302** is preferably placed in the curved state, in which case the user can feel a high realistic sensation. Another image displayed in another region of the display portion **8302** is viewed through the lenses **8305**, so that three-dimensional display using parallax or the like can be performed. Note that the structure is not limited to the structure in which one display portion **8302** is provided; two display portions **8302** may be provided and one display portion may be provided per eye of the user.

[0863] The semiconductor device of one embodiment of the present invention can be used for the display portion **8302**. The semiconductor device of one embodiment of the present invention can achieve extremely high definition. For example, a pixel is not easily seen by the user even when the user sees display that is magnified by the lenses **8305** as illustrated in FIG. **53**E. In other words, a video with a strong sense of reality can be seen by the user with use of the display portion **8302**.

[0864] FIG. **53**F is an external view of a goggles-type head-mounted display **8400**. The head-mounted display **8400** includes a pair of housings **8401**, a mounting portion **8402**, and a cushion **8403**. A display portion **8404** and a lens **8405** are provided in each of the pair of housings **8401**. The pair of display portions **8404** may display different images, whereby three-dimensional display using parallax can be performed.

[0865] A user can see display on the display portion **8404** through the lens **8405**. The lens **8405** has a focus adjustment mechanism and can adjust the position according to the user's eyesight. The display portion **8404** is preferably a square or a horizontal rectangle. This can improve a realistic sensation.

[0866] The mounting portion **8402** preferably has plasticity and elasticity so as to be adjusted to fit the size of the user's face and not to slide down. In addition, part of the mounting portion **8402** preferably has a vibration mechanism functioning as a bone conduction earphone. Thus, without additionally requiring an audio device such as earphones or a speaker, the user can enjoy video and sound only by wearing the head-mounted display **8400**. Note that the housing **8401** may have a function of outputting sound data by wireless communication.

[0867] The mounting portion **8402** and the cushion **8403** are portions in contact with the user's face (forehead, cheek, or the like). The cushion **8403** is in close contact with the user's face, so that light leakage can be prevented, which increases the sense of immersion. The cushion **8403** is preferably formed using a soft material so that the head-mounted display **8400** is in close contact with the user's face when being worn by the user. For example, a material such as rubber, silicone rubber, urethane, or sponge can be used.

Furthermore, when a sponge or the like whose surface is covered with cloth, leather (natural leather or synthetic leather), or the like is used, a gap is unlikely to be generated between the user's face and the cushion **8403**, whereby light leakage can be suitably prevented. Furthermore, using such a material is preferable because it has a soft texture and the user does not feel cold when wearing the head-mounted display **8400** in a cold season, for example. The member to be in contact with the user's skin, such as the cushion **8403** or the wearing portion **8402**, is preferably detachable, in which case cleaning or replacement can be easily performed.

[0868] FIG. **54**A illustrates an example of a television device. In a television device **7100**, a display portion **7000** is incorporated in a housing **7101**. Here, a structure in which the housing **7101** is supported by a stand **7103** is illustrated.

[0869] The semiconductor device of one embodiment of the present invention can be used for the display portion **7000**.

[0870] Operation of the television device **7100** illustrated in FIG. **54**A can be performed with an operation switch provided in the housing **7101** and a separate remote controller **7111**. Alternatively, the display portion **7000** may include a touch sensor, and the television device **7100** may be operated by touch on the display portion **7000** with a finger or the like. The remote controller **7111** may be provided with a display portion for displaying information output from the remote controller **7111**. With operation keys or a touch panel provided in the remote controller **7111**, channels and volume can be controlled and videos displayed on the display portion **7000** can be controlled.

[0871] Note that the television device **7100** has a structure in which a receiver, a modem, and the like are provided. A general television broadcast can be received with the receiver. When the television device is connected to a communication network with or without wires via the modem, one-way (from a transmitter to a receiver) or two-way (between a transmitter and a receiver or between receivers, for example) data communication can be performed.

[0872] FIG. **54**B illustrates an example of a laptop personal computer. The laptop personal computer **7200** includes a housing **7211**, a keyboard **7212**, a pointing device **7213**, an external connection port **7214**, and the like. In the housing **7211**, the display portion **7000** is incorporated.

[0873] The semiconductor device of one embodiment of the present invention can be used for the display portion **7000**.

[0874] FIG. **54**C and FIG. **54**D illustrate examples of digital signage.

[0875] Digital signage **7300** illustrated in FIG. **54**C includes a housing **7301**, the display portion **7000**, a speaker **7303**, and the like. The digital signage **7300** can also include an LED lamp, an operation key (including a power switch or an operation switch), a connection terminal, a variety of sensors, a microphone, and the like.

[0876] FIG. **54**D is digital signage **7400** attached to a cylindrical pillar **7401**. The digital signage **7400** includes the display portion **7000** provided along a curved surface of the pillar **7401**.

[0877] In FIG. **54**C and FIG. **54**D, the semiconductor device of one embodiment of the present invention can be used for the display portion **7000**.

[0878] The larger display portion **7000** can provide a larger amount of information at a time. The larger display portion **7000** attracts more attention, so that the effectiveness of the advertisement can be increased, for example.

[0879] The use of a touch panel in the display portion **7000** is preferable because in addition to display of a still image or a moving image on the display portion **7000**, intuitive operation by a user is possible. Moreover, for an application for providing information such as route information or traffic information, usability can be enhanced by intuitive operation.

[0880] As illustrated in FIG. **54**C and FIG. **54**D, it is preferable that the digital signage **7300** or the digital signage **7400** be capable of working with an information terminal **7311** or an information terminal **7411** such as a smartphone a user has through wireless communication. For example, information of an advertisement displayed on the display portion **7000** can be displayed on a screen of the information terminal **7311** or the information terminal **7411**. By operation of the information terminal **7311** or the information terminal **7411**, display on the display portion **7000** can be switched.

[0881] It is possible to make the digital signage **7300** or the digital signage **7400** execute a game with use of the screen of the information terminal **7311** or the information terminal **7411** as an operation means (controller). Thus, an unspecified number of users can join in and enjoy the game concurrently.

[0882] An information terminal **7550** illustrated in FIG. **54**E includes a housing **7551**, a display portion **7552**, a microphone **7557**, a speaker portion **7554**, a camera **7553**, operation switches **7555**, and the like. For example, the semiconductor device of one embodiment of the present invention can be used for the display portion **7552**. The display portion **7552** has a function of a touch panel. The information terminal **7550** also includes an antenna, a battery, and the like inside the housing **7551**. The information terminal **7550** can be used as, for example, a smartphone, a mobile phone, a tablet information terminal, a tablet personal computer, an e-book reader, or the like.

[0883] The semiconductor device of one embodiment of the present invention can be suitably used in the display portion **7552**.

[0884] FIG. **54**F illustrates an example of a watch-type information terminal. An information terminal **7660** includes a housing **7661**, a display portion **7662**, a band **7663**, a buckle **7664**, an operation switch **7665**, an input/output terminal **7666**, and the like. In addition, the information terminal **7660** includes an antenna, a battery, and the like inside the housing **7661**. The information terminal **7660** is capable of executing a variety of applications such as mobile phone calls, e-mailing, viewing and editing texts, music reproduction, Internet communication, and a computer game.

[0885] The semiconductor device of one embodiment of the present invention can be suitably used in the display portion **7662**.

[0886] The display portion **7662** includes a touch sensor, and operation can be performed by touching the screen with a finger, a stylus, or the like. For example, with a touch on an icon **7667** displayed on the display portion **7662**, an application can be started. The operation switches **7665** can have a variety of functions such as time setting, power on/off operation, on/off operation of wireless communication, setting and cancellation of a silent mode, and setting and cancellation of a power saving mode. For example, the

functions of the operation switches **7665** can be set by the operation system incorporated in the information terminal **7660**.

[0887] The information terminal **7660** can execute near field communication conformable to a communication standard. For example, mutual communication between the information terminal **7660** and a headset capable of wireless communication enables hands-free calling. The information terminal **7660** includes the input/output terminal **7666**, and can perform data transmission and reception with another information terminal through the input/output terminal **7666**. In addition, charging can be performed via the input/output terminal **7666**. Note that the charging operation may be performed by wireless power feeding without using the input/output terminal **7666**.

[0888] The structure described in this embodiment can be used in combination as appropriate with any of the structures described in the other embodiments and Example.

REFERENCE NUMERALS

[0889] ANO: wiring, C**31**: capacitor, C**41**: capacitor, GL: wiring, INV: inverter circuit, LAT: latch circuit, LIN: terminal, ROUT: terminal, SL: wiring, SMP: terminal, Tr**31**: transistor, Tr**33**: transistor, Tr**35**: transistor, Tr**36**: transistor, Tr**41**: transistor, Tr**43**: transistor, Tr**45**: transistor, Tr**47**: transistor, VCOM: wiring, **10**A: semiconductor device, **10**B: semiconductor device, **10**C: semiconductor device, **10**D: semiconductor device, **10**E: semiconductor device, **10**F: semiconductor device, **10**G: semiconductor device, **10**H: semiconductor device, **10**J: semiconductor device, **10**K: semiconductor device, **10**: semiconductor device, **50**A: display apparatus, **50**: display apparatus, **51**A: pixel circuit, **51**: pixel circuit, **52**A: transistor, **52**B: transistor, **52**C: transistor, **53**: capacitor, **61**B: light-emitting device, **61**G: light-emitting device, **61**R: light-emitting device, **61**: light-emitting device, **100_1**: transistor, **100_2**: transistor, **100_3**: transistor, **100_4**: transistor, **100_*p***: transistor, **100_*q***: transistor, **100**A: transistor, **100**B: transistor, **100**C: transistor, **100**D: transistor group, **100**E: transistor group, **100**: transistor, **101**: substrate, **102**: substrate, **104*f*** conductive film, **104**: conductive layer, **106**A: insulating layer, **106**B: insulating layer, **106**C: insulating layer, **106**D: insulating layer, **106**: insulating layer, **107**: insulating layer, **108_1**: semiconductor layer, **108_2**: semiconductor layer, **108_3**: semiconductor layer, **108_4**: semiconductor layer, **108**D: region, **108*f*** metal oxide film, **108**L: region, **108**: semiconductor layer, **109**: semiconductor layer, **110*a***: insulating layer, **110*af***: insulating film, **110*b***: insulating layer, **110*bf*** insulating film, **110*c***: insulating layer, **110*cf*** insulating film, **110*f*** insulating film, **110**: insulating layer, **111**B: pixel electrode, **111**G: pixel electrode, **111**R: pixel electrode, **111**: pixel electrode, **112*a***: conductive layer, **112*a*_1**: conductive layer, **112*a***_if conductive film, **112*a*_2**: conductive layer, **112*a*_2**A: conductive layer, **112*a*_2*f*** conductive film, **112**B: conductive layer, **112*b***: conductive layer, **112*c***: conductive layer, **112*c*_1**: conductive layer, **112*c*_2**: conductive layer, **112*d***: conductive layer, **112*e***: conductive layer, **112*e*_1**: conductive layer, **112*e*_2**: conductive layer, **112*f*** conductive film, **113**B: layer, **113**G: layer, **113**R: layer, **114**: common layer, **115**: common electrode, **116*a***: conductive layer, **116*b***: conductive layer, **117**: light-blocking layer, **118**B: mask layer, **118**G: mask layer, **118**R: mask layer, **119**B: mask layer, **119**G: mask layer, **119**R: mask layer, **120*a***: insulating layer, **120*b***: insulating layer, **120*f*** insulating film, **120**: insulating layer, **123**: conductive layer, **124**B: conductive layer, **124**G: conductive layer, **124*p***: conductive layer, **124*q***: conductive layer, **124**R: conductive layer, **125**: insulating layer, **126**B: conductive layer, **126**G: conductive layer, **126*p***: conductive layer, **126*q***: conductive layer, **126**R: conductive layer, **127**: insulating layer, **128**: layer, **129**B: conductive layer, **129**G: conductive layer, **129*p***: conductive layer, **129*q***: conductive layer, **129**R: conductive layer, **130**B: light-emitting device, **130**G: light-emitting device, **130**R: light-emitting device, **131**: protective layer, **133**: opening, **135**: opening, **137*a***: opening, **137*b***: opening, **139*a***: opening, **139*b***: opening, **140**: connection portion, **141_1**: opening, **141_4**: opening, **141**: opening, **142**: adhesive layer, **1431**: opening, **143_2**: opening, **143_3**: opening, **143_4**: opening, **143**: opening, **145_1**: opening, **145_2**: opening, **145_3**: opening, **145_4**: opening, **145**: opening, **147*a***: opening, **147*b***: opening, **149**: opening, **150**: insulating layer, **152**: substrate, **153**: insulating layer, **165**: wiring, **166**: conductive layer, **172**: FPC, **173**: IC, **180**: metal oxide layer, **190**: impurity, **195**: insulating layer, **197**: insulating layer, **199**: insulating layer, **200**A: transistor, **200**B: transistor, **200**C: transistor, **200**D: transistor, **200**E: transistor, **200**F: transistor, **200**G: transistor, **200**H: transistor, **200**: transistor, **201**: transistor, **202_1**: conductive layer, **202_2**: conductive layer, **202**: conductive layer, **203**: conductive layer, **204**: conductive layer, **205**G: transistor, **205**R: transistor, **206**: conductive layer, **208**D: region, **208**L: region, **208**: semiconductor layer, **210*a***: insulating layer, **210*b***: insulating layer, **210*c***: insulating layer, **210**: insulating layer, **212*a***: conductive layer, **212*b***: conductive layer, **214**: connection portion, **230*a***: pixel, **230*b***: pixel, **230*c***: pixel, **230*d***: pixel, **230*e***: pixel, **230**: pixel, **231**: first driver circuit portion, **232**: second driver circuit portion, **233**: peripheral driver circuit, **235**: display portion, **236**: wiring, **237**: wiring, **239**: insulating layer, **240**A: pixel, **240**B: pixel, **240**: pixel, **242**: connection layer, **311**C: connection electrode, **311**G: pixel electrode, **311**R: pixel electrode, **311**: pixel electrode, **312**B: organic layer, **312**G: organic layer, **312**R: organic layer, **313**: common electrode, **314**: organic layer, **321**: protective layer, **325**: insulating layer, **326**: resin layer, **330**: connection portion, **331**: insulating layer, **761**: lower electrode, **762**: upper electrode, **763*a***: light-emitting unit, **763*b***: light-emitting unit, **763*c***: light-emitting unit, **763**: EL layer, **764**: layer, **771*a***: light-emitting layer, **771*b***: light-emitting layer, **771*c***: light-emitting layer, **771**: light-emitting layer, **772*a***: light-emitting layer, **772*b***: light-emitting layer, **772*c***: light-emitting layer, **772**: light-emitting layer, **773**: light-emitting layer, **780*a***: layer, **780*b***: layer, **780*c***: layer, **780**: layer, **781**: layer, **782**: layer, **785**: charge-generation layer, **790*a***: layer, **790*b***: layer, **790*c***: layer, **790**: layer, **791**: layer, **792**: layer, **7000**: display portion, **7100**: television device, **7101**: housing, **7103**: stand, **7111**: remote controller, **7200**: laptop personal computer, **7211**: housing, **7212**: keyboard, **7213**: pointing device, **7214**: external connection port, **7300**: digital signage, **7301**: housing, **7303**: speaker,

7311: information terminal, **7400**: digital signage, **7401**: pillar, **7411**: information terminal, **7550**: information terminal, **7551**: housing, **7552**: display portion, **7553**: camera, **7554**: speaker portion, **7555**: operation switch, **7557**: microphone, **7660**: information terminal, **7661**: housing, **7662**: display portion, **7663**: band, **7664**: buckle, **7665**: operation switch, **7666**: input/output terminal, **7667**: icon, **8000**: camera, **8001**: housing, **8002**: display portion, **8003**: operation button, **8004**: shutter button, **8006**: lens, **8100**: finder, **8101**: housing, **8102**: display portion, **8103**: button, **8200**: head-mounted display, **8201**: wearing portion, **8202**: lens, **8203**: main body, **8204**: display portion, **8205**: cable, **8206**: battery, **8300**: head-mounted display, **8301**: housing, **8302**: display portion, **8304**: fixing member, **8305**: lens, **8400**: head-mounted display, **8401**: housing, **8402**: mounting portion, **8403**: cushion, **8404**: display portion, **8405**: lens

1. A semiconductor device comprising:

a first transistor and a second transistor,

wherein the first transistor comprises a first conductive layer, a first insulating layer over the first conductive layer, a second insulating layer over the first insulating layer, a second conductive layer over the second insulating layer, a first semiconductor layer, a third insulating layer, and a third conductive layer,

wherein the first insulating layer, the second insulating layer, and the second conductive layer comprise an opening reaching the first conductive layer,

wherein the first semiconductor layer is in contact with a top surface and a side surface of the second conductive layer, a side surface of the first insulating layer, a side surface of the second insulating layer, and a top surface of the first conductive layer,

wherein the third insulating layer is over the first semiconductor layer,

wherein the third conductive layer is over the third insulating layer, and

wherein the second transistor comprises a second semiconductor layer over the second insulating layer, the third insulating layer over the second semiconductor layer, and a fourth conductive layer comprising a region overlapping with the second semiconductor layer with the third insulating layer therebetween.

2. A semiconductor device comprising:

a first transistor, a second transistor, and a substrate,

wherein the first transistor comprises a first conductive layer over the substrate, a first insulating layer over the first conductive layer, a second insulating layer over the first insulating layer, a second conductive layer over the second insulating layer, a first semiconductor layer, a third insulating layer, and a third conductive layer,

wherein the first insulating layer, the second insulating layer, and the second conductive layer comprise an opening reaching the first conductive layer,

wherein the first semiconductor layer is in contact with a top surface and a side surface of the second conductive layer, a side surface of the first insulating layer, a side surface of the second insulating layer, and a top surface of the first conductive layer,

wherein the third insulating layer is over the first semiconductor layer,

wherein the third conductive layer is over the third insulating layer,

wherein the second transistor comprises a second semiconductor layer over the second insulating layer, the third insulating layer over the second semiconductor layer, a fourth conductive layer comprising a region overlapping with the second semiconductor layer with the third insulating layer therebetween, and a fifth conductive layer over the substrate, and

wherein the fifth conductive layer comprises a region overlapping with the fourth conductive layer with the second semiconductor layer therebetween.

3. The semiconductor device according to claim **1**,

wherein the second transistor further comprises a fifth conductive layer over the first insulating layer, and

wherein the fifth conductive layer comprises a region overlapping with the fourth conductive layer with the second semiconductor layer therebetween.

4. The semiconductor device according to claim **1**, wherein each of the first semiconductor layer and the second semiconductor layer comprises a metal oxide.

5. The semiconductor device according to claim **1**, wherein the first semiconductor layer and the second semiconductor layer comprise a same material.

6. The semiconductor device according to claim **1**, wherein the third conductive layer and the fourth conductive layer comprise a same material.

7. The semiconductor device according to claim **1**,

wherein the first insulating layer comprises a fourth insulating layer, a fifth insulating layer over the fourth insulating layer, and a sixth insulating layer over the fifth insulating layer,

wherein the fourth insulating layer comprises a region having a higher film density than the fifth insulating layer, and

wherein the sixth insulating layer comprises a region having a higher film density than the fifth insulating layer.

8. The semiconductor device according to claim **1**,

wherein the first insulating layer comprises a fourth insulating layer, a fifth insulating layer over the fourth insulating layer, and a sixth insulating layer over the fifth insulating layer,

wherein the fourth insulating layer comprises a region having a higher nitrogen content than the fifth insulating layer, and

wherein the sixth insulating layer comprises a region having a higher nitrogen content than the fifth insulating layer.

9. The semiconductor device according to claim **1**,

wherein the second insulating layer comprises a seventh insulating layer and an eighth insulating layer over the seventh insulating layer, and

wherein the seventh insulating layer comprises a region having a higher film density than the eighth insulating layer.

10. The semiconductor device according to claim **1**,

wherein the second insulating layer comprises a seventh insulating layer and an eighth insulating layer over the seventh insulating layer, and

wherein the seventh insulating layer comprises a region having a higher nitrogen content than the eighth insulating layer.

11. A method for manufacturing a semiconductor device, comprising:

forming a first conductive film;

processing the first conductive film to form a first conductive layer and a second conductive layer;

forming a first insulating film over the first conductive layer and the second conductive layer;

forming a second conductive film over the first insulating film;

processing the first insulating film and the second conductive film to form a first insulating layer and a third conductive layer that have an opening in a region overlapping with the first conductive layer;

forming a first semiconductor layer being in contact with a top surface of the first conductive layer, a side surface of the first insulating layer, and a top surface and a side surface of the third conductive layer and a second semiconductor layer being in contact with a top surface of the first insulating layer;

forming a second insulating layer over the first semiconductor layer and the second semiconductor layer; and

forming, over the second insulating layer, a fourth conductive layer comprising a region overlapping with the first semiconductor layer and a fifth conductive layer comprising a region overlapping with the second semiconductor layer.

12. The semiconductor device according to claim **2**, wherein each of the first semiconductor layer and the second semiconductor layer comprises a metal oxide.

13. The semiconductor device according to claim **2**, wherein the first semiconductor layer and the second semiconductor layer comprise a same material.

14. The semiconductor device according to claim **2**, wherein the third conductive layer and the fourth conductive layer comprise a same material.

15. The semiconductor device according to claim **2**,

wherein the first insulating layer comprises a fourth insulating layer, a fifth insulating layer over the fourth insulating layer, and a sixth insulating layer over the fifth insulating layer,

wherein the fourth insulating layer comprises a region having a higher film density than the fifth insulating layer, and

wherein the sixth insulating layer comprises a region having a higher film density than the fifth insulating layer.

16. The semiconductor device according to claim **2**,

wherein the first insulating layer comprises a fourth insulating layer, a fifth insulating layer over the fourth insulating layer, and a sixth insulating layer over the fifth insulating layer,

wherein the fourth insulating layer comprises a region having a higher nitrogen content than the fifth insulating layer, and

wherein the sixth insulating layer comprises a region having a higher nitrogen content than the fifth insulating layer.

17. The semiconductor device according to claim **2**,

wherein the second insulating layer comprises a seventh insulating layer and an eighth insulating layer over the seventh insulating layer, and

wherein the seventh insulating layer comprises a region having a higher film density than the eighth insulating layer.

18. The semiconductor device according to claim **2**,

wherein the second insulating layer comprises a seventh insulating layer and an eighth insulating layer over the seventh insulating layer, and

wherein the seventh insulating layer comprises a region having a higher nitrogen content than the eighth insulating layer.

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