Cpr E 281 LAB07
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Lab 7 Answer Sheet

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Submission Instructions:

Prelab:

1. **Complete the prelab**
2. **Submit this report with the prelab completed to Canvas before your lab starts**

Lab:

1. **Complete the lab according to the instructions**
2. **Take screenshots of your ModelSim waveform (note: to receive points your NetID has to be present in the screenshot) and insert them into this document.**
3. **Include screenshots of any related block design files or Verilog files in the report**
4. **Complete this report and reupload it to Canvas**

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PRELAB:

Q1. Before you fill in the answers to this prelab make sure that you understand binary arithmentic, especially signed number representation (2's Complement) and overflow in arithmetic addition and subtraction Do the following arithmetic operations and write down the expected sum, carry and overfow:

In case of subtraction, since we are doing a 2's Complement addition Cout is the carryout of the adder.

Binary numbers to add/subtract	Sum	Cout	Overflow
1011 – 0110	**0101**	**1**	**1**
1001 - 0010	**0111**	**1**	**1**
0001 + 0111	1000	0	1
1100 + 0110	0010	1	0
0011 – 1101	0110	0	0
0101 + 1011	0000	1	0

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Q2. Complete the truth table for a full adder:

X	Y	Cin	Cout	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Q3. Complete the assignment expressions for S and Cout below:

```
module FA (X, Y, Cin, Cout, S);
input Cin, X, Y;
output Cout, S;
assign S = (expression for S);
assign Cout = (expression for Cout);
```

Expression for S: !X!YCin + !XY!Cin + X!Y!Cin + XYCin

Expression for Cout: !XYCin + X!YCin + XY!Cin + XYCin

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LAB:

<<Insert a screenshot of your BDF file (adder_4bit.bdf) here>>

<<Insert a screenshot of your BDF file (add_sub.bdf) here>>

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<<Insert a screenshot or copy your DO file here>>

<<< Insert a screenshot of your DO file waveform>>>