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Date: 9/9/2020

PRELAB:

Q1. Read section 3.0 and fill in the truth table below for Design 1 (*the farmer's problem*). Then use it to construct the POS expression.

Cabbage	Goat	Wolf	Alarm
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

POS Logic Expression: (C + !G + W) * (!C + G + !W) = Alarm

Q2. Read section 4.0 and fill in the truth table below for Design 2 (*adding the farmer*). Then use it to construct the SOP expressions.

Farmer	Cabbage	Goat	Wolf	Alarm
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

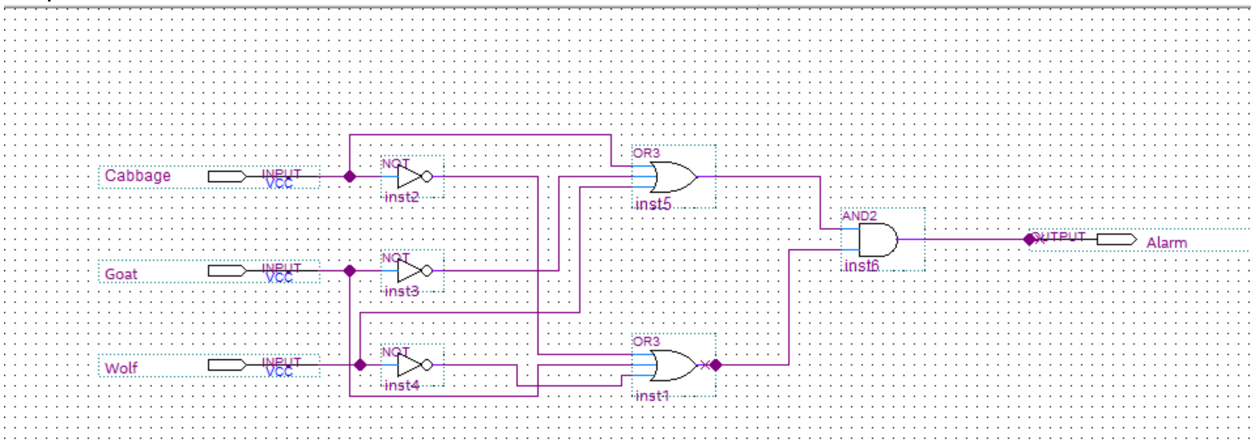
Canonical SOP Logic Expression: !F!CGW + !FCG!W + !FCGW + F!C!G!W + F!C!GW + FC!G!W = Alarm

Simplified SOP Logic Expression: F!C!G + !FGW + F!G!W + !FCG = Alarm

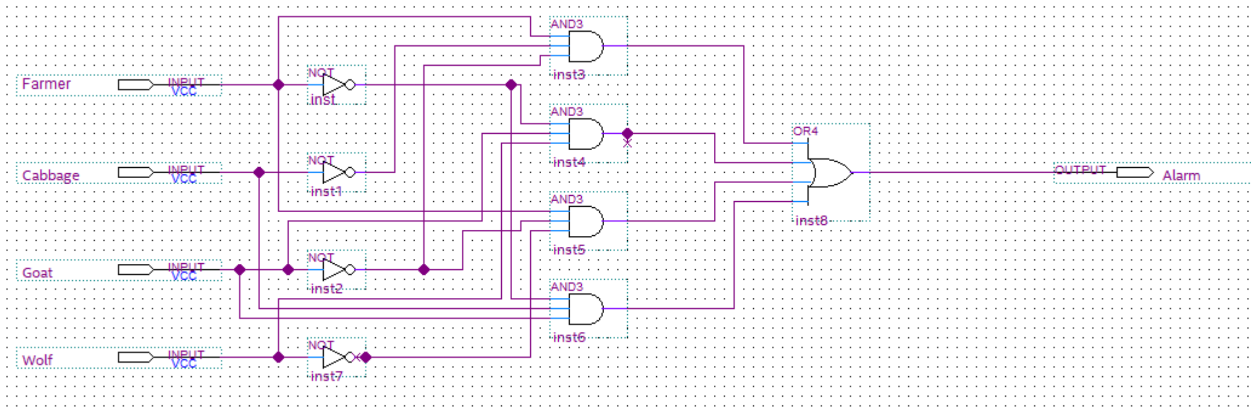
LAB:

3.0 Hardware results demonstrate correct code. TA Initials:
Schematic screenshot:

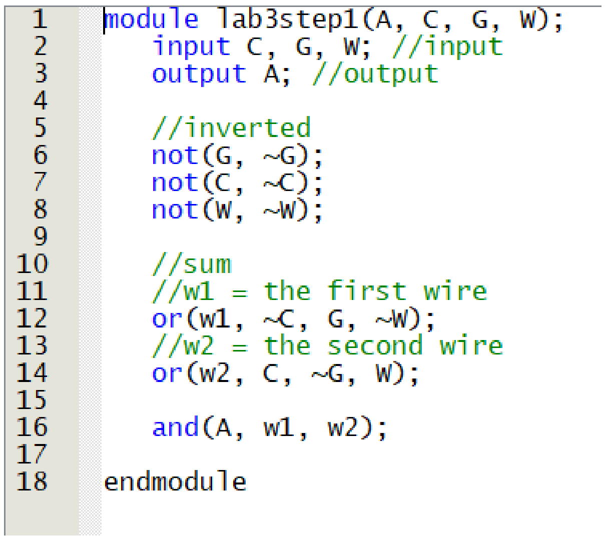
Step 0:



Step3:

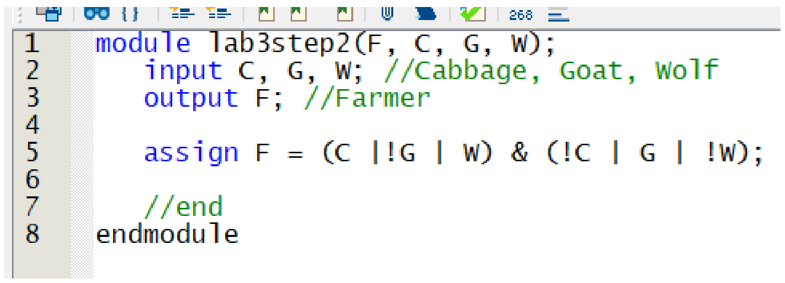


Structural Screenshots:

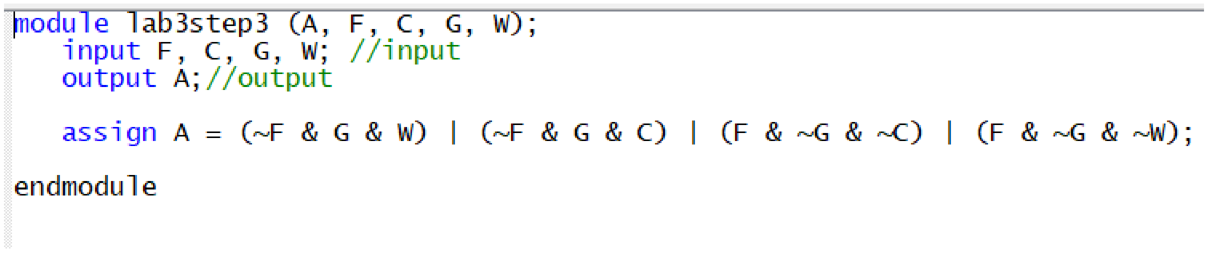


```
module lab3step1(A, C, G, W);
   input C, G, W; //input
   output A; //output

   //inverted
   not(G, ~G);
   not(C, ~C);
   not(W, ~W);

   //sum
   //w1 = the first wire
   or(w1, ~C, G, ~W);
   //w2 = the second wire
   or(w2, C, ~G, W);

   and(A, w1, w2);

endmodule
```

Behavioral Screenshots:



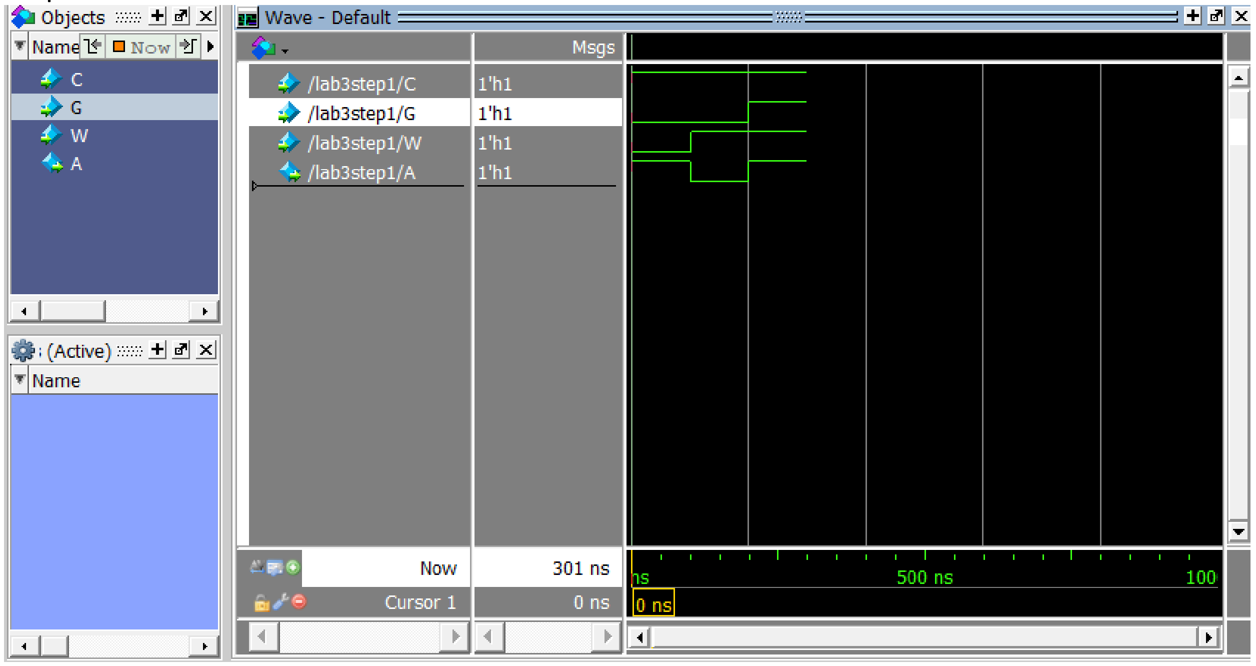
```
module lab3step2(F, C, G, W);
   input C, G, W; //Cabbage, Goat, Wolf
   output F; //Farmer

   assign F = (C |!G | W) & (!C | G | !W);

   //end
endmodule
```



```
module lab3step3 (A, F, C, G, W);
   input F, C, G, W; //input
   output A;//output

   assign A = (~F & G & W) | (~F & G & C) | (F & ~G & ~C) | (F & ~G & ~W);

endmodule
```

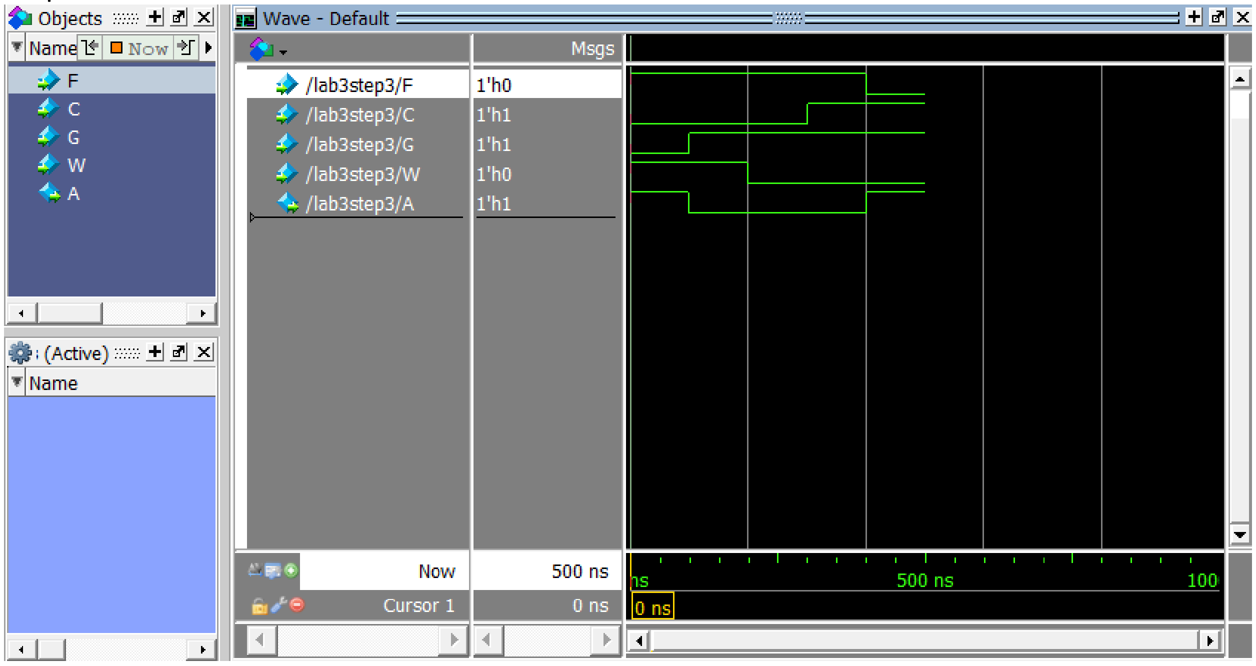
4.0 Hardware results demonstrate correct code.
Screenshot:

Step 1:



```
/lab3step1/C  1'h1
/lab3step1/G  1'h1
/lab3step1/W  1'h1
/lab3step1/A  1'h1
Now           301 ns
Cursor 1      0 ns
```

Step 3:



```
/lab3step3/F  1'h0
/lab3step3/C  1'h1
/lab3step3/G  1'h1
/lab3step3/W  1'h0
/lab3step3/A  1'h1
Now           500 ns
Cursor 1      0 ns
```