

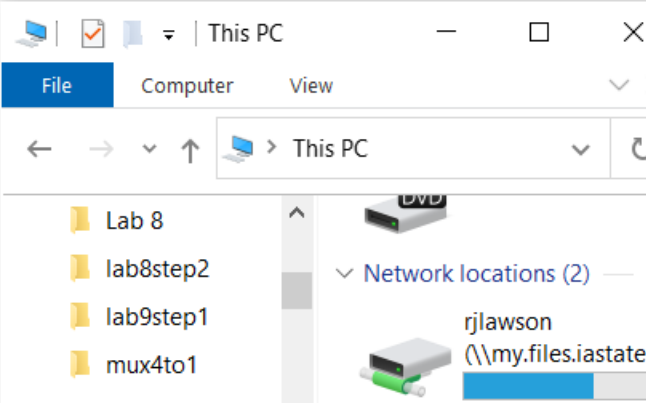
Name and Std ID: Riley Lawson rjlawson Lab Section: 6

Date: 10/22/2020

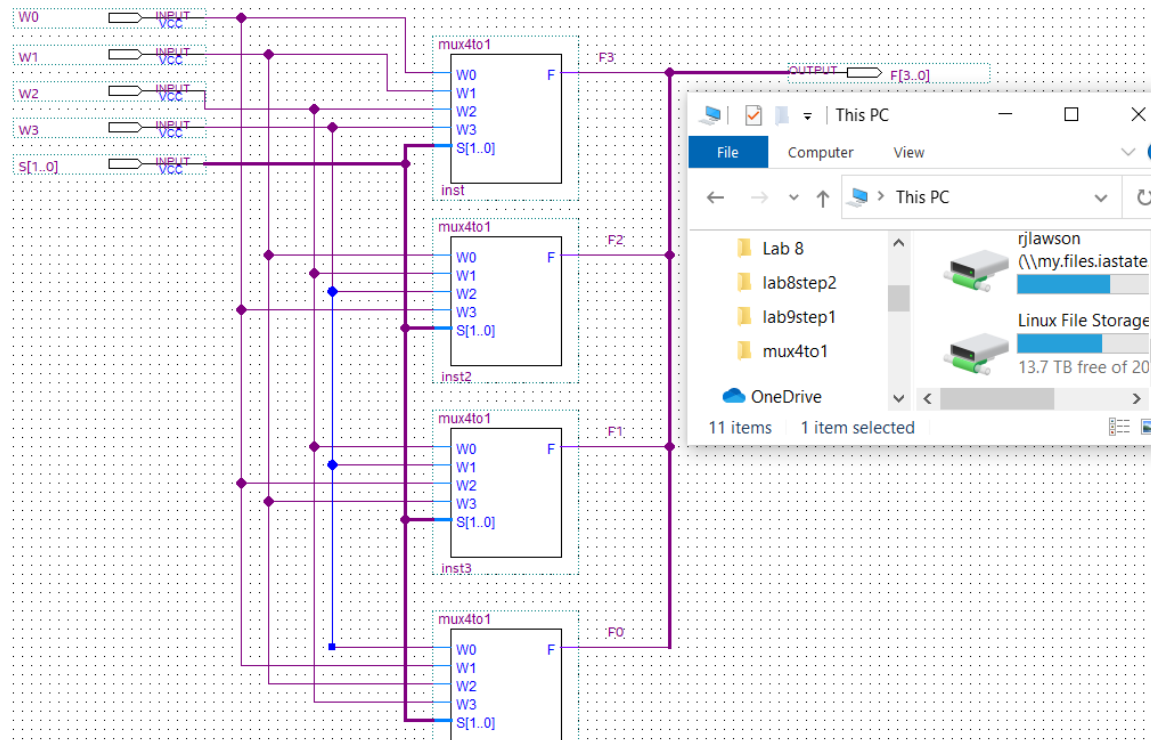
PRELAB:

Q1. Read section 2.2 and write the Verilog code for a 4-to-1 multiplexer.

```
module mux4to1(w0, w1, w2, w3, S, F);  
    input w0, w1, w2, w3;  
    input [1:0]S;  
    output F;  
    assign F = S[1] ? (S[0] ? w3:w2) : (S[0] ? w1:w0);  
endmodule
```



Q2. Design a 4-bit shifter as described in Section 3.1 of the lab description. Sketch the block diagram for your design showing the multiplexers, the inputs, outputs and the selectors to each multiplexer.

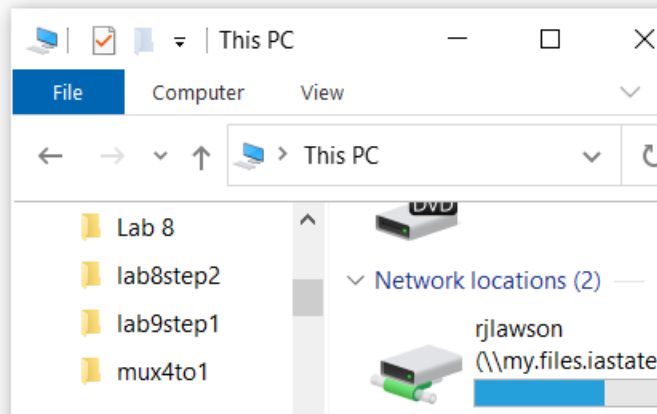


Q3. Refer to Section 3.1 of the lab description and complete the following table before you come to the lab:

X3	X2	X1	X0	X-1	X-2	X-3	S1	S0	F3	F2	F1	F0
1	0	0	1	1	1	0	0	1	0	0	1	1
1	1	1	0	0	0	0	1	1	0	0	0	0
1	1	1	0	0	1	1	0	0	1	1	1	0
1	1	0	1	0	1	0	1	0	0	1	0	1
1	0	1	1	0	1	1	0	1	0	1	1	0

```
module mux4to1(w0, w1, w2, w3, S, F);
    input w0, w1, w2, w3;
    input [1:0]S;
    output F;

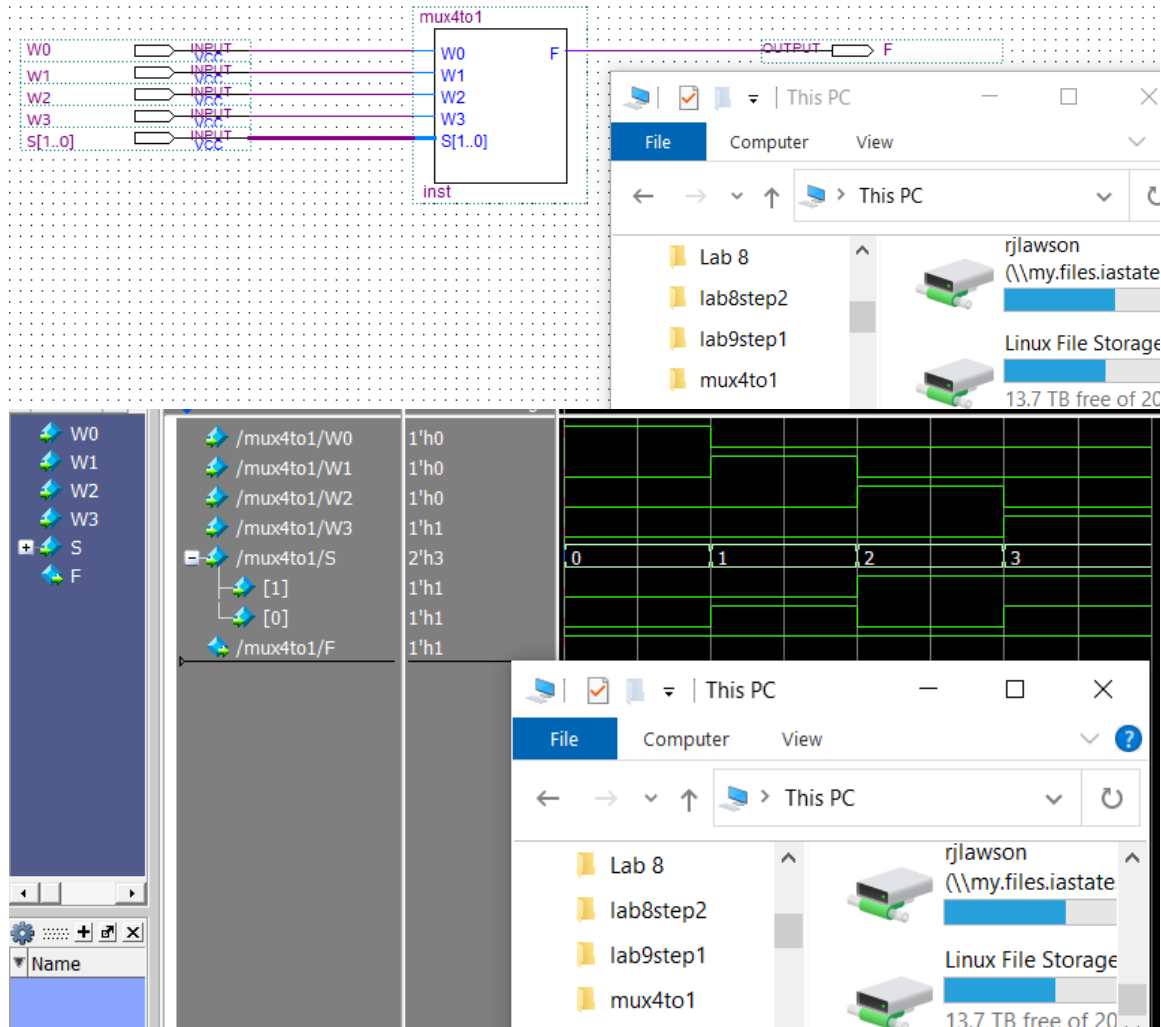
    assign F = S[1] ? (S[0] ? w3:w2) : (S[0] ? w1:w0);
endmodule
```



LAB:

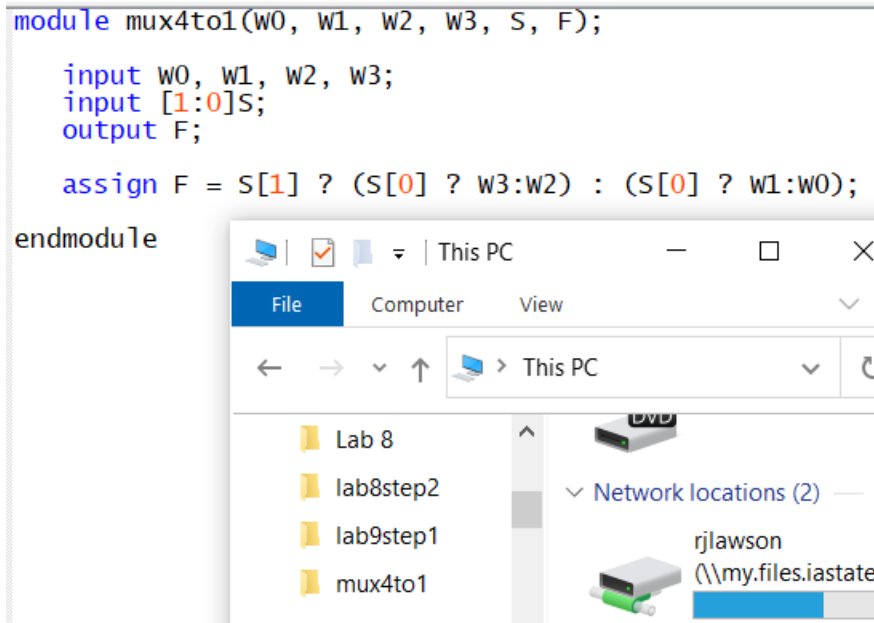
2.1 Hardware results demonstrate a good circuit.

Screenshots:



2.2 Hardware results demonstrate correct code.

Screenshots:



3.1 Hardware results demonstrate correct code.

Screenshots:

