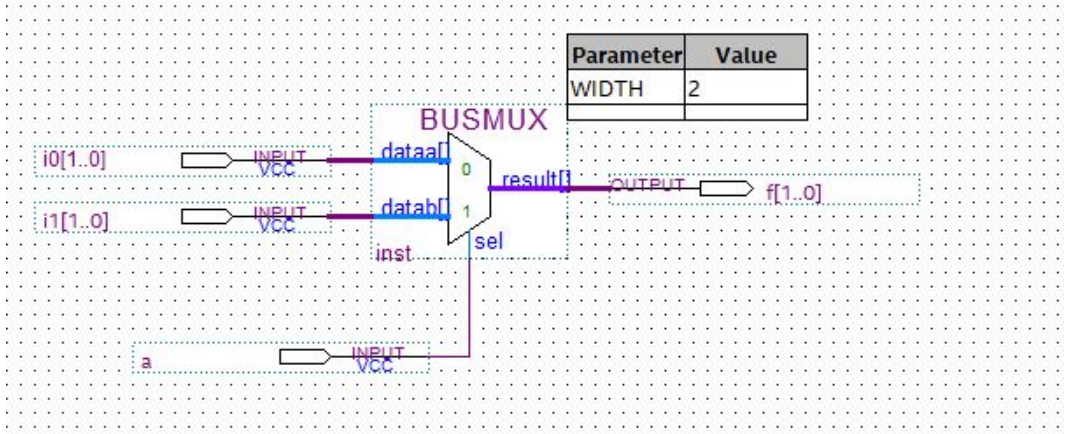
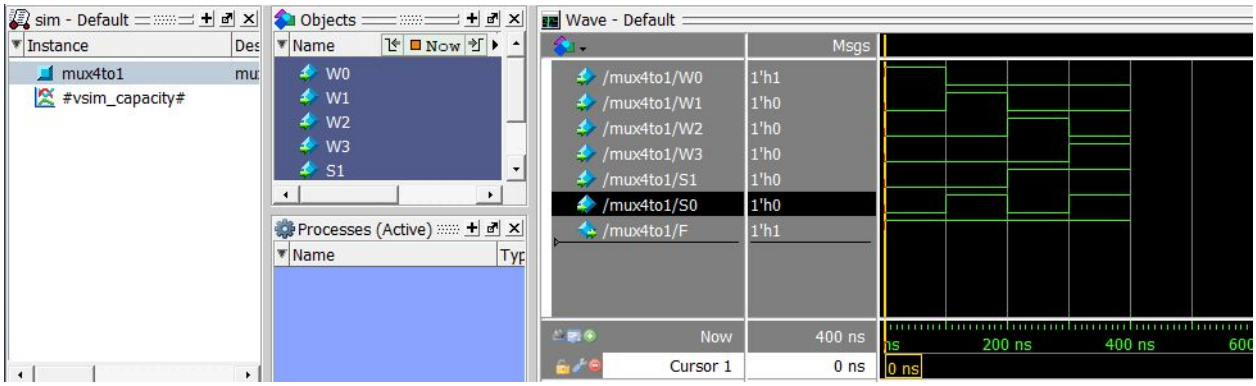
Part 1:
No simulation needed in ModelSim. This lab8step1 is not being used anywhere else in the lab because it is just creating a multiplexer using a busmux.

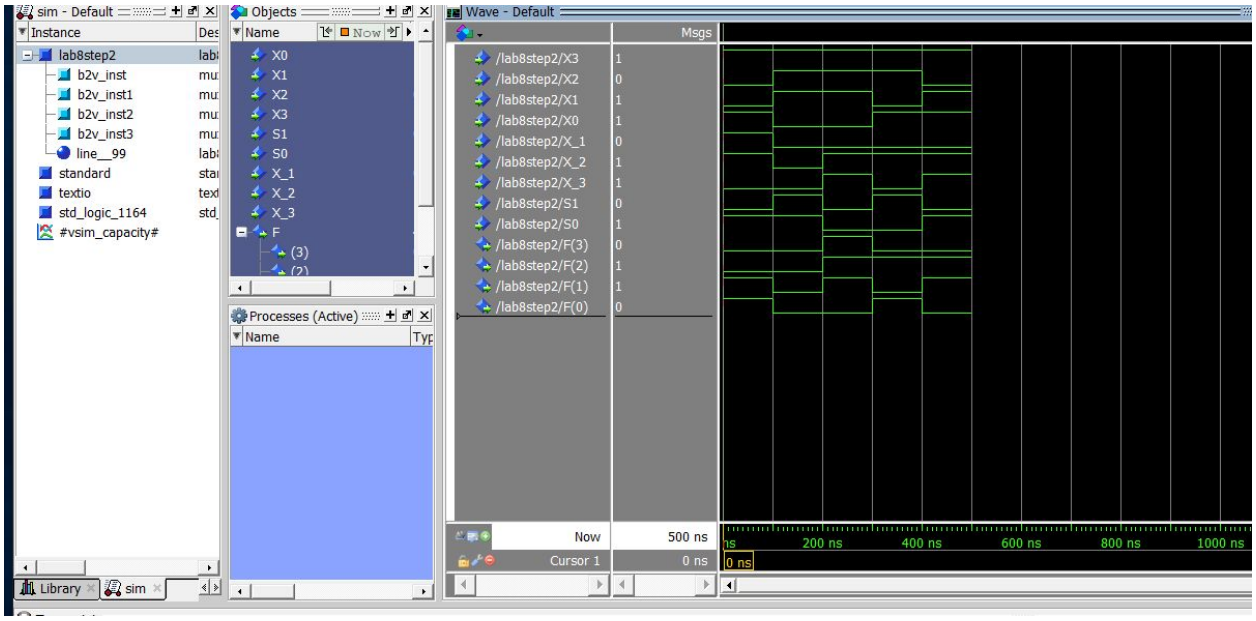


Part 2:
Only compile mux4to1.v



Part 3:

Note for part 3:
Because in vhdl, the hyphen (-) is not a valid character, students have to be told to change it to an underscore (_).
Inputs are: X3, X2, X1, X0, X_1, X_2, X_3, S1, S0
Outputs are: F[3..0].



Note:

When adding the outputs which share the same bus, like F[3..0], **DO NOT ADD F TO WAVE. Only add those highlighted ones in the screenshot into the wave.**