# Lab 6 Answer Sheet

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**Date: 10/8/2020**

**Submission Instructions:**

**Prelab:**
1. **Complete the prelab**
2. **Submit this report with the prelab completed to Canvas before your lab starts**

**Lab:**
1. **Complete the lab according to the instructions**
2. **Take screenshots of your ModelSim waveform (note: to receive points your NetID has to be present in the screenshot) and insert them into this document.**
3. **Include screenshots of any related block design files or Verilog files in the report**
4. **Complete this report and reupload it to Canvas**

**PRELAB:**

**Q1.** Add the following numbers then write them in decimal:

| Binary numbers to add<br>a3 a2 a1 a0 + b3 b2 b1 b0 | Binary result<br>C0 S3 S2 S1 S0 | Decimal conversion<br>N2 N1<br>(X3 X2 X1 X0) (X3 X2 X1 X0) |
|---|---|---|
| 1001 + 0111 | 10000 | 16 |
| 1011 + 1001 | 010100 | 20 |
| 1110 + 0101 | 010011 | 19 |
| 0010 + 1110 | 10000 | 16 |
| 1101 + 1011 | 011000 | 24 |

**Q2.** Consider the five-bit binary result (C0, S3, S2, S1, S0) representation in the table above. We would like to represent each combination as its equivalent in two decimal digits, each of which can be represented in binary as shown in the following table. Finish filling in the following truth table.

C0 →
S3 →
S2 →
S1 →
S0 →

**Binary Coded Decimal Converter**

→ N2X3
→ N2X2
→ N2X1
→ N2X0
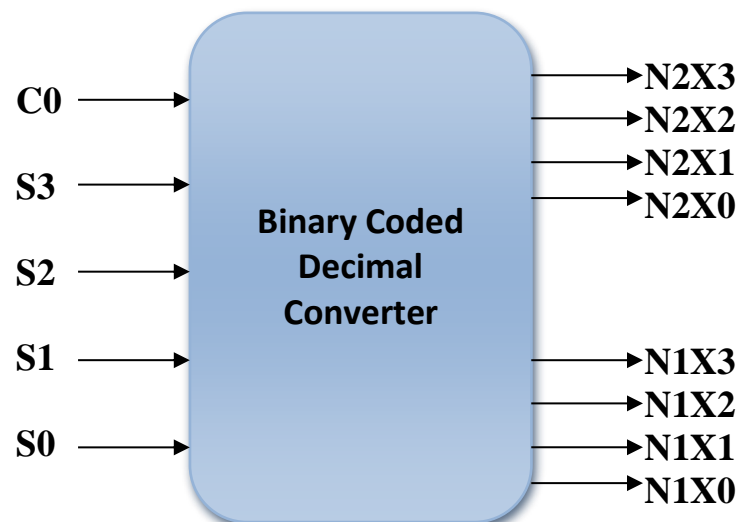
→ N1X3
→ N1X2
→ N1X1
→ N1X0

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| C0 | S3 | S2 | S1 | S0 | Decimal | | N2X3 | N2X2 | N2X1 | N2X0 | N1X3 | N1X2 | N1X1 | N1X0 |
|----|----|----|----|----|----|----|------|------|------|------|------|------|------|------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 2 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 3 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 4 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 5 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 6 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 7 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 8 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 9 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 2 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 | 3 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 | 4 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 1 | 5 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 | 0 | 1 | 6 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 7 | **0** | **0** | **0** | **1** | **0** | **1** | **1** | **1** |
| 1 | 0 | 0 | 1 | 0 | 1 | 8 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 9 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 2 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 2 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 | 2 | 2 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 | 2 | 3 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 | 2 | 4 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 | 2 | 5 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 2 | 6 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 2 | 7 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 | 2 | 8 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 2 | 9 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 3 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 3 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |

**Q3.** Find the logic expressions for N2X3, N2X2, N2X1, N2X0, N1X3, N1X2, N1X1, and N1X0 as a function of C0, S3, S2, S1 and S0:


N2X3 = 0;


N2X2 = 0;


N2X1 = (c0 & s2) | (c0 & s3)


N2X0 = (~c0 & s3 & s1) | (~c0 & s3 & s2) | (c0 & s3 & ~s2) | (s3 & s2 & s1);


N1X3 = (~c0 & s3 & ~s2 & ~s1) | (c0 & ~s3 & ~s2 & s1) | (c0 & s3 & s2 & ~s1);


N1X2 = (~c0 & ~s3 & s2) | (~c0 & s2 & s1) | (s1 & ~c0 & s2) | (c0 & s3 & ~ s2);


N1X1 = (~c0 & ~s3 & s1) | (~c0 & s3 & s2 & ~s1) | (c0 & ~s3 & ~s2 & ~s1) | (~s3 & s2 & s1) | (c0 & s3 & ~s2 & s1);


N1X0 = (s0)

**Q4.** Write the verilog code for the Binary Coded Decimal Converter from **Section 3.3** using the assign statement.

```
module binary_decimal_converter(s0, s1, s2, s3, c0, Z2, Y2, X2, W2, Z, Y, X, W);
    input s0, s1, s2, s3, c0;
    output Z2, Y2, X2, W2, Z, Y, X, W;

    assign Z2 = 0;
    assign Y2 = 0;
    assign X2 = (c0 & s2) | (c0 & s3);
    assign W2 = (~c0 & s3 & s1) | (~c0 & s3 & s2) | (c0 & s3 & ~s2) | (s3 & s2 & s1);

    assign Z = (~c0 & s3 & ~s2 & ~s1) | (c0 & ~s3 & ~s2 & s1) | (c0 & s3 & s2 & ~s1);
    assign Y = (~c0 & ~s3 & s2) | (~c0 & s2 & s1) | (s1 & ~c0 & s2) | (c0 & s3 & ~ s2);
    assign X = = (~c0 & ~s3 & s1) | (~c0 & s3 & s2 & ~s1) | (c0 & ~s3 & ~s2 & ~s1) | (~s3 & s2 & s1) | (c0 & s3 & ~s2 & s1);
    assign W = (s0);

endmodule
```
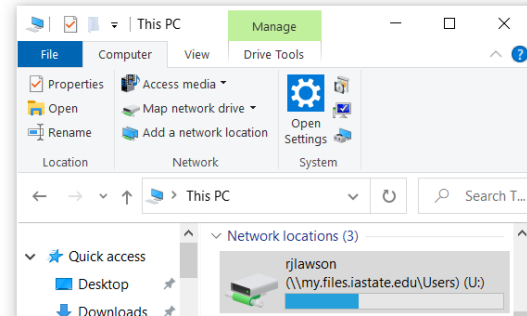
## LAB:

Hardware demonstrates a good design.
<<Insert a screenshot of your BDF file here>>

Lab 6 screenshots:

# Lab 6 Answer Sheet

**To get full points, replace this screenshot with your results**

- To find your NetID, open the start menu and search for "This PC". Then scroll down to reveal your NetID



**Example Screenshot Replace Me!**

**Must show your NetID and verified waveform**