Cpr E 281 LAB5
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

# Lab 5 Answer Sheet

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**Date: 9/23/2020**

## Submission Instructions:

**Prelab:**

1. **Complete the prelab**
2. **Submit this report with the prelab completed to Canvas before your lab starts**

**Lab:**

1. **Complete the lab according to the instructions**
2. **Take screenshots of your ModelSim waveform (note: to receive points your NetID has to be present in the screenshot) and insert them into this document.**
3. **Include screenshots of any related block design files or Verilog files in the report**
4. **Complete this report and reupload it to Canvas**

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## PRELAB:

**Q1.** Use Figure 1 and the table below to fill in the truth table on the next page.

| $X_3$ | $X_2$ | $X_1$ | $X_0$ | Display |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 |  |
| 0 | 0 | 0 | 1 |  |
| 0 | 0 | 1 | 0 |  |
| 0 | 0 | 1 | 1 |  |
| 0 | 1 | 0 | 0 |  |
| 0 | 1 | 0 | 1 |  |
| 0 | 1 | 1 | 0 |  |
| 0 | 1 | 1 | 1 |  |

| $X_3$ | $X_2$ | $X_1$ | $X_0$ | Display |
|---|---|---|---|---|
| 1 | 0 | 0 | 0 |  |
| 1 | 0 | 0 | 1 |  |
| 1 | 0 | 1 | 0 |  |
| 1 | 0 | 1 | 1 |  |
| 1 | 1 | 0 | 0 |  |
| 1 | 1 | 0 | 1 |  |
| 1 | 1 | 1 | 0 |  |
| 1 | 1 | 1 | 1 |  |

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| $X_3$ | $X_2$ | $X_1$ | $X_0$ | A | B | C | D | E | F | G |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | **0** | **0** | **0** | **0** | **0** | **0** | **1** |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |

**Q2.** Write the verilog code for the 7-Segment Display Decoder based on the truth table from Q1. You only need to write the skeleton code (i.e., a code which shows only a rough outline and no unnecessary or repetitive details) below.

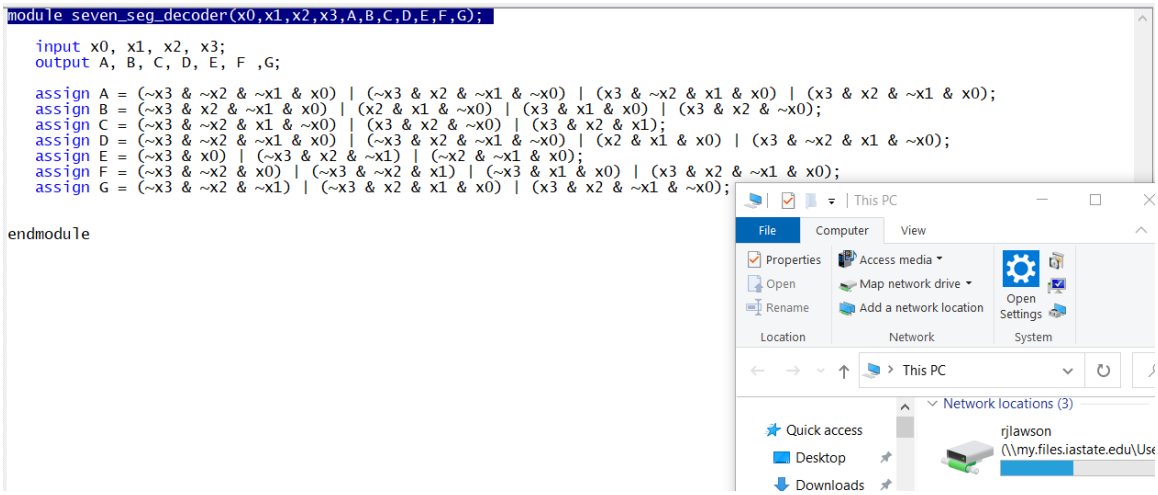
```
module seven_seg_decoder(x0,x1,x2,x3,A,B,C,D,E,F,G)

    input x0, x1, x2, x3;
    output A, B, C, D, E, F ,G;


    A = some code;
    B = some code;
    C = some code;
    D = some code;
    E = some code;
    F = some code;
    G = some code;

    x0 = some code;
    x1 = some code;
    x2 = some code;
    x3 = some code;

    All of these are connected

endmodule
```

## LAB:

### 3.0 Lab5step0

Hardware demonstrates a good circuit.

**<<<Insert a screenshot of your Verilog file>>>**



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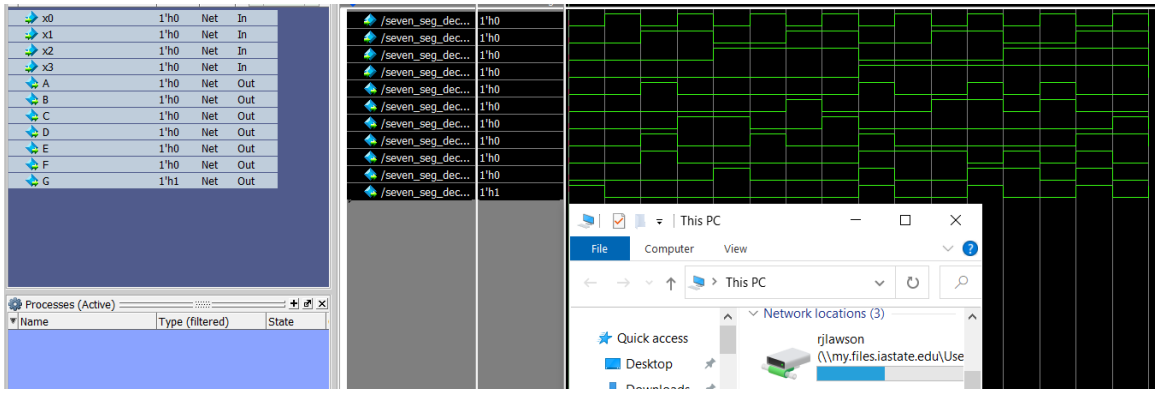
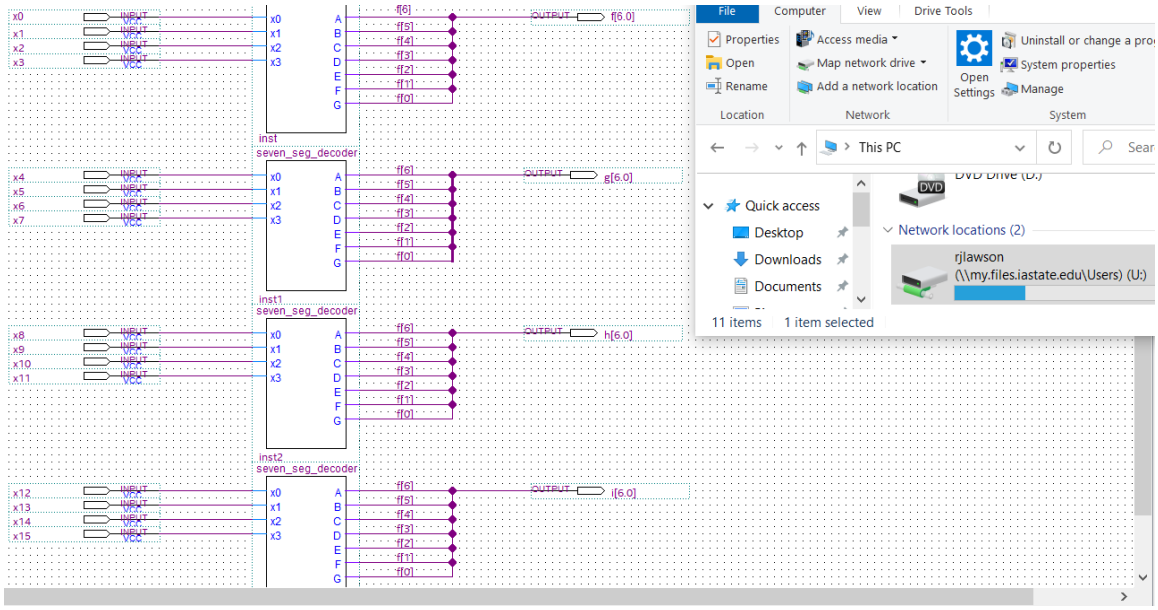
Lab5step0 Result:




**4.0 Lab5step1**

Hardware demonstrates a good circuit.

**<<<Insert a screenshot of your BDF file here>>>**



# Lab 5 Answer Sheet

Lab5step1 results: