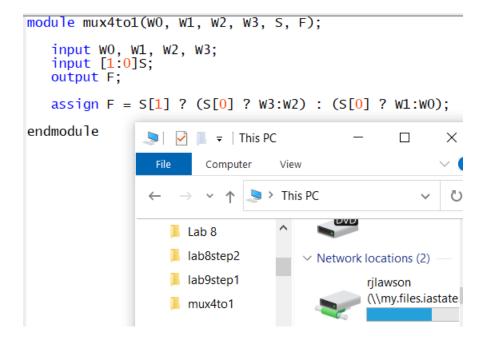
Lab 8 Answer Sheet

Name and Std ID: Riley Lawson rjlawson Lab Section: 6

Date: 10/22/2020

PRELAB:

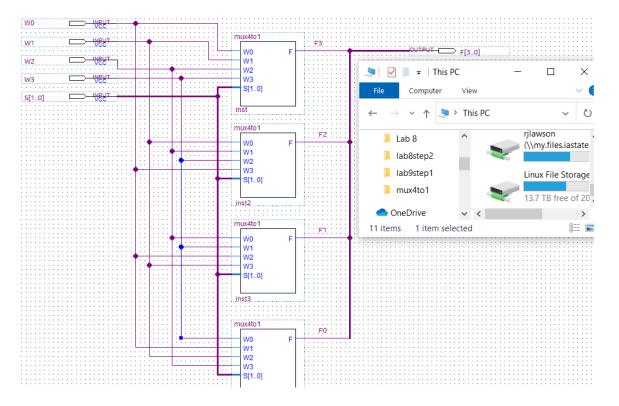
Q1. Read section 2.2 and write the Verilog code for a 4-to-1 multiplexer.



Cpr E 281 LAB08 ELECTRICAL AND COMPUTER ENGINEERING IOWA STATE UNIVERSITY

Lab 8 Answer Sheet

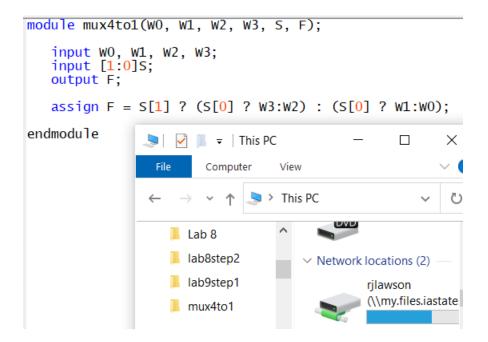
Q2. Design a 4-bit shifter as described in Section 3.1 of the lab description. Sketch the block diagram for your design showing the multiplexers, the inputs, outputs and the selectors to each multiplexer.



Lab 8 Answer Sheet

Q3. Refer to Section 3.1 of the lab description and complete the following table before you come to the lab:

Х3					X-2			S0			F1	F0
1	0	0	1	1	1	0	0	1	0	0	1	1
1	1	1	0	0	0	0	1	1	0	0	0	0
1	1	1	0	0	1	1	0	0	1	1	1	0
1	1	0	1	0	1	0	1	0	0	1	0	1
1	0	1	1	0	1	1	0	1	0	1	1	0



Lab 8 Answer Sheet

LAB:

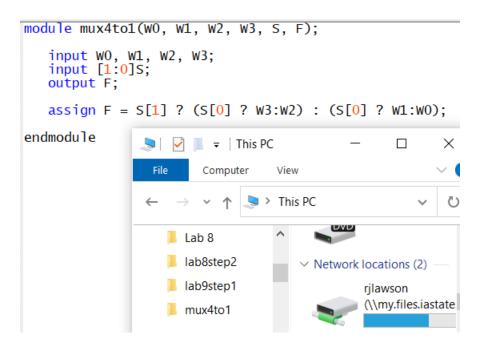
2.1 Hardware results demonstrate a good circuit.

Screenshots: mux4to1 W0 wo W1 🝃 | 📝 📗 🔻 | This PC W2 W2 W3 W3 S[1..0] Computer S[1..0] View inst > This PC rjlawson Lab 8 (\\my.files.iastate lab8step2 lab9step1 Linux File Storage mux4to1 13.7 TB free of 20 /mux4to1/W1 /mux4to1/W2 1'h1 /mux4to1/W3 2'h3 1'h1 1'h1 1'h1 2 [1] [0] /mux4to1/F 🔙 | 🛂 📗 🖚 | This PC Х File Computer View 🔙 > This PC Ö rjlawson Lab 8 (\\my.files.iastate. **+** lab8step2 🌼 :::::: 🛨 🗗 🗙 lab9step1 Linux File Storage **▼** Name mux4to1 13.7 TB free of 20 ,

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Lab 8 Answer Sheet

2.2 Hardware results demonstrate correct code. Screenshots:



3.1 Hardware results demonstrate correct code. Screenshots:

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Lab 8 Answer Sheet

