Cpr E 281 LAB08
ELECTRICAL AND COMPUTER ENGINEERING
IOWA STATE UNIVERSITY

Designing Shifters with Multiplexers

PRELAB!

Read the entire lab, and **complete** the prelab questions (Q1-Q3) on the answer sheet **before** coming to the laboratory.

1.0 Objectives

In Lab 4 you designed a multiplexer. In this lab you will learn to design shifters using multiplexers. However, first you will design a simple multiplexer for a 2-bit bus. Then you will design a 1-bit 4-to-1 Multiplexer in verilog. Finally, you will use this multiplexer to build a shifter.

2.0 Multiplexers

2.1 A Simple Bus Multiplexer

First, start a new project (***lab8step1***) and start a new block diagram. Save this file as ***lab8step1.bdf***. Bring up the **Symbol** dialog box. Type **busmux** in the '*Name:*' field and add it to the block diagram. Next, right click on the ***Parameters*** box, select **Properties**, select **Parameters** Tab and change the ***Value*** for WIDTH to **2**. This will change the width of the data ports to 2 bits. In other words, this forces the inputs and the output to be 2-bit wide buses. Click **OK**.

Next, you need to add inputs for the 2 input buses, the select signal, and the output bus. The pin connected to *dataa* name **i0[1..0]**, signifying there is a 2-bit wide bus. Name the pins connected to *datab*, *sel* and *result* to **i1[1..0], a,** and **f[1..0]** respectively. For the bus connections select the thick wire from the toolbar, or drag the input pins until they are touching the mux inputs and release them. When you move them a bus line will be drawn for you.

When you are done, save and compile the project. Once you understand your circuit, simulate the proper operation of your bus multiplexer on ModelSim and include screenshots of your results in the answersheet.

2.2 A 4 to 1 Multiplexer (1-bit)

The following is the verilog code for a 1-bit 2 to 1 multiplexer. When the selector is 0 the output f is i0 and when the selector is 1 the output is i1.

```
module mux2to1(i0, i1, s, f);
        input i0, i1, s;
        output f;
        assign  f  = s ? i1 : i0;
endmodule
```

Modify this code to build a 1-bit 4-to-1 multiplexer. The multiplexer will have the following specification:

- Four 1-bit data inputs, W0, W1, W2 and W3.
- One 2-bit selector input, S [1..0].
- One 1-bit output, F.
- When S [1..0] = 00 the output will be W0.
- When S [1..0] = 01 the output will be W1.
- When S [1..0] = 10 the output will be W2.
- When S [1..0] = 11 the output will be W3.

For a detailed explanation of multiplexers please refer to the textbook. Also, read and understand any code that you may find in your textbook for multiplexers. *Note: It will be easier to reuse this code if you do not use a bus for the W inputs.*

Create a new folder and a new project (***mux4to1***). Save the verilog code for the 1-bit 4-to-1 multiplexer as ***mux4to1.v***. Use ModelSim to test your code. When you are confident that your code is correct, take screenshots of the result and include it in your lab report. Once you are done create a default symbol for your mux4to1 so that you can use it in the next section.

3.0 Shifters

3.1 Designing a Shifter

You will now design a device called a shifter. A Shifter is built from multiplexers and shifts the outputs, based on the select signals. For this shifter, you will use 1-bit 4-to-1 multiplexer of Section 2.2. A shifter has the following inputs and outputs:

X3, X2, X1, X0	Primary Inputs
X-1, X-2, X-3	Cascading Inputs
S1, S0	Shift Count
F3, F2, F1, F0	Fixed Outputs

The shifter outputs the inputs shifted to the left 0, 1, 2, or 3 places as indicated by the 2-bit shift count (select signals). The table below summarizes the behavior:

S1	S0	F3	F2	F1	F0
0	**0**	X3	X2	X1	X0
0	**1**	X2	X1	X0	X-1
1	**0**	X1	X0	X-1	X-2
1	**1**	X0	X-1	X-2	X-3

Example:

Let the inputs have the values below:

X3	X2	X1	X0	X-1	X-2	X-3
0	1	1	0	1	0	1

If the shift count is 00, the output would be:

F3	F2	F1	F0	X-1	X-2	X-3
0	1	1	0	1	0	1

If we shifted left ONE position – i.e., shift count is 01 then the output would be:

X3	F3	F2	F1	F0	X-2	X-3
0	1	1	0	1	0	1

The result makes it look like the **Shift Count** moves the window for the output!

To develop this Shifter, start with a new block diagram. Name it as your top-entity-file. The default should be ***lab8step2*.bdf**.

Hint:
To complete the shifter design you will need four 1-bit 4-to-1 multiplexers, one for each output of the shifter. As is evident from the table summarizing the behavior of a shifter, the output bit F3 of the shifter can be X3, X2, X1 or X0 depending on the value of the shift count. A 4-to-1 multiplexer allows choosing from X3, X2, X1 and X0 based on the value of the shift count.

For this circuit you will only place **one output pin** on the block diagram and name it **F[3..0]**. Next create a small node line (orthogonal node tool), one on the output of each mux. Then run a bus line (orthogonal bus tool) to the output pin and connect each node line to the bus line. You should now have the output of each mux connected to the same bus line via a node line. Next you must label each node line to establish its position in the bus. To do this simply right click the node line and give it a name. An example is shown below in **Figure 1**.

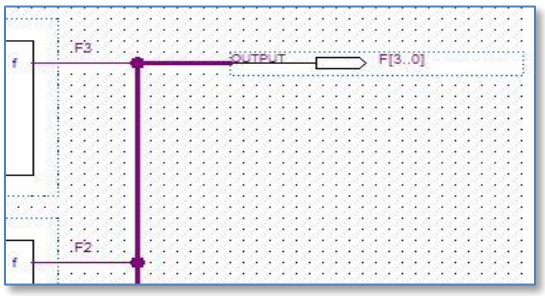

Figure 1: Node Line to Bus Line Connections

Once your circuit is ready, compile it, and then simulate it on ModelSim.

Once you understand your circuit, follow the table you filled out for prelab **Q3** and demonstrate the proper operation of your shifter to the TA.

4.0 Complete

You are done with this lab. Close all lab files, exit Quartus Prime, log off the computer and hand in your answer sheet. **Don't forget to write down your name and your lab section number**.