

# CROSS - JBUS SPECIFICATION

**Date:** 14/04/03

**Author:** CHLORIDE Silectron

**Software name and version:** 10H01045.300

**Project reference:** CROSS JBUS Protocol

**File name:** JBUS\_CROSS\_V5

## 1 Index

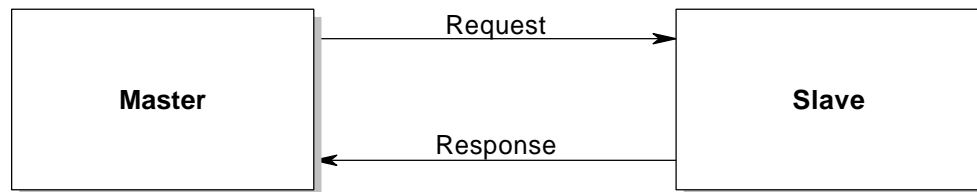
<b>1</b>	<b>INDEX.....</b>	<b>1</b>
<b>2</b>	<b>JBUS PROTOCOL.....</b>	<b>2</b>
2.1	INTRODUCTION .....	2
2.2	PRESENTATION OF THE REQUEST AND RESPONSE FRAMES.....	3
2.3	CHECKING THE MESSAGES RECEIVED FROM THE SLAVE .....	4
2.4	READING OF N WORDS: FUNCTION 3 .....	6
2.5	ALGORITHM FOR CALCULATING CRC .....	7
<b>3</b>	<b>CONFIGURATION AND FRAME DESCRIPTION .....</b>	<b>9</b>
<b>4</b>	<b>FUNCTION 3 DESCRIPTION.....</b>	<b>10</b>
4.1	MAP AREA: .....	10
<b>5</b>	<b>INTERNAL STATE:.....</b>	<b>11</b>
5.1	S1 OPERATING CONDITION (S1): .....	11
5.2	S2 OPERATING CONDITION (S2): .....	11
5.3	S1 STATIC SWITCH OPERATING CONDITION (S1-SW): .....	12
5.4	S2 STATIC SWITCH OPERATING CONDITION (S2-SW): .....	12
5.5	LOAD OPERATING CONDITION (LOAD):.....	12
5.6	SYSTEM OPERATING CONDITION (SYSTEM):.....	13
<b>6</b>	<b>MIMIC DIAGRAM:.....</b>	<b>14</b>
<b>7</b>	<b>RATINGS:.....</b>	<b>16</b>
<b>8</b>	<b>MEASURES: .....</b>	<b>17</b>
8.1	S1 MEASURES .....	17
8.2	S2 MEASURES .....	17
8.3	OUTPUT MEASURES.....	17
8.4	SYSTEM MEASURES .....	17

## 2 JBUS Protocol

### 2.1 Introduction

---

Detailed knowledge of the protocol is only essential when a computer must be programmed to be used as. Every exchange creates 2 messages: a request from the master and a response from the slave..



Every message or frame contains 4 types of information:

- the **slave number** (1 byte)

*The number of the specified slave, the target automatic machine (from 1 to FF).*

*If the number of the slave is zero, the request relates to all the slaves and there is no response message.*

- the **function code** (1 byte)

*Used to select a command (read, write, bit, word) and to check if the response is correct.*

- the **information field** (n bytes)

*This information field contains the parameters for the function: bit address, word address, bit value, word value, number of bits, number of words.*

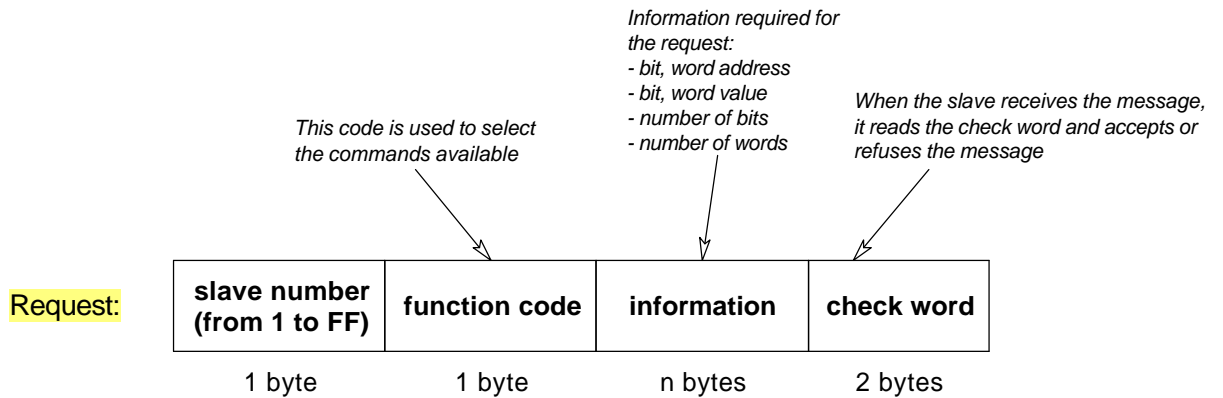
- the **check word** (2 bytes)

*Word used to detect transmission errors.*

#### **Frame synchronisation**

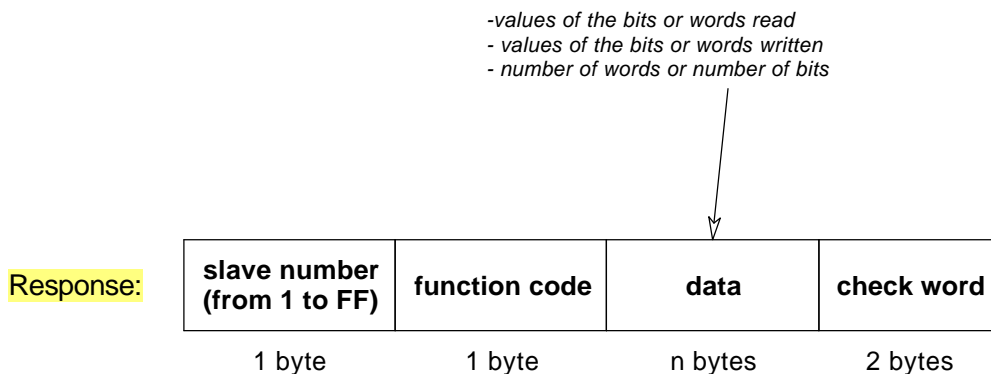
- Every character received after a pause > 3 characters is considered as the start of a frame.
- Between two frames, there must be a pause on the line corresponding to at least 3 characters.

## 2.2 Presentation of the request and response frames



The JBUS protocol has 14 functions:

- Function 1: reads n output and internal bits
- Function 2: reads n input bits
- Function 3: reads n output and internal words
- Function 4: reads n input words
- Function 5: writes 1 bit
- Function 6: writes 1 word
- Function 7: reads 8 bits rapidly
- Function 8: modification diagnostics
- Function 11: reads the event counter
- Function 12: reads the trace buffer
- Function 13: program commands
- Function 14: Function 13 diagnostics
- Function 15: writes n bits
- Function 16: writes n words

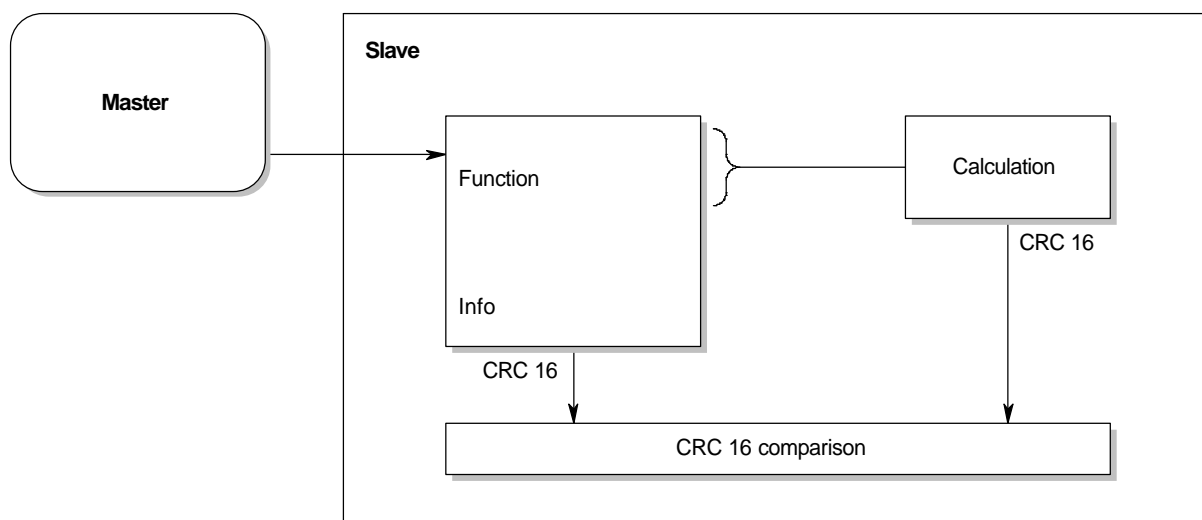


## 2.3 Checking the messages received from the slave

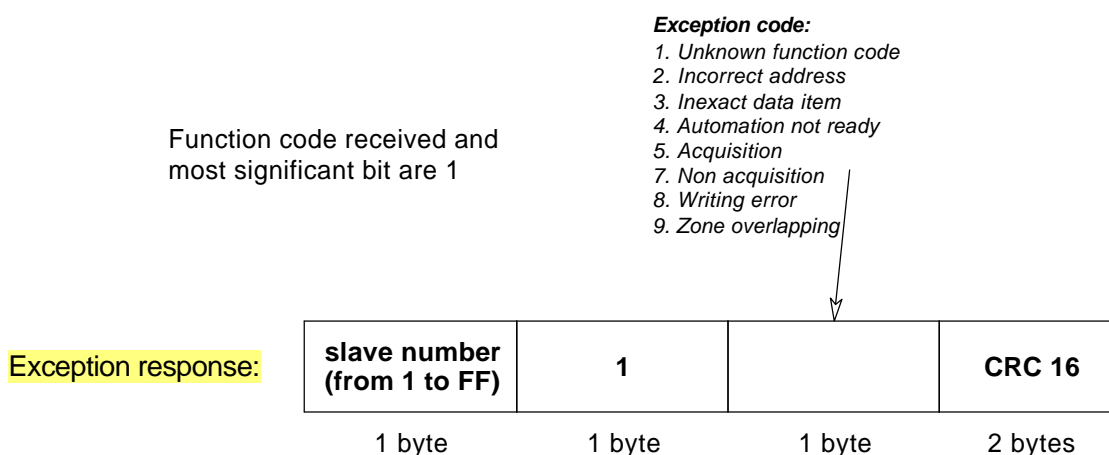
When the master sends a request, after indicating:

- the number of the slave
- the function code
- and the function parameters, it calculates and sends the content of the check word (CRC 16).

When the slave receives the request message, it saves it in the memory, calculates the CRC and compares it with the CRC 16 received.



If the message received is not correct (the two CRC 16 values are not identical), the slave does not respond. If the message received is correct but the slave cannot process it (incorrect address, inexact data, etc.), it responds with an exception frame.



**Example**

Request:	1	9	0	0	0	0	CRC 16
----------	---	---	---	---	---	---	--------

Response:	1	89H	1	CRC 16
-----------	---	-----	---	--------

**Note**

The exception responses 5 and 7 relate to the JBUS 13 and 14 functions.

## 2.4 Reading of N words: function 3

---

The number of words to be read must be  $\leq 125$ .

Function 3: reads the output and internal words

Request:

slave number	3 or 4	1 <sup>st</sup> word address		number of words		CRC 16
		PF	pf	PF	pf	
1 byte	1 byte	2 bytes		2 bytes		2 bytes

Response:

slave number	3 or 4	No. of bytes read	1 <sup>st</sup> word value		last word value		CRC 16
			PF	pf	PF	pf	
1 byte	1 byte	1 byte	2 bytes		2 bytes		2 bytes

### - example

Reading of words from 805 to 80A of slave n° 2

Request:

2	3	0805	6	CRC 16
---	---	------	---	--------

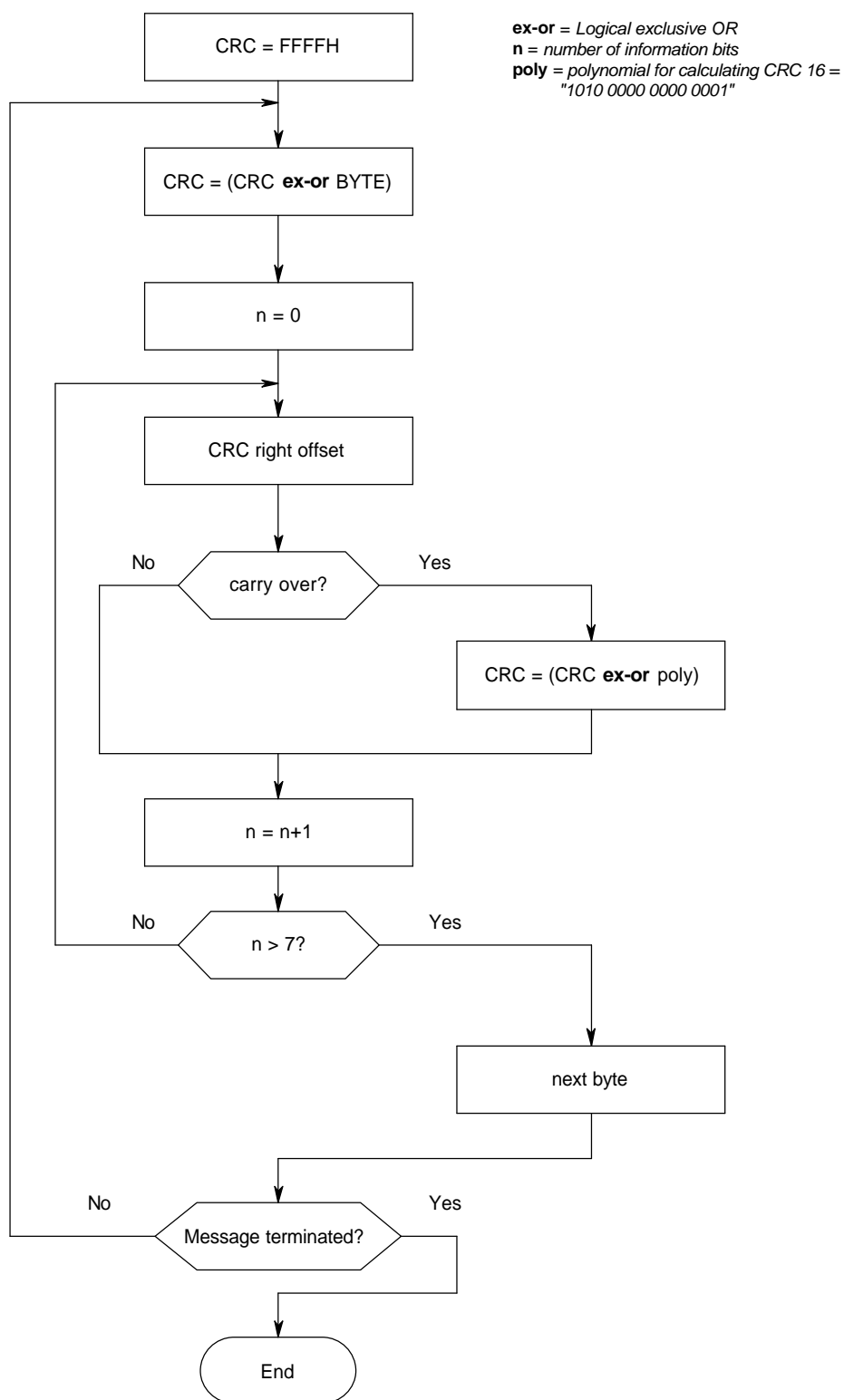
Response:

2	3	0C	XXX	.....	YYY	CRC 16
---	---	----	-----	-------	-----	--------

Value of  
word 805

Value of  
word 80A

## 2.5 Algorithm for calculating CRC



In the CRC 16, the 1<sup>o</sup> byte issued is the least significant.

**Example of CRC calculation (frame 0207)**

Initialisation of CRC register

 $\oplus$  of the 1° character

1111	1111	1111	1111
0000	0000	0000	0010

Offset 1

1111	1111	1111	1101
0111	1111	1111	1110 1
1010	0000	0000	0001

Flag at 1,  $\oplus$  polynomial

Offset 2

1101	1111	1111	1111
0110	1111	1111	1111 1
1010	0000	0000	00001

Flag at 1,  $\oplus$  polynomial

Offset 3

1100	1111	1111	1110
0110	0111	1111	1111 0

Offset 4

0011	0011	1111	0011 1
1010	0000	0000	0001

Flag at 0,

Offset 5

1001	0011	1111	1110
0100	1001	1111	1111 0

Offset 6

0010	0100	1111	1111 1
1010	0000	0000	0001

Offset 7

1000	0100	1111	1110
0100	0010	0111	1111 0

Offset 8

0010	0001	0111	1111 1
1010	0000	0000	0001

 $\oplus$  2° character

1000	0001	0011	1110
0000	0000	0000	0111

Offset 1

1000	0001	0011	1001
0100	0000	1001	1100 1
1010	0000	0000	0001

Offset 2

1110	0000	1001	1101
0111	0000	0100	1110 1
1010	0000	0000	0001

Offset 3

1101	0000	0100	1111
0110	1000	0010	0111 1
1010	0000	0000	0001

Offset 4

1100	1000	0010	0110
0110	0100	0001	0011 0

Offset 5

0011	0010	0000	1001 1
1010	0000	0000	0001

Offset 6

1001	0010	0000	1000
0100	1001	0000	0100 0

Offset 7

0010	0100	1000	0010 0
------	------	------	--------

Offset 8

0001	0010	0100	0001 0
------	------	------	--------

most  
significantleast  
significant

The CRC 16 of the frame, therefore, is: 4112



### 3 Configuration and frame description

The CHLORIDE CROSS can be connected to a J-BUS communication system. It acts as a SLAVE and this document explain how obtain information out the CROSS.

#### SERIAL DATA FORMAT:

- . *Baud rate*: 9600, 4800, 1200 baud
- . *Data bits*: 8 bits
- . *Start bits*: 1 bit
- . *Stop bits*: 1 bit
- . *Parity check*: none

#### COMMAND FRAME FORMAT:

- . *Unit id.*: 1 byte
- . *Function code*: 1 byte
- . *Information*: N bytes (depending on the function code)
- . *CRC*: 2 bytes

#### REPLY FRAME FORMAT:

- . *Unit id.*: 1 byte
- . *Function code*: 1 byte (ORED by 0x80 if exception answer occurred)
- . *Information*: N bytes (depending on the function code OR exception code)
- . *CRC*: 2 bytes

#### ERROR REPLY INFORMATION FORMAT:

- . *Exception code*: 1 bytes
- *Contents*: 1 Function code unknown
  - 2 Wrong address (addresses undefined in memory area)
  - 3 Incorrect data

#### FUNCTIONS AVAILABLE ON CROSS:

- . 3 - read N words

All function command different from function number 3 will be treated as function unknown.

## 4 FUNCTION 3 DESCRIPTION

Command information description:

- . *First word address*: 2 bytes (MSB, LSB)
- . *Word number*: 2 bytes (MSB, LSB)

Reply information description:

- . *Byte number replied*: 1 bytes
- . *Word reply*: (2 \* (word number)) bytes (MSB, LSB)

### 4.1 MAP AREA:

---

#### AREA MAP:

Area	Address (Hex)	Function	Memory type /Range
<b>Internal state</b>	00 – 11	3	bit [0 - 1]
Undefined	12 – 13	3	
<b>Mimic diagram</b>	14 – 17	3	bit [ 0 - 1]
Undefined	18 - 1D	3	
<b>Ratings</b>	1E – 2E	3	word [0 - 0xFFFF]
Undefined	2F – 45	3	
<b>Measures</b>	46 – 59	3	word [0 - 0xFFFF]
Undefined	5A – 81	3	

## 5 INTERNAL STATE:

State bit: [1 = active, 0 = inactive]  
 Reserved bit: [don't care]

### 5.1 S1 Operating condition (S1):

Off state	Alarm state	On state
Word 0x00	Word 0x01	Word 0x02
bit 0: S1 Breaker open bit 1-15: Reserved	bit 0: S1 Failure bit 1: S1 Freq. Fault bit 2: S1 Voltage fault bit 3: S1 Wrong phase rotation bit 4: Ext. S1 failure bit 5: S1 Tripping coil active bit 6-15: Reserved	bit 0: S1 Normal bit 1-15: Reserved

### 5.2 S2 Operating condition (S2):

Off state	Alarm state	On state
Word 0x03	Word 0x04	Word 0x05
Bit 0: S2 Breaker open Bit 1-15: Reserved	bit 0: S2 Failure bit 1: S2 Freq. fault bit 2: S2 Voltage fault bit 3: S2 Wrong phase rotation bit 4: Ext. S2 failure bit 5: S2 Tripping coil active bit 6-15: Reserved	bit 0: S2 Normal bit 1-15: Reserved

### 5.3 S1 Static Switch operating condition (S1-SW):

Off state	Alarm state	On state
Word 0x06	Word 0x07	Word 0x08
bit 0: Load on source2 bit 1-15: Reserved	bit 0: S1 SCR open bit 1: S1 neutral SCR open bit 2: S1 phase SCR short (*) bit 3: S1 neutral SCR short (*) bit 4-15: Reserved	bit 0: Load on source1 bit 1: S1 phase overheating bit 2: S1 neutral overheating bit 3: S1 phase SCR short bit 4: S1 neutral SCR short bit 5: S1 neutral overcurrent bit 6: S1 Source overload bit 7-15: Reserved

(\*) Please note that S1-SW Mimic Status goes on Alarm state **only if** the S1 SCR short condition is active when source 2 supply the load.

### 5.4 S2 Static Switch operating condition (S2-SW):

Off state	Alarm state	On state
Word 0x09	Word 0x0A	Word 0x0B
bit 0: Load on source1 bit 1-15: Reserved	bit 0: S2 SCR open bit 1: S2 neutral SCR open bit 2: S2 phase SCR short (*) bit 3: S2 neutral SCR short (*) bit 4-15: Reserved	bit 0: Load on source2 bit 1: S2 phase overheating bit 2: S2 neutral overheating bit 3: S2 phase SCR short bit 4: S2 neutral SCR short bit 5: S2 neutral overcurrent bit 6: S2 Source overload bit 7-15: Reserved

(\*) Please note that S2-SW Mimic Status goes on Alarm state **only if** the S2 SCR short condition is active when source 1 supply the load.

### 5.5 Load operating condition (LOAD):

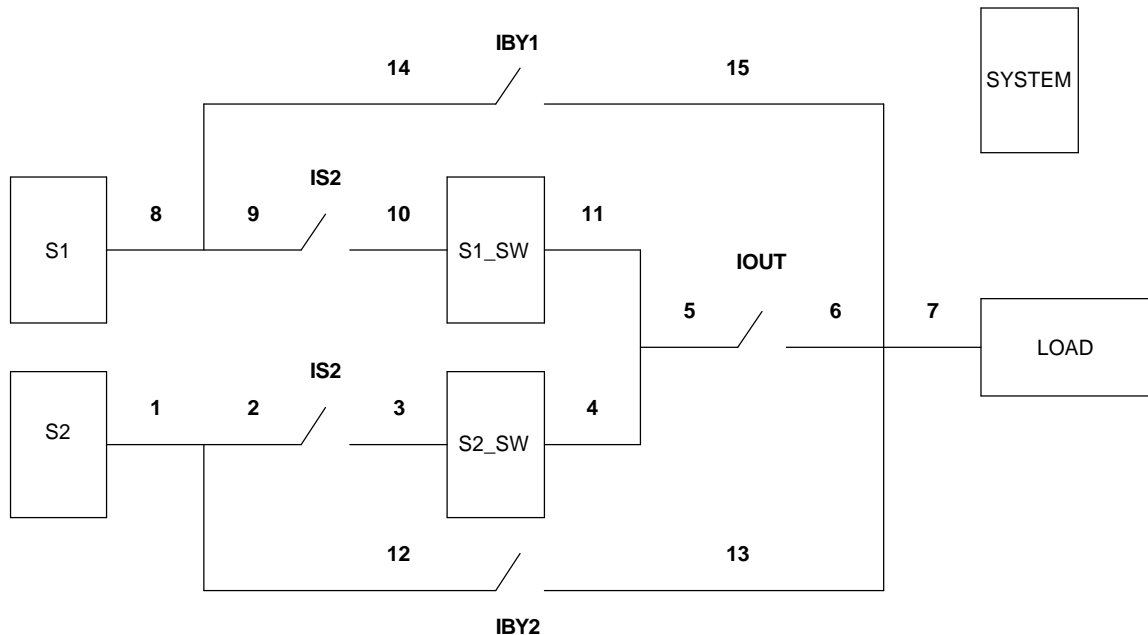
Off state	Alarm state	On state
Word 0x0C	Word 0x0D	Word 0x0E
bit 0: Out breaker open bit 1-15: Reserved	bit 0: Load not supplied bit 1-15: Reserved	bit 0: Out normal lamp bit 1: Load on reserve line bit 2: Output overload bit 3: Overload time out bit 4: Load on bad source bit 5-15: Reserved

## 5.6 System operating condition (SYSTEM):

---

Off state	Alarm state	On state
Word 0x0F	Word 0x10	Word 0x11
Bit 0-15: Reserved	bit 0: E.p.o. active bit 1: Source out of synchr. bit 2: Preferred overcurrent inhibit bit 3: Reserve overcurrent inhibit bit 4: Ext. Source sel. switch bit 5: Ext. Pref. source failure bit 6: Ext. Res. Source failure bit 7: Ext. Transfer inhibit bit 8: Ext. command conflict bit 9: Overcurrent bit 10: Transfer inhibit bit 11: Data setup lost bit 12: Aux. power failure bit 13: Bypass S1 closed bit 14: Bypass S2 closed bit 15: Reserved	bit 0: System normal bit 1: Man. command enabled bit 2: Control override bit 3: E.p.o. test enabled bit 4-15: Reserved

## 6 MIMIC DIAGRAM:



Word 0x14:

bit 0:	Segment 1	[1 = Active, 0 = Inactive]
bit 1:	Segment 2	[1 = Active, 0 = Inactive]
bit 2:	Segment 3	[1 = Active, 0 = Inactive]
bit 3:	Segment 4	[1 = Active, 0 = Inactive]
bit 4:	Segment 5	[1 = Active, 0 = Inactive]
bit 5:	Segment 6	[1 = Active, 0 = Inactive]
bit 6:	Segment 7	[1 = Active, 0 = Inactive]
bit 7:	Segment 8	[1 = Active, 0 = Inactive]
bit 8:	Segment 9	[1 = Active, 0 = Inactive]
bit 9:	Segment 10	[1 = Active, 0 = Inactive]
bit 10:	Segment 11	[1 = Active, 0 = Inactive]
bit 11:	Segment 12	[1 = Active, 0 = Inactive]
bit 12:	Segment 13	[1 = Active, 0 = Inactive]
bit 13:	Segment 14	[1 = Active, 0 = Inactive]
bit 14:	Segment 15	[1 = Active, 0 = Inactive]
bit 15:	Reserved	[1 = Active, 0 = Inactive]

- Mimic Status

On state	Off state	Alarm state
Word 0x15	Word 0x16	Word 0x17
bit 0: S1 on	bit 0: S1 off	bit 0: S1 alarm
bit 1: S2 on	bit 1: S2 off	bit 1: S2 alarm
bit 2: S1-SW on	bit 2: S1-SW off	bit 2: S1-SW alarm
bit 3: S2-SW on	bit 3: S2-SW off	bit 3: S2-SW alarm
bit 4: LOAD on	bit 4: LOAD off	bit 4: LOAD alarm
bit 5: SYSTEM on	bit 5: SYSTEM off	bit 5: SYSTEM alarm
bit 6: IS1 on	bit 6: IS1 off	bit 6: IS1 alarm
bit 7: IS2 on	bit 7: IS2 off	bit 7: IS2 alarm
bit 8: IBY1 on	bit 8: IBY1 off	bit 8: IBY1 alarm
bit 9: IBY2 on	bit 9: IBY2 off	bit 9: IBY2 alarm
bit 10: IOUT on	bit 10: IOUT off	bit 10: IOUT alarm
bit 11-15: Reserved	bit 11-15: Reserved	bit 11-15: Reserved

## 7 RATINGS:

Word 0x1E:	Ratings in A	[tenth of Amperes]
Word 0x1F:	full scale VS1 U	[tenth of Volts]
Word 0x20:	full scale VS1 V	[tenth of Volts]
Word 0x21:	full scale VS1 W	[tenth of Volts]
Word 0x22:	full scale VS2 U	[tenth of Volts]
Word 0x23:	full scale VS2 V	[tenth of Volts]
Word 0x24:	full scale VS2 W	[tenth of Volts]
Word 0x25:	full scale Vout U	[tenth of Volts]
Word 0x26:	full scale Vout V	[tenth of Volts]
Word 0x27:	full scale Vout W	[tenth of Volts]
Word 0x28:	full scale Iout U	[Amperes]
Word 0x29:	full scale Iout V	[Amperes]
Word 0x2A:	full scale Iout W	[Amperes]
Word 0x2B:	full scale Iout Neutral	[Amperes]
Word 0x2C:	full scale Neutral ? V	[tenth of Volts]
Word 0x2D:	full scale T Input Air	[tenth of °C degree]
Word 0x2E:	JBUS Protocol Revision [5]	



## 8 MEASURES:

### 8.1 S1 Measures

---

Word 0x46:	VS1 U	[tenth of volts]
Word 0x47:	VS1 V	[tenth of volts]
Word 0x48:	VS1 W	[tenth of volts]
Word 0x49:	FS1	[hundredths of hertz]

### 8.2 S2 Measures

---

Word 0x4A:	VS2 U	[tenth of volts]
Word 0x4B:	VS2 V	[tenth of volts]
Word 0x4C:	VS2 W	[tenth of volts]
Word 0x4D:	FS2	[hundredths of hertz]

### 8.3 Output Measures

---

Word 0x4E:	Vout U	[tenth of volts]
Word 0x4F:	Vout V	[tenth of volts]
Word 0x50:	Vout W	[tenth of volts]
Word 0x51:	Iout U	[tenth of amperes]
Word 0x52:	Iout V	[tenth of amperes]
Word 0x53:	Iout W	[tenth of amperes]
Word 0x54:	Iout Neutral	[tenth of amperes]
Word 0x55:	Neutral ? V	[tenth of volts]
Word 0x56:	F out	[hundredths of hertz]
Word 0x57:	Load Power	[tenth of KVA]

### 8.4 System Measures

---

Word 0x58:	Phase error	[tenth of degree]
Word 0x59:	T Input Air	[tenth of °C degree]