

FPGAlike – User Manual

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Introduction

Welcome to the FPGA Simulator Web Interface manual. This guide explains how to use our intuitive, browser-based tool for visualizing FPGA signal propagation in real-time. Users can load their own FPGA simulations (.sdf and .v files generated from tools like Impulse and ModelSim) or explore preloaded educational examples.

This tool is ideal for educators and students looking to understand FPGA behavior visually.

Project Overview

This web-based interface allows you to:

- Visualize BELs and signal routing inside an FPGA through interactive 2D diagrams.
- Perform real-time simulations reflecting accurate signal timing.
- Access preloaded Verilog applications suitable for educational demonstrations.

Getting Started

Prerequisites

Ensure you have the following installed:

- Node.js and npm
- Vite (bundled with the provided files)

Starting the Interface

Follow these steps to launch the FPGA simulator interface:

1. **Open a terminal** in the directory containing the project.
2. **Install dependencies** (only the first time):

```
npm install
```

3. **Start the server:**

```
npm run dev
```

If successful, the terminal should display:

```
Vite server running at: http://127.0.0.1:5173
```

Open this URL in your browser.

Screenshot Placeholder: Terminal showing successful launch

Using the Interface

The FPGA Simulator Web Interface has three main views accessible through tabs:

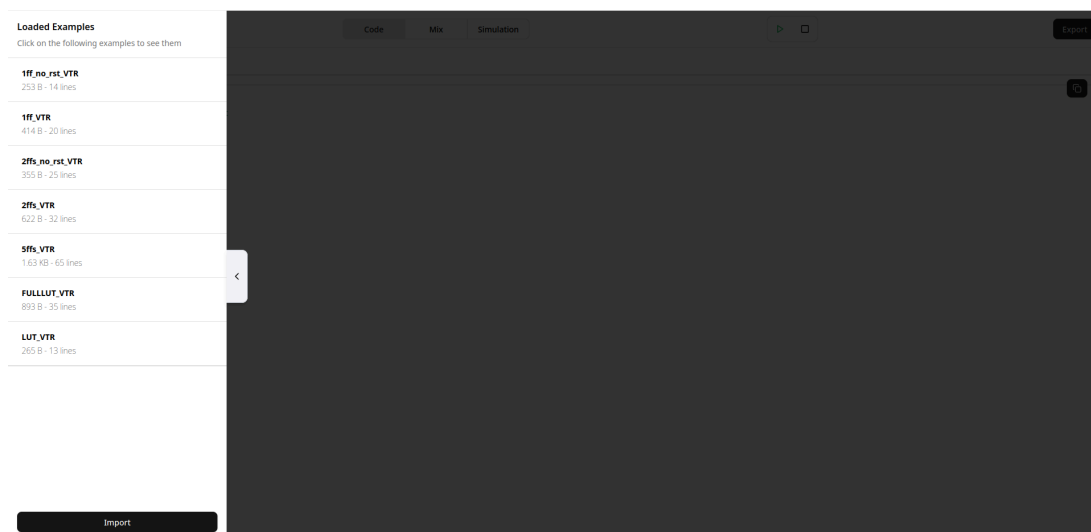
- **Code**
- **Simulation**
- **Mix**

Loading Examples or Custom Files

The collapsible sidebar on the left allows you to:

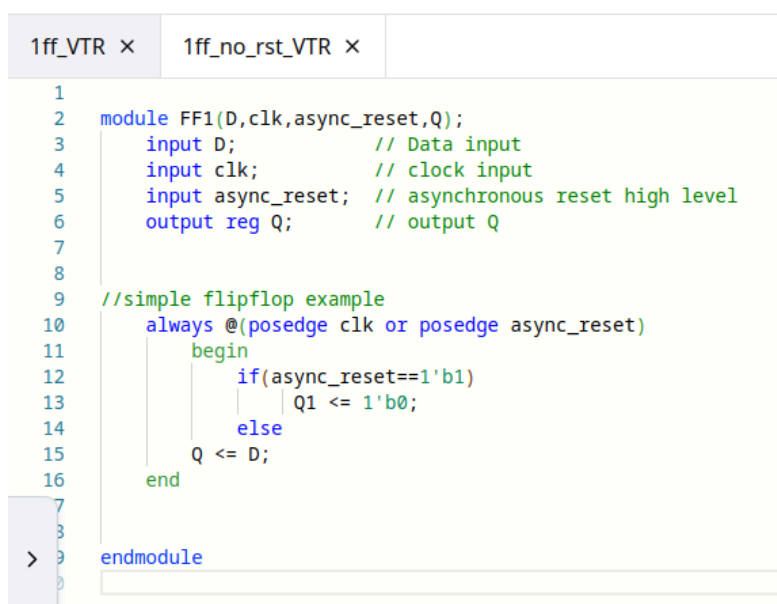
- Choose from preloaded examples.
- Load new simulation files (.sdf and .v) generated externally (Impulse, ModelSim).

Once loaded, simulations are displayed as tabs at the top, allowing seamless switching between different examples, much like browser tabs.



The "Code" View

This view (default) displays the Verilog code clearly with syntax highlighting for enhanced readability.



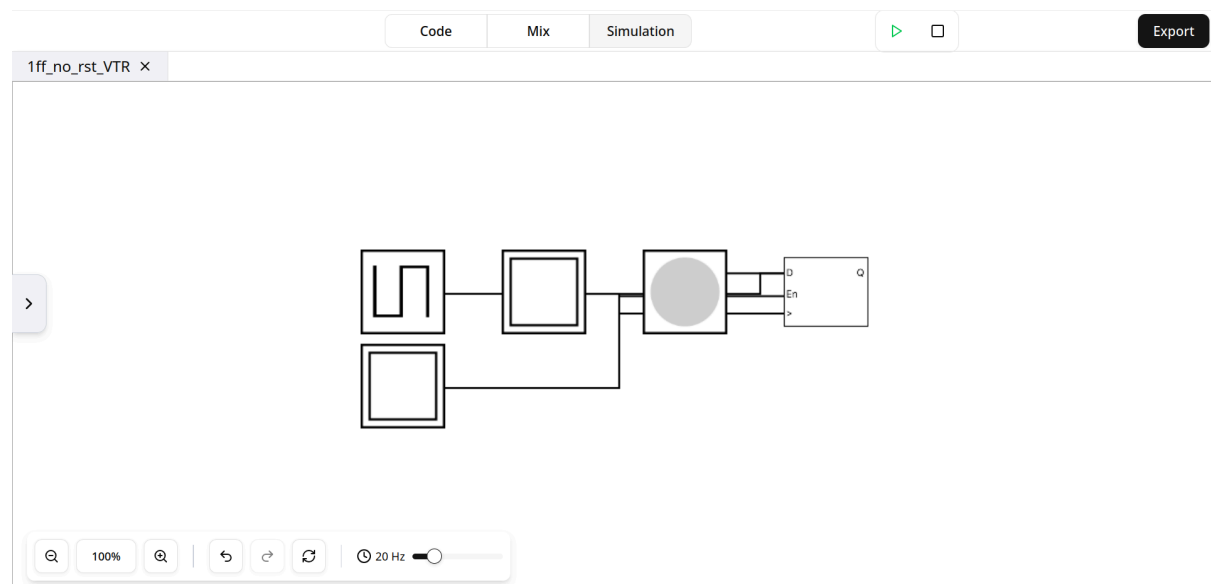
The "Simulation" View

This view visually represents FPGA components (BELs) and wires, allowing users to:

- Rearrange components by clicking and dragging.
- Pan the camera using **Shift + Scroll**.
- Zoom in/out using the mouse wheel.

Simulation Controls:

- **Play/Pause Button:** Starts or stops real-time simulation, visualizing signals propagating through wires.
- **Undo/Redo Buttons:** Revert or reapply changes to component arrangement.
- **Restore Button:** Resets the arrangement to default.

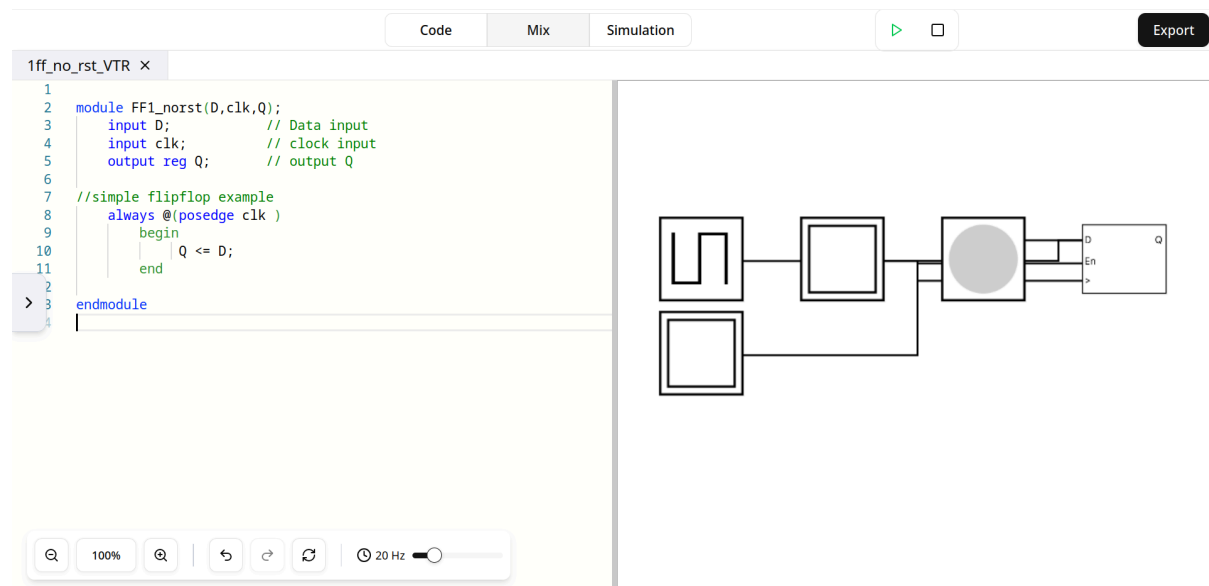


The "Mix" View

The Mix view divides the screen into two adjustable sections:

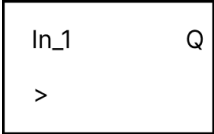
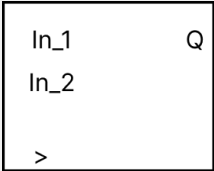
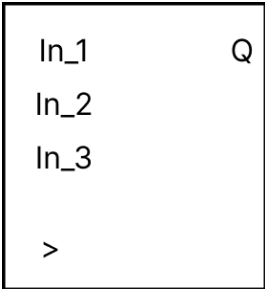
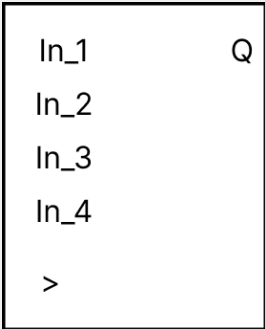

- **Left side:** Code view.
- **Right side:** Simulation view.





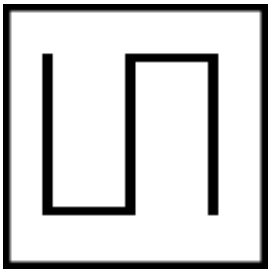
You can drag the divider to adjust the ratio between the two views according to your preference.









Component Representations

The FPGA components (BELs) can be represented in various forms to help illustrate different aspects of FPGA operation clearly:

Component	Representation
LUT1	
LUT2	
LUT3	
LUT4	
D-Flip Flop	

Component	Representation
NAND	
NOR	
XOR	
XNOR	
Clock	

D-Flip Flop with enable	<div><div>D</div><div>Q</div><div>En</div><div>></div></div>
AND	
OR	

LED on	
LED off	
Button on	
Button off	

Troubleshooting and Support

For any difficulties encountered:

- **Ensure file compatibility:** Verify your `.v` and `.sdf` files are correctly exported from Impulse or ModelSim.
- **Restart the web server:** Often resolves minor glitches.

If issues persist or you encounter errors, please contact your instructor or system administrator for further assistance.

Feedback and Contribution

Your feedback is invaluable for improving this tool. Please report bugs or suggest improvements directly on our [github issue](#)