Assignment Brief – CPU Instruction Cycle Simulator Extension

This assignment requires students to modify an HTML/JavaScript CPU simulator to implement extended instruction functionality, additional addressing modes, and a conditional branch.

Tasks

• Implement new ALU instructions: SUB, MUL, DIV, AND, OR, NOT.

• Add immediate addressing to all instructions.

• Implement register-indirect addressing (e.g., LOAD R1, (R2)).

• Implement indexed addressing (e.g., LOAD R1, 500(R2)).

• Add the conditional branch instruction JNZ.

• Create three test programs demonstrating correct functionality.

• Write a technical report (1000–1500 words) describing your implementation.

Deliverables

• Modified HTML/JS simulator file (with comments/annotations).

• Three test programs.

• Technical report.

Assessment Criteria

• Correct implementation of new instructions – 25 marks.

• Addressing modes – 25 marks.

• Control flow instruction – 15 marks.

• Code quality and organisation – 15 marks.

• Test programs – 10 marks.

• Technical report – 10 marks.

Attachment & Due Date

Note that the original code simulator_v1.html is attached for your modification. **Due date: 5 January 2026**

Optional Extra Marks

For additional marks, extend the simulator/applet interface to display the system bus.